# New Multilevel Converter Based on Cascade Connection of Double Flying Capacitor Multicell Converters and Its Improved Modulation Technique

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***Abstract*—This paper proposes a new multilevel converter based on the cascade connection of double flying capacitor multicell (DFCM) converters, as multilevel modules, to decrease the voltage diversity of the flying capacitors. Furthermore, a new switching pattern based on the phase-shifted pulse-width modulation technique is proposed to reduce the voltage ripple across the flying capacitors. Moreover, the proposed modulation technique reduces the rms value of the current flowing through flying capacitors. This results in an increase in the life time of flying capacitors and a decrease in the capacitance of the flying capacitors, to keep the same amount of the ripple, meaning a reduction in the physical size of the converter. In addition, this paper presents an analytical approach to calculate the average and rms currents of the insulated gate bipolar transistors (IGBTs)/diodes in the DFCM converter in a closed-form expression. The derived closed-form equations to calculate the average and rms currents of the IGBTs/diodes are utilized to investigate the conduction power losses in a DFCM converter and the proposed multilevel converter. Numerical results of the derived closed-form equations match the simulation results well, which validates the derived equations. Furthermore, simulation results and experimental measurements of the proposed multilevel power converter, configured by cascading two two-cell five-level DFCM converters, are presented to validate the performance of the proposed converter as well as the suggested modulation technique.**

***Index Terms*—Conduction power loss, double flying capacitor multicell (DFCM) converter, multilevel converter, natural voltage balancing, phase-shifted pulse-width modulation (PS-PWM).**

## I. Introduction

NOWADAYS, multilevel power converters are considered as the most cost-effective solutions and the state-of-the-art power conversion systems in the medium-voltage and high-power energy management market [1]–[3]. The ability to handle the power and voltage range exceeding the rating of individual power switch is the most noteworthy advantage of the multilevel converters, which features them to cover power ranges from one to tens of megawatts. The multilevel converters in comparison with the two-level converters have advantages such as low switching and conduction power losses, increased efficiency, notable enhanced power quality, reduced size of output filter, increased reliance on power converter operation due to the possible fault-tolerant feature, high modularity, and extended power range due to the high-voltage capability [4]–[8]. Neutral point clamped (NPC), flying capacitor multicell (FCM), cascaded H-bridge (CHB), and modular multilevel converter (MMC) are the standard and well-established topologies of the modular multilevel converter (MMC) emerged for medium-voltage high-power applications [9]–[15].

Recently, FCM converters have drawn more attention from industry and academia owing to their merits such as natural voltage balancing feature, transformer-less operation, and equally distribution of switching stress among semiconductor power switches [16]–[20]. Other subtopologies of FCM converters proposed by the power electronic research society are: stacked multicell [5], [9], double flying capacitor multicell (DFCM) [9], improved DFCM [10], and cascade connection of the modified FCM converters [5]. FCM converters are comprised of switching power cells connected in series to form the converter phase leg. Each switching power cell is realized by two low-/medium-voltage insulated gate bipolar transistors (IGBTs) possessing a complementary state with respect to each other, and one flying capacitor (FC). This implies that by using these series-connected switching power cell comprising low-/medium-voltage IGBTs, it is possible to achieve higher voltage/power ranges [17]–[22]. In order to generate the regularly stepped levels of the chopped input-voltage at the output side of the FCM converters and also to guarantee the natural balancing of the FC voltages, it is required for all the switching power cell to operate with the same duty cycle. The most common technique for this purpose is modulating the FCM converters by the phase-shifted pulse-width modulation (PS-PWM) [10]–[17].

However, as the voltage and power rating increases, high voltage-rating of FCs as well as diversity in their voltage rating (so reducing the converter modularity) impact the FCM converter's integrity, sizing, and price profoundly. To negate this detriment and to decrease the voltage diversity of FCs and converter's overall cost in FC-based converters, the DFCM converters are considered as a cost-effective alternative topology. Though, the DFCM converters might not be able to fulfill the restricted requirements of the high-power market deservedly because they still suffer from diversity in the voltage ratings of

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FCs. Hence, this paper proposes a new topology of the multilevel converter based on the cascade connection of the DFCM converters, as multilevel modules, to decrease the voltage diversity of the FCs. This enhancement helps to increase the modularity of the FC-based converters. Furthermore, a new modulation strategy based on the PS-PWM method is proposed to reduce the voltage ripple across the FCs. As a result, the proposed modulation method results in a smaller capacitance for FCs to retain the same voltage ripple, which means a reduction in the size and cost of the power converter. Moreover, the proposed modulation technique reduces the rms value of the currents flowing through the FCs, so resulting in a decrease in the power losses followed by a reduction in the heat produced inside of the FCs. This feature can enhance the life time and reliability of FCs [23]. For appropriate design of multilevel converters, it is a concern of utmost importance and practical interest to utilize smaller FCs to reduce the converter cost, physical size, and installation area.

This paper is organized as follows. Section II presents the proposed multilevel converter based on the cascade connection of DFCM modules controlled with a new modulation technique. Section III discusses about the conduction power loss calculation of IGBT/diode. Moreover, the approach to obtain the parameters of IGBTs/diodes from datasheet for conduction power loss calculation is discussed. So far, no research study has considered the analytical calculation of rms and average current flowing through IGBTs/diodes in DFCM converters. It is noteworthy that analytical calculation of rms and average current of IGBTs/diodes also results in analytical investigation of the conduction power losses, which is advantageous in the design procedure. Hence, Section III presents a detailed approach to analytically calculate the rms and average currents flowing through IGBTs/diodes as a function of load peak current, load power factor, and modulation index in the DFCM converter. Afterwards, numerical results of the derived closed-form equations to calculate the rms and average current of IGBTs/diodes are compared with simulation results to validate the derived equations. Finally, conduction power losses for the 28-MVA 6.6-kV 17-level (line-to-line) proposed multilevel converter are analytically calculated and investigated utilizing the derived closed-form equations. In the performed case study for the proposed multilevel converter based on the cascade connection of the DFCM modules, parameters of an ABB 5SNA 1500E250300 HiPak 2.5-kV 1.5-kA IGBT module and ABB 5SHX 19L6020 5.5-kV 1.8-kA integrated gate-commutated thyristor (IGCT) module are considered. In section IV, simulation results for the proposed multilevel converter are provided to verify its feasibility, performance, and advantages of its new modulation technique. Section V provides experimental measurements obtained from a single-phase nine-level prototype system of the proposed multilevel converter.

## II. Proposed Multilevel Converter Based on Cascade Connection of DFCM Modules

The FCs are very significant components from cost and size points of view in FC-based converters. Furthermore, the voltage rating of dc capacitors has a profound impact on their price.

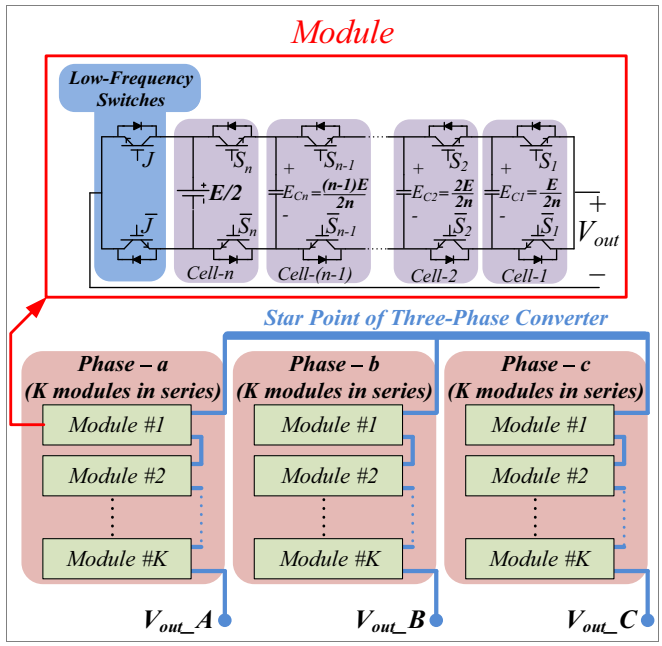


Fig. 1. Proposed multilevel converter based on the cascaded connection of $n$-cell-$(2n+1)$-level DFCM module.

In other words, capacitors possessing the higher voltage ratings retain much higher prices. Hence, it is feasible to conclude that the voltage rating of FCs is one of the price-determining factors in any FC-based converters. Since FC voltages in FC-based converters are more diverse whenever the number of cells is high, it is not more practical to have high number of cells. To negate this disadvantage, a topology called DFCM converter has been proposed wherein the number of FCs and power switches is half of those in the conventional topology of an FCM converter for generating the same stepped output voltage. More details about the principles of DFCM converter operation are presented in [9]. However, DFCM converters might not be able to fulfill the restricted requirements of high-power market deservedly because they still suffer from the diversity in voltage ratings of FCs as the number of cells increases. To overcome this issue, this paper proposes a new multilevel configuration, which is based on the cascade connection of the DFCM converters utilized as multilevel modules. By applying this approach, it is more practical and possible to increase the number of identical modules. General topology of the proposed multilevel converter is shown in Fig. 1 wherein each phase is constructed by cascade connection of $K$ modules while each module is an $n$-cell-$(2n+1)$-level DFCM converter. Therefore, the proposed multilevel converter can produce $2Kn+1$ levels in each phase with peak-to-peak voltage of $KE$. A possible modulation technique to control the proposed multilevel converter properly and to ensure the natural balancing of FC voltages in each multilevel module, which is a DFCM converter, is basically the method presented in [18]. This modulation method has been applied basically for cascaded FCM converters; however, it can be implemented for the proposed multilevel converter by amending the reference signal. In [18], it has been presented to implement PS-PWM method for each multilevel module individually, then, and from the whole

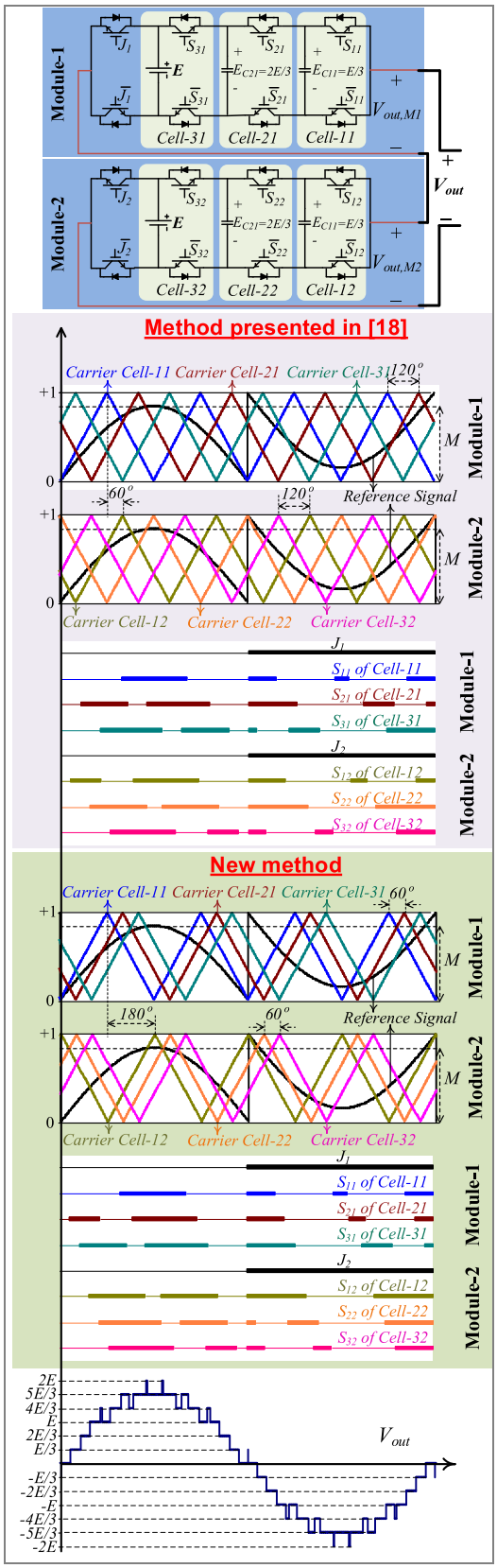


Fig. 2. 13-level (line-to-neutral) proposed multilevel converter based on the cascade connection of two three-cell seven-level DFCM modules, its modulation technique based on the method presented in [18] as well as the new modulation technique, state of the power switches, and output voltage.

converter control point of view, interleave the triangle-carriers related to the multilevel modules with respect to each other. In other words, it has been proposed to phase shift all the triangle carriers related to one module by $2\pi/n$ with respect to each other, where $n$ is the number of switching power cells in one multilevel module and $2\pi$ expresses the switching cycle. Following, it is required to phase shift the triangle carrier of the first cells in all $K$ modules by $2\pi/Kn$ with respect to each other. For instance, the 13-level proposed multilevel converter based on the cascade connection of two three-cell seven-level DFCM modules controlled with the modulation technique presented in [18] is shown in Fig. 2. This paper proposes a new modulation technique based on the PS-PWM method to reduce the voltage ripple across the FCs, so resulting in a decrease in the FCs' capacitance, and consequently, physical size of the converter. The key point of the proposed modulation technique is to consider switching power cells of all multilevel modules as a unified system and implement the PS-PWM method for all of the cells in all of the modules, and not individually for each module. This means that the phase shift between triangle carriers of two adjacent cells in one module is $2\pi/Kn$, instead of $2\pi/n$ in the method presented in [18]. Therefore, the phase shift between the triangle carriers of the first cells in two adjacent multilevel modules is $2\pi/K$, instead of $2\pi/Kn$ in the strategy presented in [18]. Fig. 2 also illustrates the new modulation technique to control the 13-level proposed multilevel converter based on the cascade connection of two three-cell seven-level DFCM modules as well as state of its switches, and output voltage. As it is shown in Fig. 2, the output voltage of the proposed multilevel converter is analogous utilizing both of the modulation techniques shown in Fig. 2. It should be mentioned that the PS-PWM is not the optimal switching method regarding the total harmonic distortion (THD) of the output line-to-line voltages, whereas the level-shifted phase-disposition PWM results in better and enhanced THD for the output line-to-line voltage. However, the PS-PWM results in natural balancing of FC voltages without any feedback control, which is required in level-shifted phase-disposition PWM. It is noteworthy that the FC-based converters are usually modulated and controlled under PS-PWM pattern to obtain the natural balancing of the FC voltages. State of power switches in the nine-level (line-to-neutral) proposed multilevel converter based on cascade connection of two two-cell five-level DFCM modules controlled with the proposed modulation technique have been demonstrated in Table I. The voltage variation of each FC, i.e., $\Delta E_{Cx} = E_{Cx}(t + \Delta t) - E_{Cx}(t)$, is determined for each switching state by taking into account the load current polarity in Table I. The state of power switches have been listed only for the positive half cycle of the output voltage since they will be just inverted for the negative half cycle of the output voltage.

The proposed multilevel converter based on the cascade connection of DFCM modules as like as other FC-based multilevel converters can be utilized in high-power application, such as motor drives, static synchronous compensator (STATCOM), flexible alternating current transmission system (FACTS), etc. However, the proposed converter needs an isolated dc link in each module as like as cascaded H-bridge converters.

TABLE I
STATE OF POWER SWITCHES AND CHARGING/DISCHARGING PROCESS OF FCS IN NINE-LEVEL (LINE-TO-NEUTRAL) PROPOSED MULTILEVEL CONVERTER BASED ON THE CASCADE CONNECTION OF TWO TWO-CELL FIVE-LEVEL DFCM MODULES CONTROLLED WITH THE NEW MODULATION TECHNIQUE

| Proposed Multilevel Converter Output Voltage | Output Voltage Module-1 | Output Voltage Module-2 | State of switches | | $\Delta E_{C12}$ | $\Delta E_{C11}$ | $i_{\mathrm{Load}}$ | Number of States |
|---|---|---|---|---|---|---|---|---|
| | | | Module-1 ($S_{22}$ , $S_{12}$) | Module-2 ($S_{21}$ , $S_{11}$) | | | | |
| $+2E$ | $+E$ | $+E$ | (1,1) | (1,1) | 0 | 0 | *whatever* | 1 |
| $+1.5E$ | $+E/2$ | $+E$ | (0,1) | (1,1) | $-$ | 0 | $i_{\mathrm{Load}} > 0$ | 4 |
| | | | | | $+$ | 0 | $i_{\mathrm{Load}} < 0$ | |
| | $+E$ | $+E/2$ | (1,1) | (1,0) | 0 | $+$ | $i_{\mathrm{Load}} > 0$ | |
| | | | | | 0 | $-$ | $i_{\mathrm{Load}} < 0$ | |
| | $+E$ | $+E/2$ | (1,1) | (0,1) | 0 | $-$ | $i_{\mathrm{Load}} > 0$ | |
| | | | | | 0 | $+$ | $i_{\mathrm{Load}} < 0$ | |
| | $+E/2$ | $+E$ | (1,0) | (1,1) | $+$ | 0 | $i_{\mathrm{Load}} > 0$ | |
| | | | | | $-$ | 0 | $i_{\mathrm{Load}} < 0$ | |
| $+E$ | 0 | $+E$ | (0,0) | (1,1) | 0 | 0 | $i_{\mathrm{Load}} > 0$ | 4 |
| | | | | | 0 | 0 | $i_{\mathrm{Load}} < 0$ | |
| | $+E/2$ | $+E/2$ | (0,1) | (1,0) | $-$ | $+$ | $i_{\mathrm{Load}} > 0$ | |
| | | | | | $+$ | $-$ | $i_{\mathrm{Load}} < 0$ | |
| | $+E$ | 0 | (1,1) | (0,0) | 0 | 0 | $i_{\mathrm{Load}} > 0$ | |
| | | | | | 0 | 0 | $i_{\mathrm{Load}} < 0$ | |
| | $+E/2$ | $+E/2$ | (1,0) | (0,1) | $+$ | $-$ | $i_{\mathrm{Load}} > 0$ | |
| | | | | | $-$ | $+$ | $i_{\mathrm{Load}} < 0$ | |
| $+0.5E$ | 0 | $+E/2$ | (0,0) | (0,1) | 0 | $-$ | $i_{\mathrm{Load}} > 0$ | 4 |
| | | | | | 0 | $+$ | $i_{\mathrm{Load}} < 0$ | |
| | 0 | $+E/2$ | (0,0) | (1,0) | 0 | $+$ | $i_{\mathrm{Load}} > 0$ | |
| | | | | | 0 | $-$ | $i_{\mathrm{Load}} < 0$ | |
| | $+E/2$ | 0 | (0,1) | (0,0) | $-$ | 0 | $i_{\mathrm{Load}} > 0$ | |
| | | | | | $+$ | 0 | $i_{\mathrm{Load}} < 0$ | |
| | $+E/2$ | 0 | (1,0) | (0,0) | $+$ | 0 | $i_{\mathrm{Load}} > 0$ | |
| | | | | | $-$ | 0 | $i_{\mathrm{Load}} < 0$ | |
| 0 | 0 | 0 | (0,0) | (0,0) | 0 | 0 | *whatever* | 1 |

## III. CONDUCTION POWER LOSS CALCULATION IN DFCM AND PROPOSED MULTILEVEL CONVERTERS

Analytic equations expressing the conduction power losses of IGBTs/diodes in multilevel converters are very advantageous in the design procedure of these power converters. They can be used to investigate the converters' performance and efficiency with any number of switching power cells and voltage levels as a function of the converter output power, load power factor, and modulation index. In this section, an analytical approach is presented to calculate the average and rms currents flowing through the IGBTs/diodes in the DFCM converter, and consequently, the proposed multilevel converter. Afterwards, the derived closed-form equations to calculate the average and rms currents of power switches and diodes are utilized to investigate the conduction power losses in the DFCM and proposed multilevel converters.

The IGBT collector–emitter voltage drop $(v_{\mathrm{CE}})$ when it is conducting can be approximated very well as follows:

$$v_{\mathrm{CE}} = v_{\mathrm{CE0}} + R_C \cdot i_C \tag{1}$$

where $v_{\mathrm{CE0}}$ is representing the IGBT on-state zero-current collector–emitter forward voltage drop and $R_C$ is collector–emitter on-state resistance. The same approximation can be used for the antiparallel diode, giving

$$v_F = v_{F0} + R_F \cdot i_F \tag{2}$$

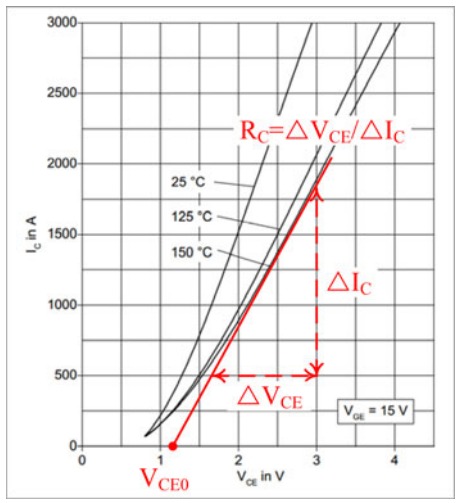


Fig. 3. Obtaining $V_{\mathrm{CE0}}$ and $R_C$ from the datasheet.

where $v_{F0}$ is representing the antiparallel diode on-state zero-current forward voltage drop and $R_F$ is antiparallel diode on-state resistance. These important parameters can be obtained directly from the IGBT datasheet; see Fig. 3 for the IGBT and Fig. 4 for the diode, which is from ABB 5SNA 1500E250300 HiPak 2.5-kV 1.5-kA IGBT module [24]. In order to take the parameter variation into account, and thus, to have a conservative calculation, the $v_{\mathrm{CE0}}$ and $v_{F0}$ values obtained from datasheet have to be scaled with $\left(\frac{V_{\mathrm{CE,MAX}}}{V_{\mathrm{CE,TYP}}}\right)$ and $\left(\frac{V_{F,\mathrm{MAX}}}{V_{F,\mathrm{TYP}}}\right)$, respectively.

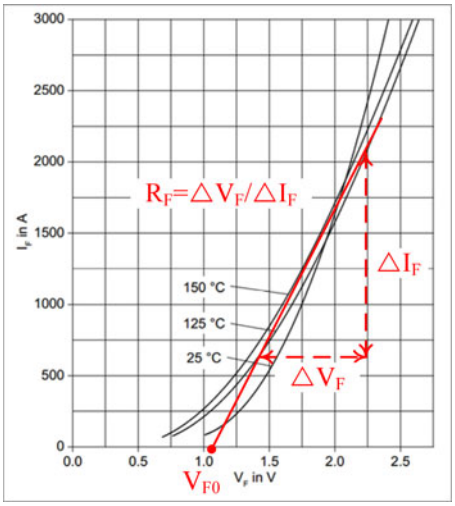


Fig. 4. Obtaining $V_{F0}$ and $R_F$ from the datasheet.

The instantaneous values of the IGBT conduction losses $(p_{\mathrm{CT}}(t))$ and the average losses $(P_{\mathrm{CT}})$ are

$$p_{\mathrm{CT}}(t) = v_{\mathrm{CE}}(t)\cdot i_C(t) = v_{\mathrm{CE0}}\cdot i_C(t) + R_C\cdot i_C^2(t) \quad (3)$$

$$P_{\mathrm{CT}} = \frac{1}{2\pi}\int_0^{2\pi}\left[p_{\mathrm{CT}}(t)\right]d(\omega t)$$

$$= \frac{1}{2\pi}\int_0^{2\pi}\left[v_{\mathrm{CE0}}\cdot i_C(t) + R_C\cdot i_C^2(t)\right]d(\omega t) \quad (4)$$

$$P_{\mathrm{CT}} = v_{\mathrm{CE0}}\cdot I_{C,\mathrm{avg}} + R_C\cdot I_{C,\mathrm{rms}}^2 \quad (5)$$

where $I_{C,\mathrm{avg}}$ and $I_{C,\mathrm{rms}}$ are the average and rms currents of the IGBT, respectively. Similar to the IGBT, the average value of the diode conduction losses $(P_{\mathrm{CD}})$ is

$$P_{\mathrm{CD}} = v_{F0}\cdot I_{D,\mathrm{avg}} + R_F\cdot I_{D,\mathrm{rms}}^2 \quad (6)$$

where $I_{D,\mathrm{avg}}$ and $I_{D,\mathrm{rms}}$ are the average and rms currents of antiparallel diode, respectively.

The next step to calculate the conduction power losses is to obtain the analytical equations expressing average and rms currents of IGBTs/diodes. The duty cycle associated with one switching power cell, for instance $S_1$, of the proposed multilevel converter based on the cascade connection of the DFCM converters varies according to the following function:

$$D(t) = \begin{cases} M\sin(\omega t) & 0 < \omega t < \pi \\ 1 + M\sin(\omega t) & \pi < \omega t < 2\pi \end{cases} \quad (7)$$

where $M$ is the modulation index, $\omega = 2\pi f$ is the angular frequency, and $f$ is the output voltage frequency. The modulation index represents the normalized voltage and is between zero and one. For the sake of simplicity in deriving analytical equations for average and rms currents, the phase current can be assumed to be sinusoidal. The actual current waveform is slightly distorted by the PWM high-frequency ripple current and motor nonlinearity. The phase current for an induction motor normally lags the phase voltage by the phase angle $\varphi$. Because the current is a simple sine function, the math works out to be much easier if the voltage is assumed to lead the current by $\varphi$, and integrate

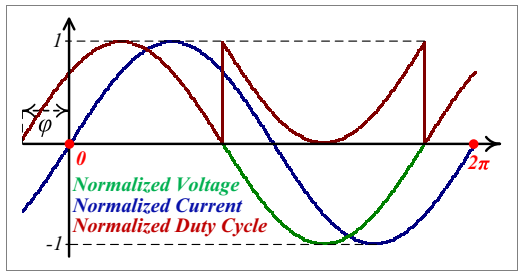


Fig. 5. Normalized value of phase voltage, phase current, and cell upper switch duty cycle in the DFCM converter.

over the current waveform. The resulting relationships are the same using either method. Thus, the phase current $(i_\phi(t))$ and duty cycle are defined according to the following equations:

$$i_\phi(t) = I_P\cdot\sin(\omega t) \quad (8)$$

$$D(t) = \begin{cases} M\sin(\omega t+\varphi) & -\varphi < \omega t < \pi-\varphi \\ 1 + M\sin(\omega t+\varphi) & \pi-\varphi < \omega t < 2\pi-\varphi \end{cases} \quad (9)$$

where $I_{\mathrm{P}}$ is the peak current. Fig. 5 illustrates the relationship between the phase voltage, phase current, and the duty cycle of top high-frequency switch $(S_x)$.

It is worth mentioning that due to the symmetrical operation of top and bottom high-frequency IGBTs/diodes ($S_x, D_x$ and $\overline{S_x}, \overline{D_x}$) in each cell, they have the same average and rms current rating. Therefore, the calculations are done only for top high-frequency IGBTs/diodes $(S_x, D_x)$ and extended to the bottom IGBTs/diodes $(\overline{S_x}, \overline{D_x})$. Likewise, the calculations are done for top low-frequency IGBT/diode $(S_J, D_J)$ and extended to the bottom low-frequency IGBT/diode $(\overline{S_J}, \overline{D_J})$.

The top IGBT carries the current whenever it is on $(D(t))$ as well as the phase current is positive, which is for $\omega t$ from 0 to $\pi$. Moreover, the top antiparallel diode carries the current whenever its associated IGBT gate signal is on $(D(t))$ as well as the phase current is negative, which is for $\omega t$ from $\pi$ to $2\pi$. The average IGBT and diode currents over the full sine wave can then be found by integrating the duty cycle times the phase current and opposite of phase current, respectively. Therefore, by assuming that the phase current is almost constant over one PWM cycle, the average current of the top IGBT can be written as follows:

$$I_{C,\mathrm{avg}} = \frac{1}{2\pi}\int_0^{\pi}\left[i_\phi(t)\cdot D(t)\right]d(\omega t)$$

$$= \frac{1}{2\pi}\int_0^{\pi-\varphi}\left[(I_P\sin(\omega t))\cdot(M\sin(\omega t+\varphi))\right]d(\omega t)$$

$$+\frac{1}{2\pi}\int_{\pi-\varphi}^{\pi}\left[(I_P\sin(\omega t))\cdot(1+M\sin(\omega t+\varphi))\right]d(\omega t) \quad (10)$$

By recalling (11), (10) can be written as (12), and simplified furthermore as (13)

$$\sin(\alpha)\cdot\sin(\beta) = \frac{1}{2}\left[\cos(\alpha-\beta) - \cos(\alpha+\beta)\right] \quad (11)$$

$$I_{C,\mathrm{avg}} = \frac{1}{2\pi}\int_0^{\pi-\varphi}\left[\frac{I_P M}{2}(\cos(\varphi) - \cos(2\omega t\right.$$

$$+\varphi))\big]d(\omega t)+\frac{1}{2\pi}\int_{\pi-\varphi}^{\pi}\left[I_P\sin(\omega t)\right]d(\omega t)+\frac{1}{2\pi}\int_{\pi-\varphi}^{\pi}\Big[\frac{I_P M}{2}\big(\cos(\varphi)-\cos(2\omega t+\varphi)\big)\Big]d(\omega t) \quad (12)$$

$$\begin{aligned} I_{C,\text{avg}} &= \frac{I_P M}{4\pi}(\pi-\varphi)\cos(\varphi)+\frac{I_P M}{4\pi}\sin(\varphi)+\frac{I_P}{2\pi}(1-\cos(\varphi))+\frac{I_P M\varphi}{4\pi}\cos(\varphi)-\frac{I_P M}{4\pi}\sin(\varphi)\\ &= \frac{I_P M}{4}\cos(\varphi)+\frac{I_P}{2\pi}(1-\cos(\varphi)) \end{aligned} \quad (13)$$

By following the aforesaid procedure and considering that the bottom low-frequency IGBT $(\overline{J})$ is on for $-\varphi<\omega t<\pi-\varphi$ and the top low-frequency IGBT $(J)$ are on for $\pi-\varphi<\omega t<2\pi-\varphi$, the average current of the top low-frequency IGBTs can be obtained as follows:

$$\begin{aligned} I_{\text{CJ,avg}} &= \frac{1}{2\pi}\int_{\pi}^{2\pi}\left[(-i_\phi(t))\cdot D_J(t)\right]d(\omega t)\\ &= \frac{1}{2\pi}\int_{\pi}^{2\pi-\varphi}\left(-I_P\sin(\omega t)\right)d(\omega t)\\ &= \frac{I_P}{2\pi}(1+\cos(\varphi)) \end{aligned} \quad (14)$$

By following the same procedure, the diode average current can be obtained as follows:

$$\begin{aligned} I_{D,\text{avg}} &= \frac{1}{2\pi}\int_{\pi}^{2\pi}\left[(-i_\phi(t))\cdot D(t)\right]d(\omega t)\\ &= \frac{1}{2\pi}\int_{\pi}^{2\pi-\varphi}\big[(-I_P\sin(\omega t))\cdot(1+M\sin(\omega t+\varphi))\big]d(\omega t)\\ &\quad+\frac{1}{2\pi}\int_{2\pi-\varphi}^{2\pi}\big[(-I_P\sin(\omega t))\cdot(M\sin(\omega t+\varphi))\big]d(\omega t) \end{aligned} \quad (15)$$

By recalling (11), (15) can be rewritten as (16), and simplified furthermore as (17)

$$I_{D,\text{avg}}=\frac{1}{2\pi}\int_{\pi}^{2\pi-\varphi}\left[-I_P\sin(\omega t)\right]d(\omega t)-\frac{1}{2\pi}\int_{\pi}^{2\pi-\varphi}\left[\frac{I_P M}{2}\left(\cos(\varphi)-\cos\left(2\omega t+\varphi\right)\right)\right]d(\omega t)-\frac{1}{2\pi}\int_{2\pi-\varphi}^{2\pi}\left[\frac{I_P M}{2}\left(\cos(\varphi)-\cos\left(2\omega t+\varphi\right)\right)\right]d(\omega t) \quad (16)$$

$$I_{D,\text{avg}}=\frac{I_P}{2\pi}(1+\cos(\varphi))-\frac{I_P M}{4}\cos(\varphi) \quad (17)$$

By following the aforementioned procedure, the average current flowing through the antiparallel diodes of the low-frequency IGBTs can be calculated as follows:

$$\begin{aligned} I_{\text{DJ,avg}} &= \frac{1}{-}\int^{\pi}\left[i_\phi(t)\cdot D_J(t)\right]d(\omega t)\\ &= \frac{1}{2\pi}\int_{\pi-\varphi}^{\pi}\left(I_P\sin(\omega t)\right)d(\omega t)\\ &= \frac{I_P}{2\pi}(1-\cos(\varphi)) \end{aligned} \quad (18)$$

As the final step, the rms current of the IGBT can be calculated as follows:

$$I_{C,\text{rms}}=\sqrt{\frac{1}{2\pi}\int_0^{\pi}\left[i_\phi^2(t)\cdot D(t)\right]d(\omega t)}=\sqrt{\begin{aligned}&\frac{1}{2\pi}\int_0^{\pi-\varphi}\left[\left(I_P\sin(\omega t)\right)^2\cdot\left(M\sin(\omega t+\varphi)\right)\right]d(\omega t)\\&+\frac{1}{2\pi}\int_{\pi-\varphi}^{\pi}\left[\left(I_P\sin(\omega t)\right)^2\cdot\left(1+M\sin(\omega t+\varphi)\right)\right]d(\omega t)\end{aligned}} \quad (19)$$

By recalling (20) and (21), (19) can be rewritten as (22), and simplified furthermore as (23)

$$\sin^2(\alpha)=\frac{1}{2}\left[1-\cos(2\alpha)\right] \quad (20)$$

$$\sin(\alpha)\cdot\cos(\beta)=\frac{1}{2}\left[\sin(\alpha+\beta)+\sin(\alpha-\beta)\right] \quad (21)$$

$$I_{C,\text{rms}}=\sqrt{\begin{aligned}&\frac{1}{2\pi}\int_0^{\pi-\varphi}\left[\frac{MI_P^2}{2}\left(1-\cos(2\omega t)\right)\cdot\left(\sin(\omega t+\varphi)\right)\right]d(\omega t)\\&+\frac{1}{2\pi}\int_{\pi-\varphi}^{\pi}\left[\frac{I_P^2}{2}\left(1-\cos(2\omega t)\right)\right]d(\omega t)\\&+\frac{1}{2\pi}\int_{\pi-\varphi}^{\pi}\left[\frac{MI_P^2}{2}\left(1-\cos(2\omega t)\right)\cdot\left(\sin(\omega t+\varphi)\right)\right]d(\omega t)\end{aligned}} \quad (22)$$

$$\begin{aligned} I_{C,\text{rms}} &= \sqrt{\begin{aligned}&\frac{MI_P^2}{12\pi}\left[\cos(2\varphi)+4\cos(\varphi)+3\right]\\&+\frac{I_P^2}{8\pi}\left[2\varphi-\sin(2\varphi)\right]\\&+\frac{MI_P^2}{12\pi}\left[-3-\cos(2\varphi)+4\cos(\varphi)\right]\end{aligned}}\\ &= \sqrt{\frac{2MI_P^2}{3\pi}\cos(\varphi)+\frac{I_P^2}{8\pi}\left[2\varphi-\sin(2\varphi)\right]} \end{aligned} \quad (23)$$

By following the same procedure, the rms current of the low-frequency IGBT can be calculated as follows:

$$\begin{aligned} I_{\text{CJ,rms}} &= \sqrt{\frac{1}{2\pi}\int_0^{\pi}\left[i_\phi^2(t)\cdot D_J(t)\right]d(\omega t)}\\ &= \sqrt{\frac{1}{2\pi}\int_0^{\pi-\varphi}\left[\left(I_P\sin(\omega t)\right)^2\right]d(\omega t)}\\ &= \sqrt{\frac{I_P^2}{8\pi}\left[2\pi-2\varphi+\sin(2\varphi)\right]} \end{aligned} \quad (24)$$

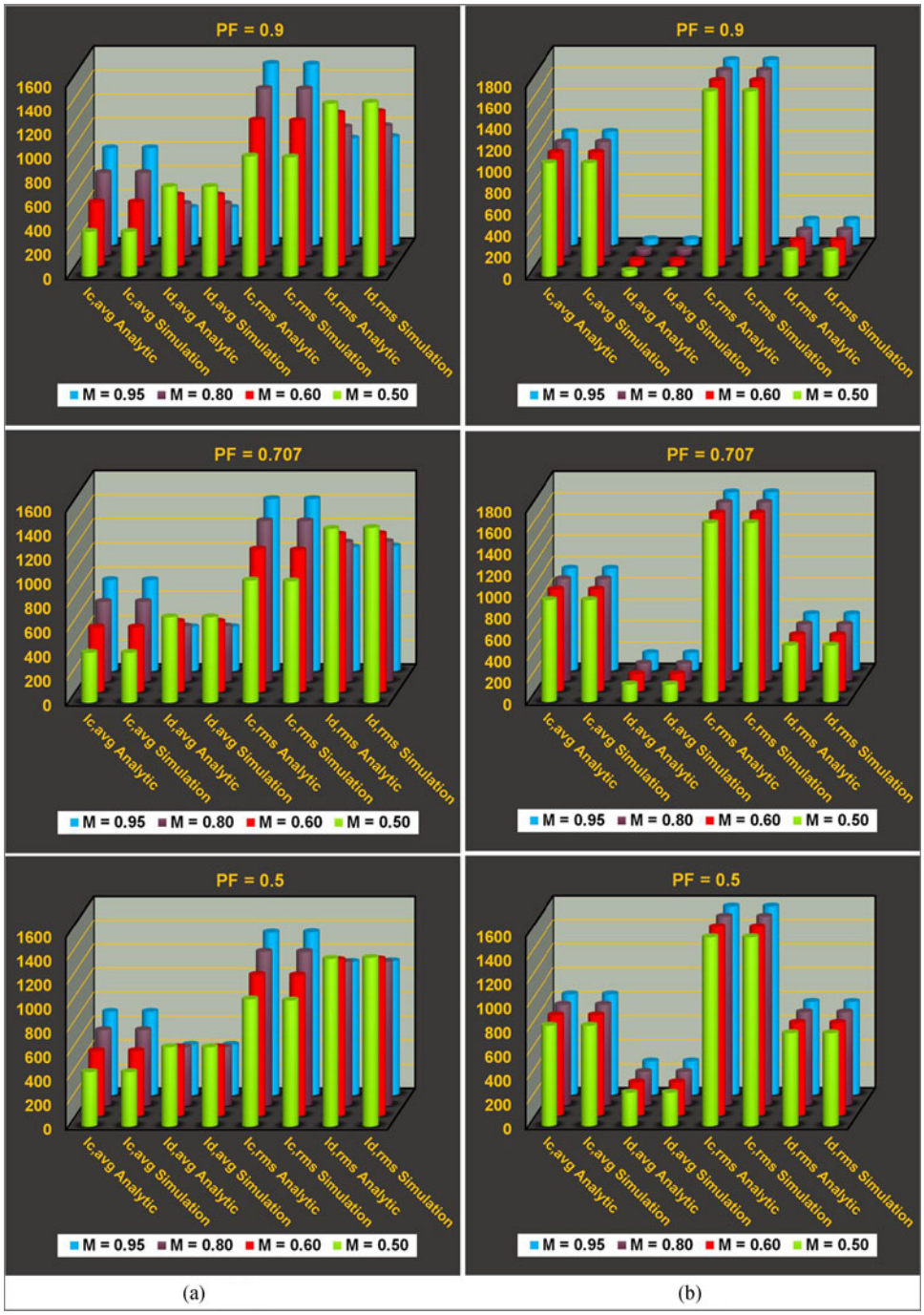


Fig. 6. Comparison between numerical computation and simulation results of average and rms currents of IGBTs/diodes in 28-MVA 6.6-kV 17-level (line-to-line) proposed multilevel converter based on cascade connection of two two-cell five-level DFCM modules considering constant load current: (a) high-frequency IGBTs/diodes; (b) low-frequency IGBTs/diodes.

The diode rms current can be obtained in the following procedure:

$$I_{D,\mathrm{rms}} = \sqrt{\frac{1}{2\pi}\int_{\pi}^{2\pi}\left[(-i_{\phi}(t))^2 \cdot D(t)\right] d(\omega t)}$$

$$= \sqrt{\begin{aligned}&\frac{1}{2\pi}\int_{\pi}^{2\pi-\varphi}\left[(-I_P\sin(\omega t))^2 \cdot (1+M\sin(\omega t+\varphi))\right] d(\omega t)\\ &+\frac{1}{2\pi}\int_{2\pi-\varphi}^{2\pi}\left[(-I_P\sin(\omega t))^2 \cdot (M\sin(\omega t+\varphi))\right] d(\omega t)\end{aligned}} \quad (25)$$

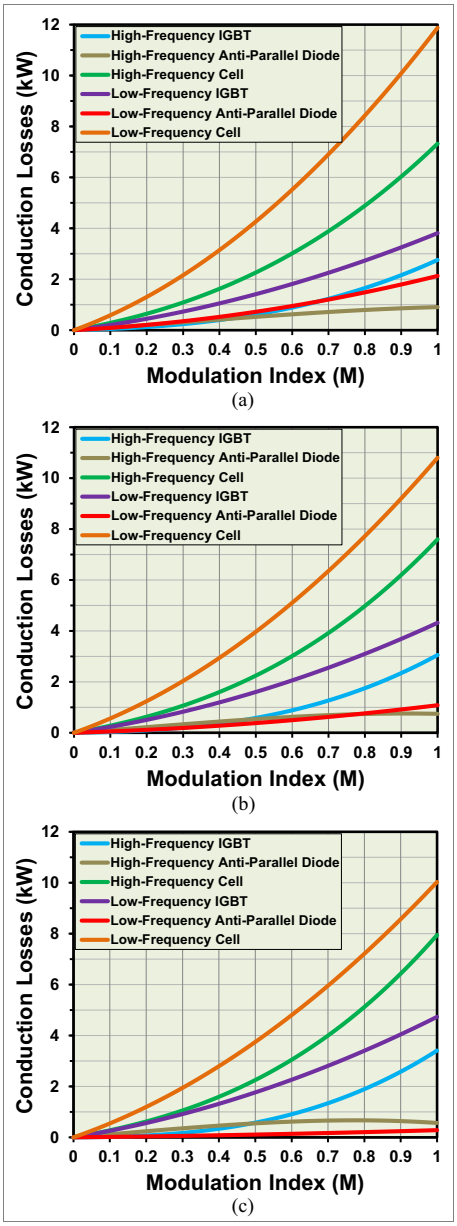


Fig. 7. Conduction power losses of IGBTs, diodes, and switching power cells in 28-MVA 6.6-kV 17-level (line-to-line) proposed multilevel converter based on cascade connection of two two-cell five-level DFCM modules considering constant load impedance: (a) $\cos(\varphi) = 0.5$; (b) $\cos(\varphi) = 0.707$; (c) $\cos(\varphi) = 0.9$.

By recalling (20) and (21), (25) can be written as (26), and simplified furthermore as (27)

$$I_{\mathrm{D,rms}} = \sqrt{\begin{aligned}&\frac{1}{2\pi}\int_{\pi}^{2\pi-\varphi}\left[\frac{{I_p}^2}{2}\left(1-\cos(2\omega t)\right)\right]d(\omega t)\\&+\frac{1}{2\pi}\int_{\pi}^{2\pi-\varphi}\left[\frac{M{I_p}^2}{2}\left(1-\cos(2\omega t)\right)\cdot\left(\sin(\omega t+\varphi)\right)\right]d(\omega t)\\&+\frac{1}{2\pi}\int_{2\pi-\varphi}^{2\pi}\left[\frac{M{I_p}^2}{2}\left(1-\cos(2\omega t)\right)\cdot\left(\sin(\omega t+\varphi)\right)\right]d(\omega t)\end{aligned}} \quad (26)$$

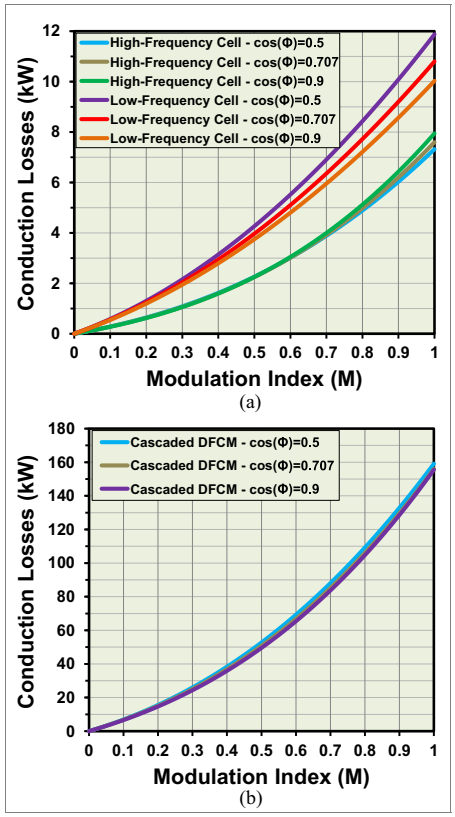


Fig. 8. Conduction power losses in 28MVA 6.6kV 17-level (line-to-line) proposed multilevel converter based on cascade connection of two two-cell five-level DFCM modules considering constant load impedance: (a) switching power cell; (b) three-phase converter.

$$I_{D,\mathrm{rms}} = \sqrt{\frac{I_P^2}{4} - \frac{I_P^2}{8\pi}\left[2\varphi - \sin(2\varphi)\right] - \frac{2MI_P^2}{3\pi}\cos(\varphi)} \quad (27)$$

The same method can be applied for calculation of the rms current flowing through the antiparallel diodes of the low-frequency IGBTs as follows:

$$\begin{aligned} I_{\mathrm{DJ,rms}} &= \sqrt{\frac{1}{2\pi}\int_0^{\pi}\left[i_{\phi}^2(t)\cdot D_J(t)\right]d(\omega t)} \\ &= \sqrt{\frac{1}{2\pi}\int_{\pi-\varphi}^{\pi}\left[\left(I_P\sin(\omega t)\right)^2\right]d(\omega t)} \\ &= \sqrt{\frac{I_P^2}{8\pi}\left[2\varphi-\sin(2\varphi)\right]} \end{aligned} \quad (28)$$

Finally, the derived closed-form expression for the average and rms current flowing through IGBTs/diodes of both high-frequency and low-frequency cells can be substituted in (5) and (6) to calculate the conduction power losses in the DFCM converter as well as the proposed multilevel converter based on cascade connection of the DFCM modules.

The numerical computation and simulation studies in PSCAD are done for a 28-MVA 6.6-kV three-phase 17-level (line-to-line) proposed multilevel converter, whereas each phase is based on two cascaded DFCM modules. Each module is comprised of two high-frequency switching power cells and one low-frequency switching power cell. In this study, a dc link of

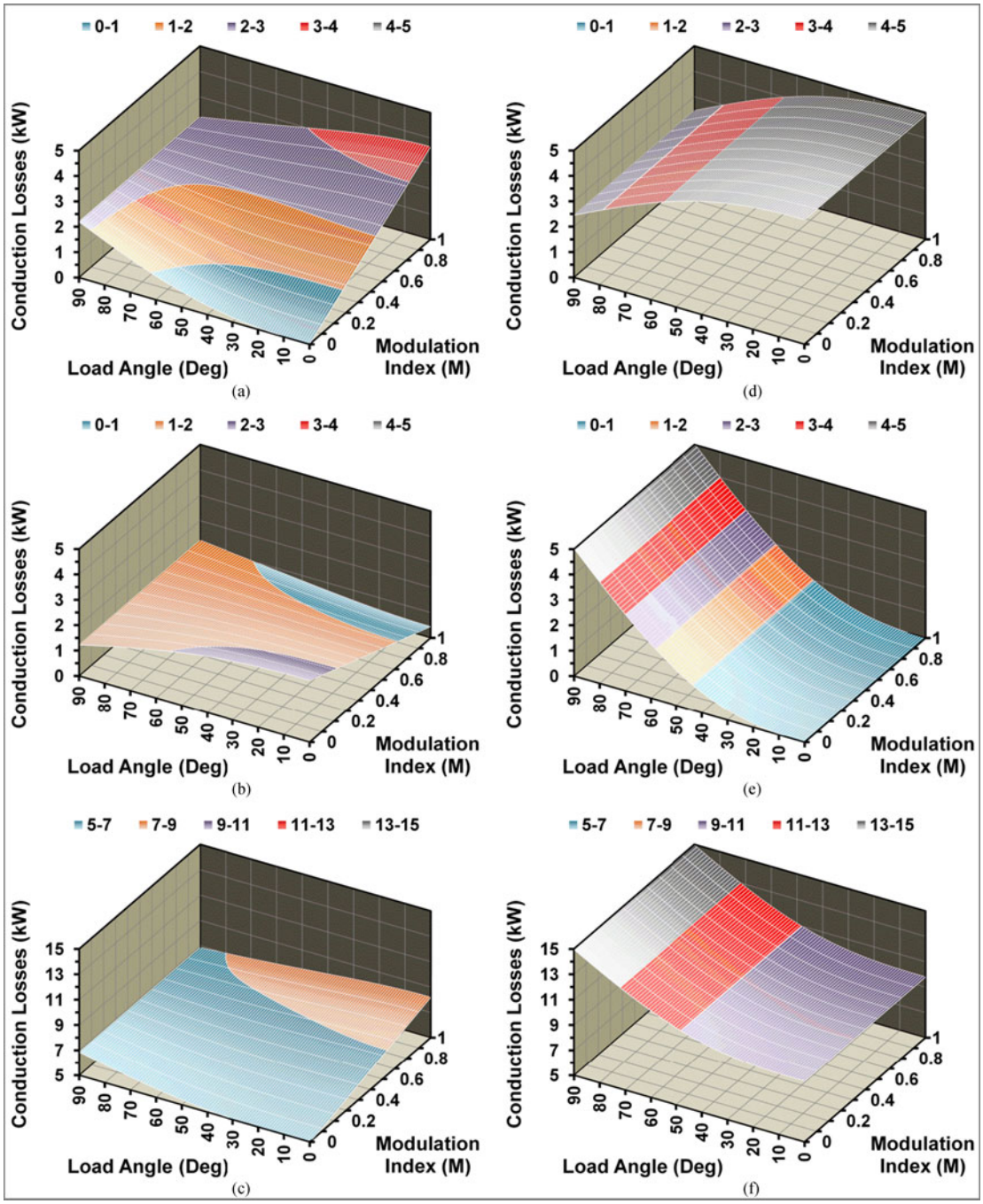


Fig. 9. Conduction power losses in 28-MVA 6.6-kV 17-level (line-to-line) proposed multilevel converter based on cascade connection of two two-cell five-level DFCM modules considering constant load current: (a) high-frequency IGBTs; (b) high-frequency diodes; (c) high-frequency switching power cell; (d) low-frequency IGBTs; (e) low -frequency diodes; (f) low-frequency switching power cell.

3 kV is used for each DFCM module in the proposed multilevel converter; thus, FCs voltage rating in each module is 1.5 kV. Moreover, ABB 5SNA 1500E250300 HiPak 2.5-kV 1.5-kA IGBT module with parameters of $V_{\rm CE0} = 1.2\,{\rm V}$, $R_C = 1\,{\rm m}\Omega$, $V_{F0} = 1.1\,{\rm V}$, and $R_F = 0.4\,{\rm m}\Omega$ is considered for the IGBT/diode of high-frequency switching power cells, whereas ABB 5SHX 19L6020 5.5-kV 1.8-kA IGCT module with parameters of $V_{\rm CE0} = 2.2\,{\rm V}$, $R_C = 0.8\,{\rm m}\Omega$, $V_{F0} = 2.7\,{\rm V}$, and $R_F = 2.3\,{\rm m}\Omega$ is chosen for the IGBT/diode of low-frequency switching power cells in DFCM modules of the proposed multilevel converters. The line peak current ($I_P$) is around 3500 A. It is worth mentioning that the utilization factor regarding the voltage of high-power medium-voltage switches is practically around 50–60%. Due to this, 2.5-kV IGBTs are selected for high-frequency switching power cells to withstand 1.5-kV and 5.5-kV IGCTs are selected for low-frequency switching power cells to withstand 3 kV. In order to verify the derived closed-form equations for calculation of rms and average current flowing through IGBTs/diodes in the DFCM modules of the proposed multilevel converters, the numerical computation

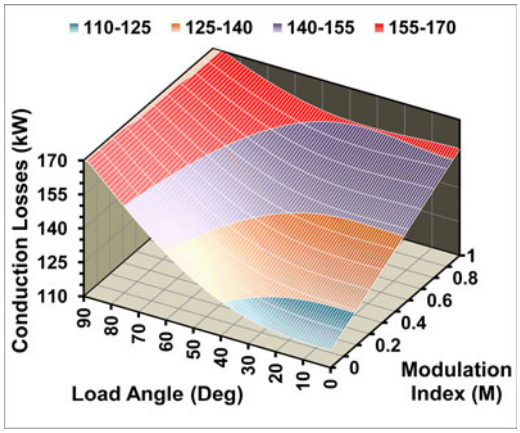


Fig. 10. Total conduction power losses in 28-MVA 6.6-kV 17-level (line-to-line) proposed multilevel converter based on cascade connection of two two-cell five-level DFCM modules considering constant load current.

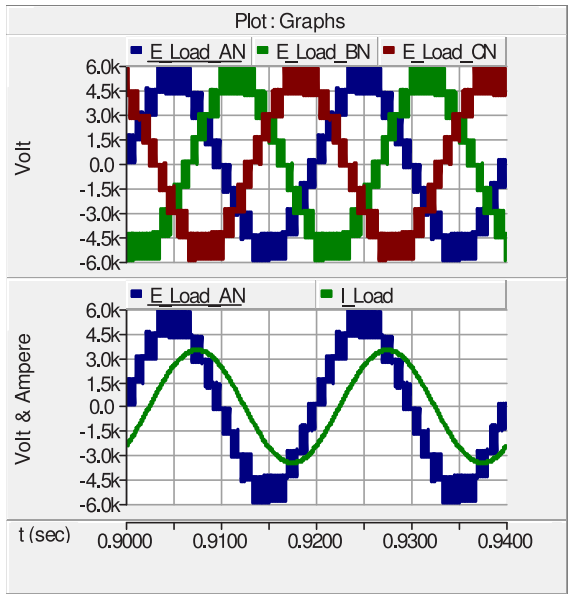


Fig. 11. Output voltage and load current of the nine-level (line-to-neutral) proposed multilevel converter based on the cascade connection of two two-cell five-level DFCM modules.

results are compared with the simulation results. This comparison is shown in Fig. 6 illustrating a good match between the numerical and simulation results, which validates derived closed-form equations. In Fig. 6, load peak current is assumed 3500 A for all modulation indices and various power factors. So, the load impedance is not considered constant. It should be mentioned that both conventional and proposed switching methods results in the same current rating for all IGBTs/diodes.

After validating the derived closed-form equations by comparing the numerical and simulation results with a great match as shown in Fig. 6, the equations are utilized to calculate the conduction power losses in the proposed multilevel converter. As a result, switching power cell components' conduction power losses as a function of modulation index and load power factor in the proposed multilevel converter based on the cascaded DFCM converters (modules) are shown in various cases in Figs. 7–10. It should be mentioned that the load impedance is considered constant in Figs. 7 and 8; hence, its current varies linearly with converter modulation index while the load peak current ($Ip = 3500$ A) in Figs. 9 and 10 is considered constant.

## IV. Simulation Results

In this section, simulation results are illustrated to verify the performance of the proposed multilevel converter and effectiveness of its new modulation technique. The simulation results are related to the same converter explained in Section III.

Line-to-neutral output voltage of the nine-level proposed multilevel converter based on the cascade connection of two two-cell five-level DFCM modules in all three phases and load current in phase A, all in steady state, are shown in Fig. 11. The converter is operated with a modulation index equal to 0.9 ($M = 0.9$) and controlled with the proposed modulation technique wherein triangle-carriers' frequency is *2* kHz. Fig. 12 illustrates FC voltages of each module in all three phases of the proposed multilevel converter controlled with both conventional [18] and the proposed modulation technique in transient and steady states. As it is obvious, the proposed switching pattern results in decreasing the voltage ripple of FCs (by 25%) that causes to use smaller capacitor to have the same voltage ripple. In other words, utilization of the proposed switching pattern causes to use smaller capacitor, which means decrease in the size and cost of the converter. The cost reduction can be more valuable in long-term operation of the converter since the capacitors usually have a short life-time and require more maintenance. In addition, rms value of current flowing through FCs is reduced from 1720 to 1520 A (by 12%), which results in less power loss (by 22%), and consequently, less heat in FCs. Since both modulation techniques are based on PS-PWM, FC voltages are balanced naturally at their target values, as shown in Fig. 12, to ensure the safe and proper operation of the proposed multilevel converter based on the cascade connection of the DFCM modules. As depicted in Fig. 13, which demonstrates the frequency spectrum of the output voltage with THD of 15%, the output voltage has harmonic clusters around the $(k \times 4 \times 2\text{kHz})^{\text{th}}$ harmonic, where *k* is an integer number and 4 is the number of all triangle carriers (the same as the number of switching power cells in all modules) intersected with reference signal. The main parameters used in the simulations are given in Table II.

## V. Experimental Results

To validate the viability of the proposed multilevel converter as well as its modulation technique, two two-cell five-level DFCM module are built utilizing BUP 314D/Siemens 1200-V 42-A IGBT modules, and connected in series to form the single-phase nine-level proposed multilevel converter. The gate drivers for IGBTs and optoisolators are *IR2111* and *6N136* ICs, respectively. It should be mentioned that an isolated power supply is used for each gate driver. The DSP TMS320F28335 from Texas Instrument has been used as a microcontroller to control the proposed multilevel converter comprising DFCM modules under the suggested modulation technique.

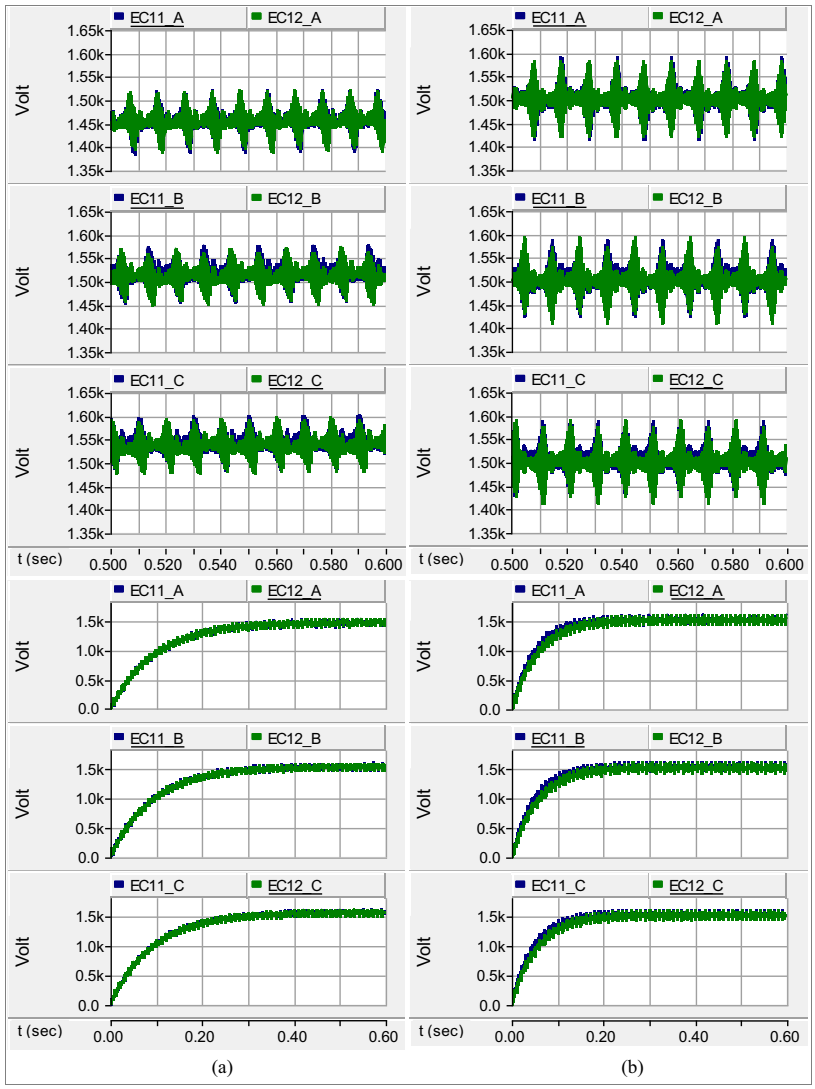


Fig. 12. FCs' voltages in the nine-level (line-to-neutral) proposed multilevel converter based on the cascade connection of two two-cell five-level DFCM modules: (a) proposed modulation technique; (b) modulation technique presented in [18].

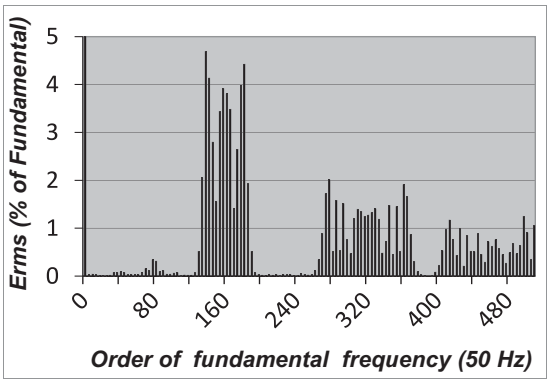


Fig. 13. Output voltage (line-to-neutral) frequency spectrum of the nine-level proposed multilevel converter based on the cascade connection of two two-cell five-level DFCM modules.

TABLE II
MAIN PARAMETERS OF THE SIMULATED THREE-PHASE 17-LEVEL (LINE-TO-LINE) PROPOSED MULTILEVEL CONVERTER BASED ON THE CASCADE CONNECTION OF TWO TWO-CELL FIVE-LEVEL DFCM MODULES

| System Parameters | Values |
|---|---|
| Converter power rating | 28 MVA |
| dc link voltage ($E$) | 3000 V |
| Flying capacitors ($C$) | 2000 $u$F |
| PS-PWM carrier frequency | 2 kHz |
| Fundamental output voltage frequency | 50 Hz |
| Resistive-inductive load impedance line-to-neutral ($Z$) | 1.5 Ω |
| Load power factor | 0.9 |

The measurement of the output voltage and load current, frequency spectrum of output voltage, and FC voltages taken from the prototype are presented in Figs. 14–16. The dc link voltage of each module is 48 V and the resistive–inductive load is 5 Ω and 2.6 mH. As shown in Fig. 15, output voltage of the nine-level proposed multilevel converter has harmonic clusters around integer multiples of 20 kHz, while the switching frequency is 5 kHz. As shown in Fig. 16, FC voltages are stabilized and fixed at their requisite values, i.e., 24 V, without any feedback control

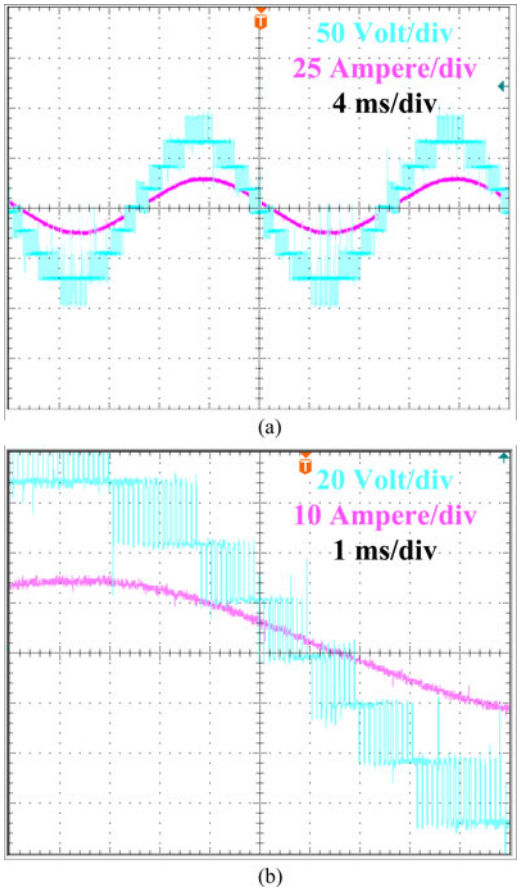


Fig. 14. Output voltage and load current in the nine-level (line-to-neutral) proposed multilevel converter based on the cascade connection of two two-cell five-level DFCM modules.

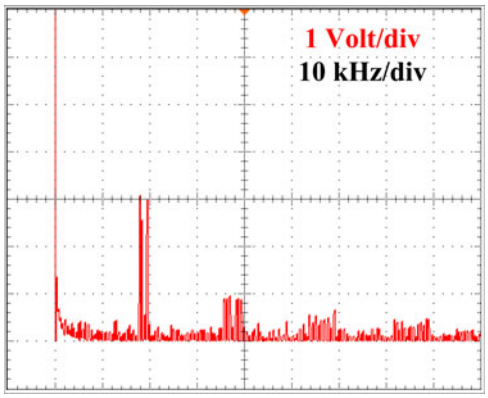


Fig. 15. Frequency spectrum of output voltage of the nine-level (line-to-neutral) proposed multilevel converter based on the cascade connection of two two-cell five-level DFCM modules.

signals, which substantiate the natural balancing property in the proposed multilevel converter operated under the suggested modulation technique.

## VI. Conclusion

The DFCM converters have significant advantages in comparison with FCM converters. However, voltage diversity of FCs

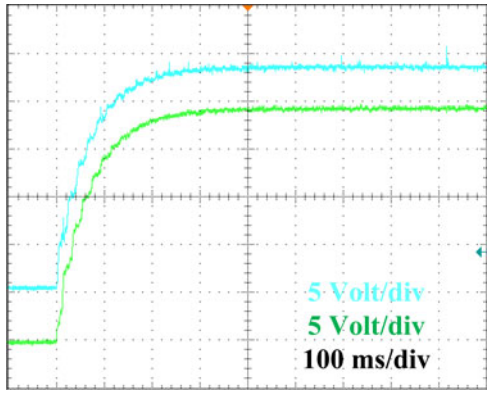


Fig. 16. FC voltages in the nine-level (line-to-neutral) proposed multilevel converter based on the cascade connection of two two-cell five-level DFCM modules.

is problematic in applications requiring a high number of cells. This paper proposed cascade connection of DFCM converters to increase the modularity of the inverter circuit. Moreover, a new modulation technique was proposed to control the converter properly. Since the proposed modulation technique is based on PS-PWM, FC voltages in DFCM modules, which are connected in series, stabilized at their target values. This confirms the natural voltage balancing feature of FCs in the proposed multilevel converter operated under the suggested modulation technique. Furthermore, the proposed modulation strategy reduces the voltage ripple across the FCs as well as the rms value of currents flowing through them. This advantage results in a decrease in FCs' capacitance, and consequently, physical size of the power converter. Using FCs with smaller capacitance reduces the converter cost, physical size, and installation area. Moreover, closed-form equations are derived to calculate the rms and average current flowing through the IGBTs/diodes in the DFCM converter. The derived closed-form equations are utilized to calculate the conduction power losses in the DFCM converter, and consequently, in the proposed multilevel converter, which is based on the cascade connection of the DFCM modules. Numerical results for the derived closed-form equations match the simulation results confirming their correctness. The proposed converter controlled with its new switching strategy is simulated and the results as well as experimental measurements were presented to validate their viability, effectiveness, and performance.

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