Hybrid Three-Level and Half-Bridge DC–DC Converter With Reduced Circulating Loss and Output Filter Inductance

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***Abstract*—A hybrid three-level (TL) and half-bridge (HB) dc–dc converter is proposed in this paper. The TL dc–dc converter and HB converter have their own transformers, respectively. Compared with conventional TL dc–dc converters, the proposed one has no additional switch at the primary side of the transformer, where the TL converter shares the lagging switches with the HB converter. In order to reduce the circulating current in the primary side, a blocking capacitor is used to reset the primary winding current of the TL converter. Moreover, the rectifier stage is composed of four diodes in the center-tap rectification, forcing the circulating current at the primary side to stay zero during the freewheeling period. The magnetizing inductor of the HB transformer can extend the zero voltage switching operation range of the lagging switches even at light loads. Furthermore, the proposed converter can reduce the output filter inductance. Due to the advantages mentioned above, the efficiency of the converter is improved dramatically. The features and design guidelines of the proposed converter are given in the paper. Finally, the performance of the converter is verified by a 1-kW experimental prototype.**

***Index Terms*—Phase shift, reduced circulating current, three-level (TL), zero voltage switching (ZVS).**

I. Introduction

DUE to the voltage stress reduced to half of the input voltage and the zero voltage switching (ZVS) of the switches, the three-level (TL) dc–dc converter is widely used in high input voltage applications. A series of TL dc–dc converters are proposed in [1], [2]. The essential relationships among the family of the TL dc–dc converter have been revealed in [3], and the phase-shift controlled manner is employed in TL dc–dc converters. However, it is difficult to achieve ZVS for lagging switches especially at light loads. The switching noise and electromagnetic interference caused by hard switching degrades the performance of the converter. Moreover, the circulating current reduces the efficiency as the input voltage increases.

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In order to extend the ZVS of lagging switches, an external inductor in series with the primary winding of the transformer is employed [2]. However, the inductor leads to a large duty cycle loss and a large ringing of the secondary rectifiers. An *LC* network with an inductor and two capacitors is used to achieve wide ZVS [4]. However, the additional inductor causes additional large circulating currents. An additional inductor with two clamping diodes can be used to achieve ZVS for lagging switches, and overshoot for secondary rectifiers can be suppressed [5]. Nevertheless, it still results in large duty cycle loss. Another approach for achieving ZVS for lagging switches is to enhance the magnetizing current to charge and discharge the junction capacitors by using two coupling inductors integrated in one core [6]. Besides, a TL converter achieving the ZVS for all switches is proposed in [7] by using two series-connected transformers. For the sake of extending the ZVS range for lagging switches, a TL dc–dc converter with an auxiliary coupling inductor at the primary side is reduced [8]. The energy stored in the auxiliary circuit is minimal at full loads and gradually increases as the load current decreases. However, large circulating currents still freewheels at the primary side. Resonant TL dc–dc converters have been proposed to regulate the output voltage with high efficiency by modulating the switching frequency [9]–[11]. However, the switching frequency may vary in a wide range especially at the light loads, which makes the magnetic components and EMC design difficult. In order to overcome the drawback of wide switching frequency variation in conventional resonant converters, phase-shift control is extended to the resonant TL dc–dc converter [12]–[14].

In order to reduce the circulating current and conduction loss, a blocking capacitor is used to reset the primary winding current. In order to avoid the current flowing to the reverse direction during the freewheeling period, two diodes are series connected with the lagging switches [15]. Although the circulating current can be reduced, the conduction loss may not be optimized because of more conduction loss caused by the two additional diodes. Furthermore, the lagging legs will lose the ZVS conditions. Therefore, insulated-gate bipolar transistor (IGBT) can be used for lagging switches to achieve zero voltage and zero current switching (ZVZCS). For ZVZCS TL dc–dc converters, MOSFETs are used for leading switches to achieve ZVS, and IGBTs are used for lagging switches to achieve ZCS [16]–[18]. However, using IGBTs limits the switching frequency of the converter and the power density cannot be high. Most of the researches on TL dc–dc converter focus on HB TL dc–dc converters. Full bridge (FB) TL dc–dc converters are investigated in

[19]–[21], but there are still some disadvantage to achieve soft switching, high efficiency, and high-frequency operation for the FB TL dc–dc converters.

In order to reduce the output filter inductance, hybrid TL dc–dc converters with more than one transformer have been proposed [22]–[26]. The transformers are series connected at the primary or secondary side to reduce the voltage across the filter inductor during the freewheeling period. However, large circulating current still freewheels at the primary side of the converter [22]–[25]. In order to solve this issue, a blocking capacitor is used to reset the primary circulating current in the hybrid converter [26]. Furthermore, a two diode should be series connected with the lagging switches to block the reverse flowing path. Therefore, the converter has to work in ZVZCS mode instead of ZVS mode.

In this paper, a hybrid TL and HB dc–dc converter with reduced circulating current and output filter inductance is proposed. A blocking capacitor is used to decay the primary circulating current. However, the lagging leg switches also can achieve ZVS by using the magnetizing inductor current of the HB transformer. At the secondary side of the transformer, a novel rectifier circuit configuration composed of four diodes is proposed, which forces the circulating current decreasing and equaling to zero instead of flowing to the opposite direction during the freewheeling period. In [23]–[26], the rectifiers of the hybrid converters are the same circuit, which is actually a center-tapped full waveform rectifier. Although the proposed converter has more diodes at the rectifier stage, the conduction loss at the secondary side is not increased. Due to the two more diode at the rectifier stage, the reverse flowing path at the primary side during the freewheeling period is cut off. Therefore, the diodes connected with lagging switches are unnecessary.

This paper is organized as follows. The circuit and mode operation of the proposed converter is described in Section II. In Section III, the main features of the proposed converter are analyzed. The design guidelines of the converter are presented in Section IV. The experimental prototype with 550∼600 V input voltage and 50 V/20A output is built to verify the performance of the proposed converter in Section V. Finally, the conclusions are given in Section VI.

II. Proposed Hybrid TL Plus Half Bridge DC–DC Converter

Fig. 1 shows the circuit configuration for the proposed converter, which is composed of a TL dc–dc converter and an HB dc–dc converter. The divided capacitors C_{d1}, C_{d2}, and the flying capacitor C_{ss1} and C_{ss2} are large enough to be treated as voltage sources, i.e., $V_{Cd1} = V_{Cd2} = V_{in}/2, V_{Css1} = V_{Css2} = V_{in}/4$. The output voltage regulation is implemented by the phase-shift manner. Q_1 and Q_4 are leading switches; Q_2 and Q_3 are lagging switches. The TL converter shares the lagging switches Q_2 and Q_3 with the HB dc–dc converter. $C_1 - C_4$ are junction capacitors of the switches, and $C_1 = C_2 = C_3 = C_4 = C$. T_{r1} is the transformer of the TL converter and T_{r2} is the transformer of the HB converter. The turns ratio of the two transformers T_{r1} and T_{r2} are $n_1 : 1 : 1$ and $n_2 : 1 : 1$, respectively. L_{k1} and

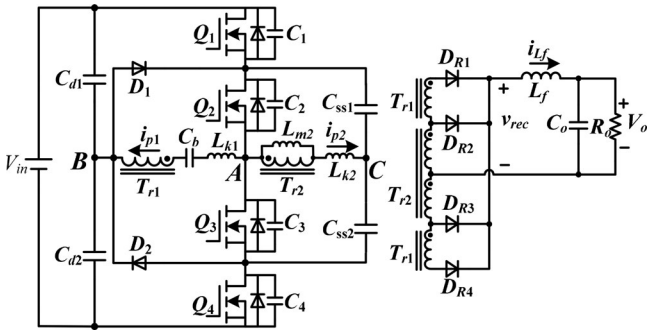

Fig. 1. Proposed hybrid TL plus HB converter.

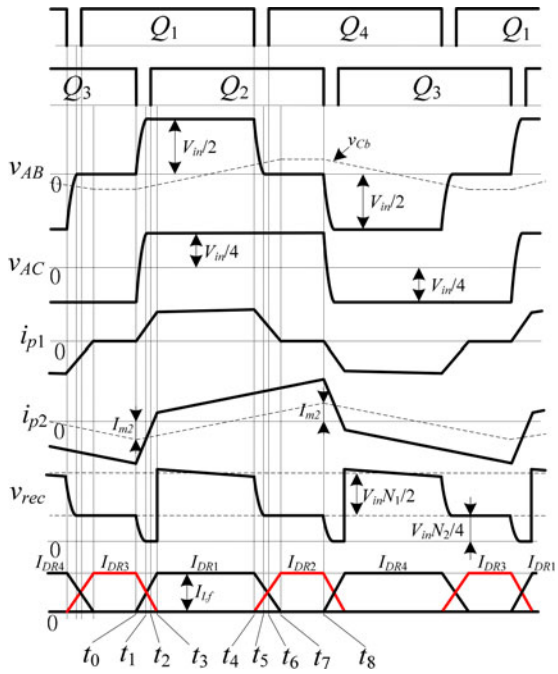

Fig. 2. Key waveforms of the proposed converter.

L_{k2} are the leakage inductors of T_{r1} and T_{r2}. The magnetizing inductor of T_{r1} is designed large enough, thus the magnetizing current during the switching period can be ignored. L_{m2} is the magnetizing inductor of T_{r2}. C_b is the blocking capacitor that is used to decay the primary current of T_{r1} and reduce the circulating current.

Fig. 2 shows the key waveforms of the proposed converter. There are eight working stages in each half-switching period.

Stage 1($[t_0, t_1]$) [see Fig. 3(a)]: Prior to t_0, Q_1, and Q_3 are on, and Q_2 and Q_4 are OFF. The primary current in T_{r1} stays at zero. The primary current in T_{r2} is negative. The output filter inductor current flows through D_{R3}. At time t_0, Q_3 is turned OFF. The voltage across the blocking capacitor is negative. The primary winding current in transformer T_{r2}, including the current reflected from the output current and the magnetizing current in T_{r2}, starts to charge and discharge the junction capacitors of Q_3 and Q_2, respectively. The primary winding current of T_{r1} starts to increase. Q_1 and D_2 conduct to charge the flying capacitors C_{ss1} and C_{ss2}. Since D_{R1} and D_{R3} are forward biased and

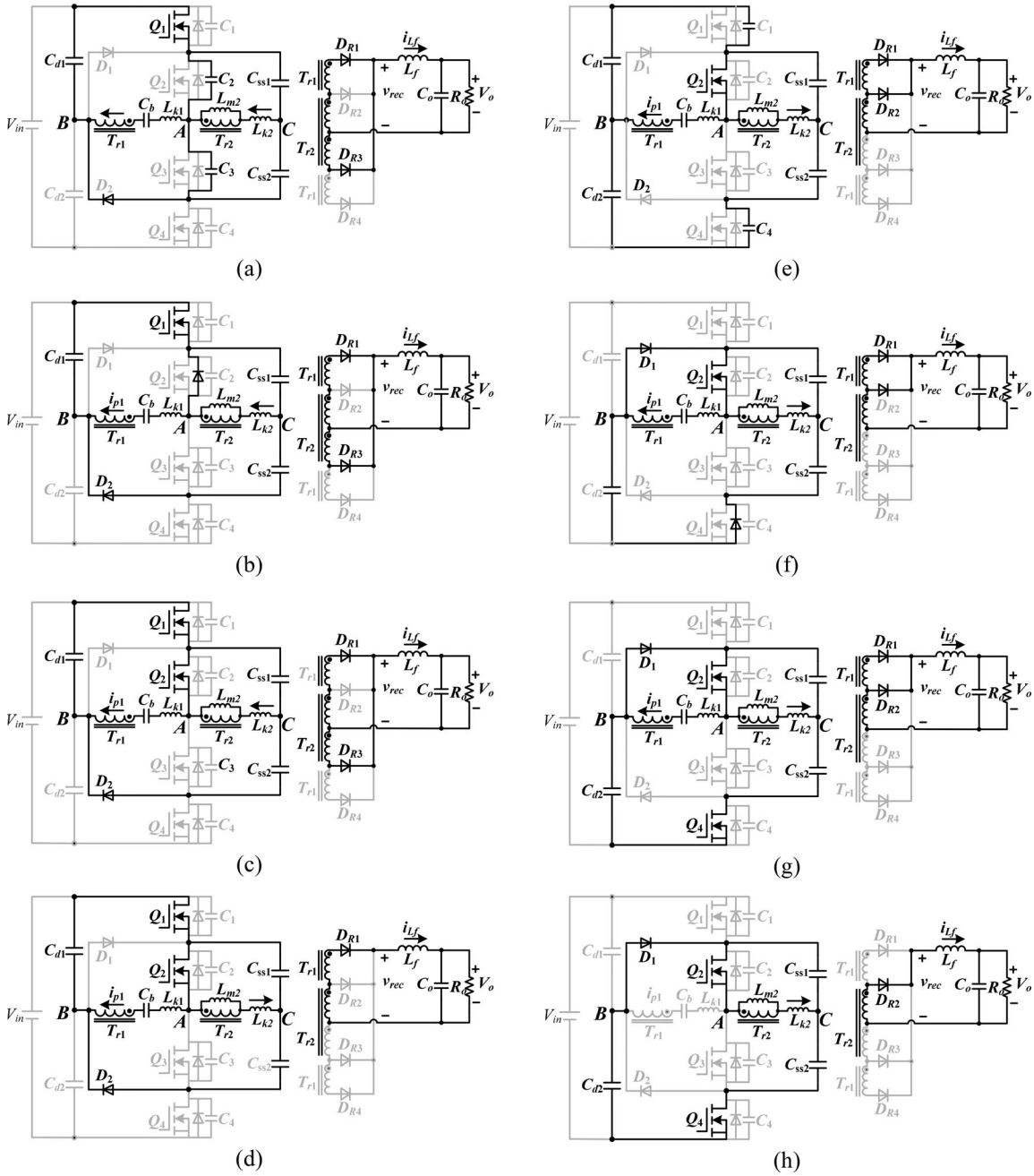

Fig. 3. Topological stages with half-switching cycle: (a) $[t_0, t_1]$, (b) $[t_1, t_2]$, (c) $[t_2, t_3]$, (d) $[t_3, t_4]$, (e) $[t_4, t_5]$, (f) $[t_5, t_6]$, (g) $[t_6, t_7]$, (h) $[t_7, t_8]$.

D_{R2} and D_{R4} are reverse biased, the current in D_{R1} starts to increase and the current in D_{R3} starts to decrease. The amplitude of the magnetizing current I_{m2} is expressed as

$$I_{m2} = \frac{V_{\text{in}} T_s}{16 L_{m2}} \tag{1}$$

where T_s is the switching period.

Stage 2 ($[t_1, t_2]$) [see Fig. 3(b)]: At time t_1, the drain-source voltage of Q_2 reaches zero, and i_{p2} flows through the body diode of Q_2. i_{p1} and i_{p2} both increase linearly. The blocking capacitor voltage v_{Cb} is charged by i_{p1}. Q_1 and D_2 still conduct to charge the flying capacitors C_{ss1} and C_{ss2}. The output filter inductor current i_{Lf} freewheels through D_{R1} and D_{R3}. The current in D_{R1} continues to increase, and the current in D_{R3} continues to decrease. i_{p1} and i_{p2} in this stage are expressed as

$$\begin{aligned} i_{p1}(t) &= i_{p1}(t_1) + \frac{V_{\text{in}} - 2v_{Cb}(t)}{2L_{k1}}(t - t_1) \\ i_{p2}(t) &= i_{p2}(t_1) + \frac{V_{\text{in}}}{4L_{k2}}(t - t_1) \end{aligned} \tag{2}$$

where $v_{Cb}(t)$ is the voltage across the blocking capacitor.

Stage 3 ($[t_2, t_3]$) [see Fig. 3(c)]: At time t_2, Q_2 is switched on with ZVS. i_{Lf} keeps on freewheeling through D_{R1} and D_{R3}. i_{p1} and i_{p2} still increase linearly as expressed in (2).

Stage 4 ($[t_3, t_4]$) [see Fig. 3(d)]: At time t_3, D_{R3} is reverse biased and all the filter inductor current flow through D_{R1}. The TL transformer and the HB transformer transfer energy to the output. The secondary winding current in T_{r2} is equal to that in T_{r1}. Ignoring the output current ripple, v_{Cb} is linearly charged by i_{p1}. $i_{p1,}$ i_{p2} and v_{rec} in this stage is expressed as

$$\begin{aligned} v_{rec}(t) &= \frac{V_{in}/2 - v_{Cb}(t-t_3)}{n_1} + \frac{V_{in}}{4n_2} \\ i_{p1}(t) &= \frac{I_{Lf}}{n_1} \\ i_{p2}(t) &= \frac{I_{Lf}}{n_2} - I_{m2} + \frac{V_{in}}{4L_{m2}}(t-t_0). \end{aligned} \tag{3}$$

Stage 5 ($[t_4, t_5]$) [see Fig. 3(e)]: When Q_1 is turned OFF at t_4, the voltages across the junction capacitors C_1 and C_4 are charged and discharged linearly by the energy stored in the output filter inductor $L_f.i_{p1}$ starts to decrease, so the current in D_{R1} decreases and the current in D_{R2} increases. The magnetizing inductor current in T_{r2} is still linearly increasing.

Stage 6 ($[t_5, t_6]$) [see Fig. 3(f)]: When C_1 reaches $V_{\rm in}/2$ and C_4 reaches zero, the body diode of Q_4 is forward biased. i_{p1} freewheels through D_1 and Q_2. The voltage across C_b is applied to the primary winding of T_{r1}, which forces i_{p1} to decrease rapidly. The current in D_{R1} continue decreasing and the current in D_{R2} continues increasing.

Stage 7 ($[t_6, t_7]$) [see Fig. 3(g)]: At time t_6, Q_4 is turned ON with ZVS. The primary winding current of T_{r1} continues decreasing and freewheels through D_1 and Q_2. The current in D_{R1} continues reducing and the current in D_{R2} continues increasing.

Stage 8 ($[t_7, t_8]$) [see Fig. 3(h)]: Stage 9 starts when i_{p1} decays to zero. D_1 and Q_4 still conduct to charge flying capacitors C_{ss1} and C_{ss2}. Then D_{R2} carries all the filter inductor current, and D_{R1} and D_{R4} are reverse biased. Therefore, the flowing path of the secondary current in T_{r1} is blocked. The filter inductor current only can flow through D_{R2} and the secondary winding of T_{r2}. Without current flowing in secondary winding of T_{r1}, the primary winding current in T_{r1} keeps zero. The voltage across C_b stays constant in this stage. i_{p2} and $v_{\rm rec}$ in this stage is expressed as

$$\begin{aligned} v_{\rm rec}(t) &= \frac{V_{\rm in}}{4n_2} \\ i_{p2}(t) &= \frac{I_{Lf}}{n_2} - I_{m2} + \frac{V_{\rm in}}{4L_{m2}}(t-t_0). \end{aligned} \tag{4}$$

III. Analysis of the Converter

A. DC Conversion Ratio

In practice, the voltage across the blocking capacitor is very low. Therefore, in order to simplify the analysis, it can be negligible. Moreover, ignoring the duty cycle loss, the dc conversion ratio of the converter in continuous conduction mode can be derived from the volt-second balance for the output filter, which

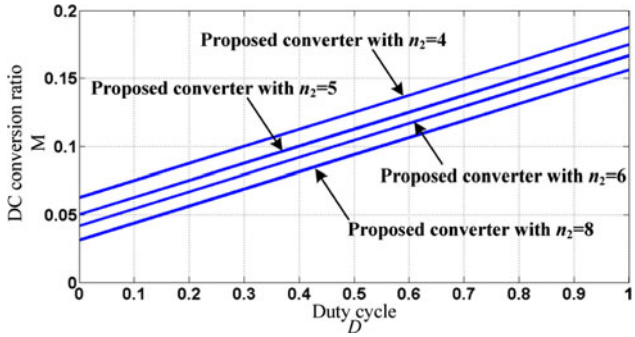

Fig. 4. DC conversion ratio versus duty cycle.

can be written by

$$\left(\frac{V_{\rm in}}{2n_1} + \frac{V_{\rm in}}{4n_2} - V_o\right) D + \left(\frac{V_{\rm in}}{4n_2} - V_o\right)(1-D) = 0 \tag{5}$$

where D is the duty cycle. Based on (5), the dc conversion ratio of the converter is expressed as

$$M = \frac{V_o}{V_{\rm in}} = \frac{D}{2n_1} + \frac{1}{4n_2}. \tag{6}$$

Fig. 4 shows dc conversion ratio versus duty cycle for different n_2 when $n_1 = 4$. As seen, for different n_2, the curves of the conversion ratios are parallel lines. As seen in (6), the lowest conversion ratio for the proposed converter is $1/4n_2$, which means the lowest conversion ratio is determined by the turns ratio of T_{r2}.

B. Voltage of the Blocking Capacitor

During one complete switching period, the time duration during t_0–t_3 and t_4–t_7 is rather short. Therefore, the maximum voltage across the blocking capacitor is approximately expressed as

$$v_{Cb\_\max} \approx \frac{1}{2C_b}\int_{t_3}^{t_4} \frac{I_{Lf}}{n_1} dt = \frac{I_{Lf}{\rm DT}_s}{4n_1 C_b}. \tag{7}$$

In terms of (7), the maximum voltage of the blocking capacitor is associated with the load current, duty cycle, and the capacitance of C_b. Larger capacitance of C_b can reduce its maximum voltage, but too low voltage can not allow i_{p1} to be reset to zero. Therefore, C_b should meet the following condition:

$$v_{Cb\_\max} \approx \frac{I_{Lf}DT_s}{4n_1 C_b} > L_{k1}\frac{I_{Lf}/n_1}{(1-D)T_s/2}. \tag{8}$$

Rewriting (8), the maximum value of C_b is expressed as

$$C_b < \frac{D(1-D)T_s^2}{8L_{k1}}. \tag{9}$$

Moreover, v_{Cb_max} should not be larger than $V_{\rm in}/2$, otherwise the working stage of the converter may become abnormal. The minimum value of C_b should meet the following condition:

$$v_{Cb\_\max} \approx \frac{I_{Lf}DT_s}{4n_1 C_b} < V_m \tag{10}$$

where V_m is the maximum allowable voltage, which is less than $V_{in}/2$. Therefore, the minimum value of C_b is expressed

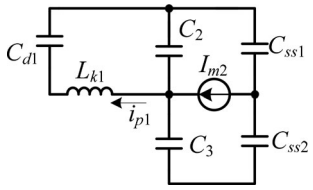

Fig. 5. Equivalent circuit in Stage 1 at light loads.

as

$$C_b > \frac{I_{Lf} D T_s}{4 n_1 V_m}. \tag{11}$$

C. ZVS Condition of Switches

In order to achieve ZVS for leading switches, their junction capacitor voltage should drop to zero before the switch is turned ON. In this working stage, the leading switches are charged and discharged by the primary currents in T_{r1} and T_{r2}, which are all reflected from the energy stored in the output filter inductor. Conventionally, the leading switches are easy to achieve ZVS even at light loads.

For the conventional TL dc–dc converter, the ZVS of lagging switches is achieved by the energy stored in the leakage inductor. For the proposed converter, the ZVS for lagging switches is achieved by the primary current in T_{r2}, which include the energy stored in the leakage inductor and magnetizing inductor of T_{r2}. At heavy loads, the energy stored in the leakage inductor of T_{r2} is large enough to achieve ZVS. However, at light loads, the energy stored in the leakage inductor is too low to achieve ZVS. In this case, the magnetizing inductor current should be large enough to charge and discharge the junction capacitors of the lagging switches. Ignoring the low leakage inductor current of T_{r2} at light loads, the equivalent circuit in Stage 1 is shown in Fig. 5.

Moreover, the initial state in this stage is $v_{C2}(0) = V_{in}/2, v_{C3}(0) = 0$, and $i_{p1}(0) = 0$. According to Fig. 5, the primary current in T_{r1} and voltages across C_2 and C_3 are expressed as

$$\begin{aligned} i_{p1} &= I_{m2} - I_{m2}\cos[\omega_m (t - t_0)] \\ v_{C_2}(t) &= \frac{V_{in}}{2} - \frac{I_{m2}}{2C\omega_m} \cdot \sin[\omega_m (t - t_0)] \\ v_{C_3}(t) &= \frac{I_{m2}}{2C\omega_m} \cdot \sin[\omega_m (t - t_0)] \end{aligned} \tag{12}$$

where $\omega_m = 1/\sqrt{2CL_{k1}}$. In order to achieve ZVS for the lagging switches, the voltage across C_2 should be discharged to zero within the dead time, which is given by

$$\begin{aligned} v_{C2} &= \frac{V_{\text{in}}}{2} - \frac{I_{m2}}{2C\omega_m}\sin\omega_m t_{\text{dead}} \\ &= \frac{V_{in}}{2} - \frac{V_{\text{in}} T_s}{32 L_{m2} C\omega_m}\sin\omega_m t_{\text{dead}} \le 0. \end{aligned} \tag{13}$$

Hence, the magnetizing inductance L_{m2} for the ZVS condition should be designed as follows:

$$L_{m2} \le \frac{T_s}{16C\omega_m}\sin\omega_m t_{\text{dead}} \tag{14}$$

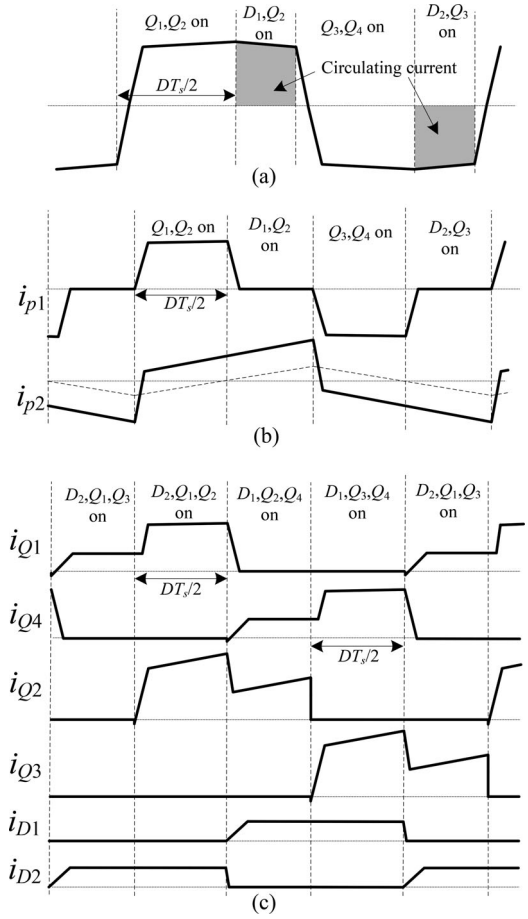

Fig. 6. Primary winding current of the transformers and the currents of the primary semiconductors (a) Conventional TL converter, (b) Proposed converter, (c) Currents of the primary semiconductors.

where t_{dead} is the dead time between Q_2 and Q_3. As seen in (14), the ZVS condition is independent of the loads. With the aid of the magnetizing inductor of the T_{r2}, the ZVS of lagging switches can be ensured within a wide load range.

D. Current Stress of the Primary Semiconductors.

The primary winding currents in the transformers of the conventional TL converter and the proposed converter are shown in Fig. 6(a) and (b). Fig. 6(c) shows the currents of the primary semiconductors. As seen in Fig. 6(a), ignoring the duty cycle loss and output current ripple, the primary winding rms current in the conventional TL dc–dc converter $I_{p1\_c}^{rms}$ can be expressed as

$$I_{p1\_c}^{rms} \approx \frac{V_o}{nR_o}. \tag{15}$$

Therefore, the rms current in leading switches Q_1 and Q_4 is approximately evaluated as $I_{p1\_c}^{rms}\sqrt{\frac{D}{2}} \approx \frac{V_o}{n_1 R_o}\sqrt{nM}$. Furthermore, the rms current of the lagging switches Q_2 and Q_3 is expressed as $I_{pr1\_c}^{rms}/\sqrt{2}$. The current freewheels through the clamping diode and lagging switch during the freewheeling interval. Ignoring the output current ripple and duty cycle loss, the rms current in the primary clamping diodes for conventional

TL converter is expressed as

$$i_{D1,D2\_conv}^{rms} = \sqrt{\frac{1}{Ts}\int_{D\frac{T_s}{2}}^{\frac{T_s}{2}}\left(\frac{V_o}{nR_o}\right)^2 dt} = \frac{V_o}{n_1 R_o}\sqrt{\frac{1-D}{2}} \approx \frac{V_o}{n_1 R_o}\sqrt{\frac{1}{2}-nM}. \quad (16)$$

As seen in Fig. 6(b) and (c), for the proposed converter, the primary winding current amplitude of T_{r1} is equal to V_o/n_1R_o. During Stage 5–8, the current flows through the leading switch and clamping diode to charge capacitors C_{ss1} and C_{ss2}, and the current is approximately equal to $\left(\frac{V_o}{R_o}\frac{V_{in}}{4n_2}\right)/\frac{V_{\rm in}}{2} = \frac{V_o}{2n_2R_o}$. Therefore, ignoring the output current ripple and duty cycle loss, the rms current flowing through the leading switches for the proposed converter is approximately evaluated as

$$\begin{aligned} & i_{Q1,Q4}^{\rm rms} \\ &= \sqrt{\frac{1}{Ts}\left(\int_0^{D\frac{T_s}{2}}\left(\frac{V_o}{n_1R_o}+\frac{V_o}{2n_2R_o}\right)^2 dt + \int_{D\frac{T_s}{2}}^{\frac{T_s}{2}}\left(\frac{V_o}{2n_2R_o}\right)^2 dt\right)} \\ &= \frac{V_o}{R_o}\sqrt{\frac{1}{8n_2^2}+\left(\frac{1}{2n_1^2}+\frac{1}{2n_1n_2}\right)D} \\ &\approx \frac{V_o}{R_o}\sqrt{\frac{1}{8n_2^2}+\left(\frac{1}{2n_1^2}+\frac{1}{2n_1n_2}\right)\left(2n_1M-\frac{n_1}{2n_2}\right)}. \end{aligned} \quad (17)$$

The rms current in the clamping diodes is expressed as

$$i_{D1,D2}^{\rm rms} = \sqrt{\frac{1}{Ts}\int_0^{\frac{T_s}{2}}\left(\frac{V_o}{2n_2R_o}\right)^2 dt} = \frac{V_o}{2\sqrt{2}n_2R_o}. \quad (18)$$

As seen in (17), the rms current in the clamping diodes of the conventional TL dc–dc converter is related with the duty cycle and output power. In order to reduce the conduction loss, the duty cycle should be large enough. Comparatively, the rms current in the clamping diodes of the proposed converter is related with the turns ratio of T_{r2} and output power. As seen, *as* n_2 increases, the rms current in the clamping diodes decreases. Therefore, in order to reduce the conduction loss, the turns ratio of T_{r2} should not be designed too low. If n_2 is too low, $T_{\rm r2}$ will transfer more power to the load, which may cause more conduction loss.

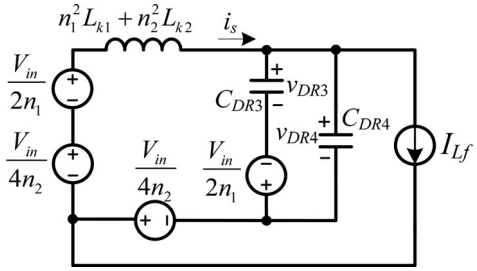

Fig. 7. Equivalent circuit of the secondary side in Stage 4.

During Stage 1–8, the magnetizing inductor current is expressed as

$$i_{Lm2}(t) = -I_{m2} + \frac{V_{\rm in}}{4L_{m2}}t. \quad (19)$$

The rms current in the lagging switches for the proposed converter is evaluated in Eqn. (20) as shown at the bottom of page.

The rms current in the primary semiconductors is related with the turns ratio of the two transformers. In order to minimize conduction loss, the turns ratio of the two transformers should be optimized, which will be discussed in detail in Section IV.

E. Voltage Stress of the Secondary Diodes

The equivalent circuit of the secondary side in Stage 4 is shown in Fig. 7, where C_{DR3} and C_{DR4} are the junction capacitance of D_{R3} and D_{R4}. Output filter inductor is supposed large enough, so the output filter inductor current can be viewed as a current source. The initial state in this Stage is $v_{DR3}(0) = v_{DR4}(0) = 0, i_s(0) = I_{Lf}$, and $i_{DR3}(0) = i_{DR4}(0) = 0$.

Assuming $C_{DR3} = C_{DR4} = C_D, v_{CD4}(t), v_{CD3}(t)$, and $i_s(t)$ are written by

$$\begin{aligned} v_{DR4}(t) &= \left(\frac{V_{in}}{n_1}+\frac{V_{in}}{2n_2}\right)[1-\cos(\omega_n(t-t_3))] \\ v_{DR3}(t) &= \left(\frac{V_{in}}{2n_1}+\frac{V_{in}}{2n_2}\right)[1-\cos(\omega_n(t-t_3))] \\ i_s(t) &= \left(\frac{V_{in}}{n_1}+\frac{V_{in}}{2n_2}\right)\frac{1}{(n_1^2L_{k1}+n_2^2L_{k2})\,\omega_n} \\ &\quad \times \sin(\omega_n(t-t_3)) + I_{Lf} \end{aligned} \quad (21)$$

$$\begin{aligned} i_{Q2,Q3}^{\rm rms} &= \sqrt{\frac{1}{Ts}\left[\int_0^{D\frac{T_s}{2}}\left(\frac{V_o}{n_1R_o}+i_{Lm2}(t)+\frac{V_o}{n_2R_o}\right)^2 dt + \int_{D\frac{T_s}{2}}^{\frac{T_s}{2}}\left(i_{Lm2}(t)+\frac{V_o}{n_2R_o}\right)^2 dt\right]} \\ &= \sqrt{\left(\frac{1}{2n_1}+\frac{1}{n_2}\right)\frac{V_o^2D}{n_1R_o^2} - \frac{V_oV_{\rm in}T_sD(1-D)}{16L_{m2}n_1R_o} + \frac{V_o^2}{2n_2^2R_o^2} + \frac{V_{\rm in}^2T_s^2}{1536L_{m2}^2}} \\ &\approx \sqrt{\left(\frac{1}{2n_1}+\frac{1}{n_2}\right)\left(2n_1M-\frac{n_1}{2n_2}\right)\frac{V_o^2}{n_1R_o^2} - \left(2n_1M-\frac{n_1}{2n_2}\right)\left(1-2n_1M+\frac{n_1}{2n_2}\right)\frac{V_oV_{\rm in}T_s}{16L_{m2}n_1R_o} + \frac{V_o^2}{2n_2^2R_o^2} + \frac{V_{\rm in}^2T_s^2}{1536L_{m2}^2}} \end{aligned} \quad (20)$$

where $\omega_n = 1/\sqrt{2C_D\left(n_1^2 L_{k1} + n_2^2 L_{k2}\right)}$. Therefore, ignoring the reverse recovery of the body diode, the maximum voltage of D_{R1} and D_{R4} is equal to $\frac{2V_{\rm in}}{n_1} + \frac{V_{\rm in}}{n_2}$, and the maximum voltage of D_{R2} and D_{R3} is equal to $\frac{V_{\rm in}}{n_1} + \frac{V_{\rm in}}{n_2}$. The voltage stress of D_{R2} and D_{R3} is lower than D_{R1} and D_{R4}.

IV. Design Considerations

This section introduces a design example of the proposed converter with 550 $\sim$ 600V input voltage and 50V/20A output. Therefore, the rated load resistance is 2.5Ω. A switching frequency of 100 kHz is adopted.

A. Turns Ratio of the Two Transformers

In order to design the two transformers, the power ratio of the two transformers should be chosen to the desired value. As illustrated in Section III E, in order to reduce the conduction loss, T_{r2} should not transfer too much power to the load. Therefore, the power ratio of the two transformers is initially selected as 2. At full loads, T_{r2} provides approximately 300 W power. Therefore, the turns ratio of T_{r2} is expressed as

$$n_2 = \frac{V_{\rm in} I_{Lf}}{4P_{T_{r2}}} = \frac{550 \times 20}{4 \times 300} = 9.16. \tag{22}$$

Therefore, the turns ratio of T_{r2} is designed as 9:1:1.

At the minimum input voltage, the duty cycle of the converter is initially chosen as 0.7. Therefore, in terms of (6), the turns ratio of T_{r1} is expressed as

$$n_2 = \frac{D}{2\left(\frac{V_o}{V_{in}} - \frac{1}{4n_2}\right)} = \frac{0.7}{2 \times \left(\frac{50}{550} - \frac{1}{4\times 9}\right)} = 5.54. \tag{23}$$

Consequently, the turns ratio of T_{r1} is designed as 5.5:1:1. At the minimum input voltage, the effective duty cycle is 0.69. At the maximum input voltage, the effective duty cycle is 0.61. For the conventional TL dc–dc operating within the same duty cycle range, the turns ratio of the transformer can be expressed as $n = \frac{DV_{\rm in}}{2V_o} = \frac{0.7\times 550}{2\times 50} = 3.85$. Therefore, it can be selected as 3.8:1:1.

B. Filter Inductor and Current Ripple

For conventional TL dc–dc converter, the voltage applied on the filter inductor is $V_{\rm in}/2n_1 - V_o$ during the power transmission, while the value is $-V_{\rm o}$ during the freewheeling period. Therefore, the current ripple of the filter inductor Δi_{Lf_c} is given by

$$\Delta i_{Lf\_c} = \frac{T_s V_{in}(1 - 2n_1 V_o/V_{\rm in}) 2n_1 V_o/V_{\rm in}}{4nL_f}. \tag{24}$$

As seen in Fig. 8, for the proposed converter, ignoring the voltage across the blocking capacitor, the voltage applied on the filter inductor is $V_{\rm in}/2n_1 + V_{\rm in}/4n_2 - V_o$ during the power transmission. During the freewheeling period, the value is $V_{\rm in}/4n_2 – V_o$. The current ripple of the filter inductor for the proposed converter is expressed as

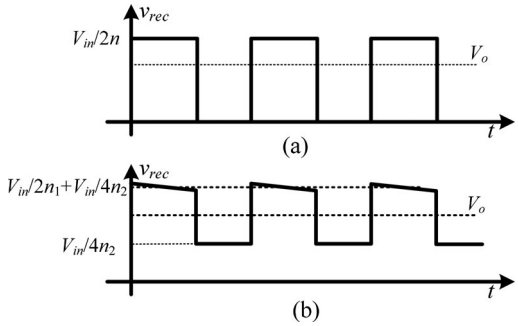

Fig. 8. Idealized rectifier voltage $v_{\rm rec}$ (a) conventional TL converter (b) proposed converter.

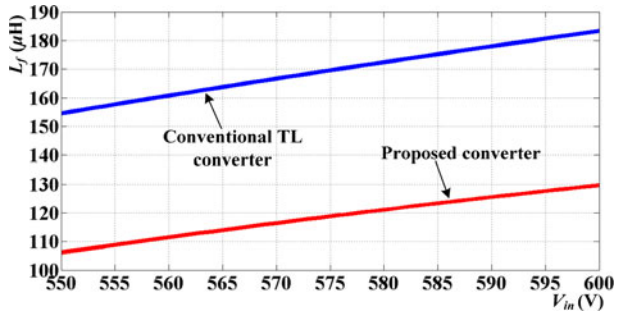

Fig. 9. Filter inductance as the function of input voltage for the desired current ripple.

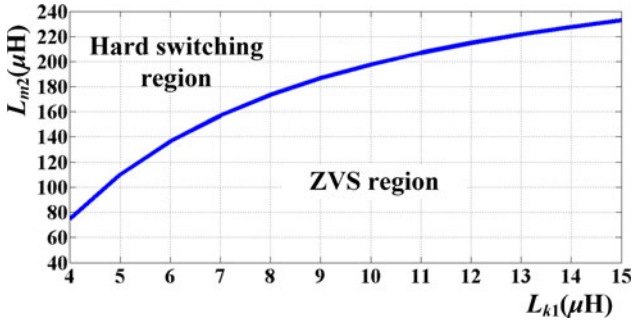

Fig. 10. Magnetizing inductance of T_{r2} versus the leakage inductance of T_{r1}.

$$\Delta i_{Lf} = \frac{T_s V_{\rm in}\left(1 - 2n_1 V_o/V_{\rm in} + n_1/(2n_2)\right)\left(2n_1 V_o/V_{\rm in} - n_1/(2n_2)\right)}{4n_1 L_f}. \tag{25}$$

For the desired output current ripple $\Delta I_{Lf} = 0.5$A and the turns ratio of the transformer designed in Section IV A, the output filter inductance versus input voltages is shown in Fig. 9. As seen in Fig. 9, compared with the conventional TL converter, the filter inductance of the proposed converter is dramatically reduced. Furthermore, the filter size and copper loss of the inductor can be reduced. Eventually, the filter inductance L_f is designed as 130 μH.

C. Magnetizing Inductance of the HB Transformer

With the specification of $C = 200p$F, $T_{\rm s} = 10$ μs and $t_{\rm dead} = 100n$s, the magnetizing inductance of T_{r2} versus the leakage inductance L_{k1} in terms of (14) is shown in Fig. 10. As seen, with the increase of L_{k1}, the magnetizing inductance L_{m2} increases.

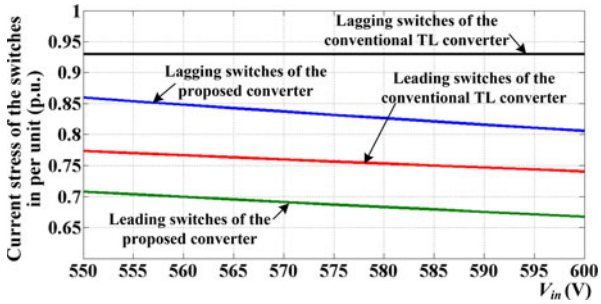

Fig. 11. Rms current of the switches in per unit as the function of the input voltage.

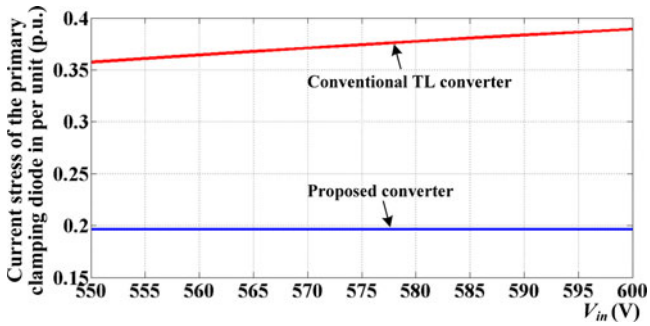

Fig. 12. Rms current of the primary clamping diodes in per unit as the function of the input voltage.

In this case, the magnetizing current in T_{r2} can be reduced, and the circulating current is reduced as well. However, larger L_{k1} causes larger duty cycle loss. Therefore, there is a tradeoff between the duty cycle loss and magnetizing current in T_{r2}.

In this paper, the leakage inductance L_{k1} is chosen as 8 μH. Therefore, the ZVS condition for lagging switches is $L_{m2} \leq$ 173 μH. Eventually, the magnetizing inductor L_{m2} is designed as 170 μH.

D. Current Stress Comparison of the Primary Semiconductors

According to the turns ratio of the transformers and magnetizing inductance L_{m2} in this section, the rms currents of the switches in per unit versus the input voltages in terms of (17) and (20) are shown in Fig. 11. As seen in Fig. 11, the current stress of the proposed converter is lower than the conventional TL converter. As analyzed in Section IV A, in order to achieve the same conversion ratio with the same duty cycle range, the turns ratio of T_{r1} for proposed converter is larger than the conventional TL converter, so the current amplitude in the primary winding of T_{r1} is lower than the conventional TL converter. Hence, the current stress of leading switches is lower than the conventional TL converter. Fig. 6(a) illustrates the circulating current of the conventional TL converter. During the freewheeling period, the lagging switches and clamping diodes have to handle higher circulating currents, causing more conduction loss. Fig. 6(b) illustrates that i_{p1} is reset to zero when the output inductor works in the freewheeling period, reducing the rms current of the lagging switches. Although the primary winding current in T_{r2} flows through the lagging switches and clamping diodes, the current stress is also lower than the conventional TL converter. Fig. 12 shows the rms current in the clamping diodes in per unit versus the input voltage. Due to the reduced circulating current, the rms current in the clamping diodes is lower than that of the conventional TL converter.

E. Blocking Capacitor C_b

The maximum voltage across the blocking capacitor is desired to be less than 100 V. According to (9) and (11), the capacitance C_b should meet the following requirements:

$$\begin{cases} C_b > \dfrac{I_{Lf} D T_s}{4 n_1 V_m} = \dfrac{20 \times 0.69 \times 10 \times 10^{-6}}{4 \times 5.5 \times 100} = 125.4(nF) \\ C_b < \dfrac{D(1-D)T_s^2}{8 L_{k1}} = \dfrac{0.69 \times (1-0.69) \times (10 \times 10^{-6})^2}{8 \times 8 \times 10^{-6}} \\ \quad = 334(nF). \end{cases} \tag{26}$$

Then C_b is chosen as 150 *nF*.

V. Experimental Verifications

In order to verify the performance of the proposed converter, a 1-kW prototype is built. The specifications of the prototype are given as follows: $V_{\rm in} = 550\text{V} \sim 600\text{V}$, $V_o = 50\text{V}$, $n_1 = 5.5$, $n_2 = 9$, $C_{d1} = C_{d2} = 20$ μF, $C_{ss1} = C_{ss2} = 4.7$ μF, $C = 200p$F, $C_b = 150n$F, $L_{m2} = 170$ μH, $L_f = 130\mu$H, $C_o = 220\mu$F. The switching frequency is 100 kHz. Each primary switch is FDP18N50. The primary clamping diode is DSEP12–12A. Rectifier diodes D_{R1} and D_{R4} are FFH30US30DN, whose forward voltage drop is 1 V. Rectifiers D_{R2} and D_{R3} are MBR20200CT, whose forward voltage drop is 0.8 V. A RCD snubber circuit is used to reduce the voltage spike of the rectifier diodes. The snubber circuit is composed of a 620 Ω resistor, a 10 *n*F capacitor, and a diode. The experimental results are shown from Fig. 13–Fig. 15.

Fig. 13 shows the key waveforms at different input voltages and output power, where *P* is the output power. Fig. 13(a) shows the experimental waveforms when $V_{\rm in} = 550\text{V}$ and $P = 1000\text{W}$. Fig. 13(b) shows the experimental waveforms when $V_{\rm in} = 600\text{V}$, and $P = 1000\text{W}$. With the increase of the input voltage, the duty cycle of the proposed converter decreases. Fig. 13(c) shows the experimental waveforms when $V_{\rm in} = 550\text{V}$ and $P = 200\text{W}$. The current amplitudes of $\rm i_{p1}$ and i_{p2} are both reduced as the output power decreases. As expected, current i_{p1} in the three mentioned cases are all reset to zero during the freewheeling period, which minimizes the conduction loss in the primary side circuit.

Fig. 14 shows current in Q_4, current in clamping diode D_1, gate signal, and drain-source voltage of switch Q_4. Fig. 14(a) shows ZVS of the leading switches at heavy loads. Fig. 14(b) shows the ZVS of the leading switches at light loads. Before Q_4 is turned on, the current in Q_4 is negative. The junction capacitor of Q_4 is discharged until the current flows through its body diode. Fig. 15 shows current in Q_3, primary winding current in T_{r2}, gate signal, and drain-source voltage of switch Q_3. Fig. 15(a) shows the ZVS of lagging switches at the heavy load. Fig. 15(b) highlights the ZVS operation of lagging switches at the light load. As seen in the experimental results, before Q_3 is turned on, the current in Q_3 is negative. The junction capacitor of Q_3 is also discharged until the current flows through its body

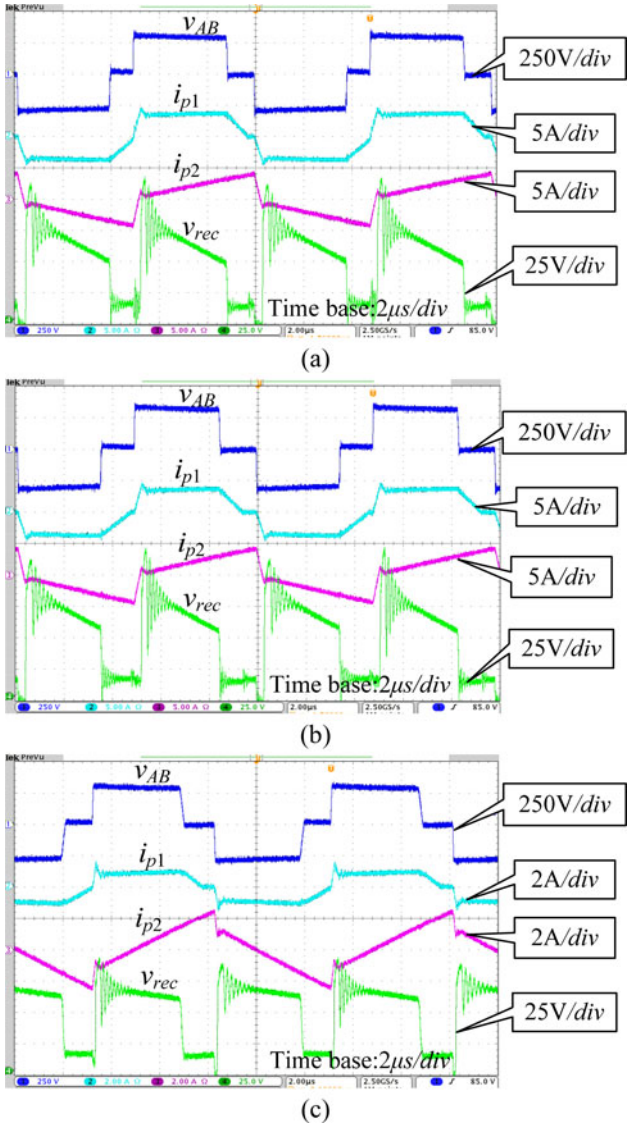

Fig. 13. Measured key waveform of the proposed converter (a) at $V_{\rm in} = 550$V and $P = 1000$W, (b) at $V_{\rm in} = 600$V and $P = 1000$W, and (c) at $V_{\rm in} = 550$V and $P = 200$W.

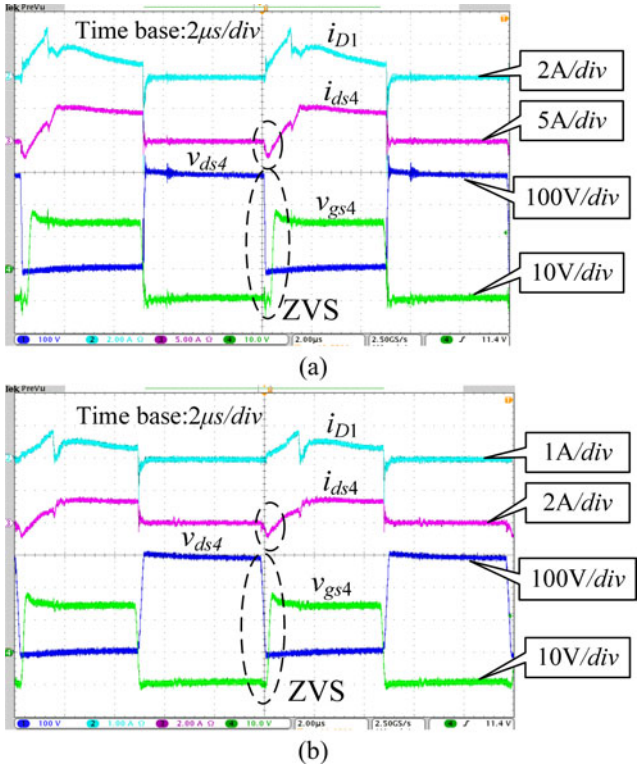

Fig. 14. Current of Q_4, primary current of the clamping diode D_1, and gate signal and drain-source voltage of switch Q_4, (a) at $V_{\rm in} = 550$V and $P = 1000$ W and (b) at $V_{\rm in} = 550$V and $P = 200$W.

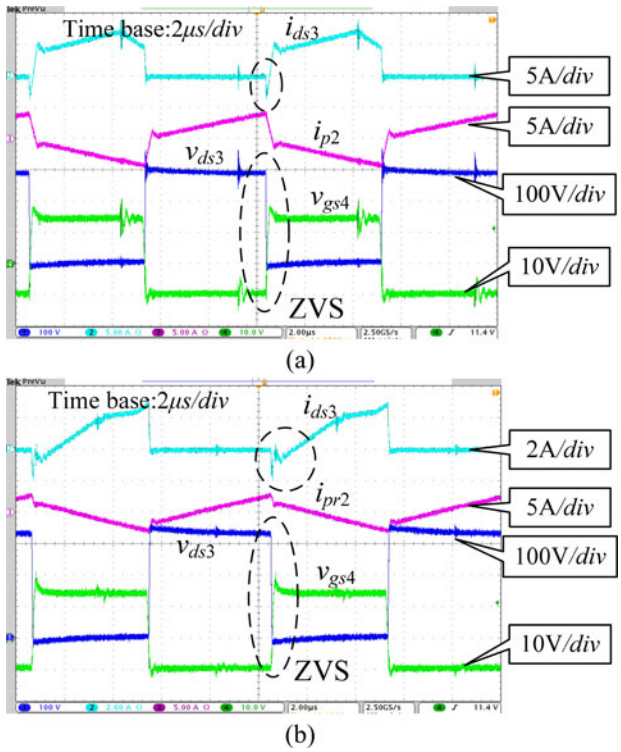

Fig. 15. Current of Q_4, current of T_{r2}, and gate signal and drain-source voltage of switch Q_3 (a) at $V_{\rm in} = 550$V and $P = 1000$W and (b) at $V_{\rm in} = 550V$ and $P = 200$W.

diode. Therefore, ZVS for all the switches is achieved over the wide load range.

In order to compare the volume of the proposed converter with the conventional one, the prototypes of the conventional TL converter is built by using the same switches and rectifier diodes as the proposed prototype. The other main components are shown in Table I.

As seen in Table I, the smaller inductor core is used for the proposed converter. Due to the reduced output current ripple, the output inductance is lower than the conventional TL converter. Therefore, smaller core and lower filter inductance leads to lower core loss and copper loss. It will be demonstrated in Fig. 17. The proposed converter distributes the power between transformers T_{r1} and T_{r2}. Although two transformers are needed, the total transformer volume is still less than the conventional one. Compared with the conventional TL converter,

TABLE I
MAIN COMPONENTS AND THEIR VOLUME

	Conventional TL converter	Proposed converter
Output Inductor core	Kool Mμ 77 195 (with 27 turns)	Kool Mμ 77 715 (with 29 turns)
Output inductor volume	79 599 mm^3	58 353 mm^3
Transformer core	EE47/20/16	T_{r1} E40/27/12+I40/7.5/12 T_{r2} E33/23/13+I33/5/13
Transformer volume	62040 mm^3	T_{r1} 34 000 mm^3; T_{r2} 23 925 mm^3
Fly capacitors	630 V 2.2μF	250 V 4.7μF 2ea
Fly capacitor volume	28 mm×19 mm×11 mm (5852 mm^3)	24 mm × 19 mm × 11 mm (5016 mm^3 2ea)
Output capacitor	100 V 220 μF (electrolytic capacitor)	
Output capacitor volume	1307 mm^3	

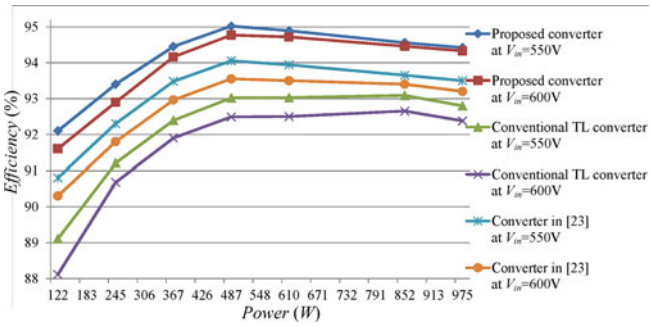

Fig. 16. Efficiency for the proposed converter, the conventional TL converter, and the converter in [23].

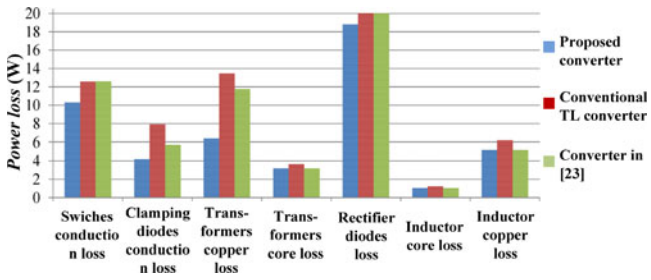

Fig. 17. Calculated power loss distribution at rated load when $\mathrm{V_{in}} = 550\mathrm{V}$.

the fly capacitor in the proposed converter is split into two. Although the voltage rating of the flying capacitor is reduced, the total volume of the flying capacitor is a little bit larger than the conventional one. However, synthesizing the volume of the major components, the power density of the proposed converter still can be improved.

The measured efficiency curves for the proposed converter, the converter in [23], and the conventional TL converter are shown in Fig. 16. Compared with the conventional TL converter, due to the reduced circulating current, the efficiency of the proposed one is greatly improved. At $V_{\mathrm{in}} = 600\mathrm{V}$, the maximum improvement at light loads is 4%, and the improvement at heavy loads is more than 2%. For the converter in [23], although the ZVS of the switches is achieved, circulating currents still freewheels at the primary side of the transformer during the freewheeling period. Therefore, the efficiency of the proposed one is higher than the converter in [23].

Fig. 17 shows the comparison of the calculated power loss distribution at full load when $V_{\mathrm{in}} = 550\mathrm{V}$. Due to the reduced circulating current, the switches conduction loss, the clamping diodes conduction loss, and the transformer copper loss are all reduced. By using smaller volume of the cores, the transformer core loss is reduced. The lower voltage rating diodes, such as Schottky diodes, are used for D_{R2} and D_{R3}, whose forward voltage drop is lower. Therefore, the conduction loss in the rectifier stage is reduced. To sum up, the efficiency of the proposed converter is higher than the conventional converter.

VI. CONCLUSION

In this paper, a hybrid TL and HB dc–dc converter by sharing the lagging switches to reduce the circulating current and output filter inductance is proposed for higher efficiency. Since the switches only undergo half of the input voltage, the proposed converter is suitable for high input voltage applications. The magnetizing inductor of the HB transformer can extend the ZVS of the lagging switches. The blocking capacitor together with the secondary novel-rectifying configuration can reset the circulating currents at the primary windings. Compared with the conventional TL dc–dc converter, the current stress of the switches and clamping diodes are all reduced, resulting in lower conduction loss. The good performance and design method has been verified by a 1-kW experimental prototype.

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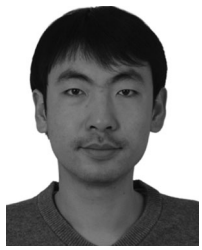

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