Enabling High-Frequency High-Efficiency Non-Isolated Boost Converters With Quasi-Square-Wave Zero-Voltage Switching and On-Chip Dynamic Dead-Time-Controlled Synchronous Gate Drive

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***Abstract*—This paper presents techniques to enable non-isolated boost converters to achieve high power efficiencies under high switching frequency and high-voltage conditions. A quasi-square-wave zero-voltage switching (QSW-ZVS) boost converter topology is proposed to achieve high-frequency soft switching without any coupled inductors in the power stage and, thus, minimize the switching power loss of the converter. An on-chip dynamic dead-time controller is developed to provide near-optimum dead time for power FETs during switching transitions under different output voltage and load current conditions in order to achieve ZVS with minimal body diode conduction loss of power FETs. A synchronous gate driver is also proposed to provide fast propagation delays and output signal rise/fall time, enabling megahertz operation of the converter. A hardware boost converter prototype is built with the synchronous gate driver circuitry implemented in a 0.5-μm high-voltage CMOS process. The proposed QSW-ZVS boost converter provides an output voltage of 150 V and delivers an output power of 130 W. The peak power efficiency of the proposed converter achieves 92.7% at the switching frequency of 1 MHz. Compared with state-of-the-art gate drivers, the worst-case propagation delay of the proposed synchronous gate driver is improved by at least 7.6 times. The operation frequency of the proposed non-isolated boost converter is also improved by at least 15 times compared with other state-of-the-art counterparts.**

***Index Terms*—Dynamic dead-time controller (DDTC), high-frequency boost converters, high-voltage (HV) synchronous gate driver, quasi-square-wave zero-voltage switching (QSW-ZVS), zero-voltage switching (ZVS) technique.**

I. Introduction

In recent years, 100s-of-Watt non-isolated boost converters are commonly used in microinverters to first step-up low dc voltage to the line voltage before dc–ac conversions for photovoltaic and fuel-cell systems [1]–[4]. To design these non-isolated boost converters, many previous efforts have focused on exploring various converter topologies to realize high step-up ratios [4]–[10]. It is, however, lack of discussions in the literature on how to lower the cost and improve the power density of these converters by reducing their volume and weight. In fact, for low cost and high power density considerations, both the number and the size of off-chip components need to be minimized in these boost converters. The required number of passive components can be reduced by selecting proper converter topology and its switching scheme after taking the converter power efficiency into considerations. The required size of components such as the inductor and the capacitor in the power stage can be decreased by increasing the converter switching frequency. Operating the converter at a high switching frequency could, however, be limited by the power efficiency of the converter and the speed of the gate drive especially under the high-voltage (HV) condition. This paper, thus, aims at presenting seamless integration of effective soft-switching converter topology and new custom-designed high-speed gate drive to enable HV non-isolated boost converters to achieve high power efficiencies while running at the high switching frequency.

Regarding the number of components in the power stage, hard-switching converters always require the smallest number of passive components. The switching power loss P_{sw} at the switching node of the hard-switching boost converter is proportional to the converter switching frequency and the square of the voltage swing ΔV_{sw} at the switching node. P_{sw} would be significantly increased under the HV condition due to a large value of ΔV_{sw}, thereby limiting the switching frequency and the power efficiency of the converter. Another major concern of using hard-switching synchronous boost converters is its high *dv*/*dt* kick-back effect at the switching node [11]. Both low-side and high-side power FETs could be turned ON simultaneously during switching transitions to result in the large shoot-through current. This not only gives rise to the short-circuit power loss to greatly degrade the converter power efficiency but also poorly affects the reliability of the converter.

To minimize the switching loss and ensure the system reliability of the converters, different soft-switching techniques have been reported [10], [12]–[16]. Previously reported quasi-resonant converters can enable zero-voltage switching (ZVS) for power FETs during switching transitions [12]–[14]. For example, the non-isolated boost converter in [12] requires two extra auxiliary components: An inductor and a capacitor to form the

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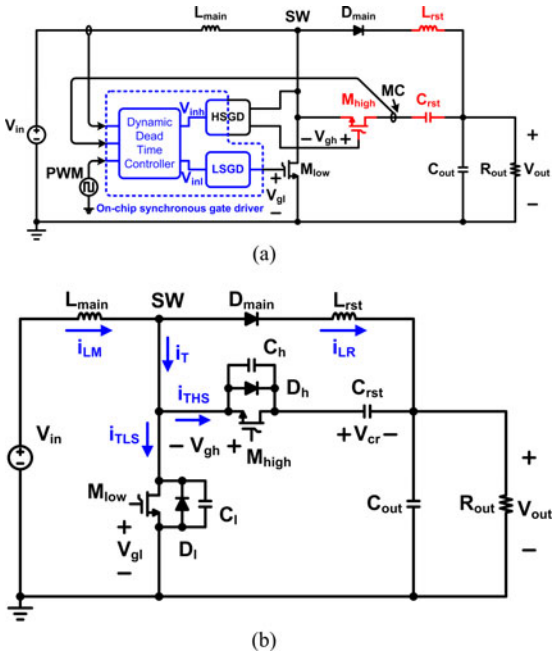

Fig. 1. (a) Schematic of the proposed QSW-ZVS boost converter with a custom-designed dynamic dead-time-controlled synchronous gate driver, and (b) equivalent circuit of the proposed boost converter.

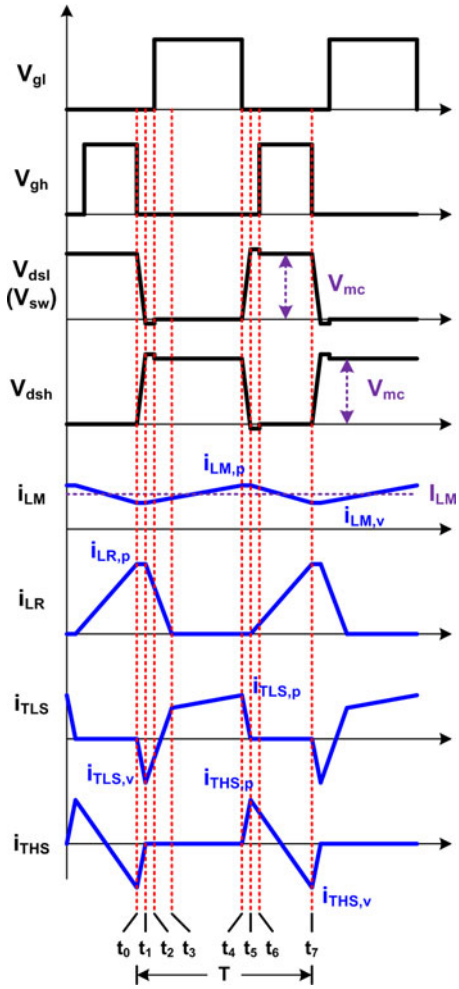

Fig. 2. Key waveforms of the proposed QSW-ZVS boost converter.

resonance for achieving ZVS. However, the resonance imposes large voltage stress on power FETs and large-size power FETs are needed to handle the increased voltage stress for the reliability concern. These large-size power FETs would have large input/output capacitance and on-resistance, limiting the gate-drive speed and increasing the converter conduction power loss. The resonance can also be generated by the leakage inductance of a power transformer and an auxiliary capacitor in the power stage [13], [14]. However, the power transformer is not suitable for non-isolated converters. Recently, non-isolated quasi-square-wave zero-voltage switching (QSW-ZVS) converter topologies that rely on using a coupled inductor to generate auxiliary current for realizing ZVS have been reported [10], [15], [16]. Due to the concern of high ac core loss of the coupled inductor under high frequencies, these converters only operate at low frequencies of less than 66 kHz for power efficiency consideration. Hence, it is crucial to develop a non-isolated QSW-ZVS boost converter topology that can perform high-frequency ZVS while still achieving high power efficiency.

To enable high-frequency operation of non-isolated synchronous boost converters, a high-speed synchronous gate driver for driving both high-side and low-side power FETs under HV condition is essential. However, there is lack of discussions in the literature on the design of high-speed HV synchronous gate driver. Existing synchronous gate drivers available from industrial products only provide long propagation delays of 100s of nanosecond [17]–[20], which would not be fast enough to enable the converters operating in the megahertz range. Another challenge of the HV synchronous gate driver is to provide appropriate dead time between low-side and high-side power FETs during switching transitions of the synchronous converter. If the dead time is too long, the turn-on time of body diodes of both power FETs is increased, resulting in large body diode conduction loss to degrade the converter power efficiency. If the dead time is too short, ZVS cannot be established, resulting in large converter switching loss. The shoot-through current could also exist, giving rise to the short-circuit power loss to further lower the converter power efficiency. Previously, the dead time is tuned manually under different load conditions. This trial-and-error method is time consuming and only suitable for low-frequency open-loop converters. The capability of automatically generating the optimal dead time for power FETs at high speed is crucial to improve the power efficiency of high-frequency synchronous converters via establishing ZVS and minimizing short-circuit loss and body diode conduction loss. It is also beneficial for saving design time and can be extended to closed-loop power converters.

A new non-isolated QSW-ZVS boost converter with an on-chip dynamic dead-time-controlled HV synchronous gate driver is proposed to deliver 130-W 150-V output and achieve the peak power efficiency of about 93% at a high switching frequency of 1 MHz. The required inductance and capacitance of the proposed converter can be significantly reduced by operating at 1 MHz for decreasing the required size and BOM cost of the components. This paper is organized as follows. Section II

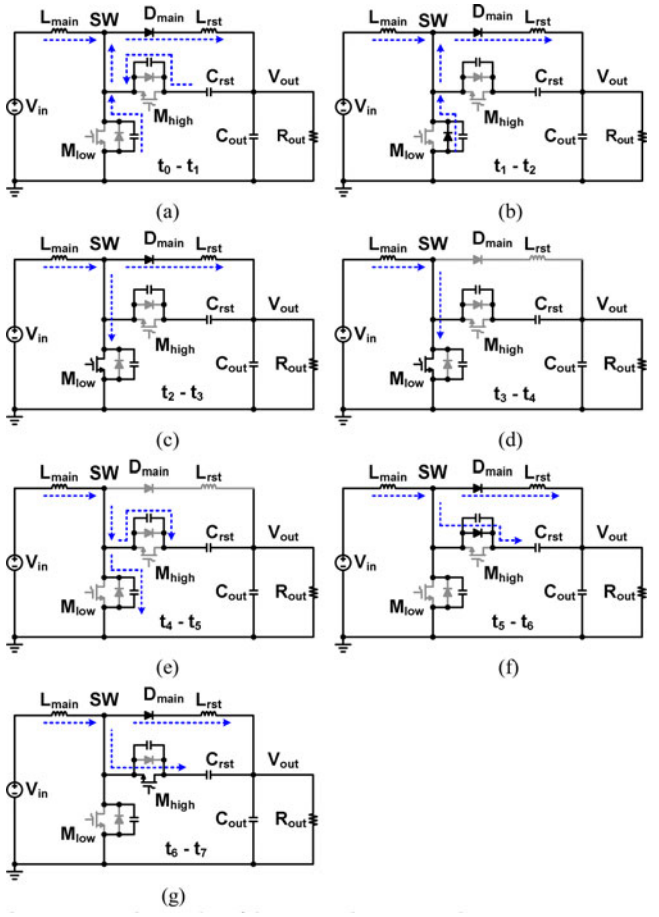

Fig. 3. Operation modes of the proposed QSW-ZVS boost converter.

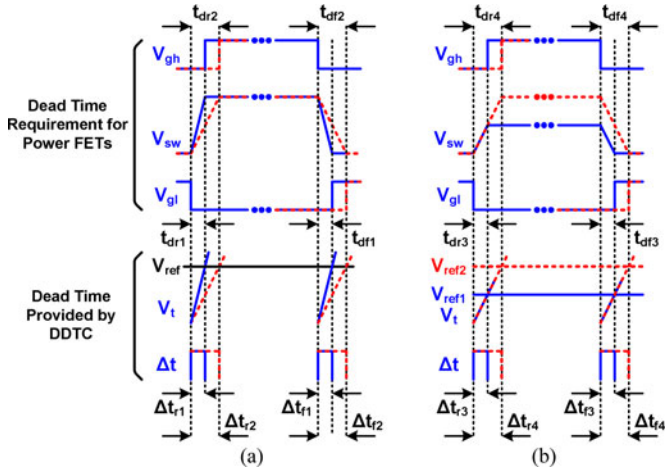

Fig. 4. Dead time requirement and generation by the DDTC under different (a) load currents and (b) output voltages.

presents the structure, the operation principle, and design procedures of the proposed non-isolated QSW-ZVS boost converter. The implementation and the design considerations of the proposed synchronous gate driver with the dynamic dead-time controller (DDTC) will be discussed in Section III. Finally, measurement results and conclusions are given in Sections IV and V, respectively.

II. Proposed Non-Isolated QSW-ZVS Boost Converter

A. Structure and Operation Principle of Proposed Converter

Fig. 1(a) shows the structure of the proposed non-isolated QSW-ZVS boost converter [21]. In contrast to the generic hard-switching asynchronous boost converter with a single main power FET M_{low}, a diode D_{main} and an inductor L_{main}, three additional components: a high-side power FET M_{high}, a reset capacitor C_{rst}, and a small auxiliary inductor L_{rst} are added in the proposed converter. Since the proposed converter does not require any coupled inductor, the ac core loss can be minimized by operating the converter at a high frequency. Three added components are used to create transient current to charge or discharge the parasitic capacitance at the switching node SW of the boost converter in order to realize ZVS during switching transitions. If ZVS is established for turning on both power FETs M_{low} and M_{high}, the converter switching loss at node SW can be minimized, thereby greatly improving the power efficiency of the converter especially under HV high-frequency operation. A custom-designed HV synchronous gate driver, which consists of a DDTC, a high-side gate driver (HSGD) and a low-side gate driver (LSGD), is also developed for driving both M_{low} and M_{high} of the proposed converter. The DDTC senses voltage V_{mc} at the internal node of the converter and automatically provides suitable dead time during switching transitions of power FETs M_{low} and M_{high} for achieving ZVS operation with minimal body diode conduction loss. Both designs of HSGD and LSGD enable fast propagation delays of the proposed synchronous gate driver to be within 12 ns, allowing the proposed converter to properly operate at high frequencies. The detailed design considerations of DDTC, HSGD, and LSGD will be discussed in Section III.

To analyze the operation of the proposed boost converter, an equivalent circuit model as shown in Fig. 1(b) is used. Output capacitors (C_h, C_l) and body diodes (D_h, D_l) of power FETs M_{high} and M_{low} are included in the circuit model. To simplify the circuit analysis, the following assumptions are made;

1) all components are ideal; i.e., the on-resistance of power FETs, parasitic resistance of inductors (L_{main}, L_{rst}), the ESR of capacitors (C_{out}, C_{rst}), and the forward voltage drop of D_{main} are neglected;
2) capacitors C_{out} and C_{rst} are sufficiently large, so the voltages across them are considered to be constant.

The proposed boost converter is operated in the continuous conduction mode and the key timing waveforms associated with different components are given in Fig. 2. There are seven subintervals in a switching period and their operations shown in Fig. 3 are described below.

Subinterval 1 [t_0–t_1]: At t_0, M_{high} is turned OFF. As shown in Fig. 3(a), both power FETs M_{low} M_{high} are OFF, both body diodes D_l and D_h are OFF, and the main diode D_{main} is ON in this subinterval. Since the main inductor current i_{LM} and the auxiliary inductor current i_{LR} are maintained at the valley level $i_{LM,v}$ and peak value $i_{LR,p}$, respectively, a current

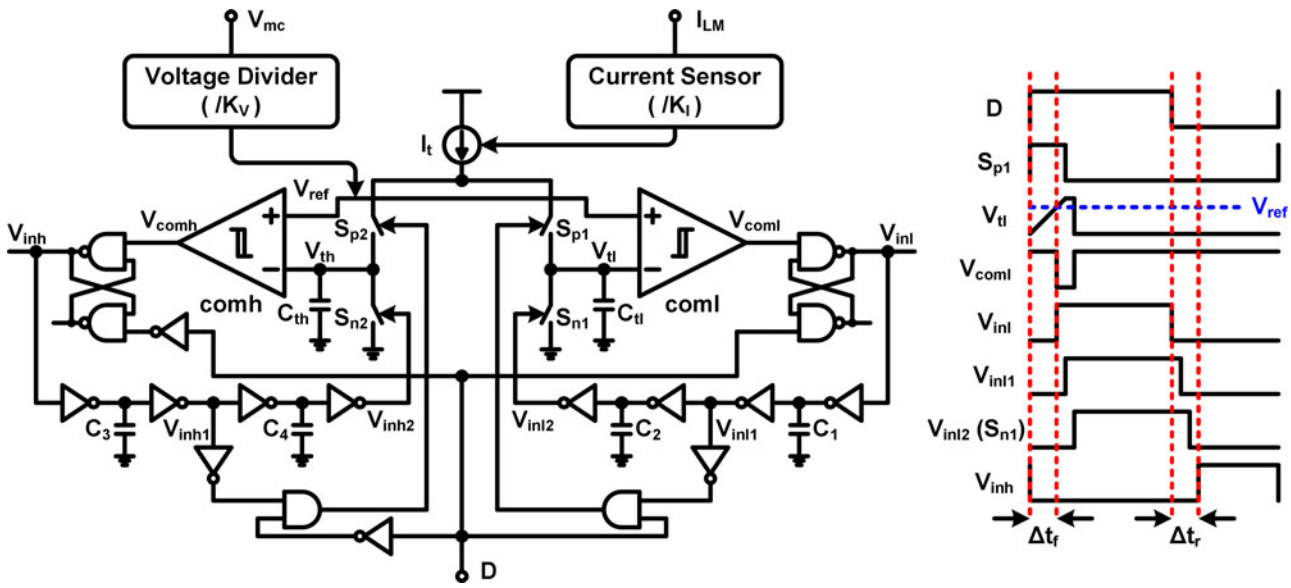

Fig. 5. Schematic and key timing waveforms of the proposed DDTC circuit.

difference $i_T (= i_{LM,v} - i_{LR,p} = i_{TLS} + i_{THS})$ is generated based on KCL, where i_{TLS} and i_{THS} are the total low-side and high-side currents associated with M_{low} and M_{high}, respectively. The negative value of i_T discharges the parasitic capacitors C_l and C_h at node SW such that the voltage V_{sw} at SW is decreasing in this subinterval as indicated in Fig. 2. Once V_{sw} reaches 0, this subinterval ends.

Subinterval 2 [t_1–t_2]: After discharging V_{sw} to 0, ZVS of power FET M_{low} is established as M_{low} is still OFF. In this subinterval as shown in Fig. 3(b), parasitic diode D_l is ON and V_{sw} is, thus, clamped at $-V_{FD}$, where V_{FD} is the forward voltage drop of D_l. The duration of this subinterval needs to be minimized by the proper design of the gate driver of M_{low} for minimizing the body diode conduction power loss. Once the gate voltage V_{gl} is changed to logic "1" to turn on M_{low}, this subinterval ends.

Subinterval 3 [t_2–t_3]: At t_2, M_{low} and D_l are turned ON and OFF, respectively, as shown in Fig. 3(c). Voltage V_{sw} is 0. Hence, i_{LM} continues to ramp up and i_{LR} keeps on decreasing. The value of $i_T (= i_{TLS} = i_{LM} - i_{LR})$ is increasing and changes from negative to positive in this interval. Once i_{LR} is decreased to 0, D_{main} becomes reverse biased, $i_{LM} = i_T$, and this subinterval ends.

Subinterval 4 [t_3–t_4]: In this subinterval, i_{LR} is maintained at 0. As shown in Fig. 3(d), i_{LM} is equal to i_{TLS} and continues to increase. This subinterval ends when i_{LM} reaches the peak value, $i_{LM,p}$, and M_{low} is turned OFF as V_{gl} changing to logic "0."

Subinterval 5 [t_4–t_5]: At t_4, M_{low} is turned OFF. M_{low}, M_{high}, D_{main}, D_l, and D_h are OFF in this subinterval as shown in Fig. 3(e). Since the variation of i_{LM} is much smaller than the value $i_{LM,p}$ during this subinterval, current i_{LM} is assumed constant at $i_{LM,p}$ and current $i_{LR} = 0$. Current $i_T (= i_{LM,p} = i_{THS} + i_{TLS})$ charges the parasitic capacitors C_l, C_h at node SW such that the voltage V_{sw} is increasing. This also causes i_{TLS} to keep on decreasing. Once i_{TLS} reaches 0 that implies V_{sw} settling to the final value, this subinterval ends. Note that when V_{sw} reaches V_{out}, D_{main} would start conducting. However, since D_{main} only conducts in a short duration within this subinterval, the value of i_{LR} is small and is assumed as 0 in this subinterval for simplicity.

Subinterval 6 [t_5–t_6]: After completely charging node SW at t_5, ZVS of power FET M_{high} is established as M_{high} is still OFF. Since parasitic diode D_h is conducting as shown in Fig. 3(f), voltage V_{sw} becomes $V_{mc} + V_{FD}$, where V_{FD} is also the forward voltage drop of D_h and $V_{mc} = V_{cr} + V_{out}$. V_{cr} is the voltage across C_{rst}. As shown in Fig. 2, i_{LM} starts ramping down while i_{LR} is increasing. The duration of this subinterval needs to be minimized by the proper design of the gate driver of M_{high} for minimizing the body diode conduction power loss. Once the gate voltage V_{gh} is changed to logic "1" to turn on M_{high}, this subinterval ends.

Subinterval 7 [t_6–t_7]: In this time interval, both M_{high} and D_{main} are ON as shown in Fig. 3(g). Voltage V_{sw} equals to V_{mc}. Hence, i_{LM} continues to ramp down and i_{LR} keeps on increasing. The value of $i_T (= i_{THS} = i_{LM} - i_{LR})$ is decreasing and changes from positive to negative in this interval. Once i_{THS} reaches its valley value $i_{THS,v}$, V_{gh} is changed to logic "0" to turn off M_{high}. The proposed converter will start the next switching period and repeat the operation of subinterval 1.

B. Design Procedure of the Proposed Converter

To obtain conversion ratio *M* and voltage V_{mc} of the proposed converter, the dead time during switching transitions is assumed to be negligible. Two assumptions used in the previous section are also adopted here to simplify the analysis.

Based on KCL at the switching node of the converter in Fig. 1(b), the value of i_{LM} is given as

$$i_{LM} = i_T + i_{LR} = i_{TLS} + i_{THS} + i_{LR}. \quad (1)$$

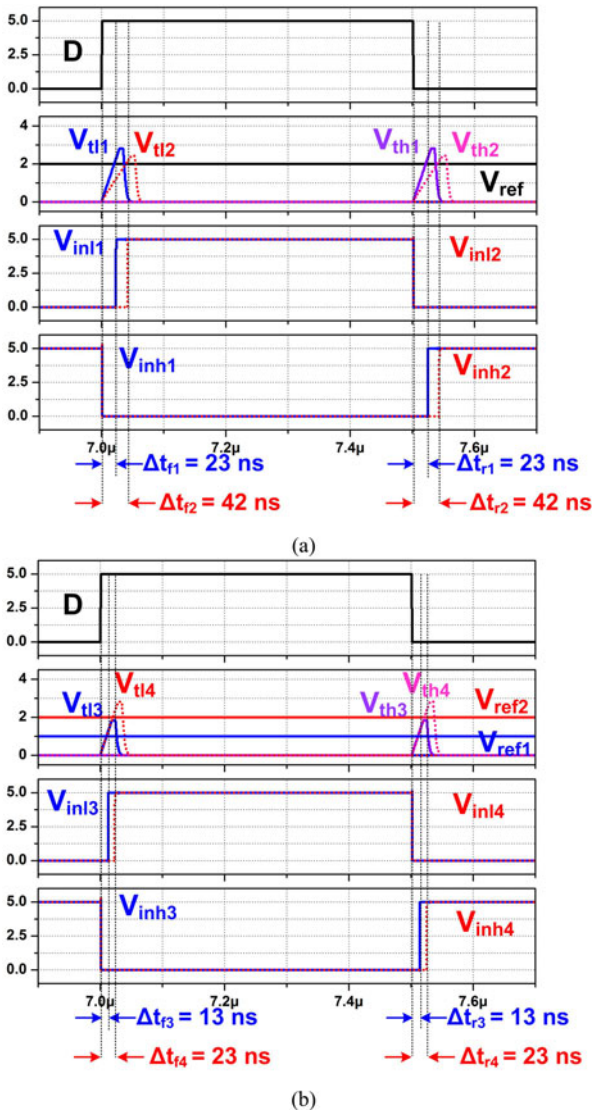

Fig. 6. Simulation results of the DDTC under (a) different values of I_{LM} (same V_{mc}) and (b) different values of V_{mc} (same I_{LM}).

From (1), both $i_{LM,v}$ and $i_{LM,p}$ can be obtained from instants at t_0 and t_5 in Fig. 2, respectively, as

$$i_{LM,v} = i_{THS,v} + i_{LR,p} \tag{2}$$

$$i_{LM,p} = i_{THS,p}. \tag{3}$$

The average current I_{LM} of the main inductor can be then obtained by combining (2) and (3) as

$$I_{LM} = \frac{1}{2} \times (i_{LM,p} + i_{LM,v}) = \frac{1}{2} \times (i_{THS,p} + i_{THS,v} + i_{LR,p}) = \frac{1}{2} \times i_{LR,p} \tag{4}$$

where $i_{THS,p} = -i_{THS,v}$ due to zero net current flowing into C_{rst} in the steady state. During duration $(1 - D) \times T$, current i_{LR} of L_{rst} increases linearly and the amount of increase Δi_{lr} is given as

$$\Delta i_{lr} = i_{LR,p} = \frac{V_{mc} - V_{out}}{L_{rst}} \times (1 - D)T \tag{5}$$

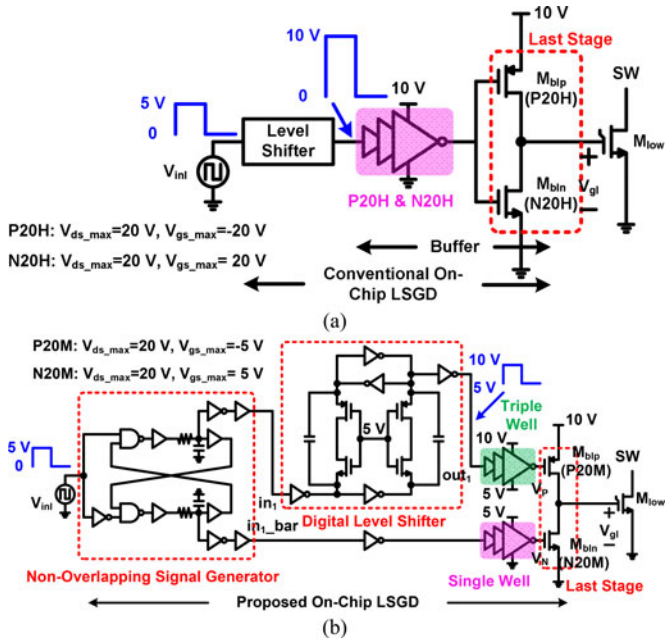

Fig. 7. Schematics of (a) conventional and (b) proposed LSGDs.

where voltage across L_{rst} is equal to $(V_{mc} - V_{out})$ as there is no voltage drop across M_{high} and D_{main}. By substituting (4) into (5), V_{mc} can be obtained as

$$V_{mc} = V_{out} + \frac{2 \times L_{rst} \times I_{LM}}{(1 - D) \times T} = V_{out} + \frac{2 \times L_{rst} \times P_{out}}{(1 - D) \times T \times V_{in}} \tag{6}$$

where P_{out} is the output power of the converter and is equal to the input power $P_{in} = V_{in} \times I_{in} = V_{in} \times I_{LM}$ due to the assumption of the lossless power stage. In this design, V_{out} is 150 V. The maximum value of V_{mc} and the voltage at the switching node are about 240 V that is still lower than the maximum voltage amplitude caused by *LC* resonance in typical resonant converters. Also, by using the volt-second balance of L_{main} in the steady state, the relationship between V_{in} and V_{mc} is given as

$$V_{in} \times DT + (V_{in} - V_{mc}) \times (1 - D)T = 0. \tag{7}$$

By substituting (7) into (6), the voltage conversion ratio M between V_{out} and V_{in} is given as

$$M = \frac{V_{out}}{V_{in}} = \frac{V_{mc}}{V_{in}} - \frac{2 \times L_{rst} \times P_{out}}{(1 - D) \times T \times V_{in}^2} = \frac{1}{1 - D} - \frac{2 \times L_{rst} \times P_{out}}{(1 - D) \times T \times V_{in}^2}. \tag{8}$$

From (8), the duty ratio *D* has to be increased to compensate for the reduction in the switching period *T* due to high-frequency operation for getting the same value of M.

Both values of L_{main} and C_{out} of the proposed converter can be designed based on the considerations of the main inductor current ripple Δi_{lm} and the output voltage ripple ΔV_{out}, respectively. They are given as follows

$$\Delta i_{lm} = \frac{V_{in} - 0}{L_{main}} \times DT \Rightarrow L_{main} \geq \frac{V_{in}}{\Delta i_{LM,max}} \times DT \tag{9}$$

TABLE I
SIMULATED PERFORMANCE COMPARISONS OF CONVENTIONAL AND PROPOSED LSGDS

	Conventional		Proposed	
	M_{blp} (P20H)	M_{bln} (N20H)	M_{blp} (P20M)	M_{bln} (N20M)
L_{min} (μm)	1.1	0.5	0.6	0.5
Width (mm)	45	22	28.8	22
Rising Time at V_{gl} (ns)	3.98		3.99	
Falling Time at V_{gl} (ns)	3.99		3.94	
Gate Voltage Swing of Buffer Last Stage	10 V		5 V	
Gate Switching Loss of Buffer Last Stage at f_{sw} = 1 MHz	11 mW		3.45 mW	
Short-Circuit Loss of Buffer Last Stage at f_{sw} = 1 MHz	30 mW		Nil	
Total Power Loss* of LSGD at f_{sw} = 1 MHz	91 mW		54 mW	

* Total power loss is simulated when the LSGD is loaded with a 1-nF output capacitor.

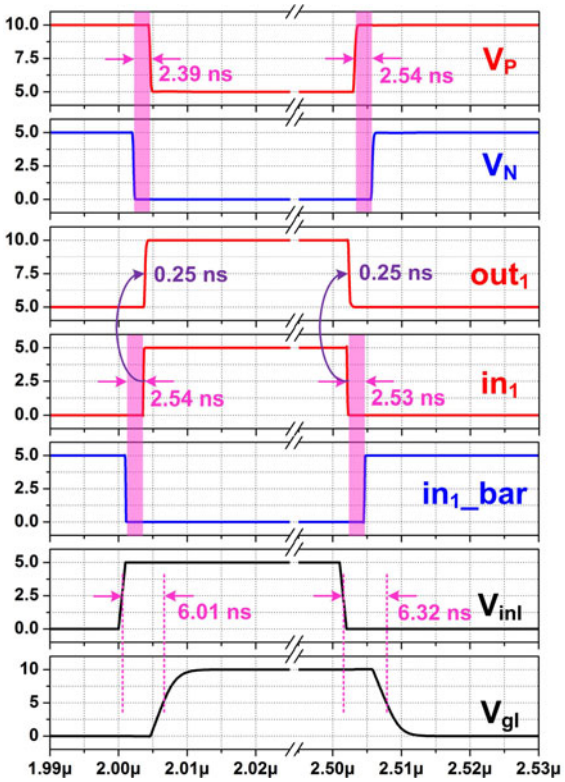

Fig. 8. Simulated results of the proposed LSGD.

$$\Delta V_{\text{out}} = \frac{V_{\text{out}} \times DT}{R_{\text{out}} \times C_{\text{out}}} = \frac{P_{\text{out}} \times DT}{V_{\text{out}} \times C_{\text{out}}} \Rightarrow C_{\text{out}} = \frac{P_{\text{out}} \times DT}{V_{\text{out}} \times \Delta V_{\text{out}}}. \tag{10}$$

Regarding the design of C_{rst}, its value needs to be much larger than the output capacitance of M_{high} (that is about 200 pF) for maintaining a constant voltage V_{cr} across C_{rst} in the steady state. C_{rst} is thus arbitrarily chosen as 2.2 μF in this design. The selection of L_{rst} is crucial as it determines that the total equivalent capacitance C_x at node SW can be charged or discharged to establish ZVS of power FETs during switching transitions. Without the loss of generality, L_{rst} can be determined to discharge voltage V_{SW} to 0 during subinterval [t_0–t_1]. Both $i_{LR}(t)$ and $V_{sw}(t)$ are given as

$$L_{\text{rst}} \times \frac{di_{LR}(t)}{dt} = V_{\text{sw}}(t) - V_{\text{out}} \tag{11}$$

$$C_x \times \frac{dV_{\text{sw}}(t)}{dt} = i_{LM}(t) - i_{LR}(t). \tag{12}$$

Since the variation of i_{LM} is less than $\pm 0.1 I_{LM}$, $i_{LM}(t)$ is assumed to be a constant value I_{LM} for simplicity of analysis.

By combining (11) and (12) and using the following initial conditions for $i_{LR}(t)$ and $V_{sw}(t)$ at t_0 as

$$i_{LR}(t_0) = i_{LR,p} = 2 \times I_{LM} \tag{13}$$

$$V_{\text{sw}}(t_0) = V_{mc}. \tag{14}$$

The value $V_{sw}(t)$ can be derived as

$$V_{\text{sw}}(t) = A \times \cos\left(\frac{t - t_0}{\sqrt{L_{\text{rst}} \times C_x}}\right) - B \times \sin\left(\frac{t - t_0}{\sqrt{L_{\text{rst}} \times C_x}}\right) + V_{\text{out}} \tag{15}$$

where $A = V_{mc} - V_{out}$ and $B = I_{LM} \times \sqrt{\frac{L_{rst}}{C_x}}$.

Since $V_{sw}(t)$ needs to be discharged to 0 for complete ZVS operation, it needs to satisfy the following condition as

$$\sqrt{(V_{mc} - V_{\text{out}})^2 + \left(I_{LM} \times \sqrt{\frac{L_{rst}}{C_x}}\right)^2} > V_{\text{out}}. \tag{16}$$

From (16), the value of L_{rst} can be found as

$$L_{\text{rst}} > \frac{C_x \times (V_{\text{out}}^2 - (V_{mc} - V_{\text{out}})^2)}{I_{LM}^2}. \tag{17}$$

Based on (17), a small-value surface-mounted inductor L_{rst} of 2.7 μH is used in this design.

C. Design Consideration of Dead Time Generation

Appropriate dead time provided by the synchronous gate driver is crucial during switching M_{low} and M_{high} in order to simultaneously minimize the body diode conduction loss of power FETs and enable ZVS operation in the proposed converter. Ideally, the dead time equals to the transition time Δt for voltage V_{sw} changing between 0 and V_{mc} at the switching node SW and Δt is given as

$$\Delta t = C_x \cdot \frac{\Delta V_{\text{sw}}}{I} \tag{18}$$

where ΔV_{sw} equals to V_{mc} and I is maintained at $i_{THS,p} = i_{THS} + i_{TLS}$ ($i_{THS,v} = i_{THS} + i_{TLS}$) at the rising (falling) edge of V_{sw} under [t_4–t_5] ([t_0–t_1]). Both $i_{THS,p}$ and $i_{THS,v}$ have the same magnitude. From Fig. 2, $i_{THS,p}$ equals to $i_{LM,p}$. If L_{main} is sufficiently large, the current ripple of the main inductor would be much smaller than the average inductor current I_{LM}. Hence, both $i_{THS,p}$ and $i_{THS,v}$ can be approximated as I_{LM} and the

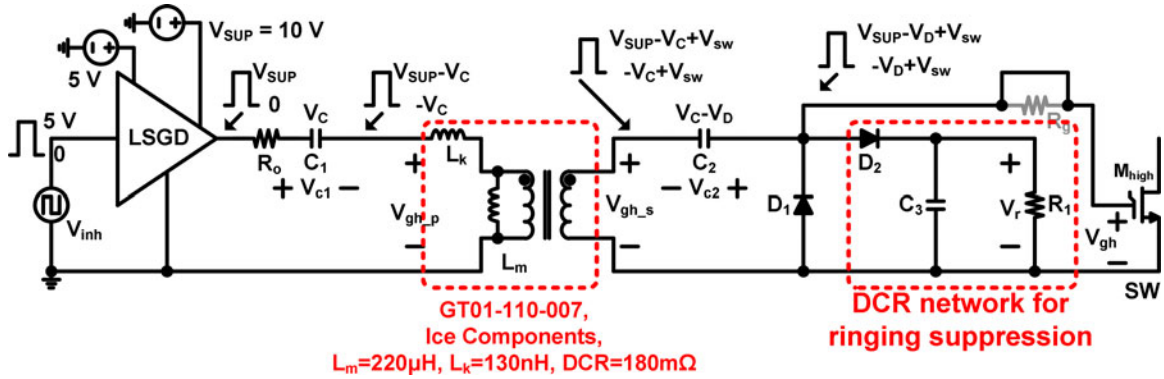

Fig. 9. Schematic of the proposed transformer-based HSGD.

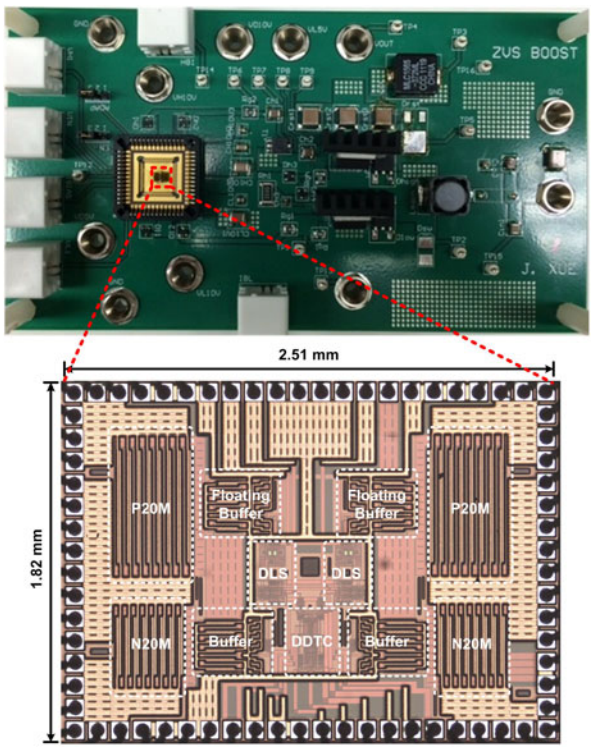

Fig. 10. Hardware prototype of the proposed QSW-ZVS boost converter and the chip micrograph of the proposed synchronous gate driver.

desirable rising-edge dead time t_{dr} and falling-edge dead time t_{df} can then be given as

$$t_{dr} \approx t_{df} \approx C_x \cdot \frac{V_{mc}}{I_{LM}}. \tag{19}$$

From (19), since both t_{dr} and t_{df} are dependent on values of V_{mc} and I_{LM}, both desirable dead times would change under different output voltages or load currents. Fig. 4(a) illustrates that both t_{dr2} and t_{df2} would decrease to the corresponding t_{dr1} and t_{df1} when the load current increases due to the increase in I_{LM}, where the value of V_{mc} is maintained at the same value under different load currents. Similarly, with the same load current, Fig. 4(b) shows that t_{dr4} and t_{df4} will reduce to the corresponding t_{dr3} and t_{df3} when the value of V_{mc} decreases. Hence, fixed dead time is insufficient to enable ZVS under different conditions in the proposed boost converter. A DDTC is, thus, proposed to satisfy (19) under different output voltages and load currents. The circuit implementation of the DDTC will be discussed in Section III-A.

TABLE II
SUMMARY OF PROPOSED QSW-ZVS BOOST CONVERTER

Supply Voltage, V_{in}	48–60 V
Output Voltage, V_{out}	150 V
Output Power	130 W
Inductors	$L_{main} = 68\ \mu$H (Coilcraft MSS1278T, 0.0683 inch^3) $L_{rst} = 2.7\ \mu$H (Coilcraft MLC1555, 0.0409 inch^3)
Capacitors	$C_{out} = 6.6\ \mu$F (TDK C5750X7T2E225K250KE, 0.0146 inch^3) $C_{rst} = 2.2\ \mu$F (TDK C5750X7T2E225K250KE, 0.0049 inch^3)
Power Switches M_{low} and M_{high}	Fairchild FQP16N25
Power Diode	STPSC806
Switching Frequency	1 MHz
Max. Power Efficiency	92.7%

III. Implementations of On-Chip Dynamic Dead-Time-Controlled Synchronous Gate Driver

A. Dynamic Dead-Time Controller

Fig. 5 shows the schematic of the proposed DDTC circuit with its timing diagram, which consists of a current sensor to scale down I_{LM} to I_t by K_I times, a voltage divider to scale down V_{mc} to V_{ref} by K_v times, and two identical capacitors C_{th} and C_{tl} (i.e., $C_{th} = C_{tl} = C_t$) that are scaled down from C_x by K_C times. There are also two comparators (coml and comh) to determine the dead time between outputs V_{inl} and V_{inh}. Initially, all switches S_{p1}, S_{p2}, S_{n1}, and S_{n2} in the DDTC circuit are OFF. When duty ratio D is changed from 0 to logic "1" (i.e., voltage V_{sw} at switching node SW starts decreasing in Fig. 2), signal V_{inh} is switched to 0 and S_{p1} is turned ON. Current I_t starts charging capacitor C_{tl} such that voltage V_{tl} starts increasing linearly from 0. Once V_{tl} is larger than V_{ref}, the output V_{coml} of the comparator coml changes to 0 and causes V_{inl} to switch from 0 to logic "1." Hence, falling-edge transition time Δt_f between V_{inh} and V_{inl} is generated by the proposed

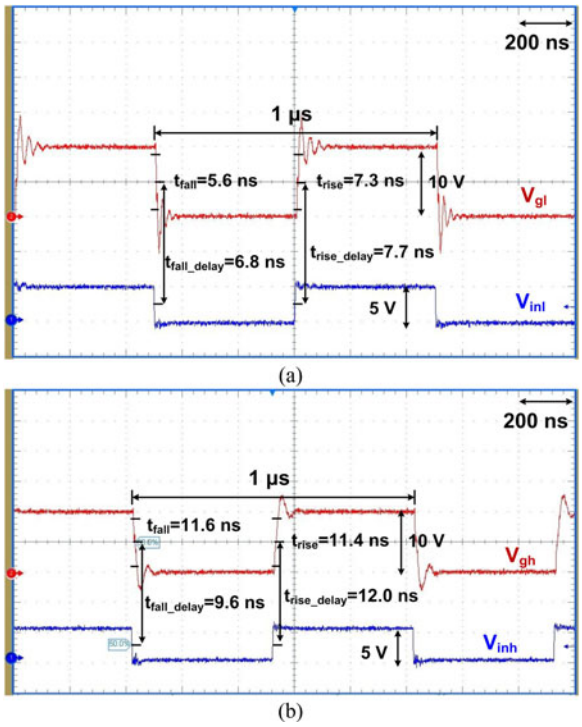

Fig. 11. Measured input and output waveforms of (a) LSGD and (b) HSGD.

DDTC. After certain delay caused by C_1, S_{p1} is turned OFF and V_{tl} stops increasing. Switch S_{n1} is then turned ON to discharge C_{tl} until V_{tl} reaches 0. Signal V_{inl} is maintained at logic "1" until the falling edge of *D*. When V_{inl} goes to 0, S_{n1} is turned OFF and all the circuits for switching the logic state of V_{inl} are reset to the initial condition until the next rising edge of *D*. Similarly, once *D* is changed from logic "1" to 0, voltage V_{sw} at switching node SW starts increasing. The rising-edge transition time Δt_r between V_{inl} and V_{inh} is generated by turning ON S_{p2}, charging C_{th} with I_t, and making the decision with comparator comh.

In the DDTC circuit, since $C_t = C_{th} = C_{tl} = C_x/K_C$, $V_{ref} = V_{mc}/K_V$, $I_t = I_{LM}/K_l$, and the relationship among K_l, K_V, and K_C is set as

$$K_I = K_C \times K_V \tag{20}$$

both Δt_r and Δt_f are then given as

$$\Delta t_r = \Delta t_f = \frac{K_I}{K_C \times K_V} \times C_x \times \frac{V_{mc}}{I_{LM}} = C_x \times \frac{V_{mc}}{I_{LM}} \approx t_{dr} \approx t_{df}. \tag{21}$$

Hence, the desirable rising-edge dead time t_{dr} and falling-edge dead time t_{df} given in (19) can be generated by the proposed DDTC.

In the proposed DDTC circuit, $K_V = K_C = 100$ and $K_l = 10000$ are used. Fig. 6 shows the simulated performances of the DDTC circuit. As indicated in Fig. 6(a), both dead times Δt_{r1} and Δt_{f1} are 23 ns under V_{mc} of 200 V and I_{LM} of 2 A. When I_{LM} is decreased to 1 A, Δt_{r2} and Δt_{f2} of 42 ns are resulted. Based on (19), t_{dr} (and t_{df}) is estimated to increase from 20 to 40 ns when I_{LM} is decreased by 1 A. Similarly, Fig. 6(b) shows that Δt_{r4} and Δt_{f4} of 23 ns under V_{mc} of 200 V and I_{LM} of 2 A are decreased to Δt_{r3} and Δt_{f3} of 13 ns when V_{mc} is reduced to 100 V. According to (19), t_{dr} (and t_{df}) is estimated to decrease from 20 to 10 ns when V_{mc} is decreased by 100 V. Since the simulated dead times generated by the proposed DDTC circuit under different values of V_{mc} and I_{LM} agree well with the desirable dead time requirement calculated from (19), the proposed DDTC circuit is proved to automatically provide near optimal dead time for driving power FETs under different conditions.

B. On-Chip LSGD

Fig. 7 shows two different implementations of the LSGD for driving power FET M_{low}. Fig 7(a) shows the conventional design [17]–[20], [22], which adopts a single-branch buffer chain. When M_{low} is an external power MOSFET (Fairchild FQP16N25), its gate-to-source voltage is 10 V and the output swing of each buffer stage in this LSGD would be 10 V. To implement this buffer, gate-to-source and drain-to-source voltages of all on-chip transistors in the buffer then require at least 10 V. Hence, in the 120-V 0.5-μm AMS process, thick-oxide transistors p20H and n20H that have the maximum allowable gate-to-source and drain-to-source voltage of 20 V have to be used to implement the buffer. It should be noted that the size and the corresponding input capacitance of the thick-oxide transistor are much larger than those of the medium-oxide counterpart for realizing the same on-resistance. In the design of the LSGD, large-size thick-oxide transistors M_{blp} and M_{bln} are used in the buffer last stage to provide sufficient driving capability for M_{low}. The gate switching loss for driving the buffer last stage is proportional to the total input capacitance of M_{blp} and M_{bln} and V_g^2, where V_g is the gate voltage swing of M_{blp} and M_{bln}. With large input capacitance of thick-oxide transistors and large value of V_g of 10 V in this conventional LSGD, large gate switching loss of the buffer last stage would be resulted.

Fig. 7(b) shows the structure of the proposed LSGD to significantly reduce the power loss of the conventional design. A dual-branch architecture for driving buffer last stage is developed to enable 1) adopting medium-oxide devices (p20M and n20M) to realize transistors M_{blp} and M_{bln}; 2) reducing gate voltage swing for M_{blp} and M_{bln} to 5 V; and 3) using thin-oxide devices for implementing other stages of the buffer. The gate switching loss of the buffer in the proposed LSGD can, thus, be greatly reduced. In addition, a nonoverlapping signal generator is adopted in the proposed LSGD to produce dead time to minimize the shoot-through current of large-size transistors M_{blp} and M_{bln} during switching transitions, thereby eliminating the short-circuit power loss in the LSGD. A digital level shifter to shift up signal from 0–5 V at node in_1 to 5–10 V at the buffer input is needed in the driver. The propagation delay of this level shifter should be much smaller than the dead time produced by the nonoverlapping signal to minimize the overall propagation delay of the LSGD.

Table I provides the performance comparisons of the conventional and proposed LSGDs. The sizing of both M_{blp} and

TABLE III
PERFORMANCE COMPARISONS OF STATE-OF-THE-ART GATE DRIVERS

	ON Semi NCP5181 [17]	ST L6384 [18]	Fairchild FAN7393 [19]	IXYS IX2127 [20]	TI LM5114 [24]	**This work**
Output of driver (V)	10–20	≤ 14	10–20	9–12	4–12.6	**~10**
Output source/sink current (A)	1.4/2.2	0.4/0.65	2.5/2.5	0.25/0.5	1.3/7.6	**4.0/4.0**
Turn-on rising time* (ns)	40	50	40	23	8	**11.4 (worst case)**
Turn-off falling time* (ns)	20	30	20	20	3.2	**11.6 (worst case)**
Turn-on delay* (ns)	100	200	550	100	27	**12 (worst case)**
Turn-off delay* (ns)	100	200	200	73	24	**9.6 (worst case)**
Synchronous Design	Yes	Yes	Yes	Yes	No	**Yes**
Dynamic Dead Time	No	No	No	No	No	**Yes**

* Output capacitor is 1 nF.

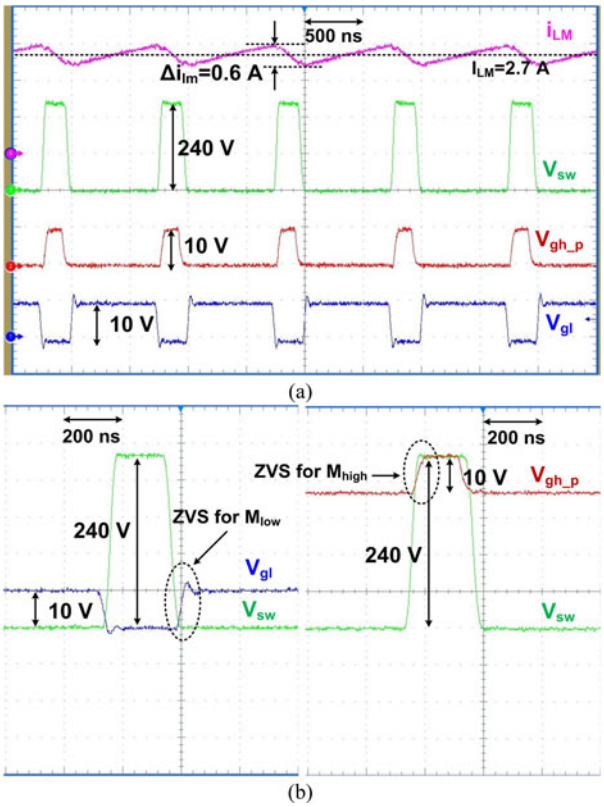

Fig. 12. Measured waveforms of the proposed QSW-ZVS boost converter at 1-MHz frequency, 48-V V_{in}, 150-V V_{out}, and 2.7-A I_{in}: (a) normal and (b) close-up views of V_{sw}, V_{gh_p}, and V_{gl}.

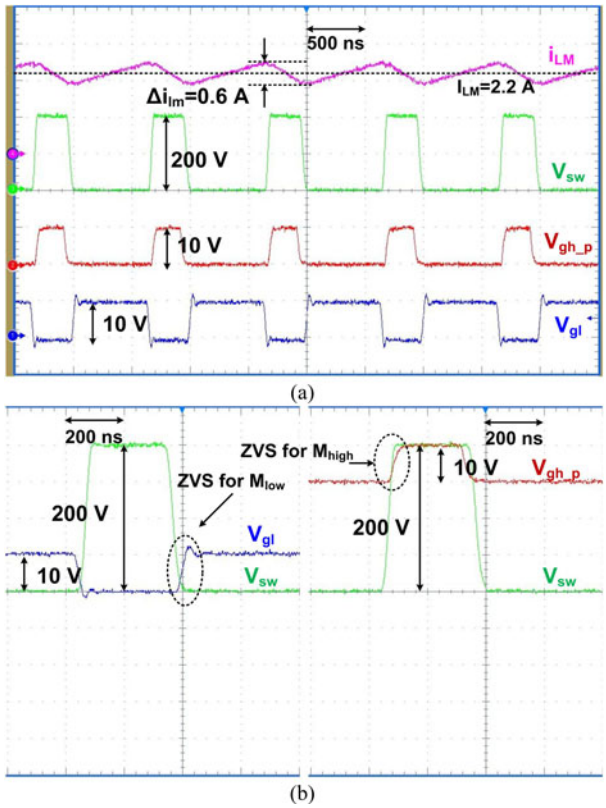

Fig. 13. Measured waveforms of the proposed QSW-ZVS boost converter at 1-MHz frequency, 60-V V_{in}, 150-V V_{out}, and 2.2-A I_{in}: (a) normal and (b) close-up views of V_{sw}, V_{gh_p}, and V_{gl}.

M_{bln} in both designs are selected to provide about 4 ns in both rising and falling times of output voltage V_{gl} of the LSGDs with an output capacitor of 1 nF. The area of each LSGD is dominated by the large-size power transistors M_{blp} and M_{bln}. Since the size of M_{blp} in the proposed LSGD is much smaller than that in the conventional counterpart, the chip area of the proposed LSGD would be much smaller than that of the conventional counterpart. In addition, both gate switching loss and short-circuit power loss of the buffer last stage contribute significantly to the total power loss of the LSGD, and they are reduced by 11.9 times compared to those of the conventional LSGD. Together with the switching power needed for driving the 1-nF output capacitor at 1-MHz switching frequency, the total power loss of the proposed LSGD is about 1.7 times smaller than that of the conventional LSGD. It should be noted that the smaller the size of the load capacitor, the larger the improvement in the total power loss would be resulted in the proposed LSGD over the conventional counterpart.

Fig. 8 provides the simulated transient responses of the proposed LSGD. Based on simulated signals in_1 and in_1_bar, the nonoverlapping signal generator is proved to provide about 2.5-ns dead time. The propagation delay of the digital level shifter for generating in_1 of 0–5 V to out_1 of 5–10 V is 0.25 ns (10× smaller than the dead time). With an inverter gate delay at the low side for matching the delay of the digital level shifter, the dead time between signals V_P and V_N for driving M_{blp} and M_{bln} is almost the same as that between in_1 and in_1_bar such that the shoot-through current in the

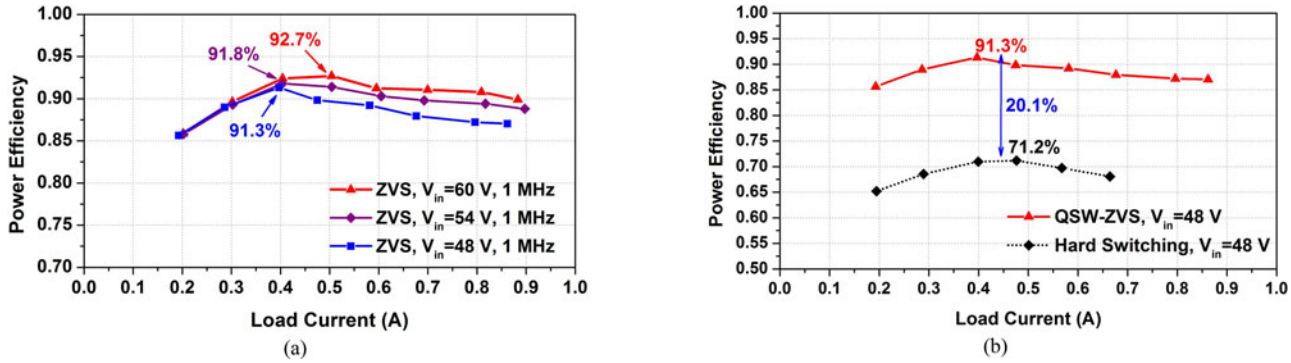

Fig. 14. (a) Measured power efficiency of the proposed QSW-ZVS boost converter under different input voltages and (b) comparison of the measured converter power efficiency between the proposed QSW-ZVS and the hard-switching cases.

buffer last stage can be eliminated. In addition, the simulated propagation delays between input V_{inl} and output V_{gl} of the gate driver are about 6 ns (only 0.6% of the switching period of 1 MHz).

C. High-Side Gate Driver

Fig. 9 shows the schematic of the proposed HSGD to produce suitable gate-drive signal V_{gh} for the power FET M_{high}. Since the output voltage of the converter is 150 V and the maximum allowable common-mode voltage is only 120 V in the fabrication process, a transformer-based ac-coupled HSGD is developed. The proposed HSGD consists of the on-chip LSGD to provide the driving capability for M_{high} and a few external components including C_1, C_2, C_3, D_1, D_2, R_1, and a signal transformer. Ceramic capacitors $C_1 = C_2 = 1\ \mu$F and $C_3 = 150$ nF are used and R_o is the intrinsic output resistance of the LSGD in Fig. 9.

Similar to the previous design of the isolated gate driver [22], C_1 is used to downshift the output signal of the LSGD to allow voltage across the primary side of the transformer swinging between a negative voltage $-V_C$ and a positive voltage $V_{SUP} - V_C$ in order to prevent the saturation of the transformer. Since $V_C = D \times V_{SUP}$ and D is the duty ratio of the input signal V_{inh}, voltage $(V_{SUP} - V_C)$ developed across the secondary side of the transformer could be smaller than the threshold voltage of M_{high} if C_2 is not used and D is large. In this case, M_{high} could never be turned ON. The presence of C_2 and D_1 removes the dependence of V_{gh} on the value of V_C such that V_{gh} can swing between $-V_D$ and $V_{SUP} - V_D$, where V_D is the diode forward voltage drop of about 0.7 V and is much smaller than V_{SUP} of 10 V. In this isolated HSGD, the intrinsic output resistance R_o of the LSGD, the leakage inductance of the transformer L_k, and the input capacitance C_{ihigh} of M_{high} form a second-order *LRC* circuit and the quality factor Q of this *LRC* circuit equals to $\sqrt{\frac{L_k}{C_{ihigh}}}\frac{1}{R_o}$.

Since the value of R_o is small for providing large driving capability to M_{high}, the value of Q is much larger than 1 and increases with the value of L_k. Hence, V_{gh} would have large-amplitude ringing that could cause false turn-on of M_{high} and affect the device safety. To reduce the ringing, a series resistance R_g in Fig. 9 is typically added to reduce the Q-value of the *LRC* circuit [22], [23]. However, this R_g would significantly increase the propagation delay of the HSGD. Instead of using R_g, a DCR network involving D_2, C_3, and R_1 is thus proposed in this HSGD to simultaneously address the issues of ringing and speed of gate driving. When the amplitudes of the overshoots at the rising and falling edges of V_{gh} are large, D_2 is turned ON, and R_1 draws current from the gate terminal of M_{high} to dampen the ringing of V_{gh}. The smaller the value of R_1 is, the faster the ringing suppression of V_{gh} could be resulted. The value of R_1 is chosen to be 500 Ω in this design.

IV. Measurement Results and Discussion

A hardware prototype of the proposed QSW-ZVS boost converter with an on-chip dynamic dead-time-controlled synchronous gate driver was developed to operate at 1-MHz switching frequency and deliver up to 130-W output power. Fig. 10 shows the PCB of the proposed converter and the chip micrograph of the custom-designed proposed dynamic dead-time-controlled gate driver. The power loop and gate driver loops are minimized on the PCB to reduce the parasitic conduction loss and improve the reliability. The chip consists of the proposed DDTC and two LSGDs (one for driving M_{low} and the other for the HSGD) by using 120-V AMS 0.5-μm CMOS process. The total chip area is 4.57 mm^2. The PWM input in Fig. 1(a) to the proposed gate driver is generated by an external voltage mode PWM controller. Table II summarizes the components and performance of the proposed converter.

Fig. 11(a) and (b) shows the measured input and output waveforms of the LSGD and HSGD, respectively, under the load capacitor of 1 nF. Fig. 11(a) depicts that the turn-on and turn-off propagation delays between the input signal V_{inl} and the output V_{gl} of the LSGD are 7.7 and 6.8 ns, respectively. These results agree well with the simulated results shown in Fig. 8. Similarly, the turn-on and turn-off propagation delays shown in Fig. 11(b) between the input signal V_{inh} and the output V_{gh} of the HSGD are 12.0 and 9.6 ns, respectively. For driving a 1-nF load capacitor, the power dissipation of the proposed HSGD is 220 mW that is only 0.17% of the output power of 130 W. The power dissipation of the whole synchronous gate driver including DDTC circuit, LSGD, and HSGD is 278 mW that is only 0.21– 0.96% of the output power ranging from 30 to 130 W. Table III provides the performance comparisons of the proposed synchronous gate driver with different state-of-the-art HV gate drivers. Compared with reported synchronous gate drivers

TABLE IV
PERFORMANCE COMPARISONS OF STATE-OF-THE-ART NON-ISOLATED QSW-ZVS POWER CONVERTERS

Converter Topology	TPE 10 [16] Non-Isolated Bidirectional Converter	TIE 08 [15]	TPE 12 [10] Non-Isolated Boost Converter	**This Work**
V_{in} (V)	24–30	25–40	15	**48–60**
V_{out} (V)	200	200	200	**150**
Max. P_{out} (W)	200	200	100	**130**
Maximum Power Efficiency	91%	92%	95%	**~93%**
Frequency (kHz)	66	66	50	**1000**
Operation	Quasi-Square-Wave	Quasi-Square-Wave	Quasi-Square-Wave	**Quasi-Square-Wave**
Transient Current for ZVS	Coupled Inductor	Coupled Inductor	Coupled Inductor	**Auxiliary Inductor**
Total Components in Converters	7	7	8	**7**
(Number of power FET, Diode, Coupled Inductor, Inductor, Capacitor)	(3, 0, 1, 2, 1)	(2, 1, 1, 1, 2)	(1, 3, 1, 0, 3)	**(2, 1, 0, 2, 2)**
Magnetizing Inductance / Inductors	1.6 mH [1], 1.5 μH, 1.5 μH	2 mH [1], 1.5 μH	764 μH [1]	**68 μH [2], 2.7 μH (Surface Mount)**
Capacitors	N. A.	440 μF [3], 12 μF	220 μF [3], 47 μF, 47 μF	**6.6 μF [3], 2.2 μF (Ceremic)**

[1]Magnetizing inductance of the coupled inductor.
[2]Inductance of the main inductor.
[3]Output capacitance.

[17]–[20], the worst-case turn-on and turn-off propagation delays of the proposed design are improved by at least 8.3 times and 7.6 times, respectively. The worst-case propagation delay of the proposed design is even faster than the reported LSGD [24] by at least 2.3 times. The proposed gate driver is the only one having the DDTC to adaptively provide near optimum dead time for driving M_{low} and M_{high} to ensure ZVS operation with minimal body diode conduction loss under different output voltages and load currents.

Figs. 12 and 13 show the measured waveforms of the proposed QSW-ZVS boost converter with the proposed dynamic dead-time-controlled synchronous gate driver under different input voltages V_{in} (thus different values of I_{LM}). In Figs. 12(b) and 13(b), as V_{gl} changes to logic "1" after V_{sw} decreases to 0, it proves the ZVS operation of low-side power MOSFET M_{low} under $V_{in} = 48$ V (60 V). Similarly, since V_{sw} changes to logic "1" before V_{gh_h} becomes logic "1" in Figs. 12(b) and 13(b), the ZVS operation of high-side power MOSFET M_{high} is achieved under $V_{IN} = 48$ V (60 V). Figs. 12 and 13 prove that the proposed DDTC enables ZVS of power MOSFETs under different values of I_{LM}.

Fig. 14(a) provides the measured power efficiencies of the proposed QSW-ZVS boost converter operating at a high frequency of 1 MHz under different input voltages. The peak power efficiencies of the proposed QSW-ZVS boost converter reach 91.3%, 91.8%, and 92.7% at V_{in} of 48, 54, and 60 V, respectively. Fig. 14(b) provides the measured power efficiencies of both hard-switching synchronous boost converter (without D_{main}, L_{rst}, and C_{rst}) and the proposed QSW-ZVS converter with the same power FETs and same synchronous gate driver when V_{in} is 48 V and V_{out} is 150 V at 1 MHz. Compared with the hard switching converter, the power efficiency of the proposed QSW-ZVS power converter is significantly better in all load currents and the peak power efficiency is improved by 20.1%. The huge power efficiency improvement in the proposed QSW-ZVS converter is mainly due to the minimization of the large switching loss at the high frequency of 1 MHz under different load currents. In addition, high *dv*/*dt* slewing at the switching node of the hard-switching 1-MHz synchronous converter would lead to large short-circuit power loss. These switching and short-circuit power losses would increase the temperature of power FETs drastically, leading to the increase in their on-resistance and thus the conduction power loss. Moreover, high *dv*/*dt* slewing of the 1-MHz hard-switching converter also causes reliability issue of power FETs under large load currents of and beyond 660 mA.

Table IV provides the performance comparisons of the proposed QSW-ZVS converter with other state-of-the-art nonisolated boost converters. With the proposed QSW-ZVS scheme and high-speed dynamic dead-time-controlled synchronous gate driver, the proposed converter can deliver similar maximum output power and provide similar maximum power efficiency while operating at least 15.2 times; higher switching frequency compared to other state-of-the-art non-isolated boost converters. High switching frequency operation helps to reduce the required component values/sizes and improve the power density of the converter.

V. CONCLUSION

A nonisolated QSW-ZVS boost converter with an on-chip dynamic dead-time-controlled synchronous gate driver has been introduced, discussed, and verified in this paper. The proposed QSW-ZVS boost converter enables high-frequency ZVS to minimize converter switching loss without any coupled inductors. The dynamic dead-time-controlled synchronous gate driver is also developed to generate near optimal dead time under different output voltages and load currents, and to achieve fast propagation delays for enabling megahertz operation of the converter. Both the proposed gate driver and QSW-ZVS boost converter have been verified experimentally, and their performances significantly advance state-of-the-art synchronous gate drivers and non-isolated boost converters. The proposed high-speed dynamic dead-time-controlled synchronous gate driver and QSW-ZVS boost converter topology enable power converters to simultaneously achieve high power efficiency and high operation frequency and are suitable for low-cost and small-size HV converters in photovoltaic and fuel-cell applications.

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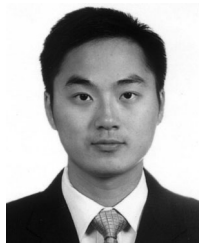

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