Correspondence

Discussion and Comments on "L-Z Source Inverter"

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***Abstract*—In this correspondence, it is shown that there are some problems when an inductive load is considered in Figs. 2–5 of the original paper [1]. The objective of this correspondence is to point out these problems using analysis and detailed computer simulation.**

Comment 1: In voltage source inverters (VSI), loads are inductive in many situations like induction motor load, *RL* load, or when a *LC* filter is used before a pure resistive load. Therefore, investigation on the effect of an inductive load in L-Z source inverters is very important.

In recent years, many Z source inverter topologies have been proposed in the literature [2]–[5]. All of them have one common characteristic: there is at least one capacitor in their impedance network. However, there is not any capacitor in the proposed L-Z source inverter [1]. Therefore, it causes some problems when an inductive load is connected to the L-Z inverter which is shown in Figs. 2 or 4 of the original paper. When the inverter goes to its nonshoot through state, the inductive load becomes series with the network inductors (as it is shown in Figs. 3(a) or 5(a) of the original paper). As a result, the inductors currents change suddenly and voltage spike appears across the dc link voltage (V_i).

Based on the above explanation, it is clear that the inductive load (*RL* load) that is shown in Figs. 3, 5, 18(c), and 19(c) of the original paper should be replaced with a pure resistive or a capacitive load (series *RC* load) in order to let the circuit work properly and the voltage spike across the dc link voltage to be removed.

In addition, equations (6) and (18) of the original paper are not appropriate when an inductive load is connected to the circuits of Figs. 2 or 4 of original paper.

In order to verify the above analysis, Fig. 3 of the original paper is simulated with following circuit parameters:

$L_1 = L_2 = 45\,\mu$H, D (duty cycle) $= 0.2$, $V_{\rm dc} = 48$ V, $R_l = 10\ \Omega$, $L_l = 1$ mH

The dc link voltage (V_i) is shown in Fig. A1.

From Fig. A1, it is clear that there is a spike voltage across the dc link voltage when an inductive load is connected to the circuit of Fig. 3 (or Fig. 5) of original paper. Also, from Fig. 1, it is obvious that the mentioned "spike" is not just a noise. It is a real voltage stress with possible damage of the semiconductor devices.

Comment 2: Equations (6)–(10) and (18)–(21) of the original paper are correct while both of following conditions are satisfied:

1) pure resistive or capacitive load are connected to Figs. 3 and 5 of the original paper;
2) network inductors work in continuous conduction mode (CCM). Similar to conventional boost converter, the voltage gain depends only on the duty cycle (D) when the inductors work in CCM.

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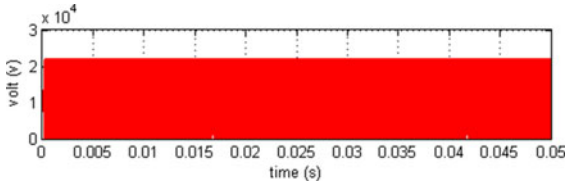

Fig. A1. DC link voltage with the inductive load.

Comment 3: In page 5, second column of the original paper, a snubber circuit is proposed for the L-Z source inverter and its application is restricted only for when the impedance network works in discontinuous conduction mode (DCM) or when the dc link voltage is disturbed by other undesired interferences. However, the snubber circuit is mandatory even when the impedance network works in CCM, because of the following reason:

When an inductive load is connected to the inverter, during some active states the inductive load becomes series with the network inductors. Therefore, a voltage spike will appear across the dc link voltage as it is mentioned in comment 1 of this correspondence.

Comment 4: In the Section IV of original paper, the correct control method is simple boost control, while it is mistakenly mentioned maximum boost control.

Comment 5: Our resimulation results using circuit parameters of the original paper show that the results in Figs. 21 and 22 of the original paper show different results. (The interested readers can simulate the circuit with the original paper circuit parameters [1].) With the snubber circuit values that are proposed in the original paper ($C_s = 0.1\ \mu$F and $R_s = 20$ k), our simulation results show that there is a voltage spike across the dc link voltage and also the output voltage is not sinusoid. It is possible to design a new snubber circuit ($C_S = 40\ \mu$F and $R_S = 1\ \Omega$) using methods presented in [6] to overcome the aforementioned problems. However, high power loss in the snubber resistor is still a major drawback of this circuit. Therefore, design a snubber circuit with low power loss and using smaller capacitor might be a new research era for this study.

References

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