Design Space Analysis and ρ–η Pareto Optimization of LC Output Filters for Switch-Mode AC Power Sources

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***Abstract*—In this study, the design space (DS) concept is refined and utilized to design the output filter of a 10-kW, four-quadrant, three-phase, switch-mode controllable AC power source (CPS). The DS concept is based on the simultaneous consideration of multiple criteria that are derived from application-oriented specifications for the CPS regarding quality and transient response of the output voltage, and limited reactive power demand of the output filter. In this paper, the output filter of the studied CPS needs to satisfy six different criteria, which, in the case of a single-stage LC filter, leads to bounds on the values of L and C that can be indicated by boundary curves in an L-C plane. The intersection set of all boundary curves defines the DS, in which all six specifications can be fulfilled. For the considered requirements, it is shown that the DS is empty for a single-stage LC filter, but exists for a two-stage LC filter, which is therefore employed as an output filter of the CPS. To fully exploit the 4D DS of the two-stage LC filter, a multi objective optimization, resulting in the power density–efficiency Pareto front, is performed to determine the most compact and/or most efficient filter design among all possible filter realizations with parameters in the DS. From the outcome of this optimization, the filter design with the highest power density of $14.6\,\mathrm{kW/dm^3}$ ($239\,\mathrm{W/in^3}$), for an efficiency of 99.4%, is realized in hardware. Finally, all six specifications for the CPS are successfully verified by experimental measurements.**

***Index Terms*—Converter control, design space, *LC* output filter, Pareto optimization, power source.**

I. Introduction

FOR developing and testing power electronics equipment and associated control strategies, controllable AC power sources (CPSs), which have the capability to emulate certain electrical characteristics, feature shorted durations of development and test procedures, i.e., are saving costs and efforts. Example applications of CPSs are motor emulators for testing inverters [1]–[3] (also in combination with power hardware-in-the-loop simulations [4]); grid emulators for testing utility connected distributed generators [5]–[7], such as fuel cell based systems [8] (this can include the testing of safety and protection functions [9] and testing of the implemented control strategy, which again can be done with hardware-in-the-loop simulations [10]); and grid emulators for optimizing the control scheme for traction vehicles [11].

Such CPSs can basically be implemented with a linear (e.g., [12]) or a switch-mode power amplifier (e.g., [13]). To reduce the weight and the volume, a switched system is preferred.

The output stage of the CPS considered in this paper is shown in Fig. 1. As further explained in Section II, the system needs to comply with specifications regarding qualities and transient responses of all three output voltages $v_{\mathrm{A,out}}$, $v_{\mathrm{B,out}}$, and $v_{\mathrm{C,out}}$ and needs to achieve the efficiency specified at the nominal operating point (cf., Table I). Because the CPS actually is a switch-mode power supply, the amplitudes of the harmonics in the switched output voltages (e.g., $v_{\mathrm{A}0}$ in Fig. 1) need to be attenuated by an output filter to comply with the given requirements. In the simplest case, the output filter is implemented as a single-stage LC filter according to Fig. 2(a). The component values used for the LC filter are restricted, not only in their minimum values, to fulfill the output voltage quality requirements, but also in their maximum values, to satisfy the dynamic specifications.

A literature survey reveals numerous publications on the design of the output filter with boundary conditions defined by specifications, which typically deal with only one aspect, such as conducted EMI [17]–[19], output voltage ripple [20], [21], or current ripple [22]–[24]. For the case at hand, however, multiple requirements need to be satisfied. For this purpose, the concept of the design space (DS), first employed in [25] to design a single-stage LC filter for a 20-W synchronous buck converter in order to comply with static and dynamic output voltage regulation specifications, is considered most promising. The DS concept is based on multiple criteria that are derived from all dynamic and static specifications. In case of [25], these criteria define bounds on the values of L and C, which can be represented by boundary curves in an L-C plane. The intersection set of all boundary curves builds the DS. Thus, the strength of the DS approach is that all combinations of filter parameter values that comply with all specifications are identified. Another publication related to the DS concept details the implications of changing specifications and/or requirements on the DS calculated for a 0.6-W buck converter including PWM delays and filter resonances in voltage mode [26]. Both studies [25], [26] are limited to single-stage LC filters and do not detail any further optimization of the filter using the calculated DS, e.g., with respect to power density or efficiency.

Subsequent to the identification of the DS, the filter can be optimized, e.g., by means of multiobjective optimization with

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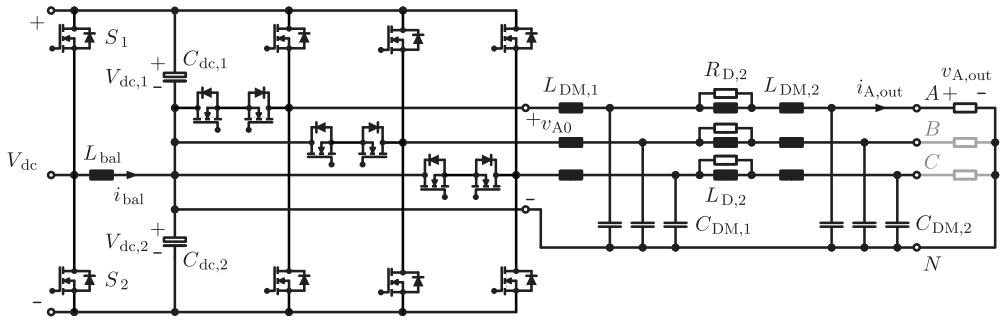

Fig. 1. Schematic of the three-phase plus neutral conductor output stage of the CPS considered in this paper including a two-stage LC output filter (cf., Fig. 2). In case asymmetrical three-phase loads are supplied, a balancer circuit with elements S_1, S_2, and L_{bal} is necessary to achieve in average equal dc-link voltages $V_{\mathrm{dc},1}$ and $V_{\mathrm{dc},2}$ [14].

TABLE I
ELECTRICAL SPECIFICATIONS OF THE POWER CONVERTER CONSIDERED FOR THE REALIZATION OF A CPS

Nominal output power $P_{\mathrm{out,n}}$	10 kW
Nominal rms output voltage $V_{\mathrm{A,out,n}}$ (line to neutral)	230 V
Nominal peak output voltage $V_{\mathrm{A,out,n,peak}}$ (line to neutral)	325 V
Max. peak output voltage $V_{\mathrm{A,out,max,peak}}$ (line to neutral)	350 V
Nominal DC-link voltage $V_{\mathrm{dc,n}} = V_{\mathrm{dc,1,n}} + V_{\mathrm{dc,2,n}}$	700 V
Max. DC-link voltage $V_{\mathrm{dc,max}}$	800 V
Nominal rms output current $I_{\mathrm{A,out,n}}$	14.5 A
Nominal peak output current $I_{\mathrm{A,out,n,peak}}$	20.5 A
Output frequency f_{out}	50 Hz
Output stage switching frequency f_{s}	$\leq$ 48 kHz
Nominal efficiency η_{n}	$\geq$ 95%

To generate an output voltage with high dynamics in the range of $[\pm 350\,\mathrm{V}]$, the DC-link voltage is increased from $V_{\mathrm{dc,n}} = 700\,\mathrm{V}$ to $V_{\mathrm{dc,max}} = 800\,\mathrm{V}$. Otherwise, $V_{\mathrm{dc,n}}$ is preferred to ensure a high efficiency of the CPS.

respect to maximal power density, maximal efficiency, and/or minimal cost [27]. Two main approaches for multiobjective optimization exist: aggregate function techniques, which summarize all considered objective functions in a single objective function (for this, the relative importance of all objective functions needs to be known *a priori*) and Pareto front (PF) techniques, which do not weight the different objectives in advance [28]. In the present work, the PF method is used, since high power density and high total efficiency are simultaneously desired and the relative importance of the two objective functions is not *a priori* known. Literature related to engineering specific multiobjective PF optimizations commonly proposes the following three approaches: first, heuristic genetic/evolutionary algorithms [28]–[30]; second, algorithms with guaranteed convergence to the Pareto-optimal solution [31]–[33]; and third, iterative grid search algorithms with an appropriate discretization of the variables [34], [35]. Because it is not guaranteed that the first category of heuristic algorithms finds Pareto-optimal solutions [36], i.e., minimal volume and/or maximum efficiency, the two latter categories are favored. Among these, the grid search algorithm is selected due to its numerical robustness and simplicity of implementation.

Remark: The DS concept is not limited to the design of LC filters. In [37], for example, the $\mathrm{ESR_C}$-C DS of the output capacitor of a fast switching (530 kHz) 9-W buck converter is calculated to meet constraints regarding the output voltage and the peak-to-peak inductor current ripples for different operating points. Furthermore, the DS concept is applied to controller designs [38], [39], to outlay advanced digital low-pass filters [40], to devise linear compensators [41], and to assess the proper functioning of RAM memory cells [42].

In this study, a complete design procedure is proposed for a two-stage LC output filter [45], which is based on the DS concept and includes a final filter optimization with respect to power density ρ, and/or efficiency η, using the ρ–η PF. Furthermore, experimental results are presented. In the following, the requirements defined for the AC source output stage are described in Section II. Section III discusses the implications of these specifications on the filter DS and details equations for the related constraints, which confine the search domain in the parameter space for any final filter design procedure. From all filter designs with component values in the DS, the final output filter is determined from a ρ–η PF analysis in Section IV. According to the calculated results, a maximum power density of the filter of $14.6\ \mathrm{kW/dm^3}$ ($239\ \mathrm{W/in^3}$) and an efficiency of 99.4% can be achieved with a two-stage approach with $L_{\mathrm{DM},1} = 154\ \mu\mathrm{H}$, $C_{\mathrm{DM},1} = 4.7\ \mu\mathrm{F}$, $L_{\mathrm{DM},2} = 11.7\ \mu\mathrm{H}$, and $C_{\mathrm{DM},2} = 4.1\ \mu\mathrm{F}$. Finally, Section V verifies the calculated outcomes by means of experimental results for this two-stage LC filter.

II. SPECIFICATIONS OF THE AC SOURCE

Fig. 1 depicts the output stage of the CPS, which is a four quadrant three-phase plus neutral conductor, three-level, T-type voltage source converter. The basic electrical specifications of this power converter are listed in Table I; details are given in [46]. It is noted that the midpoint N of the DC-link acts as reference point for the output voltage of the phases A, B, and C to provide an option for connection of a load star point, and to ensure maximum flexibility of the output voltage generation and/or an individual operation of the phases, which, however, requires that the output filter is realized without any inductive elements coupling the phases. Thus, the filter design considerations can be limited to a single-phase equivalent circuit as given in Fig. 2(a).

For the investigated CPS, a switching frequency of 48 kHz is selected to achieve the dynamic performance requirements, and therefore, the IGBTs used in [46] are replaced by SiC

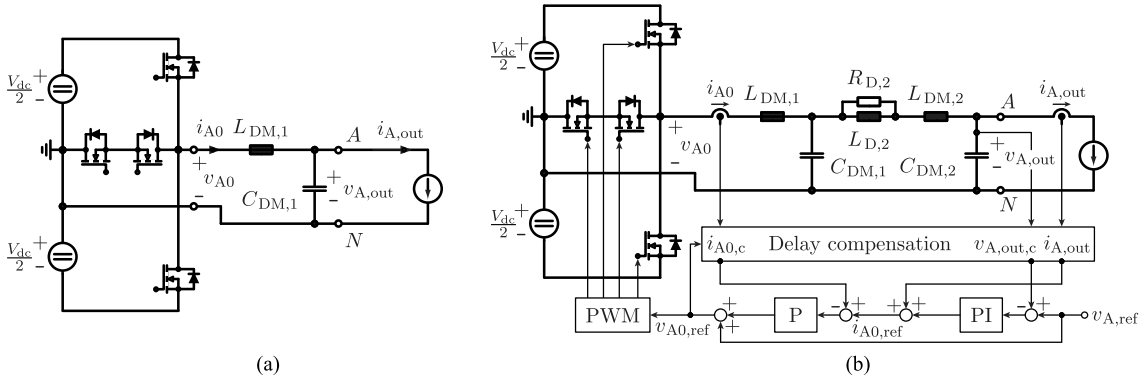

Fig. 2. (a) Simplified single-phase equivalent circuit of the CPS for a single-stage LC output filter and (b) a two-stage LC output filter with a series $R_{\mathrm{D},2}L_{\mathrm{D},2}$ damping branch of the second filter stage. The load is represented as a current source. In (b), the control scheme [43] employed in Section V is added to the equivalent circuit. It consists of an outer voltage control loop for $v_{\mathrm{A,out}}$, with feedforward of the reference voltage v_{ref}, an inner current control loop for i_{A0}, with feedforward of the load current $i_{\mathrm{A,out}}$, and a sampling plus PWM delay compensation [44] to achieve a satisfactory control performance (cf., Section V).

TABLE II
REQUIRED PROPERTIES OF THE CPS

Output voltage quality	$\mathrm{THD_v} < 2.5\%$ (cf., IEEE 1547 [15])
Output voltage slew rate	$SR \geq 203\,\mathrm{V/ms}$
Max. transient output voltage dip $\Delta v_{\mathrm{A,out}}$ due to a stepwise output current change $\Delta i_{\mathrm{A,out}}$	$\left\lvert\frac{\Delta v_{\mathrm{A,out}}}{\Delta i_{\mathrm{A,out}}}\right\rvert \leq \frac{28\,\mathrm{V}}{5\,\mathrm{A}} = 5.6\,\Omega$
Limited filter capacitor reactive power demand	$Q_{\mathrm{cap,max}} \leq 10\% \cdot \frac{P_{\mathrm{out,n}}}{3} = 333\ \mathrm{VA}$
Conducted EMI	CISPR 11, Class A [16]

MOSFETs. Furthermore, only a constant output frequency is considered, since the CPS is used for emulating a 50 Hz grid. Table II lists additional requirements, which are summarized below.

Output voltage quality requirements are differently specified for sinusoidal and arbitrary output voltage waveforms: For sinusoidal output voltages, a total harmonic distortion of $\mathrm{THD_v} < 2.5\%$ (cf., IEEE 1547, IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems [15]) is specified; for arbitrary output voltage waveforms, a minimum average slew rate SR_{min} is defined. In this context, the *response of the converter to a reference voltage step* of $\Delta v_{\mathrm{ref}} = 10\% \cdot V_{\mathrm{out,n,peak}} = 32.5\,\mathrm{V}$ is required to be completed after $t_{\mathrm{step}} = 160\,\mu\mathrm{s}$ [cf., Fig. 3(a)]. This requirement is summarized using a minimum average slew rate[1]

$$SR_{\mathrm{min}} = \frac{10\% \cdot 325\,\mathrm{V}}{160\,\mu\mathrm{s}} = 203\,\mathrm{V/ms}. \tag{1}$$

Accordingly, with SR_{min}, the converter can generate a sinusoidal output voltage reference with a frequency of 1 kHz and an amplitude of 32 V.[2] With this, and according to the results of the derivation presented in Section III-A, a small-signal bandwidth of the closed output voltage control loop of approximately 4 kHz is estimated, i.e., the CPS is capable of tracking a reference voltage which leads to an output voltage waveform that does not exceed the slew rate specified in (1) and contains frequency components up to 4 kHz.

An output voltage transient provoked by a step change of the voltage reference, v_{ref}, generates also a bridge-leg output current transient, which, depending on the output current, possibly drives the converter in its current limitations. This would then lead to a nonlinear behavior of the controlled converter, which is undesired. Thus, for the slew rate calculation, it is assumed that the CPS can always abruptly increase its output voltage by 32.5 V without running into its current limitation. This is experimentally verified in Section V-A, where the required increase of the bridge-leg output current is roughly 4 A.

The *maximum transient output voltage dip*, $\Delta V_{\mathrm{A,out,max}}$, that occurs *due to a stepwise output current change* $\Delta I_{\mathrm{A,out}}$ can be characterized by means of an impedance

$$Z_{\mathrm{step,max}} = \left\lvert\frac{\Delta V_{\mathrm{A,out,max}}}{\Delta I_{\mathrm{A,out}}}\right\rvert. \tag{2}$$

According to predefined requirements, $\Delta V_{\mathrm{A,out}}$ must not exceed 28 V (8% of $V_{\mathrm{A,out,max,peak}}$) for $\Delta I_{\mathrm{A,out}} = 5\,\mathrm{A}$, which yields $Z_{\mathrm{step,max}} = 5.6\,\Omega$ [cf., Fig. 3(b)].

To limit the current stress on the components of the power circuit, the *maximum reactive power demand of all filter*

[1]The definition of the average slew rate adopted in this paper is different from the definition of the slew rate known from operational amplifiers (OpAmps). For OpAmps, the slew rate is defined as the "maximum rate at which the output voltage of the OpAmp can change," i.e., $(dv/dt)_{\mathrm{max}}$, which is typically determined for a full-scale large-signal input voltage step [47].

[2]The $|dv/dt|$ of a sinusoidal function with amplitude V_{sig} and frequency f_{sig} is maximal at its zero crossings and can be calculated as $2 \cdot \pi \cdot f_{\mathrm{sig}} \cdot V_{\mathrm{sig}}$, which gives $201\,\mathrm{V/ms}$ for $V_{\mathrm{sig}} = 32\,\mathrm{V}$ and $f_{\mathrm{sig}} = 1\,\mathrm{kHz}$. Accordingly, to change the output voltage by 32 V with an average rate of change of $201\,\mathrm{V/ms}$ leads to a required time interval of $\Delta t = t_{\mathrm{step}} = 32\,\mathrm{V}/201\,\mathrm{V/ms} = 159.2\,\mu\mathrm{s} \approx 160\,\mu\mathrm{s}$.

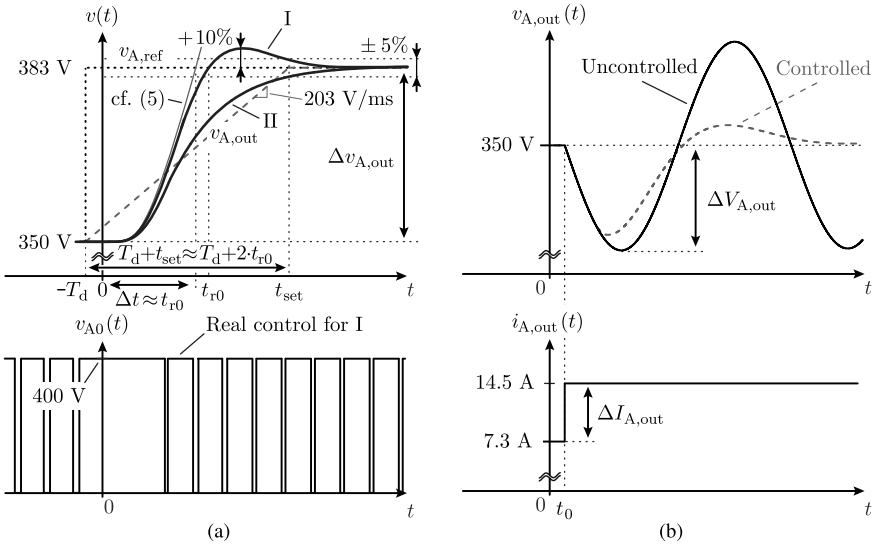

Fig. 3. (a) Visualization of the CPS' output voltage dynamic behavior resulting for idealized control [thin gray line; basis for the slew rate calculation; cf., (5)] and resulting for a real control (solid lines) and (b) illustration of the transient output voltage dip for a single-stage filter with $L_{\mathrm{DM},1} = 154\,\mu\mathrm{H}$ and $C_{\mathrm{DM},1} = 4.6\,\mu F$ in the case of $\Delta I_{\mathrm{A,out}} = 7.2\,\mathrm{A}$ resulting for an uncontrolled (solid line) and controlled output voltage (dashed line). In (a), options I and II of the dynamic behavior of $v_{\mathrm{A,out}}$ represent an underdamped and overdamped system, respectively. The voltage ripples are neglected for the depicted waveforms.

capacitors, $|Q_{\mathrm{cap,max}}|$, must not exceed 10% of the nominal output power, $P_{\mathrm{out,n}}$, at nominal operating conditions, i.e., at $V_{\mathrm{out,n}} = 230\,\mathrm{V}$ and $f_{\mathrm{out}} = 50\,\mathrm{Hz}$.

For preventing a disturbance of sensitive loads supplied by the CPS, the *levels of conducted EMI noise emissions* are restricted according to CISPR 11, Class A, i.e., in the frequency range between 150 kHz and 500 kHz, the conducted emissions need to be less than $79\,\mathrm{dB\mu V}$ and between $500\,\mathrm{kHz}$ and $30\,\mathrm{MHz}$ less than $73\,\mathrm{dB\mu V}$ [16].

III. DS Constraints

In order to fulfill the requirements listed in Table II with the described inverter, a single-stage LC output filter, as shown in Fig. 2(a), could be considered at first. This output filter serves as an accompanying example throughout this section, for which the dimensioning based on the DS approach is subsequently elaborated.

The parameters for the filter DS calculation include all possible values of all filter components and all possible values of further inverter parameters, which are linked to the filter design, e.g., the switching frequency f_{s}. For a single-stage LC filter four such parameters, i.e., $L_{\mathrm{DM},1}$, $C_{\mathrm{DM},1}$, f_{s}, and V_{dc}, exist, which are restricted by

$$L_{\mathrm{DM},1} > 0,\ C_{\mathrm{DM},1} > 0,\ f_{\mathrm{s}} > 0,\ \text{and}\ V_{\mathrm{dc}} > 0. \tag{3}$$

In the rest of this paper, the switching frequency f_{s} is kept constant at $48\,\mathrm{kHz}$ and the DC-link voltage is fixed to either $V_{\mathrm{dc}} = 700\,\mathrm{V}$ or $V_{\mathrm{dc}} = 800\,\mathrm{V}$ for each requirement. Accordingly, a two-dimensional (2D) parameter space spanned by $L_{\mathrm{DM},1}$ and $C_{\mathrm{DM},1}$ is obtained for the single-stage LC output filter shown in Fig. 2(a).

The given CPS specifications and requirements (discussed in Section II and listed in Tables I and II), however, impose five restrictions on the values of $L_{\mathrm{DM},1}$ and/or $C_{\mathrm{DM},1}$. The calculation of the filter DS further includes a sixth constraint that limits the peak-to-peak ripple of the bridge-leg output current to prevent high-frequency winding and core losses in $L_{\mathrm{DM},1}$. All six constraints are detailed below.

It is to be noted that, in this paper, a constant output frequency f_{out} of $50\,\mathrm{Hz}$ is specified. If a generation of output frequencies greater than $50\,\mathrm{Hz}$ would be required, a frequency-dependent current derating of the CPS and/or one additional constraint need to be considered. With these measures, the impacts of increased reactive currents in the filter capacitors at higher output frequencies on the current delivered by the power stage are taken into account. In this context, the need for a high output frequency accompanies the need for a high switching frequency: it can be shown that in the case of a single-stage LC filter, the ratio $f_{\mathrm{s}}/f_{\mathrm{out}}$ needs to satisfy

$$\frac{f_{\mathrm{s}}}{f_{\mathrm{out}}} = \frac{\pi}{4}\,\frac{k_{\mathrm{i}}/k_{\mathrm{v}}}{Q/P} \tag{4}$$

where k_{i} denotes the ratio of maximum inductor current ripple to peak output current, k_{v} the ratio of maximum output voltage ripple to peak output voltage, and Q/P denotes the specific reactive power demand of the filter. With $k_{\mathrm{i}} = 60\%$, $k_{\mathrm{v}} = 2\%$, and $Q/P = 10\%$, the switching frequency needs to be at least 236 times the output frequency, or, for $f_{\mathrm{s}} = 48\,\mathrm{kHz}$, a maximum output frequency of approximately $200\,\mathrm{Hz}$ results.

A. Output Voltage Slew Rate

According to Section II, the minimum average slew rate, SR_{min}, that must be achieved with the output filter is equal to $203\,\mathrm{V/ms}$. This section derives the inequality for L and C that corresponds to this slew rate requirement. To simplify the analysis, idealized voltage control of the CPS is assumed, i.e., the controller applies the maximum possible voltage to the input of the filter network until the required filter output voltage

is obtained, such that the maximum possible rate of change of the output voltage is achieved.

If an input voltage step $\Delta v_{\mathrm{A}0} > 0$ is applied to a single-stage LC filter [cf., Figs. 1 and 2(a)], the current through the filter inductor increases and subsequently the capacitor voltage, i.e., output voltage, starts to change as well. The presented result considers the response to a positive input voltage step (the bridge-leg constantly applies $+V_{\mathrm{dc}}/2$ until the output voltage reaches its new reference value) and neglects the implication of the changing capacitor voltage $v_{\mathrm{A,out}}$ on the inductor current $i_{\mathrm{A}0}$, which, for $m := v_{\mathrm{A,out}}/\frac{V_{\mathrm{dc}}}{2}$, gives

$$\Delta v_{\mathrm{A,out}} \approx \frac{V_{\mathrm{dc}}}{4 \cdot L_{\mathrm{DM},1} \cdot C_{\mathrm{DM},1}} \cdot (1-m) \cdot \Delta t^2 \tag{5}$$

[thin gray line in Fig. 3(a)]. Accordingly, the idealized slew rate is

$$SR_0(\Delta v_{\mathrm{A,out}}) = \sqrt{\frac{\Delta v_{\mathrm{A,out}}^2}{\Delta t^2}} = \sqrt{\frac{V_{\mathrm{dc}}}{4 \cdot L_{\mathrm{DM},1} \cdot C_{\mathrm{DM},1}} \cdot (1-m) \cdot \Delta v_{\mathrm{A,out}}}. \tag{6}$$

The slew rate decreases for increasing modulation index m, since the voltage applied to the filter inductor decreases. Thus, the minimum slew rate occurs for the maximum modulation index (cf., Table I)[3]

$$m_{\max} = \frac{V_{\mathrm{A,out,max,peak}}}{V_{\mathrm{dc,max}}/2} = \frac{350\,\mathrm{V}}{400\,\mathrm{V}} = 0.875. \tag{7}$$

In a real system, the slew rate calculated with (6) may not be achievable, in particular due to the time delay of the employed pulse width modulator and the limited control bandwidth of the closed output voltage control loop. The pulse width modulator is operated with double update mode and, therefore, causes a time delay of $T_{\mathrm{d}} = 1/(2 \cdot f_{\mathrm{s}}) = 10.4\,\mu\mathrm{s}$. The limited bandwidth of the closed voltage control loop is considered based on the assumption that the required change of the output voltage, $\Delta v_{\mathrm{A,out}}$, is performed within the settling time $t_{\mathrm{set}} > t_{\mathrm{r}0}$ (cf., Fig. 3(a); for $t \geq t_{\mathrm{set}}$, $v_{\mathrm{A,out}}$ remains in a $\pm 5\%$ tolerance band of $v_{\mathrm{A,ref}}$) and that $t_{\mathrm{set}}/t_{\mathrm{r}0} \approx 2$ applies, which is justified based on a comparison of the dynamic characteristic of the CPS [43] with a second-order low-pass filter with a damping ratio of $0.6 \leq \zeta \leq 1.2$. The solid black lines in Fig. 3(a), labeled I and II, denote the expected output voltage transients of the controlled system for $\zeta = 0.6$ (underdamped) and $\zeta = 1.2$ (overdamped), respectively, and include the time delay T_{d}. With this, the effective slew rate in the presence of closed-loop voltage control, SR [dashed line in Fig. 3(a)], can be related to the required rise time of the filter, $t_{\mathrm{r}0}$, as

$$SR = \frac{\Delta v_{\mathrm{A,out}}}{T_{\mathrm{d}} + t_{\mathrm{set}}} \approx \frac{\Delta v_{\mathrm{A,out}}}{T_{\mathrm{d}} + 2 \cdot t_{\mathrm{r}0}} = 203\ \mathrm{V/ms} \tag{8}$$

[3] $m_{\max}$ is obtained for $v_{\mathrm{A,out}}(t) = V_{\mathrm{A,out,max,peak}}$ and $V_{\mathrm{dc}} = V_{\mathrm{dc,max}}$, since the CPS' dc-link voltage is increased to $V_{\mathrm{dc}} = 800\,\mathrm{V}$ in case an output voltage in the range of $[\pm 350\,\mathrm{V}]$ must be generated with a high dynamic.

which, for $\Delta v_{\mathrm{A,out}} = 10\% \cdot 325\,\mathrm{V} = 32.5\,\mathrm{V}$ [cf., (1) in Section II], yields

$$t_{\mathrm{r}0} = \frac{1}{2} \cdot \left(\frac{\Delta v_{\mathrm{A,out}}}{SR} - T_{\mathrm{d}} \right) \approx 75\,\mu\mathrm{s}. \tag{9}$$

Thus, the filter is required to realize an idealized slew rate, SR_0 [cf., (6) for $\Delta t = t_{\mathrm{r}0}$], of

$$SR_0 = \frac{\Delta v_{\mathrm{A,out}}}{t_{\mathrm{r}0}} \approx 434\,\mathrm{V/ms}. \tag{10}$$

Furthermore, (9) allows for the estimation of the achievable small-signal bandwidth of the closed voltage control loop, f_{c}, according to [48],

$$f_{\mathrm{c}} \approx \frac{1.8}{2 \cdot \pi \cdot t_{\mathrm{r}0}} \approx 4\,\mathrm{kHz}. \tag{11}$$

Suitable values of $L_{\mathrm{DM},1}$ and $C_{\mathrm{DM},1}$, achieving the required minimum attainable filter slew rate, can be found with (6), (7), and (10) considering

$$SR_0 = 434\,\mathrm{V/ms} \leq \sqrt{\frac{V_{\mathrm{dc}}}{4 \cdot L_{\mathrm{DM},1} \cdot C_{\mathrm{DM},1}} \cdot \frac{1}{8} \cdot 32.5\,\mathrm{V}}. \tag{12}$$

Fig. 4 depicts the values of the maximum allowable filter inductances $L_{\mathrm{DM},1}$ that result for solving (12) for $L_{\mathrm{DM},1}$, i.e.,

$$L_{\mathrm{DM},1} \leq \frac{V_{\mathrm{dc}}}{4 \cdot C_{\mathrm{DM},1}} \cdot \frac{32.5\,\mathrm{V}}{8 \cdot (434\,\mathrm{V/ms})^2} = L_{\mathrm{DM},1,\max} \tag{13}$$

for $1\,\mu\mathrm{F} \leq C_{\mathrm{DM},1} \leq 30\,\mu\mathrm{F}$ (gray-dashed line with label "Out. voltage slew rate"). The arrow points into the area where (12) is fulfilled. $L_{\mathrm{DM},1,\max}$ is directly proportional to the DC-link voltage V_{dc} and inversely proportional to the filter capacitance $C_{\mathrm{DM},1}$.

An accurate value [instead of the simplified expression (6)] for the filter slew rate SR can be calculated with a numerical solver, by means of Laplace transformation. Fig. 4 compares $L_{\mathrm{DM},1,\max}$ obtained with the simplified [cf., (12), label "Approx."] and the accurate expressions [label "Exact"], respectively. The difference between the two lines results from the fact that the approximation assumes a constant voltage difference of $(1-m) \cdot V_{\mathrm{dc}}/2$ across the inductor $L_{\mathrm{DM},1}$ during the entire time interval Δt. In the real system, however, the voltage across $L_{\mathrm{DM},1}$ reduces when the output voltage $v_{\mathrm{A,out}}$ increases. In this example, the approximation leads to a mean relative error of 14%. For the DS of the two-stage LC filter (cf., Fig. 6), no simplified expressions are used and solely the accurate calculation based on the Laplace transformation is considered.

B. Transient Output Voltage Dip

A stepwise change in the output current of $\Delta I_{\mathrm{A,out}}$ leads to a transient in the output voltage $v_{\mathrm{A,out}}$, which, in the end, is compensated by the control of the CPS [controlled LC filter, dashed line in Fig. 3(b)]. However, due to the discrete-time control of the CPS, the compensating action of the control occurs with a time delay. Thus, the height of the voltage dip $\Delta V_{\mathrm{A,out}}$ is in a first approximation only determined by the LC filter elements, i.e., the control does not reduce the voltage dip significantly

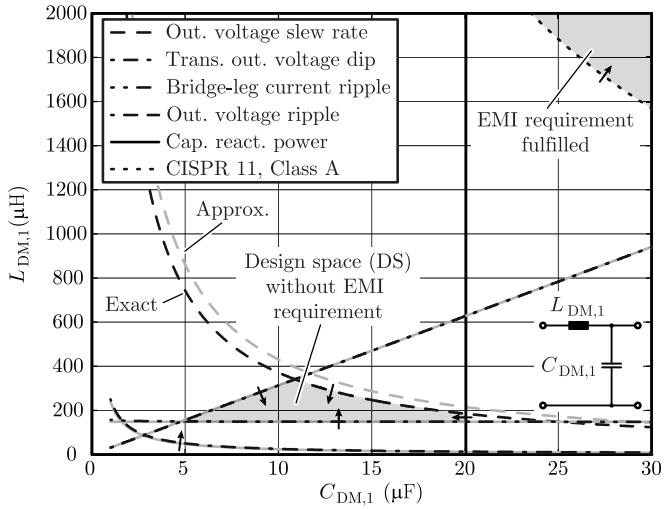

Fig. 4. DS of a single-stage LC filter [cf., Fig. 2(a)], which leads to an empty DS because the compliance with CISPR 11, Class A (boundary depicted in the upper right corner) does not permit to achieve the required slew rate of $203\,\mathrm{V/ms}$. Each arrow points toward the area where the corresponding requirement can be met. The black lines are obtained from the accurate computations and the gray lines result from the approximate expressions.

[cf., Fig. 3(b)] as also experimentally verified in Section V-B for the final realized filter design. Accordingly, $\Delta V_{\mathrm{A,out}}$ is directly obtained from

$$\Delta V_{\mathrm{A,out}} = \Delta I_{\mathrm{A,out}} \cdot \sqrt{\frac{L_{\mathrm{DM,1}}}{C_{\mathrm{DM,1}}}} = \Delta I_{\mathrm{A,out}} \cdot Z_{\mathrm{step}} \qquad (14)$$

[uncontrolled single-stage LC filter; cf., Fig. 3(b)]. Thus, to fulfill the requirements specified in Section III-A, the DS is constrained according to

$$Z_{\mathrm{step}} = \sqrt{\frac{L_{\mathrm{DM,1}}}{C_{\mathrm{DM,1}}}} \leq Z_{\mathrm{step,max}} = 5.6\,\Omega \qquad (15)$$

or the maximum allowable inductance $L_{\mathrm{DM,1}}$ is limited according to

$$L_{\mathrm{DM,1}} \leq C_{\mathrm{DM,1}} \cdot (5.6\,\Omega)^2 = L_{\mathrm{DM,1,max}}. \qquad (16)$$

In case of a more advanced filter structure, e.g., a two-stage LC filter (cf., Fig. 6), no closed-form solution for Z_{step} is available and Z_{step} is rather determined numerically in the time domain for an output current step of height $\Delta I_{\mathrm{A,out}}$ occurring at $t = t_0$

$$\Delta V_{\mathrm{A,out}} = V_{\mathrm{A,out,0}} - \min\left[v_{\mathrm{out}}(t)\right]\big|_{t > t_0}$$
$$Z_{\mathrm{step}} = \frac{\Delta V_{\mathrm{A,out}}}{\Delta I_{\mathrm{A,out}}}. \qquad (17)$$

For the approximate assumption of negligible influence of the control on $\Delta V_{\mathrm{A,out}}$, the actual value of the initial output voltage $V_{\mathrm{A,out,0}}$ has no effect on the value of Z_{step} due to the linear nature of the two-stage filter. Due to the same reason, any step amplitude $\Delta I_{\mathrm{A,out}} > 0$ can be selected.

It is noted from (16) that the maximum allowable inductance $L_{\mathrm{DM,1,max}}$ is directly proportional to $C_{\mathrm{DM,1}}$. $L_{\mathrm{DM,1,max}}\,(C_{\mathrm{DM,1}})$ is plotted in Fig. 4, based on the relation (16) and (17), respectively. The approximated and the exactly calculated results fit nicely.

C. Bridge-Leg Output Current Ripple

Provided that the output voltage ripple at the switching frequency is negligible, a triangular inductor current ripple results and the respective peak-to-peak ripple value is equal to

$$\Delta I_{\mathrm{A}0} = \frac{m \cdot (1-m) \cdot V_{\mathrm{dc}}}{2 \cdot L_{\mathrm{DM,1}} \cdot f_{\mathrm{s}}} \underset{m=0.5}{\leq} \frac{V_{\mathrm{dc}}}{8 \cdot L_{\mathrm{DM,1}} \cdot f_{\mathrm{s}}}$$
$$\leq 60\% \cdot I_{\mathrm{A,out,n,peak}} = 12.3\,\mathrm{A}. \qquad (18)$$

A maximum peak-to-peak inductor current ripple of $12.3\,\mathrm{A}$ ($\pm 30\% \cdot I_{\mathrm{A,out,n,peak}}$) is defined for $V_{\mathrm{dc}} = V_{\mathrm{dc,n}} = 700\,\mathrm{V}$ as compromise between the volume of $L_{\mathrm{DM,1}}$ (and hence the size of the filter), the high-frequency copper and core losses in $L_{\mathrm{DM,1}}$, and the achievable measurement accuracy when sampling the bridge-leg output current close to its average value [45].

Expression (18) can be rearranged for $L_{\mathrm{DM,1}}$

$$L_{\mathrm{DM,1}} \geq \frac{V_{\mathrm{dc}}}{98.4\,\mathrm{A} \cdot f_{\mathrm{s}}} = L_{\mathrm{DM,1,max}} \qquad (19)$$

i.e., the minimum allowable $L_{\mathrm{DM,1}}$ is proportional to the DC-link voltage V_{dc}, inversely proportional to the switching frequency f_{s}, and independent of $C_{\mathrm{DM,1}}$. For more complex filter topologies, the value of $\Delta I_{\mathrm{A}0}$ is calculated numerically in order to consider the voltage ripple across $C_{\mathrm{DM,1}}$ at the switching frequency. The result of this accurate calculation is also given in Fig. 4; only marginal differences between the simplified (19) and the accurate expressions result for practical filter component values.

D. Output Voltage Ripple

At the nominal rms output voltage $v_{\mathrm{A,out}} = V_{\mathrm{A,out,n}} = 230\,\mathrm{V}$, $f_{\mathrm{out}} = 50\,\mathrm{Hz}$, and $V_{\mathrm{dc}} = 800\,\mathrm{V}$, the output voltage distortion remains within the specified limit of $\mathrm{THD_v} < 2.5\%$ (cf., IEEE 1547 [15]), if the peak-to-peak ripple $\Delta V_{\mathrm{A,out}}$ is lower than $22.8\,\mathrm{V}$. With the triangular inductor current given by (18), $\Delta V_{\mathrm{A,out}}$ becomes

$$\Delta V_{\mathrm{A,out}} = \frac{m \cdot (1-m) \cdot V_{\mathrm{dc}}}{16 \cdot L_{\mathrm{DM,1}} \cdot C_{\mathrm{DM,1}} \cdot f_{\mathrm{s}}^2}$$
$$\underset{m=0.5}{\leq} \frac{V_{\mathrm{dc}}}{64 \cdot L_{\mathrm{DM,1}} \cdot C_{\mathrm{DM,1}} \cdot f_{\mathrm{s}}^2} \leq 22.8\,\mathrm{V} \qquad (20)$$

which yields the inequality

$$L_{\mathrm{DM,1}} \geq \frac{V_{\mathrm{dc}}}{1457.2\,\mathrm{V} \cdot C_{\mathrm{DM,1}} \cdot f_{\mathrm{s}}^2} = L_{\mathrm{DM,1,min}}. \qquad (21)$$

From the derived relation, it can be seen that the value of $L_{\mathrm{DM,1}}$ has to be increased with the DC-link voltage V_{dc} and could be reduced for higher capacitances $C_{\mathrm{DM,1}}$. Furthermore, there is a quadratic dependence on the switching frequency f_{s}, as the impedance of $L_{\mathrm{DM,1}}$ increases and the impedance of $C_{\mathrm{DM,1}}$ decreases linearly with f_{s}. For the two-stage filter topology (cf., Fig. 6), the value of $\Delta v_{\mathrm{A,out}}$ is only calculated numerically. The

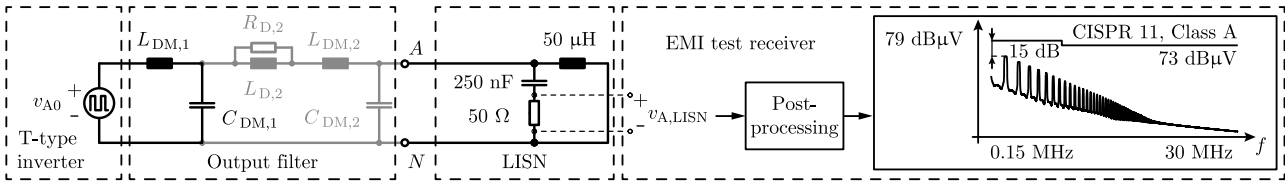

Fig. 5. Equivalent circuit used to model the emitted conducted DM noise of the CPS. The model includes the noise source $v_{\mathrm{A}0}$, the output filter, the LISN, and the test receiver. In the "postprocessing" block, the spectral components of $v_{\mathrm{A,LISN}}$ ($v_{\mathrm{A}0}$ has edges with infinite slope) are computed and the worst case output values of the EMI test receiver with quasi-peak detector are estimated according to [49, eq. (9)].

numerical computation of $L_{\mathrm{DM},1,\min}$ and its approximation by (21) agree well and are depicted in Fig. 4.

E. Capacitive Reactive Power

The reactive power demand caused by the filter capacitor of a phase at the output frequency f_{out} is given by

$$|Q_{\mathrm{cap}}| = 2 \cdot \pi \cdot f_{\mathrm{out}} \cdot C_{\mathrm{DM},1} \cdot V_{\mathrm{A,out,n}}^2 \leq |Q_{\mathrm{cap,max}}| = \frac{1\,\mathrm{kVA}}{3} \tag{22}$$

($|Q_{\mathrm{cap,max}}| = 10\% \cdot P_{\mathrm{out,n}}$). Thus, for $C_{\mathrm{DM},1}$, the inequality

$$C_{\mathrm{DM},1} \leq \frac{|Q_{\mathrm{cap,max}}|}{2 \cdot \pi \cdot f_{\mathrm{out}} \cdot V_{\mathrm{A,out,n}}^2} = C_{\mathrm{DM},1,\max} \tag{23}$$

applies, which is independent of $L_{\mathrm{DM},1}$. $C_{\mathrm{DM},1,\max}$ is shown in Fig. 4. In the case of the two-stage filter, the value of $C_{\mathrm{DM},1}$ in (23) is replaced by the sum of all DM filter capacitors that belong to the considered phase A, i.e., $C_{\mathrm{DM},1}$ and $k \cdot C_{\mathrm{DM},1}$ (cf., Fig. 6).

F. Limits of Conducted EMI

This criterion compares the emitted levels of conducted differential-mode (DM) EMI to the maximum levels allowed for the CISPR 11 norm, Class A. Fig. 5 depicts the noise source model that is employed to calculate the EMI emission: it consists of a voltage source $v_{\mathrm{A}0}(t)$, with edges of infinite slope, representing the inverter stage, the EMI filter, the line impedance stabilization network (LISN), and the test receiver. Only DM EMI noise is considered as the star point of the three-phase filter is connected to the DC-link voltage center point. A margin of 15 dB is included in the design of the filter to ensure that any common-mode (CM) emissions (resulting, e.g., from parasitic capacitive coupling of the power transistors to ground [50]) could also be accommodated in the limits of the CISPR 11 norm.[4] The EMI noise voltage is calculated based on the approach presented in [49], which employs a worst case estimation.

G. Discussion

Fig. 4 shows the DS which is obtained for a single-stage LC output filter *excluding* the compliance with CISPR 11, Class A: for $C_{\mathrm{DM},1}$ ranging from 5 to 20 µF, all selected criteria

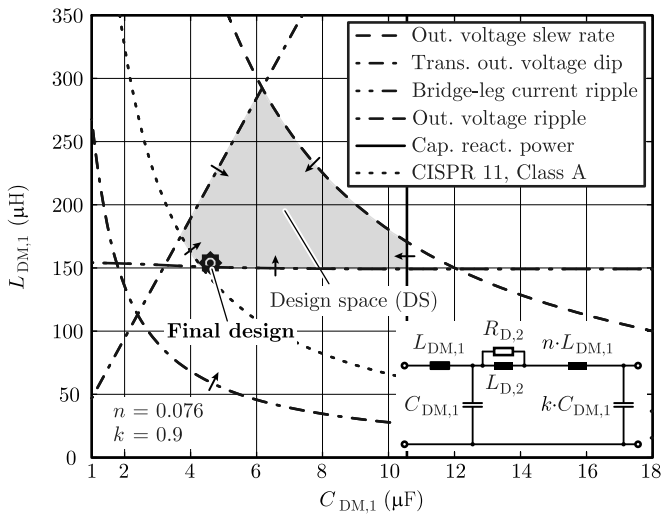

Fig. 6. DS for a two-stage LC output filter [cf., Fig. 2(b)] for $n = L_{\mathrm{DM},2}/L_{\mathrm{DM},1} = 0.076$ and $k = C_{\mathrm{DM},2}/C_{\mathrm{DM},1} = 0.9$, as resulting from the optimization in Section IV-B (cf., Table III).

can be satisfied. However, as clearly visible, the DS is empty if the EMI requirement should also be fulfilled. To obtain the required attenuation of conducted noise, increased values of $L_{\mathrm{DM},1}$ and $C_{\mathrm{DM},1}$ would be required, which would not allow to fulfill the slew rate requirement.

Options to overcome this issue are presented in [45]. There, adding an LC stage to the single-stage filter, i.e., employing a two-stage LC output filter [cf., Fig. 2(b)], is identified to be most effective with respect to cost, construction volume, and efficiency. For defining the two-stage LC output filter, two variables, n and k, are introduced

$$n := \frac{L_{\mathrm{DM},2}}{L_{\mathrm{DM},1}},\ k := \frac{C_{\mathrm{DM},2}}{C_{\mathrm{DM},1}}. \tag{24}$$

With $L_{\mathrm{DM},1}$, $C_{\mathrm{DM},1}$, n, and k, a four-dimensional (4D) parameter space results.[5] To obtain a clear illustration of the DS, it is depicted in the $C_{\mathrm{DM},1}$–$L_{\mathrm{DM},1}$ plane for fixed n and k values as shown in Fig. 6 for $n = 0.076$ and $k = 0.9$. (The calculation of the DS illustrated in Fig. 6 is based on exact numerical computations of the different requirements as explained above.) According to Fig. 6, in the case of a two-stage LC filter approach, dedicated values of $L_{\mathrm{DM},1}$, $C_{\mathrm{DM},1}$, n, and k exist with

[4] If required, the model could be extended with respect to CM EMI noise using the approach presented in [51] and [52].

[5] For given $L_{\mathrm{DM},2} = n \cdot L_{\mathrm{DM},1}$ and $C_{\mathrm{DM},2} = k \cdot C_{\mathrm{DM},1}$ the values of the damping components $L_{\mathrm{D},2}$ and $R_{\mathrm{D},2}$ are determined according to (25). Thus, $L_{\mathrm{D},2}$ and $R_{\mathrm{D},2}$ do not represent free parameters in this paper.

which all requirements can be simultaneously fulfilled. The determination of n and k is detailed in Section IV-B.

According to [53], the second LC filter stage is passively damped with a serial RL-branch. The optimal value $R_{\mathrm{D},2,\mathrm{opt}}$ of the damping resistor $R_{\mathrm{D},2}$ for a given damping inductance $L_{\mathrm{D},2}$ is computed such that the filter input-to-output transfer function leads to the smallest resonance gain A_{rr}, in contrast to [54], where $R_{\mathrm{D},2}$ is calculated to result in the minimal peak of the filter output impedance. For the filter design

$$a = \frac{L_{\mathrm{D},2}}{L_{\mathrm{DM},2}} = 2, \text{and}$$

$$R_{\mathrm{D},2} = R_{\mathrm{D},2,\mathrm{opt}} = \sqrt{\frac{L_{\mathrm{DM},2}}{C_{\mathrm{DM},2}}} \cdot \frac{2 \cdot a}{\sqrt{2 \cdot a^2 + 6 \cdot a + 4}} \quad (25)$$

are used to obtain a maximum A_{rr} of 6 dB. With $A_{\mathrm{rr}} = 6$ dB, the second filter stage is of approximate Chebyshev type (with ripple factor $\epsilon = 0.12$ [55]).

IV. Two-Stage Filter Design

The different criteria detailed in Section III constrain the DS of the two-stage LC output filter as, for example, shown in Fig. 6. However, in order to facilitate the realization of the most suitable output filter for the CPS, within the DS, an appropriate selection procedure has to be defined. In this study, a multi-objective filter optimization, based on the ρ–η PF [35], is conducted for the two-stage LC output filter depicted in Fig. 2(b). The loss and volume models needed for this optimization are summarized in Section IV-A. Section IV-B details the optimization procedure and discusses the calculated optimization results.

A. Losses and Volumes of Inductors and Capacitors

The inductor losses comprise copper and core losses. The calculation of the copper losses considers DC and AC losses (by reason of skin and proximity effects), which, for $L_{\mathrm{DM},1}$, are computed with

$$P_{\mathrm{cu}} = R_{\mathrm{dc}} \cdot I_{\mathrm{A,out,n}}^2 + \sum_{m=1}^{I_m \geq 5\% \cdot I_1} R_{\mathrm{ac},m} \cdot I_m^2 \quad (26)$$

where I_m is the rms value of the mth harmonic of the inductor current ripple. R_{dc} and $R_{\mathrm{ac},m}$ are calculated according to [56], [57] for a temperature of 100 °C. Equation (26) considers all harmonics with an rms value larger than or equal to 5% of the rms value I_1 of the first harmonic. The calculations of the current ripples for the inductors of the second filter stage [cf., Fig. 2(b)] are based on the simplifying assumption that the high-frequency AC components of the current through $L_{\mathrm{DM},1}$, $i_{\mathrm{A0,ripple}}(t)$, can be represented by a single harmonic at the switching frequency with an rms value of

$$i_{\mathrm{A0,ripple,rms}} = \sqrt{\frac{1}{T_{\mathrm{s}}} \cdot \int_0^{T_{\mathrm{s}}} i_{\mathrm{A0,ripple}}(t)^2 \cdot dt} \underset{m=0.5}{=} \frac{V_{\mathrm{dc,max}}}{\sqrt{3} \cdot 16 \cdot L_{\mathrm{DM},1} \cdot f_{\mathrm{s}}}. \quad (27)$$

The current ripples through $L_{\mathrm{DM},2}$ and $L_{\mathrm{D},2}$ are then computed based on $i_{\mathrm{A0,ripple,rms}}$ and employing linear network analysis.

To realize the winding of the inductors, enameled copper wires are considered, because for the case at hand, enameled wire leads to lower ohmic losses compared to litz wire due to the greater achievable winding area filling factor [17].

The core losses P_{fe} are calculated with the improved generalized Steinmetz equation (iGSE) according to [57], [58]. The Steinmetz parameters k, α, and β, needed for evaluating the iGSE, are given at a core temperature of 100 °C in [59] and [60] for the selected ferrite (N27 and N87 materials) E-cores from TDK EPCOS [61] to realize the inductors. Ferrite cores are utilized because of lower cost compared to nanocrystalline cores and due to a constant inductance over current compared to powder cores.

The evaluation of the copper and core losses requires the bridge-leg output current, $i_{\mathrm{A0,ripple}}(t)$, and the flux density in the core, $B(t)$, which are computed for the following worst case conditions:

$$\begin{aligned} &\text{max. DC-link voltage:} && V_{\mathrm{dc}} = V_{\mathrm{dc,max}} = 800\,\mathrm{V}, \\ &\text{DC output current:} && I_{\mathrm{A,out}} = 17\,\mathrm{A}, \\ &\text{modulation index:} && m = v_{\mathrm{A,out}} / \frac{V_{\mathrm{dc,max}}}{2} = 0.5, \\ &\rightarrow \text{DC out. voltage:} && v_{\mathrm{A,out}} = 200\,\mathrm{V}. \end{aligned} \quad (28)$$

The modulation index $m = 0.5$ leads to the maximum current ripple ΔI_{A0} (cf., Section III-C) and thus also to the maximum flux density ripple ΔB, which results in the maximum core losses according to the iGSE. To compute the current ripple ΔI_{A0} through $L_{\mathrm{DM},1}$, the voltage across $C_{\mathrm{DM},1}$ is assumed constant over one switching period T_{s}. The current is increased from the nominal value $I_{\mathrm{A,out,n}} = 14.5$ A to $I_{\mathrm{A,out}} = 17$ A for the following reason. One application of the CPS could be the emulation of a low voltage mains (e.g., 230 V/400 V). The tolerance of the mains voltage is according to [62] (IEC standard voltages) $+10\%/-14\%$. Thus, to supply a load with $P_{\mathrm{A,out,n}} = 3.3$ kW for an emulated rms mains voltage of $230\,\mathrm{V} \cdot (1 - 0.14) = 198$ V leads to a rms current of $I_{\mathrm{A,out}} = 16.7\,\mathrm{A} \approx 17\,\mathrm{A}$.

Finally, to verify that the calculated winding losses P_{cu} and core losses P_{fe} do not lead to excessive temperature rises in the inductor, the maximum temperature $T_{\mathrm{L,max}}$ of the inductor is approximated with

$$T_{\mathrm{L,max}} = R_{\mathrm{th}} \cdot (P_{\mathrm{fe}} + P_{\mathrm{cu}}) + 40\,^{\circ}\mathrm{C} \quad (29)$$

assuming an ambient temperature of 40 °C. The thermal resistance R_{th} is calculated with the empirical relation given in [63, Fig. 2] for E-cores

$$R_{\mathrm{th}} = \left(53 \cdot \left(V_{\mathrm{eff}}\,[\mathrm{cm}^3]\right)^{-0.54}\right) \frac{\mathrm{K}}{\mathrm{W}} \quad (30)$$

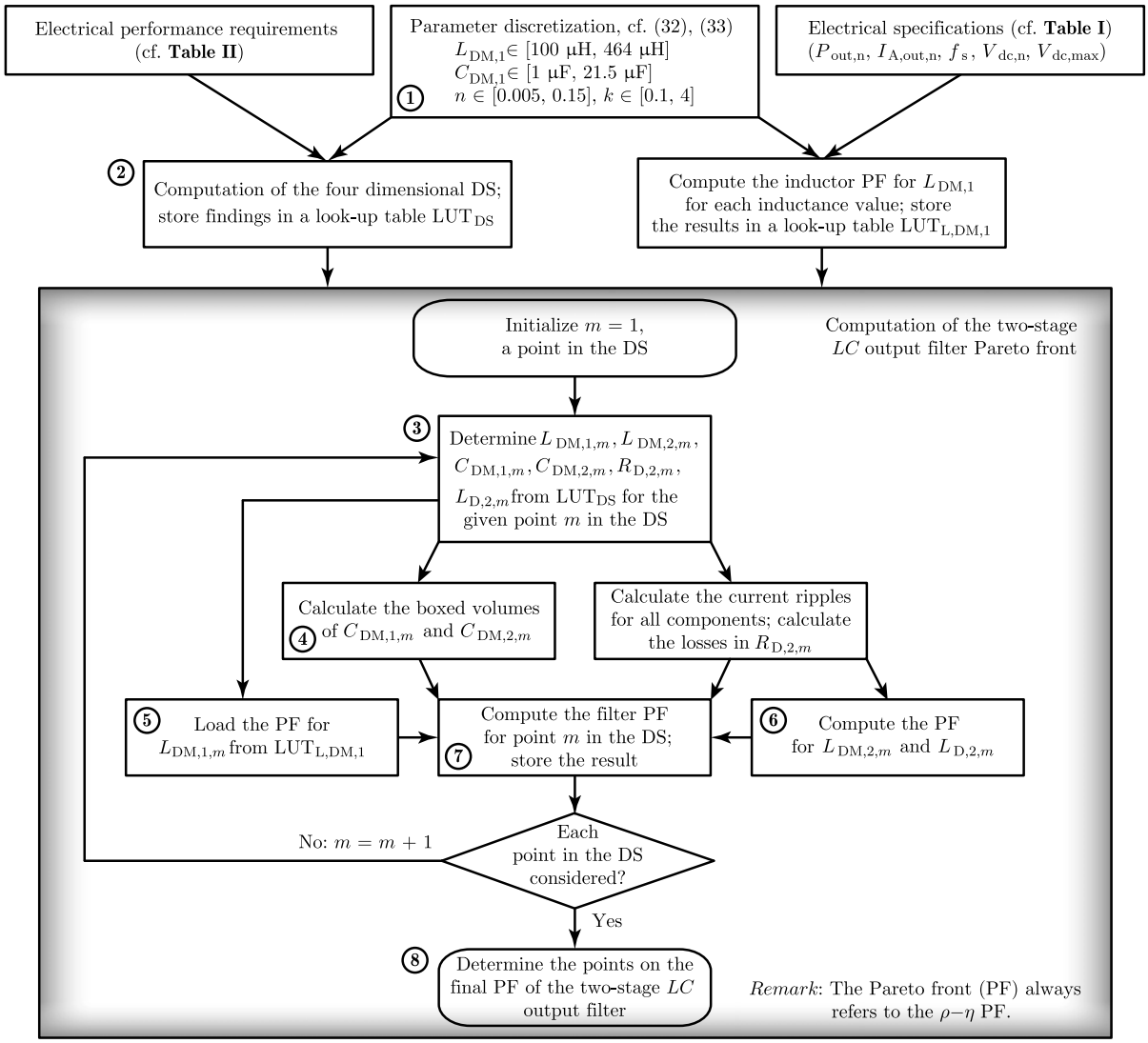

Fig. 7. Flowchart to compute the ρ–η PF for a two-stage LC output filter [cf., Fig. 2(b)].

where V_{eff} is the effective core volume.[6] Inductor designs which exceed $T_{\mathrm{L,max}} = 100\,^{\circ}\mathrm{C}$ are excluded from the Pareto optimization explained in the next section.

The boxed volume of the inductor is calculated with the dimensions of the core and the estimated dimensions of the winding heads (including the bobbin dimensions) [61].

The capacitors of the output filter are realized with X2/305 V rated MKP (polypropylene) film capacitors from EPCOS [64]. Their dielectric losses are negligible compared to the inductor losses. The boxed volume of the capacitor with capacitance $C_{\mathrm{DM},i}$ ($i = 1, 2$) is estimated with

$$V_{C_{\mathrm{DM},i,\mathrm{boxed}}} = 4.15\ \frac{\mathrm{cm}^3}{\mu\mathrm{F}} \cdot C_{\mathrm{DM},i}[\mu F] + 1.54\ \mathrm{cm}^3. \quad (31)$$

This is a fit to the boxed volumes computed for the capacitors with a lead spacing of 27.5 mm given in [64], which are considered to be most suitable for the investigated output filter.

[6]Relation (30) is experimentally derived generating only winding losses in the components. However, as stated in [63, Remark 2, Sec. 2], the same relation was found while heating the core with only core losses.

B. Filter Design and Optimization

The loss and volume models are employed to compute the ρ–η PF of the two-stage LC filter [cf., Fig. 2(b)] based on the 4D DS with design variables $L_{\mathrm{DM},1}$, $C_{\mathrm{DM},1}$, n, and k (detailed in Section III-G). Fig. 7 depicts the flowchart of the optimization procedure. In a first step, the different criteria for the CPS derived in Section III are evaluated for high numbers of values of $L_{\mathrm{DM},1}$, $C_{\mathrm{DM},1}$, n, and k (box ① in Fig. 7). In order to achieve a constant relative (percentaged) change between adjacent values of inductances and capacitances, i.e., $L_{\mathrm{DM},1,i+1}/L_{\mathrm{DM},1,i} = \mathrm{const.}$ and $C_{\mathrm{DM},1,j+1}/C_{\mathrm{DM},1,j} = \mathrm{const.}$, geometric series are selected

$$\begin{aligned} L_{\mathrm{DM},1,i} &= L_{\mathrm{DM},1,\min} \cdot 10^{\frac{i}{48}}, \\ L_{\mathrm{DM},1,\min} &= 100\,\mu\mathrm{H},\ 0 \le i \le 32,\ i \in \mathbb{N}_0 \\ C_{\mathrm{DM},1,j} &= C_{\mathrm{DM},1,\min} \cdot 10^{\frac{j}{12}}, \\ C_{\mathrm{DM},1,\min} &= 1\,\mu\mathrm{F},\ 0 \le j \le 16,\ j \in \mathbb{N}_0. \end{aligned} \quad (32)$$

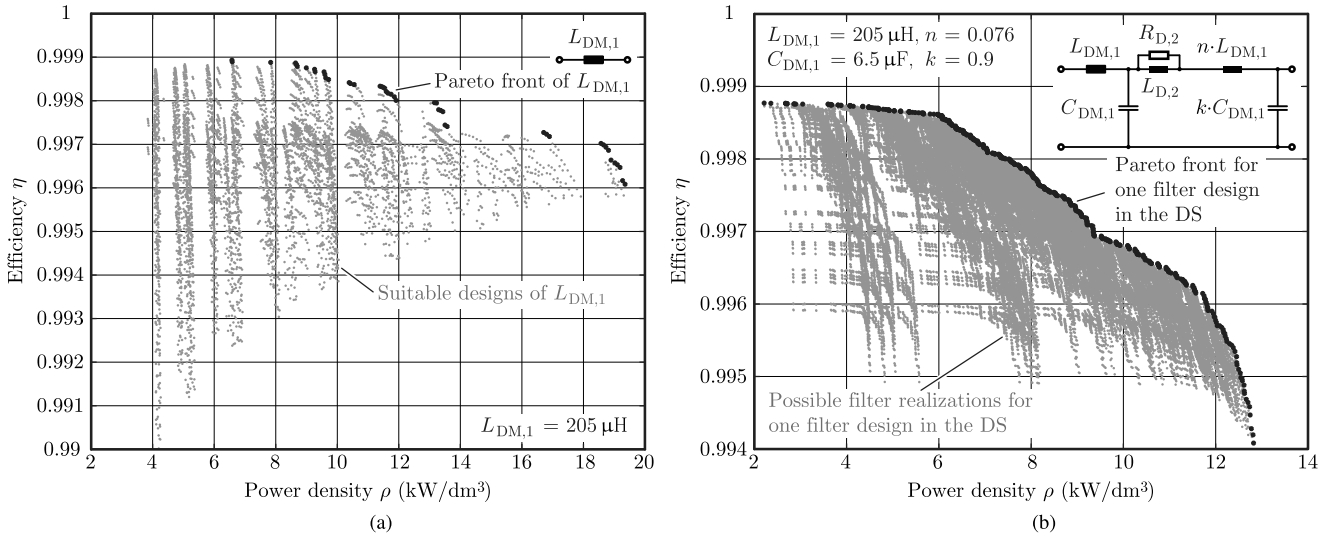

Fig. 8. (a) Exemplary ρ–η PF for inductor $L_{\mathrm{DM},1}$ to achieve an inductance of 205 µH. (b) Exemplary ρ–η PF of the whole filter for one arbitrary selected filter design in the DS with parameters $L_{\mathrm{DM},1} = 205\,\mu\mathrm{H}$, $C_{\mathrm{DM},1} = 6.5\,\mu\mathrm{F}$, $n = 0.076$, and $k = 0.9$. The PF of the filter is calculated based on the three inductor PFs for $L_{\mathrm{DM},1}$, $L_{\mathrm{DM},2}$, and $L_{\mathrm{D},2}$.

With this, $L_{\mathrm{DM},1,i}$ and $C_{\mathrm{DM},1,j}$ are selected according to the commonly known E48 and E12 series of preferred values, respectively [65] (also known from the partitioning of ohmic values of commercially available resistors). Furthermore, a comparably high resolution is used for the inductors, due to the possibility of tuning inductances by altering the lengths of the air gap, and a reduced resolution is considered for the capacitances, on the basis of available capacitance values. The values of n and k are selected based on linear distributions

$$\begin{aligned} n &\in [0.005, 0.15], \qquad & n_{\mathrm{step}} &= 0.005, \\ k &\in [0.1, 4], & k_{\mathrm{step}} &= 0.05. \end{aligned} \tag{33}$$

In total $33 \times 17 \times 30 \times 79 \approx 1.3$ million points result.[7]

It is noted that the filter components have tolerances, which, however, are not considered in the presented computation because the focus is on the derivation of the DS and the ρ–η Pareto optimization.[8] The impact of these tolerances on the DS are elaborated in the Appendix. If required, these implications can be included for a given confidence interval by means of worst case assumptions. The particular combination of component values that leads to the worst case, however, needs to be determined separately for each considered criterion that confines the DS.

The 4D DS is calculated for the inductances and capacitances given with (32) and (33), which, for this particular application, results in 40 512 different quadruples of ($L_{\mathrm{DM},1}$, $C_{\mathrm{DM},1}$, n, k), which fulfill all criteria (box ② in Fig. 7).

In a second step, the ρ–η PF of the two-stage LC filter is calculated for the previously computed 4D DS. The approach behind the PF computation is detailed for an arbitrary point in the middle of the DS given by

$$L_{\mathrm{DM},1} = 205\,\mu\mathrm{H},\ C_{\mathrm{DM},1} = 6.5\,\mu\mathrm{F},\ n = 0.076, \text{ and } k = 0.9 \tag{34}$$

leading to $L_{\mathrm{D},2} = 31.2\,\mu\mathrm{H}$ and $R_{\mathrm{D},2} = 1.33\,\Omega$ [cf., (25), Fig. 6, and ③ in Fig. 7].

For this exemplary point in the DS, all filter capacitors are selected and all inductors are designed. It is assumed that capacitors with capacitance values of $C_{\mathrm{DM},1} = 6.5\,\mu\mathrm{F}$ and $C_{\mathrm{DM},2} = k \cdot C_{\mathrm{DM},1} = 5.9\,\mu\mathrm{F}$ exist and thus the volumes $V_{C_{\mathrm{DM},1}}$ and $V_{C_{\mathrm{DM},2}}$ of $C_{\mathrm{DM},1}$ and $C_{\mathrm{DM},2}$ are calculated with (31) [④in Fig. 7]. The inductors are designed with a dedicated design procedure, which considers 30 different ferrite E-cores from EPCOS [61], up to five stacked cores, up to $N_{\max}$ turns, and wire diameters ranging from $0.1\,\mathrm{mm}$ to $d_{\mathrm{wire,max}}$ with a step size of $d_{\mathrm{wire,step}} = 0.1\,\mathrm{mm}$. The maximum number of turns $N_{\max}$ is determined such that the maximum air gap length, indicated in the data sheet for each core [61], is not exceeded and $d_{\mathrm{wire,max}}$ is calculated based on the core and bobbin dimensions in order to fit the winding into the available volume.

This results in 5 848 suitable designs for $L_{\mathrm{DM},1}$, 13 237 suitable designs for $L_{\mathrm{DM},2}$, and 13 899 suitable designs for $L_{\mathrm{D},2}$, obtaining also the losses $P_{L_{\mathrm{DM},1}}$, $P_{L_{\mathrm{DM},2}}$, and $P_{L_{\mathrm{D},2}}$ and volumes $V_{L_{\mathrm{DM},1}}$, $V_{L_{\mathrm{DM},2}}$, and $V_{L_{\mathrm{D},2}}$ of $L_{\mathrm{DM},1}$, $L_{\mathrm{DM},2}$, and $L_{\mathrm{D},2}$ for all designs as explained in Section IV-A.

To get each and every possible two-stage LC filter realization, all suitable inductor designs for $L_{\mathrm{DM},1}$, $L_{\mathrm{DM},2}$, and $L_{\mathrm{D},2}$ need to be combined with each other, leading to 108×10^{10} filter realization options. An effective reduction of the number of different filter realizations is achieved if only the inductor designs are considered that give a high power density and/or efficiency. The corresponding inductor designs are directly obtained by taking those design results that form the PF in the respective

[7]It is remarked that different discretizations of $L_{\mathrm{DM},1}$, $C_{\mathrm{DM},1}$, n, and k can be used, based on particular needs, e.g., based on available or preferred component values.

[8]The final components could be selected carefully such that the measured and calculated component values fit closely (cf., Table III).

TABLE III
TWO-STAGE LC OUTPUT FILTER [CF., FIG. 2(B)] DESIGN RESULTING FROM THE ρ–η PARETO OPTIMIZATION (CF., FIGS. 7 AND 9) AND ITS HARDWARE REALIZATION (CF., SECTION IV-A)

Component	*Result from the Pareto Optimization*	*Calculated Boxed Volume*	*Hardware Realization*	*Measured Value* at* 48 kHz	*Measured Boxed Volume*
$L_{\mathrm{DM},1}$	154 µH	146.8 cm^3	4 × 2× E 47/20/16 (ferrite N87, EPCOS) $N = 13$, $\varnothing_{\mathrm{cu}} = 2.5\,\mathrm{mm}$, $d_{\mathrm{air}} = 1.83\,\mathrm{mm}$	154.2 µH	157.3 cm^3
$C_{\mathrm{DM},1}$	4.6 µF	20.6 cm^3	4.7 µF$_{\mathrm{rated}}$||0.68 µF$_{\mathrm{rated}}$ X2/305V$_{\mathrm{rms}}$ AC B32924C3475M and B32923C3684M (MKP, EPCOS)	4.7 µF	24.0 cm^3
$L_{\mathrm{DM},2}$	11.6 µH	9.4 cm^3	3 × 2× E 20/10/6 (ferrite N27, EPCOS) $N = 8$, $\varnothing_{\mathrm{cu}} = 1.4\,\mathrm{mm}$, $d_{\mathrm{air}} = 1.03\,\mathrm{mm}$	11.7 µH	10.2 cm^3
$C_{\mathrm{DM},2}$	4.1 µF	18.7 cm^3	4.7 µF$_{\mathrm{rated}}$ X2/305 V$_{\mathrm{rms}}$ AC B32924C3475M (MKP, EPCOS)	4.1 µF	17.9 cm^3
$L_{\mathrm{D},2}$	23.1 µH	16.6 cm^3	2 × 2× E 25/13/7 (ferrite N27, EPOCS) $N = 14$, $\varnothing_{\mathrm{cu}} = 1.8\,\mathrm{mm}$, $d_{\mathrm{air}} = 1.78\,\mathrm{mm}$	22.4 µH	19.4 cm^3
$R_{\mathrm{D},2}$	1.36 Ω	Neglected	2.67 Ω||2.7 Ω = 1.34 Ω Thick film 2512 SMD 1W resistors	1.34 Ω	0.01 cm^3

* Measured with the Agilent impedance analyzer 4294A (40 Hz — 110 MHz) and without pre-magnetization for the inductors and DC voltage offset for the capacitors.

ρ–η plane; cf., Fig. 8(a) for $L_{\mathrm{DM},1}$ [⑤and ⑥in Fig. 7].[9] An inductor design with ρ_j and η_j is on the PF if its η_j is greater than the efficiencies η of all other designs with a higher power density $\rho > \rho_j$.

To find filter realizations with minimal volume (→ maximum power density) for a given efficiency and/or with minimum losses (→ maximum efficiency) for a given volume, only the inductor designs on the corresponding inductor PF can be considered, because the inductor designs for given inductance values $L_{\mathrm{DM},1}$, $L_{\mathrm{DM},2}$, and $L_{\mathrm{D},2}$ are independent from each other, and the losses and volumes are strictly greater than zero, i.e. $P_{L_{\mathrm{DM},1}} > 0$, $P_{L_{\mathrm{DM},2}} > 0$, and $P_{L_{\mathrm{D},2}} > 0$ and $V_{L_{\mathrm{DM},1}} > 0$, $V_{L_{\mathrm{DM},2}} > 0$, and $V_{L_{\mathrm{D},2}} > 0$. Therefore, only 46 designs on the inductor PF are considered for $L_{\mathrm{DM},1}$, 51 for $L_{\mathrm{DM},2}$, and 51 for $L_{\mathrm{D},2}$, resulting in $46 \times 51 \times 51 = 119\,646$ two-stage filter realizations [gray points in Fig. 8(b)]. The power density ρ_q and efficiency η_q of a filter design q can be computed according to

$$\rho_q = \frac{P_{\mathrm{A,out,n}}}{V_{L_{\mathrm{DM},1},q} + V_{C_{\mathrm{DM},1},q} + V_{L_{\mathrm{DM},2},q} + V_{C_{\mathrm{DM},2},q} + V_{L_{\mathrm{D},2},q}}$$

$$\eta_q = \frac{P_{\mathrm{A,out,n}}}{P_{\mathrm{A,out,n}} + \left(P_{L_{\mathrm{DM},1},q} + P_{L_{\mathrm{DM},2},q} + P_{L_{\mathrm{D},2},q} + P_{R_{\mathrm{D},2},q}\right)} \tag{35}$$

where $P_{\mathrm{A,out,n}}$ is equal to $10\,\mathrm{kW}/3$ and $P_{R_{\mathrm{D},2},q}$ denote the losses of the damping resistor $R_{\mathrm{D},2}$. To further reduce the number of filter realizations of the selected point in the DS ($L_{\mathrm{DM},1} = 205\,\mu\mathrm{H}$, $C_{\mathrm{DM},1} = 6.5\,\mu\mathrm{F}$, $n = 0.076$, and $k = 0.9$), again, only the resulting filter ρ–η PF as depicted in Fig. 8(b), consisting of 559 points, is taken and stored [⑦in Fig. 7].

As explained for the selected quadruple [cf., (34)], the filter PF for each quadruple in the DS is computed in the same manner, and the final ρ–η PF of the two-stage LC output filter, as shown in Fig. 9 (black points), can be calculated from the filter PFs [⑧

[9]Because the voltage across $C_{\mathrm{DM},1}$ is assumed to be constant, the inductor PFs for all inductance values of $L_{\mathrm{DM},1}$ are only computed once and stored in a lookup table (cf., Fig. 7).

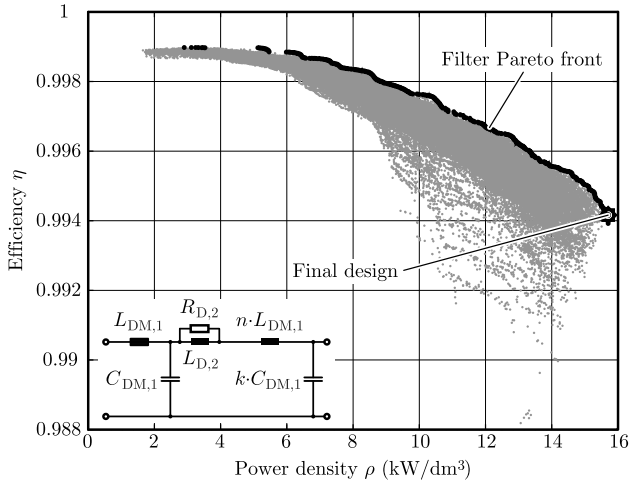

Fig. 9. Result of the ρ–η Pareto optimization for a two-stage LC output filter [cf., Fig. 2(b)] in its 4D DS [cf., Fig. 7] resulting in the filter PF. The final design (cf., Table III) is indicated and achieves a calculated power density of $15.7\ \mathrm{kW/dm^3}$ ($257\ \mathrm{W/in^3}$) for an efficiency of 99.4%. Compared to the initially considered arbitrary point in the DS [cf., (34)] leading to $12.8\ \mathrm{kW/dm^3}$ for the same efficiency of 99.4% [cf., Fig. 8(b)], the design on the filter PF shows a 18% higher power density.

in Fig. 7]. From all designs on this final filter PF, the filter design with the highest power density of $\rho = 15.7\,\mathrm{kW/dm^3}$ still has a reasonable high efficiency of $\eta = 99.4\%$ and hence is selected and realized as summarized in Table III.

It is noted that the presented ρ–η PF calculation for the two-stage LC filter could be extended, in the same way as discussed in this section, also to LC filters with a higher number of stages.

V. EXPERIMENTAL RESULTS

To validate the proposed filter design approach for the selected two-stage LC output filter (cf., Table III), the compliance to the six requirements defined in Section III is verified (cf., Table IV). According to Table IV, all requirements can be fulfilled and the numerical calculations closely fit with the measured results. In

TABLE IV
COMPARISON BETWEEN THE CALCULATED AND MEASURED PERFORMANCE INDEXES AS DEFINED IN SECTION III (CF., TABLE II) FOR THE ρ–η PARETO OPTIMIZED AND REALIZED TWO-STAGE LC OUTPUT FILTER [CF., FIG. 2(B)] WITH THE MEASURED VALUES AS GIVEN IN TABLE III

Requirement	*Required Min./Max. Value*	*Calculated Value*	*Measured Value*
Output voltage slew rate *SR* (cf., Section III-A)	min. $203\,\mathrm{V/ms}$	$322\,\mathrm{V/ms}$	$324\,\mathrm{V/ms}$
Transient output voltage dip $\rightarrow Z_{\mathrm{step}}$ (cf., Section III-B)	max. $5.6\,\Omega$	$4.7\,\Omega$	$4.2\,\Omega$
Bridge-leg current ripple Δi_{A0} (cf., Section III-C)	max. $12.3\,\mathrm{A}$	$12.0\,\mathrm{A}$	$12.2\,\mathrm{A}$
Output voltage ripple $\Delta v_{\mathrm{A,out}}$ (cf., Section III-D)	max. $22.8\,\mathrm{V}$	$2.5\,\mathrm{V}$	$2.6\,\mathrm{V}$
Capacitive reactive power Q_{cap} (cf., Section III-E)	max. $333\,\mathrm{VA}$	$147\,\mathrm{VA}$	$146\,\mathrm{VA}^*$
Conducted EMI limit (cf., Section III-F)	max. $79\,\mathrm{dB\mu V}(f < 500\,\mathrm{kHz})$	$62.4\,\mathrm{dB\mu V}$ @ $192\,\mathrm{kHz}$	$57.1\,\mathrm{dB\mu V}$ @ $192\,\mathrm{kHz}$

* This value is calculated with $(230\,\mathrm{V})^2/|\underline{Z}_{\mathrm{out}}|$ based on the measured output impedance $\underline{Z}_{\mathrm{out}} = 363\,\Omega \cdot \mathrm{e}^{-\mathrm{j}\cdot 89.97^\circ}$ at $f_{\mathrm{out}} = 50\,\mathrm{Hz}$ with the input of the filter being open.

this context, it should again be noted that a margin of $15\,\mathrm{dB}$ is included in the filter design to ensure a very low EMI noise level of the generated output voltage.

As can be seen by comparing columns three and six of Table IV, the boxed volumes of the built inductors $L_{\mathrm{DM},1}$, $L_{\mathrm{DM},2}$, and $L_{\mathrm{D},2}$ are 7%, 8%, and 14% larger than the calculated ones, resulting in a measured power density of $\rho_{\mathrm{meas}} = 14.6\,\mathrm{kW/dm^3}$ $(239\,\mathrm{W/in^3})$ instead of $\rho = 15.7\,\mathrm{kW/dm^3}$ $(257\,\mathrm{W/in^3})$ [deviation of 7%]. The main reason is that each turn, with the wires of the selected wire diameters, requires a certain radius of curvature to be wound around the middle leg of the E-core.

To measure accurately the total losses of the output filter for the conditions given in (28), i.e., $I_{\mathrm{A,out}} = 17\,\mathrm{A}$ and $V_{\mathrm{A,out}} = 200\,\mathrm{V}$ for $V_{\mathrm{dc}} = V_{\mathrm{dc,max}} = 800\,\mathrm{V}$, resulting in a modulation index of $m = 0.5$ and/or the maximum peak-to-peak bridge-leg output current ripple, the DC losses were measured separately from the AC losses. DC losses of $13.0\,\mathrm{W}$ were measured in the thermal equilibrium for a DC current $I_{\mathrm{A0}} = I_{\mathrm{A,out}} = 17\,\mathrm{A}$. The measured value results from the multiplication of the measured DC voltage and DC current at the input of the filter for a shorted output. The voltage and the current were measured with Multimeters Fluke 189, which leads to an error of 1% [66] for the DC power (loss) measurement. The calculated DC losses of $12.8\,\mathrm{W}$ agree with the measured value (deviation of 2%). On the other hand, AC losses of $5.3\,\mathrm{W}$ were measured with a Yokogawa WT3000 power analyzer for no load, $V_{\mathrm{A,out}} = 200\,\mathrm{V}$, and $V_{\mathrm{dc}} = V_{\mathrm{dc,max}} = 800\,\mathrm{V}$, and just after the entire filter was operated in the thermal equilibrium under the conditions of (28), in order to measure the losses for component temperatures corresponding to the mentioned conditions. According to the data sheet of the power analyzer [67], the error of this measurement is 11%. A comparison to the calculated value of $6.6\,\mathrm{W}$ reveals that the calculation overestimates the AC losses by 20%. Accordingly, the total measured losses of the filter are $13.0\,\mathrm{W} + 5.3\,\mathrm{W} = 18.3\,\mathrm{W}$ (measurement error of $\pm 4\%$), which is in good agreement with the calculated losses of $12.8\,\mathrm{W} + 6.6\,\mathrm{W} = 19.4\,\mathrm{W}$ (deviation of 6%). Thus, the calculated and measured efficiencies are both 99.4%.

Moreover, the measured (black line) and calculated (gray lines) input to output transfer function $(v_{\mathrm{A,out}}/v_{\mathrm{A0}})$ of the realized two-stage LC filter with series RL damping branch of the second stage, is depicted in Fig. 10, showing a good agreement

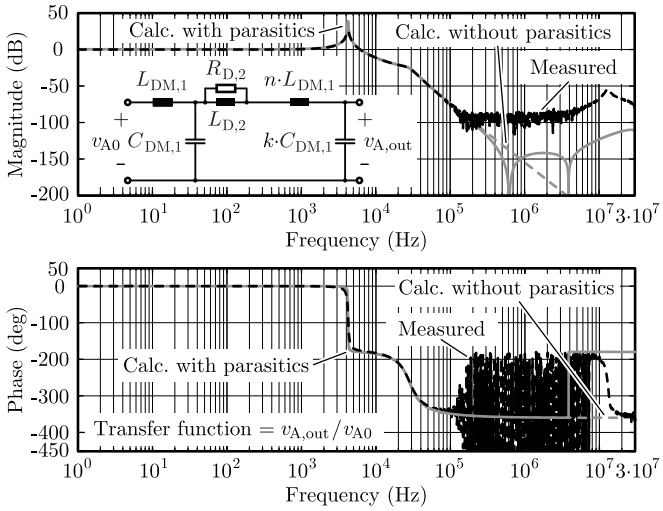

Fig. 10. Measured (black dashed line) and calculated (gray lines) input to output transfer function of the realized two-stage LC filter with a series RL damping branch of the second stage (cf., Table III). It is remarked that the first resonance peak at $4.2\,\mathrm{kHz}$ is actively attenuated by the current control loop [cf., Fig. 2(b)] and that the second resonance peak at $27\,\mathrm{kHz}$ is passively damped by the serial RL branch. For the dashed gray line ideal components are assumed, whereas for the solid gray line the parasitic capacitances and inductances of the inductors and capacitors (determined by separate measurements) are included. The measurement was conducted with a Bode 100 network analyzer (Omicron Lab, [68]) and shows a good agreement with the calculation until $100\,\mathrm{kHz}$, where the noise floor of the measurement device is reached (specified as $-100\,\mathrm{dB}$ in [68]).

until $100\,\mathrm{kHz}$, where the noise floor of the measurement device is reached for attenuations higher than $100\,\mathrm{dB}$.

It is noted that the maximum inductor temperatures T_{meas} were only roughly measured as summarized in Table V for the conditions as employed in the calculation given by (28), i.e., $I_{\mathrm{A,out}} = 17\,\mathrm{A}$ and $V_{\mathrm{A,out}} = 200\,\mathrm{V}$ for $V_{\mathrm{dc}} = V_{\mathrm{dc,max}} = 800\,\mathrm{V}$. The ambient temperature was $T_{\mathrm{a}} = 30\,^\circ\mathrm{C}$. The relative errors $(T_{\mathrm{meas}} - T_{\mathrm{a}})/(T_{\mathrm{calc}} - T_{\mathrm{a}})$ of the measurements compared to the calculated temperatures T_{calc} are -16%, 27%, and 14% for $L_{\mathrm{DM},1}$, $L_{\mathrm{DM},2}$, and $L_{\mathrm{D},2}$, respectively, and are in the expected tolerance range. The measured (over) temperatures for $L_{\mathrm{DM},2}$ and $L_{\mathrm{D},2}$ could be explained by the close proximity of $L_{\mathrm{DM},2}$ and $L_{\mathrm{D},2}$.

In the following, the measurement results for each requirement are discussed. It is anticipated that for the measurement of the output voltage slew rate *SR*, transient output voltage dip,

TABLE V
MAXIMUM MEASURED INDUCTOR TEMPERATURES (OCCURRING AT THE WINDING SURFACE) AT AN AMBIENT TEMPERATURE OF 30 °C AND FOR THE CONDITIONS GIVEN BY (28), I.E., $I_{\mathrm{A,out}} = 17\,\mathrm{A}$ AND $V_{\mathrm{A,out}} = 200\,\mathrm{V}$ FOR $V_{\mathrm{dc}} = V_{\mathrm{dc,max}} = 800\,\mathrm{V}$

Inductor	*Max. Measured Temperature* T_{meas}	*Max. Calculated Temperature* T_{calc}
$L_{\mathrm{DM},1}$	81.2 °C	90.8 °C
$L_{\mathrm{DM},2}$	105.9 °C	89.8 °C
$L_{\mathrm{D},2}$	94.5 °C	86.4 °C

The temperatures were measured with a Fluke Ti9 thermal imager (emissivity of 0.95) and for the calculation the same ambient temperature of 30 °C is used instead of 40 °C, which is assumed for the ρ–η PF optimization (cf., Section IV-A).

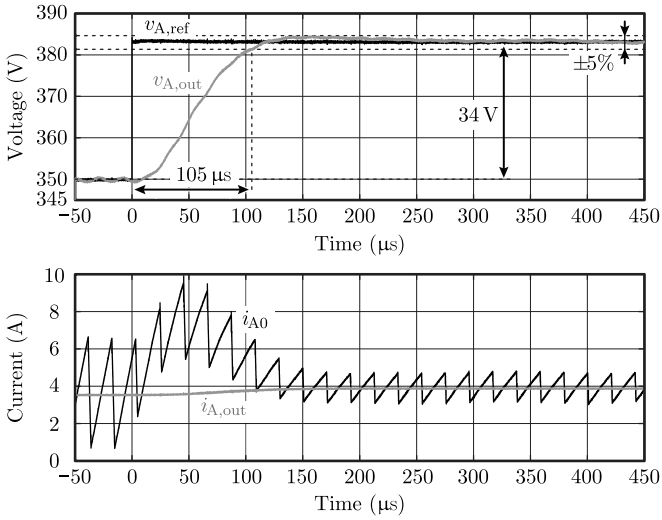

Fig. 11. Measured reference voltage $v_{\mathrm{A,ref}}$, output voltage $v_{\mathrm{A,out}}$, bridge-leg output current i_{A0}, and load current $i_{\mathrm{A,out}}$, resulting in a measured slew rate of $SR_{\mathrm{meas}} = 34\,\mathrm{V}/105\,\mu\mathrm{s} = 324\,\mathrm{V/ms}$, to verify the calculated *SR* of $322\,\mathrm{V/ms}$. The output voltage reference $v_{\mathrm{A,ref}}$ is determined from the voltage measured at a general purpose I/O pin of the employed DSP.

and bridge-leg output current Δi_{A0}, the load current source of Fig. 2(b) is replaced by a resistor of 97 Ω.[10]

A. Output Voltage Slew Rate Measurement

The measured output voltage step response from $u_{\mathrm{A,ref}} = 350\,\mathrm{V}$ to $u_{\mathrm{A,ref}} = 384\,\mathrm{V}$ is depicted in Fig. 11. The employed control architecture is shown in Fig. 2(b) and described in detail in [43].[11]

The digital controller, implemented using a TMS320F2808 digital signal processor, generates the step of the output voltage reference and, at the same time, changes the logical state of one of its general purpose I/O pins. The time $\Delta t_{\mathrm{meas}} = 105\,\mu\mathrm{s}$ is measured from this instant until the output voltage enters the $\pm 5\%$ tolerance band and stays in the band [cf., Fig. 3(a)] as

[10]With a load resistor of 97 Ω, the output power is half of the nominal value of one of the three phases, i.e., $P_{\mathrm{A,out}} = 50\% \cdot P_{\mathrm{out,n}}/3 = (400\,\mathrm{V})^2/97\,\Omega = 1.65\,\mathrm{kW}$.

[11]Voltage controller $G_{\mathrm{v}} = k_{\mathrm{pv}} \cdot \frac{1+s\cdot T_{\mathrm{iv}}}{s\cdot T_{\mathrm{iv}}}$ with $k_{\mathrm{pv}} = 51\,\mathrm{mA/V}$, $T_{\mathrm{iv}} = 177\,\mu\mathrm{s}$; current controller $G_{\mathrm{i}} = k_{\mathrm{pi}}$ with $k_{\mathrm{pi}} = 6.4\,\mathrm{V/A}$.

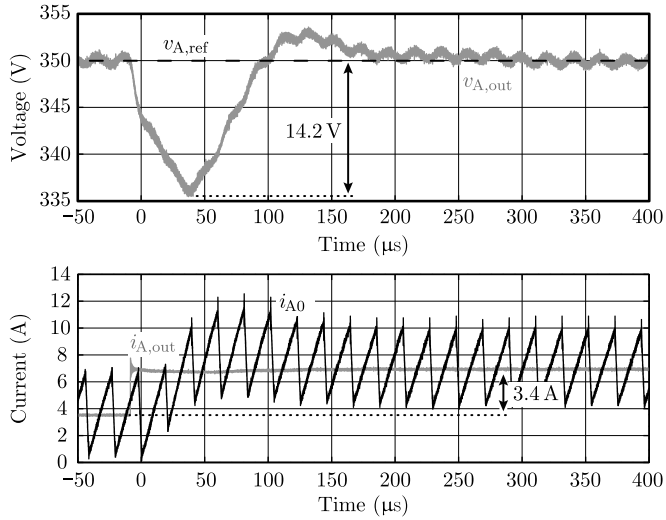

Fig. 12. Measured output voltage $v_{\mathrm{A,out}}$, bridge-leg output current i_{A0}, and load current $i_{\mathrm{A,out}}$, resulting in a measured transient output voltage dip $\Delta V_{\mathrm{A,out,meas}} = 14.2\,\mathrm{V}$, verifying the calculated value of $\Delta V_{\mathrm{A,out}}$ of 16 V.

depicted in Fig. 11. Accordingly, the measured slew rate is

$$SR_{\mathrm{meas}} = \frac{34\,\mathrm{V}}{105\,\mu\mathrm{s}} = 324\,\mathrm{V/ms} \tag{36}$$

which is very close to the calculated value of $322\,\mathrm{V/ms}$ due to the proper controller tuning.

B. Transient Voltage Dip Measurement

To generate a load step of $\Delta I_{\mathrm{A,out}} = 3.4\,\mathrm{A}$, a 100-Ω resistor chopper (cf., [69]) is connected in parallel to the 97-Ω load resistor. Fig. 12 shows the measured output voltage dip due to this change in the load current, which leads to

$$Z_{\mathrm{step,meas}} = \frac{14.2\,\mathrm{V}}{3.4\,\mathrm{A}} = 4.2\,\Omega. \tag{37}$$

This $Z_{\mathrm{step,meas}}$ is only 11% lower than the value, 4.7 Ω, obtained without control (cf., Table IV). The reason for this is the implemented controller design; a more aggressive voltage controller would reduce the transient output voltage dip, but would increase the overshoot of the output voltage step response and/or the settling time such that the specified limit could not be met anymore (cf., Section III-A).

C. Bridge-Leg Output Current Ripple Measurement

The ripple of the bridge-leg output current i_{A0} is measured for a DC-link voltage of $V_{\mathrm{dc}} = V_{\mathrm{dc,n}} = 700\,\mathrm{V}$ and a constant modulation index of $m = u_{\mathrm{A,out}}/\frac{V_{\mathrm{dc,n}}}{2} = 0.5$; cf., Section III-C. This modulation index is selected because the largest current ripple occurs for $m = 0.5$. The measurement result is given in Fig. 13 and leads to

$$\Delta I_{\mathrm{A0,meas}} = 12.2\,\mathrm{A} \tag{38}$$

which matches closely with the computed value of 12 A (the inductance of $L_{\mathrm{DM},1}$ has been measured as 154.2 µH, i.e., deviates

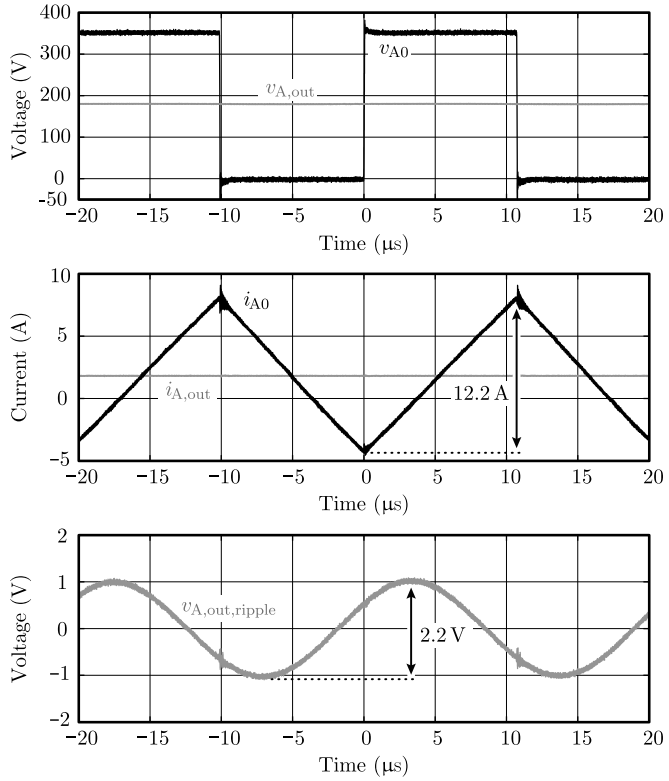

Fig. 13. Measured bridge-leg output voltage $v_{\mathrm{A}0}$, output voltage $v_{\mathrm{A,out}}$, bridge-leg output current $i_{\mathrm{A}0}$, and load current $i_{\mathrm{A,out}}$, resulting in a peak-to-peak bridge-leg output current ripple $\Delta I_{\mathrm{A}0,\mathrm{meas}} = 12.2\,\mathrm{A}$, to verify the calculated $\Delta I_{\mathrm{A}0}$ of 12.0 A. The output voltage ripple is measured with AC-coupling in the bottom graph and has a peak-to-peak value of 2.2 V. The reason for the slightly higher voltage of $v_{\mathrm{A}0}$ at the end of the switching transients is that in the interlocking time the body diode of the MOSFET is conducting instead of its channel. This leads to a higher voltage drop over the switch until the MOSFET turns on and the current commutes to the channel.

by only 0.1% from the value $154\,\mu\mathrm{H}$ assumed for the calculation, cf., Table III; the dc-link voltage is adjusted to $700\,\mathrm{V}$ with an error of 0.7%).

D. Output Voltage Ripple Measurement

The time behavior of the output voltage ripple is shown in Fig. 13 for $V_{\mathrm{dc}} = 700\,\mathrm{V}$. To measure the maximum output voltage ripple, the DC-link voltage is increased to $V_{\mathrm{dc}} = V_{\mathrm{dc,max}} = 800\,\mathrm{V}$ (cf., Section III-D). A peak-to-peak voltage ripple of

$$\Delta V_{\mathrm{A,out,meas}} = 2.6\,\mathrm{V} \tag{39}$$

is obtained ($m = 0.5$). The measured value is close to the calculated maximum voltage ripple of $2.5\,\mathrm{V}$ despite the tolerance of $\pm 20\%$ of the capacitance for the MKP capacitors for the two following reasons. First, a small capacitor rated at $0.68\,\mu\mathrm{F}$ was added to the capacitor rated at $4.7\,\mu\mathrm{F}$ to realize $C_{\mathrm{DM},1}$ (cf., Table III). Thus, the measured capacitance of $C_{\mathrm{DM},1}$ deviates by only 2% from the calculated value. And second, for $C_{\mathrm{DM},2}$ an capacitor with an overrated capacitance (rated at $4.7\,\mu\mathrm{F}$ for a desired value of $4.1\,\mu\mathrm{F}$) was selected to obtain an exact match between measured and calculated value (cf., Table III). Furthermore, as shown in the previous section for $L_{\mathrm{DM},1}$, the measured

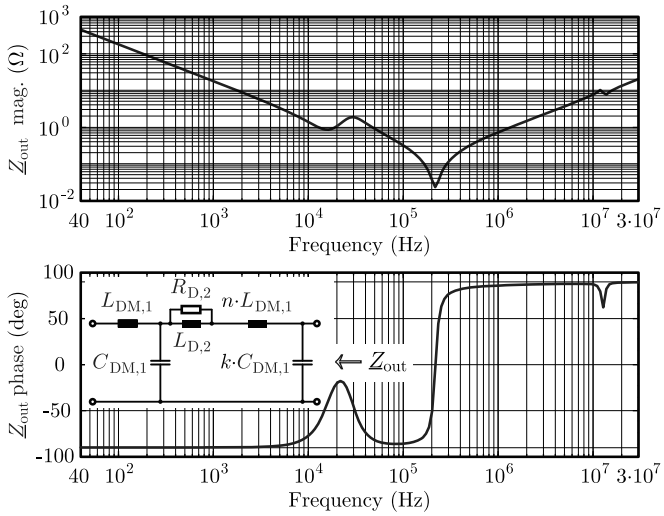

Fig. 14. Measured output impedance $\underline{Z}_{\mathrm{out}}$ of the designed two-stage LC filter (cf., Table III) with an open filter input as indicated in the figure.

filter inductances are also very close to the calculated values for $L_{\mathrm{DM},2}$ (1% deviation) and $L_{\mathrm{D},2}$ (3% deviation).

E. Maximum Capacitive Reactive Power Measurement

To assess the reactive power consumption of the filter at an output frequency of $f_{\mathrm{out}} = 50\,\mathrm{Hz}$, the output impedance $\underline{Z}_{\mathrm{out}}$ (open input) of the two-stage LC output filter is measured as shown in Fig. 14. At $50\,\mathrm{Hz}$, the output impedance is nearly perfectly capacitive, $\underline{Z}_{\mathrm{out}} = 363\,\Omega \cdot \mathrm{e}^{-\mathrm{j}\cdot 89.97^{\circ}}$, and accordingly the measured capacitive reactive power of the filter is computed to

$$Q_{\mathrm{cap,meas}} = \frac{V_{\mathrm{A,out,n}}^2}{|\underline{Z}_{\mathrm{out}}|} = \frac{(230\,\mathrm{V})^2}{363\,\Omega} = 146\ \mathrm{VA}. \tag{40}$$

This value fits with the calculated reactive power of 147 VA (cf., Table IV) due to the accurate realization of the filter capacitances as indicated in Section V-D.

F. Conducted EMI Measurement

The conducted noise emissions of the CPS are measured using the setup shown in Fig. 15. In this study, only DM emissions are considered (cf., Section III-F), and thus, a DM and CM noise separation is applied [70]. Still, two CM chokes [3× T60006-L2050-W516 (Vacuumschmelze GmbH), 5 turns] are used for this measurement, as depicted in Fig. 15, keeping the difference between DM and CM noise smaller than $40\,\mathrm{dB}$ to achieve meaningful measurement results with the noise separator which shows a limited CM rejection ratio [70].

The CM choke at the output of the two-stage LC filter (cf., Fig. 15) adds $1.8\,\mu\mathrm{H}$ of DM filtering inductance through its leakage inductance. At the frequency of $4 \times 48\,\mathrm{kHz} = 192\,\mathrm{kHz}$, where the first peak of the measured DM noise occurs, this results in an impedance magnitude of $2 \cdot \pi \cdot 192\,\mathrm{kHz} \cdot 1.8\,\mu\mathrm{H} = 2.2\,\Omega$. This additional impedance is negligible compared to the $50\,\Omega$ of the LISNs.

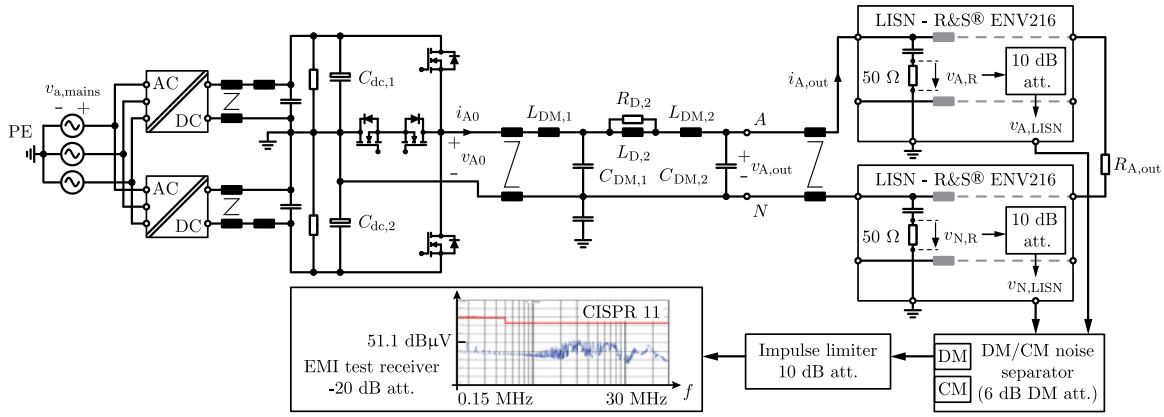

Fig. 15. Conducted EMI measurement setup to measure the DM noise emission of the CPS employing two LISNs at the filter output and a DM/CM noise separator. The attenuations of 10 dB of the LISNs (for increased accuracy) and of 10 dB of the impulse limiter (used to protect the test receiver) are compensated by the −20 dB of the EMI test receiver. The additional attenuation of 6 dB of the noise separator is counterbalanced by adding 6 dB to the measurement results a posteriori (cf., Fig. 16). Thus, in (41) the actually generated noise level is given.

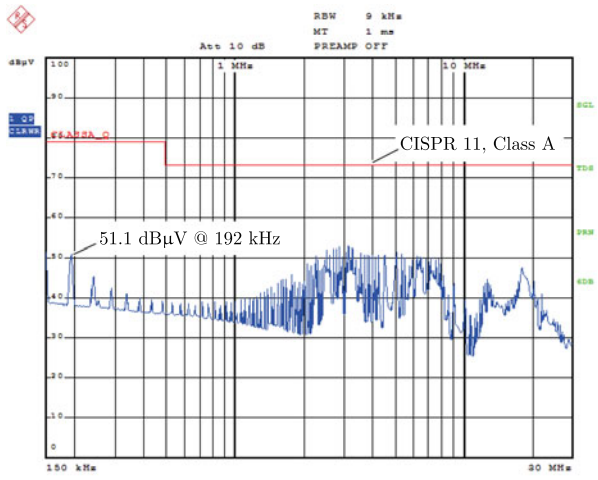

Fig. 16. Measured DM noise emission of the CPS employing the experimental setup as given in Fig. 15 with a DM/CM noise separator. This separator generates an additional attenuation of 6 dB and thus the actual DM noise emission at the frequency of the fourth switching harmonic (= 192 kHz) is 51.1 dBµV + 6 dB = 57.1 dBµV. The attenuations of 10 dB of the LISN circuits and of 10 dB of the impulse limiter are compensated by the −20 dB of the EMI test receiver; cf., Fig. 15.

As can be seen from Fig. 16, at 192 kHz (fourth switching frequency harmonic and/or first harmonic located in the EMI measurement range), the measured DM noise emission is

$$\text{Meas. DM noise}\,(@192\,\text{kHz}) = 57.1\,\text{dB}\mu\text{V}. \qquad (41)$$

The EMI measurement is conducted for a DC-link voltage of $V_{\text{dc}} = V_{\text{dc,max}} = 800\,\text{V}$, for an output voltage of $v_{\text{A,out}} = V_{\text{A,out,n}} = 230\,\text{V}$ (cf., Section III-F) and at a reduced output power of $3.3\,\text{kW}/6 = 550\,\text{W}$ because the emitted noise spectrum is independent of the load current (the inductors are built with ferrite and an air gap), i.e., show a largely linear behavior.

The measured noise emission of 57.1 dBµV deviates by 5.3 dB from the calculated value of 62.4 dBµV (cf., Table IV), because the computation is based on a worst case consideration, for which all amplitudes of the harmonics are summed up within the 9 kHz band of the test receiver; cf., [49].

VI. Conclusion

In this paper, the DS concept is utilized to provide a basis for the multiobjective optimization of the output filter of a 10-kW four-quadrant three-phase switch-mode CPS with $f_{\text{s}} = 48\,\text{kHz}$ and $[0, 350\,\text{V}]$ output phase voltage range. The DS concept permits to simultaneously consider multiple criteria that result from application-oriented specifications of the CPS such as

1) minimum output voltage slew rate;
2) maximum transient output voltage dip;
3) maximum bridge-leg output current ripple;
4) maximum output voltage ripple;
5) maximum capacitive reactive power;
6) limits of conducted EMI noise emissions.

These specifications lead to corresponding limits for the output filter component values. The intersection set of all limits, in which all requirements can be fulfilled defines the DS. The strength of the presented approach is that a clear graphical representation of the DS is obtained, e.g., the limits can be drawn in the L-C plane for a single-stage LC filter, which typically would be considered in a first step of the filter analysis. From the drawn limits, it can then directly be identified that, for the case at hand, the resulting DS of a single-stage filter is empty because the compliance to the limits of conducted EMI does not allow a common intersection of all limits. Thus, the number of degrees of freedom needs to be increased, which can be achieved by introducing a two-stage LC filter. This results in a nonempty 4D DS. To fully exploit this DS, a multiobjective optimization is performed and the ρ–η PF is determined, which allows us to identify the most compact and/or most efficient filter designs among all possible filter realizations with parameters in the DS. The PF calculation of the two-stage LC output filter involves nearly 1.1×10^{12} different filter designs. To drastically reduce this very high number, a design procedure benefiting from preoptimized component designs is discussed in detail. From the optimization results, the Pareto optimal filter design with the highest power density is selected, resulting in $\rho = 14.6\,\text{kW/dm}^3$ ($239\,\text{W/in}^3$) for $\eta = 99.4\%$. As verified by measurements on a filter hardware demonstrator, the optimal filter ensures compliance to all specifications of the CPS. It should

TABLE VI
BEST CASE, NOMINAL CASE, AND WORST CASE PERFORMANCE INDEXES CALCULATED FOR THE COMPONENT VALUES OF THE FINAL FILTER DESIGN, I.E., $L_{\mathrm{DM},1} = 154\,\mu\mathrm{H}$, $C_{\mathrm{DM},1} = 4.7\,\mu\mathrm{F}$, $L_{\mathrm{DM},2} = 11.7\,\mu\mathrm{H}$, $C_{\mathrm{DM},2} = 4.1\,\mu\mathrm{F}$, $L_{\mathrm{D},2} = 22.4\,\mu\mathrm{H}$, AND $R_{\mathrm{D},2} = 1.34\,\Omega$ (CF., TABLE III), AND FOR INDUCTANCE TOLERANCES OF $\pm 10\%$ AND CAPACITANCE TOLERANCES OF $\pm 20\%$

Requirement	*Best Case*	*Nominal Case*	*Worst Case*	*Worst Case Component Values*
Out. voltage slew rate *SR*	$360\,\mathrm{V/ms}$	$322\,\mathrm{V/ms}$	$275\,\mathrm{V/ms}$	$L_{\mathrm{DM},1} = 154\,\mu\mathrm{H} + 10\%$, $L_{\mathrm{DM},2} = 11.7\,\mu\mathrm{H} + 10\%$, $L_{\mathrm{D},2} = 22.4\,\mu\mathrm{H} + 10\%$, $C_{\mathrm{DM},1} = 4.7\,\mu\mathrm{F} + 20\%$, $C_{\mathrm{DM},2} = 4.1\,\mu\mathrm{F} + 20\%$, $R_{\mathrm{D},2} = 1.34\,\Omega$
Trans. out. voltage dip $\rightarrow Z_{\mathrm{step}}$	$4.1\,\Omega$	$4.7\,\Omega$	$5.4\,\Omega$	$L_{\mathrm{DM},1} = 154\,\mu\mathrm{H} + 10\%$, $L_{\mathrm{DM},2} = 11.7\,\mu\mathrm{H} + 10\%$, $L_{\mathrm{D},2} = 22.4\,\mu\mathrm{H} + 10\%$, $C_{\mathrm{DM},1} = 4.7\,\mu\mathrm{F} - 20\%$, $C_{\mathrm{DM},2} = 4.1\,\mu\mathrm{F} - 20\%$, $R_{\mathrm{D},2} = 1.34\,\Omega$
Bridge-leg current ripple $\Delta i_{\mathrm{A}0}$	$10.8\,\mathrm{A}$	$12.0\,\mathrm{A}$	$13.4\,\mathrm{A}$	$L_{\mathrm{DM},1} = 154\,\mu\mathrm{H} - 10\%$, $L_{\mathrm{DM},2} = 11.7\,\mu\mathrm{H} - 10\%$, $L_{\mathrm{D},2} = 22.4\,\mu\mathrm{H} - 10\%$, $C_{\mathrm{DM},1} = 4.7\,\mu\mathrm{F} - 20\%$, $C_{\mathrm{DM},2} = 4.1\,\mu\mathrm{F} - 20\%$, $R_{\mathrm{D},2} = 1.34\,\Omega$
Out. voltage ripple $\Delta v_{\mathrm{A,out}}$	$1.4\,\mathrm{V}$	$2.5\,\mathrm{V}$	$5.6\,\mathrm{V}$	$L_{\mathrm{DM},1} = 154\,\mu\mathrm{H} - 10\%$, $L_{\mathrm{DM},2} = 11.7\,\mu\mathrm{H} - 10\%$, $L_{\mathrm{D},2} = 22.4\,\mu\mathrm{H} + 10\%$, $C_{\mathrm{DM},1} = 4.7\,\mu\mathrm{F} - 20\%$, $C_{\mathrm{DM},2} = 4.1\,\mu\mathrm{F} - 20\%$, $R_{\mathrm{D},2} = 1.34\,\Omega$
Cap. reactive power Q_{cap}	$117\,\mathrm{VA}$	$147\,\mathrm{VA}$	$175\,\mathrm{VA}$	$C_{\mathrm{DM},1} = 4.7\,\mu\mathrm{F} + 20\%, C_{\mathrm{DM},2} = 4.1\,\mu\mathrm{F} + 20\%$
Conducted EMI limit	$60.4\,\mathrm{dB\mu V}$	$62.4\,\mathrm{dB\mu V}$	$71.1\,\mathrm{dB\mu V}$	$L_{\mathrm{DM},1} = 154\,\mu\mathrm{H} - 10\%$, $L_{\mathrm{DM},2} = 11.7\,\mu\mathrm{H} - 10\%$, $L_{\mathrm{D},2} = 22.4\,\mu\mathrm{H} + 10\%$, $C_{\mathrm{DM},1} = 4.7\,\mu\mathrm{F} - 20\%$, $C_{\mathrm{DM},2} = 4.1\,\mu\mathrm{F} - 20\%$, $R_{\mathrm{D},2} = 1.34\,\Omega$

The last column summarizes the worst case component values. The tolerance of $R_{\mathrm{D},2}$ is neglected.

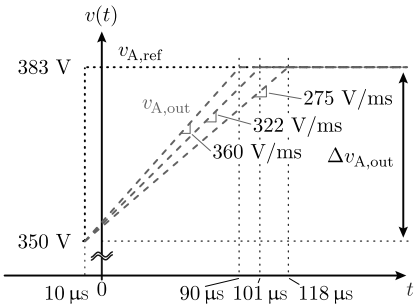

Fig. 17. Best case, nominal case, and worst case slew rates, i.e., 360 V/ms, 322 V/ms, and 275 V/ms, respectively, obtained for the component values of the final filter design considering tolerances of $\pm 10\%$ for the inductances and $\pm 20\%$ for the capacitances. The tolerance of the damping resistor $R_{\mathrm{D},2}$ is neglected. It is noted that for the hardware realization of the filter the components were selected carefully such that the calculated and measured values fit closely as shown in Table III. This minimizes the impact of component tolerances on the output filter performance leading to a good agreement between measured and calculated performance indexes (cf., Table IV).

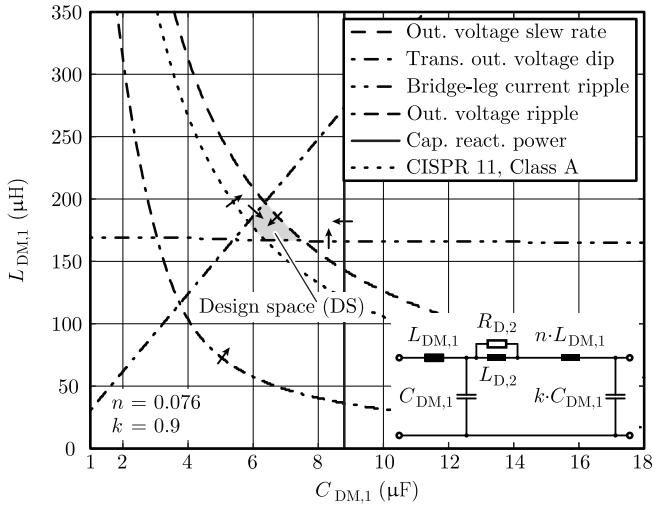

Fig. 18. DS for the two-stage LC output filter [cf., Fig. 2(b)] for nominal $n = L_{\mathrm{DM},2}/L_{\mathrm{DM},1} = 0.076$ and $k = C_{\mathrm{DM},2}/C_{\mathrm{DM},1} = 0.9$, which results from the optimization in Section IV-B (cf., Table III) for the worst case combinations of component values, according to Table VI, if tolerances of $\pm 10\%$ are considered for the inductances and $\pm 20\%$ for the capacitances ($R_{\mathrm{D},2}$ has no tolerance). The resulting DS is considerably smaller than the DS calculated for the exact component values; cf., Fig. 6.

finally be noted that the resulting filter design is also advantageous concerning output voltage control. Because the resonant frequency of the first filter stage is by a factor of roughly 7 lower than the one of the second filter stage, the second filter stage can be omitted in a first step, i.e., the controller design can be carried out assuming a single-stage LC filter. The closed control loop will, therefore, show a limited gain at frequencies higher than the corner frequency of the first filter stage. Accordingly, the second filter stage cannot be dynamically compensated, which requires to add the passive RL damping.

APPENDIX
DS INCLUDING COMPONENT TOLERANCES

The values of the passive components of the investigated two-stage LC output filter, in particular inductances and capacitances, are subject to tolerances. The impacts of these tolerances on the resulting DS are disregarded in Sections III and IV, to focus on the derivation of the DS and the subsequent ρ–η Pareto optimization.[12] This appendix describes a method, which considers the implications of tolerances of the component values on the resulting DS.

To guarantee that all the required properties of the considered AC source specified in Table II can be fulfilled for real components with tolerances, the calculation of the DS needs to include the variation of the component values, because higher or lower than nominal (or desired) component values affect the filter performance indexes listed in Table IV, as exemplary shown in Fig. 17 for the slew rate. The inductors and capacitors are assumed to have tolerances of $\pm 10\%$ and $\pm 20\%$, respectively,[13] while the tolerance of the damping resistor $R_{\mathrm{D},2}$ is neglected. Thus, the two-stage output filter contains five components with

[12]The hardware realization of the two-stage LC output filter (cf., Table III) uses carefully selected components, such that calculated and measured values agree. For this, the air gaps of the inductors were tuned to achieve the calculated inductances and the capacitors with the best fitting capacitances were selected from a set of available capacitors.

[13]The inductor is realized with an air gap (cf., Table III) and hence its inductance is roughly proportional to the length of the air gap. It is assumed that the air gap length is $1\,\mathrm{mm}$ which can be adjusted within $\pm 0.1\,\mathrm{mm}$, i.e., within $\pm 10\%$, and hence the tolerance of the inductance is $\pm 10\%$. The tolerance of the capacitance is according to [64] $\pm 20\%$.

uncertain component values. With these component tolerances, the best and worst case performance indexes, e.g., the highest and the lowest slew rates, respectively, can be determined based on given filter component values. This is exemplarily illustrated in Fig. 17 for the nominal filter values identified in the course of this study, i.e., $L_{\mathrm{DM},1} = 154\,\mu\mathrm{H}$, $C_{\mathrm{DM},1} = 4.7\,\mu\mathrm{F}$, $L_{\mathrm{DM},2} = 11.7\,\mu\mathrm{H}$, $C_{\mathrm{DM},2} = 4.1\,\mu\mathrm{F}$, $L_{\mathrm{D},2} = 22.4\,\mu\mathrm{H}$, and $R_{\mathrm{D},2} = 1.34\,\Omega$ (cf., Section IV-B and Table III). In this example, the worst case is obtained for the values of $L_{\mathrm{DM},1}$, $L_{\mathrm{DM},2}$, $L_{\mathrm{D},2}$, $C_{\mathrm{DM},1}$, and $C_{\mathrm{DM},2}$ being 10% and 20% higher, respectively.

Table VI summarizes the best and worst case performance indexes calculated for the above mentioned component tolerances and all criteria considered in Section III. The last column of Table VI lists the particular combinations of component tolerances, which lead to the respective worst case performance indexes. According to the results listed in this column, different combinations of component tolerances result for the different criteria.

Fig. 18 depicts the DS that results if each criteria is evaluated based on the respective combinations of component tolerances listed in Table VI, to ensure that all the required properties of the AC source can be met in any case. Compared to the DS calculated with the nominal (exact) component values shown in Fig. 6, the DS with component tolerances as given in Fig. 18 is considerably smaller.

REFERENCES

[1] M. Oettmeier, R. Bartelt, C. Heising, V. Staudt, A. Steimel, S. B, Tietmeier. Bock, and C. Doerlemann, "Power-electronic-based machine emulator for high-power high-frequency drive converter test," in *Proc. IEEE Veh. Power Propulsion Conf.*, 2010, pp. 1–6.

[2] M. Oettmeier, R. Bartelt, C. Heising, V. Staudt, A. Steimel, S. Tietmeyer, B. Bock, and C. Doerlemann, "Machine emulator: Power-electronics based test equipment for testing high-power drive converters," in *Proc. 12th Int. Opt. Elect. Electron. Equipment Conf.*, 2010, pp. 582–588.

[3] Y. Srinivasa Rao and M. C. Chandorkar, "Real-time electrical load emulator using optimal feedback control technique," *IEEE Trans. Ind. Electron.*, vol. 57, no. 4, pp. 1217–1225, Apr. 2010.

[4] G. Lauss, F. Lehfuss, A. Viehweider, and T. Strasser, "Power hardware in the loop simulation with feedback current filtering for electric systems," in *Proc. 37th Conf. IEEE Ind. Electron. Soc.*, 2011, pp. 3725–3730.

[5] N. Kim, S.-Y. Kim, H.-G. Lee, C. Hwang, G.-H. Kim, H.-R. Seo, M. Park, and I.-K. Yu, "Design of a grid-simulator for a transient analysis of grid-connected renewable energy system," in *Proc. Int. Electr. Mach. Syst. Conf.*, 2010, pp. 633–637.

[6] R. Lohde and F. W. Fuchs, "Laboratory type PWM grid emulator for generating disturbed voltages for testing grid connected devices," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–9.

[7] S. Turner, D. J. Atkinson, A. G. Jack, and M. Armstrong, "Development of a high bandwidth multi-phase multilevel power supply for electricity supply network emulation," in *Proc. Eur. Conf. Power Electron. Appl.*, 2005, pp. P.1–P.7.

[8] P. J. Tritschler, E. Rullière, and S. Bacha, "Emulation of fuel cell systems," in *Proc. 19th Int. Electr. Mach. Conf.*, 2010, pp. 1–5.

[9] R. Zhang, M. Cardinal, P. Szczesny, and M. Dame, "A grid simulator with control of single-phase power converters in d-q rotating frame," in *Proc. 33rd IEEE Power Electron. Spec. Conf.*, 2002, vol. 3, pp. 1431–1436.

[10] W. Ren, M. Steurer, and L. Qi, "Evaluating dynamic performance of modern electric drives via power-hardware-in-the-loop simulation," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2008, pp. 2201–2206.

[11] C. Heising, R. Bartelt, M. Oettmeier, V. Staudt, and A. Steimel, "Analysis of single-phase 50-kW 16.7-Hz PI-controlled four-quadrant line-side converter under different grid characteristics," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 523–531, Feb. 2010.

[12] (2014, Apr. 29). Spitzenberger & Spies GmbH & Co. [Online]. Available: http://www.spitzenberger.de/Produkte.aspx

[13] (2014, Apr. 29). Ametek Programmable Power. [Online]. Available: http://www.calinst.com/products/index.htm

[14] D. O. Boillat and J. W. Kolar, "Integrated isolation and voltage balancing link of 3-phase 3-level PWM rectifier and inverter systems," in *Proc. Int. Power Electron. Conf. (ECCE Asia)*, 2014, pp. 1073–1080.

[15] *IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems*, IEEE Standard 1547-2003 (R2008), 2003 (Reaffirmed 2008).

[16] *Industrial, Scientific and Medical Equipment—Radio-frequency disturbance characteristics—Limits and Methods of Measurement*, IEC Standard CISPR 11, Edition 5.0, May 2009.

[17] D. O. Boillat, J. W. Kolar, and J. Mühlethaler, "Volume minimization of the main DM/CM EMI filter stage of a bidirectional three-phase three-level PWM rectifier system," in *Proc. IEEE Energy Convers. Cong. Expo. (ECCE USA)*, 2013, pp. 2008–2019.

[18] T. Friedli, M. Hartmann, and J. W. Kolar, "The essence of three-phase PFC rectifier systems—Part II," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 543–560, Feb. 2014.

[19] Y. Levron, H. Kim, and R. Erickson, "Design of EMI filters having low harmonic distortion in high-power-factor converters," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3403–3413, Jul. 2014.

[20] S. B. Dewan and P. D. Ziogas, "Optimum filter design for a single-phase solid-state UPS system," *IEEE Trans. Ind. Appl.*, vol. IA-15, no. 6, pp. 664–669, Nov. 1979.

[21] L. Michels, R. F. De Camargo, F. Botteron, H. A. Grudling, and H. Pinheiro, "Generalised design methodology of second-order filters for voltage-source inverters with space-vector modulation," *IEE Proc. Electr. Power Appl.*, vol. 153, no. 2, pp. 219–226, 2006.

[22] J. Muehlethaler, M. Schweizer, R. Blattmann, J. W. Kolar, and A. Ecklebe, "Optimal design of LCL harmonic filters for three-phase PFC rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3114–3125, Jul. 2013.

[23] Z. Zou, Z. Wang, and M. Cheng, "Modeling, analysis, and design of multifunction grid-interfaced inverters with output LCL filter," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3830–3839, Jul. 2014.

[24] T.-F. Wu, L.-C. Lin, N. Yao, Y.-K. Chen, and Y.-C. Chang, "Extended application of D-Σ digital control to single-phase bi-directional inverter with LCL filter," *IEEE Trans. Power Electron.*, vol. pp, no. 99, 2014, to be published.

[25] A. Bjeletić, L. Corradini, D. Maksimovic, and R. Zane, "Specifications-driven design space boundaries for point-of-load converters," in *Proc. 26th IEEE Appl. Power Electron. Conf.*, 2011, pp. 1166–1173.

[26] C. Ó Mathúna, J. A. Cobos, B. Allard, and N. Wang, "Power supply on chip," in *Proc. 29th IEEE Appl. Power Electron. Conf.*, 2014, Tutorial, p. 250.

[27] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner, "Performance trends and limitations of power electronic systems," in *Proc. 6th Int. Conf. Integr. Power Electron. Syst.*, 2010, pp. 1–20.

[28] P. Lefranc, X. Jannot, and P. Dessante, "Virtual prototyping and pre-sizing methodology for buck DC-DC converters using genetic algorithms," *IET Power Electron.*, vol. 5, no. 1, pp. 41–52, 2012.

[29] A. Husain and K.-Y. Kim, "Design optimization of manifold microchannel heat sink through evolutionary algorithm coupled with surrogate model," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 3, no. 4, pp. 617–624, Apr. 2013.

[30] P. K. Rout, D. P. Acharya, and G. Panda, "A multiobjective optimization based fast and robust design methodology for low power and low phase noise current starved VCO," *IEEE Trans. Semicond. Manuf.*, vol. 27, no. 1, pp. 43–50, Feb. 2014.

[31] H. Mukaidani and H. Xu, "Pareto optimal strategy for stochastic weakly coupled large scale systems with state dependent system noise," *IEEE Trans. Autom. Control*, vol. 54, no. 9, pp. 2244–2250, Sep. 2009.

[32] S. X. Chen and H. B. Gooi, "Jump and shift method for multi-objective optimization," *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4538–4548, Oct. 2011.

[33] Q. Li, M. Liu, and H. Liu, "Piecewise normalized normal constraint method applied to minimization of voltage deviation and active power loss in an AC-DC hybrid power system," *IEEE Trans. Power Systems*, vol. PP, no. 99, pp. 1-9, Aug. 2014.

[34] C. Marxgut, J. Muhlethaler, F. Krismer, and J. W. Kolar, "Multiobjective optimization of ultraflat magnetic components with PCB-integrated core," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3591–3602, Jul. 2013.

[35] T. M. Andersen, C. M. Zingerli, F. Krismer, J. W. Kolar, N. Wang, and C. O. Mathuna, "Modeling and pareto optimization of microfabricated inductors for power supply on chip," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4422–4430, Sep. 2013.

[36] X.-B. Hu, M. Wang, and E. Di Paolo, "Calculating complete and exact Pareto front for multiobjective optimization: a new deterministic approach for discrete problems," *IEEE Trans. Cybern.*, vol. 43, no. 3, pp. 1088–1101, Jun. 2013.
[37] A. De Nardo, N. Femia, G. Petrone, and G. Spagnuolo, "Optimal buck converter output filter design for point-of-load applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 4, pp. 1330–1341, Apr. 2010.
[38] J. Ackermann, "Parameter space design of robust control systems," *IEEE Trans. Autom. Control*, vol. AC-25, no. 6, pp. 1058–1072, Dec. 1980.
[39] V. Besson and A. T. Shenton, "An interactive parameter space method for robust performance in mixed sensitivity problems," *IEEE Trans. Autom. Control*, vol. 44, no. 6, pp. 1272–1276, Jun. 1999.
[40] M. D. Lutovac, D. V. Tošić, and B. L. Evans, "Design space approach to advanced filter design," in *Proc. 3rd Int. Conf. Telecomm. Modern Satellite, Cable Broadcast. Serv.*, 1997, pp. 179–190.
[41] C. Fernandez, A. Lazaro, P. Zumel, V. Valdivia, C. Martinez, and A. Barrado, "Design space boundaries of linear compensators applying the k-factor method," in *Proc. 28th IEEE Appl. Power Electron. Conf.*, Mar. 2013, pp. 2706–2711.
[42] R. Dorrance, F. Ren, Y. Toriyama, A. A. Hafez, C.-K. K. Yang, and D. Markovic, "Scalability and design-space analysis of a 1T-1MTJ memory cell for STT-RAMs," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 878–887, Apr. 2012.
[43] P. Cortés, D. O. Boillat, H. Ertl, and J. W. Kolar, "Comparative evaluation of multi-loop control schemes for a high-bandwidth AC power source with a two-stage LC output filter," in *Proc. Int. Conf. Renewable Energy Res. Appl.*, 2012, pp. 1–10.
[44] T. Nussbaumer, M. L. Heldwein, G. Gong, S. D. Round, and J. W. Kolar, "Comparison of prediction techniques to compensate time delays caused by digital control of a three-phase buck-type PWM rectifier system," *IEEE Trans. Industrial Electron.*, vol. 55, no. 2, pp. 791–799, Feb. 2008.
[45] D. O. Boillat, T. Friedli, J. Mühlethaler, J. W. Kolar, and W. Hribernik, "Analysis of the design space of single-stage and two-stage LC output filters of switch-mode AC power sources," in *Proc. IEEE Power Energy Conf. Illinois*, 2012, pp. 1–8.
[46] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, Feb. 2013.
[47] H. Zumbahlen, Ed., *Basic Linear Design*. Norwood, MA, USA: Analog Devices, Inc., 2007, p. 1275.
[48] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, *Feedback Control of Dynamic Systems*, 5th ed. Englewood Cliffs, NJ, USA: Prentice-Hall, 2006, p. 910.
[49] M. L. Heldwein, T. Nussbaumer, and J. W. Kolar, "Differential mode EMC input filter design for three-phase AC-DC-AC sparse matrix PWM converters," in *Proc. 35th IEEE Power Electron. Spec. Conf.*, 2004, vol. 1, pp. 284–291.
[50] M. Hartmann, H. Ertl, and J. W. Kolar, "EMI filter design for a 1 MHz, 10 kW three-phase/level PWM rectifier," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1192–1204, Apr. 2011.
[51] T. Nussbaumer, K. Raggl, and J. W. Kolar, "Design guidelines for interleaved single-phase boost PFC circuits," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2559–2573, Jul. 2009.
[52] K. Raggl, T. Nussbaumer, G. Doerig, J. Biela, and J. W. Kolar, "Comprehensive design and optimization of a high-power-density single-phase boost PFC," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2574–2587, Jul. 2009.
[53] D. O. Boillat and J. W. Kolar, "Modeling and experimental analysis of a coupling inductor employed in a high performance AC power source," in *Proc. 1st Int. Conf. Renewable Energy Res. Appl.*, 2012, pp. 1–18.
[54] R. W. Erickson, "Optimal single resistor damping of input filters," in *Proc. 14th Appl. Power Electron. Conf.*, 1999, vol. 2, pp. 1073–1079.
[55] U. Tietze and C. Schenk, *Halbleiter-Schaltungstechnik*, 12th ed. Berlin, Germany: Springer-Verlag, 2002.
[56] A. Van den Bossche and V. C. Valchev, *Inductors and Transformers for Power Electronics*. Boca Raton, FL, USA: CRC Press, 2005.
[57] J. Muehlethaler, "Modeling and multi-objective optimization of inductive power components," Ph.D. dissertation, ETH Zurich, Zurich, Switzerland, 2012.
[58] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *Proc. IEEE Workshop Comput. Power Electron.*, 2002, pp. 36–41.
[59] EPCOS AG, "Ferrite and accessories—SIFERRIT material N27," Tech. Rep., Sep. 2006.
[60] EPCOS AG, "Ferrite and accessories—SIFERRIT material N87," Tech. Rep., Sep. 2006.
[61] TDK EPCOS. (2014). E/ELP cores and accessories. [Online]. Available: http://www.epcos.com/epcos-en/529420/products/product-catalog/ferrites- and-accessories/e-elp-cores-and-accessories
[62] *IEC Standard Voltages*, IEC Standard IEC 60038, Ed. 7.0, 2009.
[63] S. A. Mulder, "On the design of low profile high frequency transformers," in *Proc. 5th Int. High Freq. Power Conv. Conf.*, 1990, pp. 141–159.
[64] EPCOS AG, "Film capacitors—EMI suppression capacitors (MKP)," Series/Type: B32921C/D ... B32928C/D, Jan. 2014.
[65] *Preferred Number Series for Resistors and Capacitors*, IEC Standard IEC 60063, Ed. 2.0, 1963.
[66] Fluke Corporation, "Fluke 187/189 true-rms digital multimeter—Extended specifications," Tech. Rep. Rev. A-8/00, 2000.
[67] Yokogawa Electric Corporation, "WT3000 precision power analyzer," Tech. Rep. Bull. 7603-00E, 2004.
[68] Omicron Lab, "Bode 100 vector network analyzer technical data," Tech. Rep., 2006.
[69] P. Cortés, D. O. Boillat, T. Friedli, M. Schweizer, J. W. Kolar, J. Rodriguez, and W. Hribernik, "Comparative evaluation of control schemes for a high bandwidth three-phase AC source," in *Proc. 7th Int. Power Electron. Motion Control Conf.*, 2012, vol. 1, pp. 321–329.
[70] S. Wang, F. C. Lee, and W. G. Odendaal, "Characterization, evaluation, and design of noise separator for conducted EMI noise diagnosis," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 974–982, Jul. 2005.

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