DCM Analysis of Single-Switch-Based ZVZCS Converters With a Tapped Inductor

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***Abstract*—The analysis of a novel single-active-switch-based zero voltage and zero current switching (ZVZCS) tapped boost converter in the discontinuous conduction mode (DCM) is proposed in this paper. The ZVZCS converter includes a lossless snubber composed of three diodes and two capacitors and exhibits novel ZVZCS operation for wide operating ranges of duty cycles, load currents, and input voltages. The voltage stress of the active switch is always less than the load voltage, and soft switching turn-on and turn-off are achieved without cumbersome current or voltage sensing, which could not have been obtained from quasi-resonant converters that also have an active switch. Detailed analyses of the DCM and the component stresses of the proposed converter are presented. Experiments for a 450-W prototype exhibited 99.0% of the maximum efficiency with a SiC JFET at the switching frequency of 50 kHz, and the ZVZCS operation is guaranteed, even for the DCM under the experimental conditions. Moreover, the proposed ZVZCS principle has been applied to a tapped buck–boost converter case, which was also experimentally verified.**

***Index Terms*—Boost converter, buck–boost converter, SiC JFET, single switch, tapped inductor, zero voltage and zero current switching (ZVZCS).**

I. Introduction

HIGHER switching frequency for reducing the size and weight of converters and filters is one of the most important issues in power electronics. In particular, demands for high-frequency applications in electric vehicles, renewable energy systems, and light-emitting diode drivers are recently increasing [1]–[10]. Another vital issue for reducing the energy loss and generated heat of converters is higher power efficiency [11]–[15]. To meet these demands, numerous soft switching techniques achieving zero voltage switching (ZVS) and/or zero current switching (ZCS) of converters have been presented over the last several decades [1]–[53]. Despite of the advantages of soft switching, the ZVS and/or ZCS techniques have demerits such as additional active devices [15]–[19], [49]–[53], excessive component stresses [22]–[24], [39]–[41], [54], [55], cumbersome voltage and/or current sensing [25]–[29], limited operating range and nonlinearity of converters [5]–[8], [30]–[34], [42]–[46], [56], and high frequency ringing after ZCS turn-off [35]–[37]. Conventional converters, on the other hand, do not have such problems except for the biggest demerit of hard switching characteristics. Therefore, a soft switching converter of an active switch with no larger stresses, having the same operating characteristics as the conventional hard switching converters, is required as a remedy to the demerits of existing techniques.

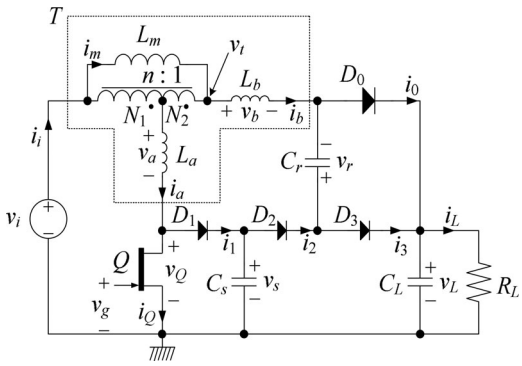

Fig. 1. Circuit diagram of the proposed single-switch-based ZVZCS tapped boost converter.

As a candidate of such a soft switching technique, a single-switch-based zero voltage and/or zero current switching (ZVZCS) for a tapped boost converter example was proposed [57], as shown in Fig. 1. For the ZVZCS operation of the converter, a lossless snubber circuit composed of three small-size diodes and two capacitors is added to an ordinary tapped boost converter. When the active switch is turned ON, it is in the ZCS with the help of the leakage inductance of a tapped inductor. When turned OFF, the energy of the leakage inductance is transferred to a snubber capacitor through a diode, which results in the ZVS of the active switch. The energy of the snubber capacitor is then retrieved through a diode and a capacitor connected to the end of the tapped inductor when the active switch is turned ON again. The single-switch-based ZVZCS tapped boost converter has the advantages of a wide ZVZCS range, low voltage stress, load-independent switching, low current stress of the snubber, robust dc gain, and negligible diode reverse recovery phenomena.

In this paper, the operation principles and design considerations, such as component voltage and current stresses, for the discontinuous conduction mode (DCM), which was not covered

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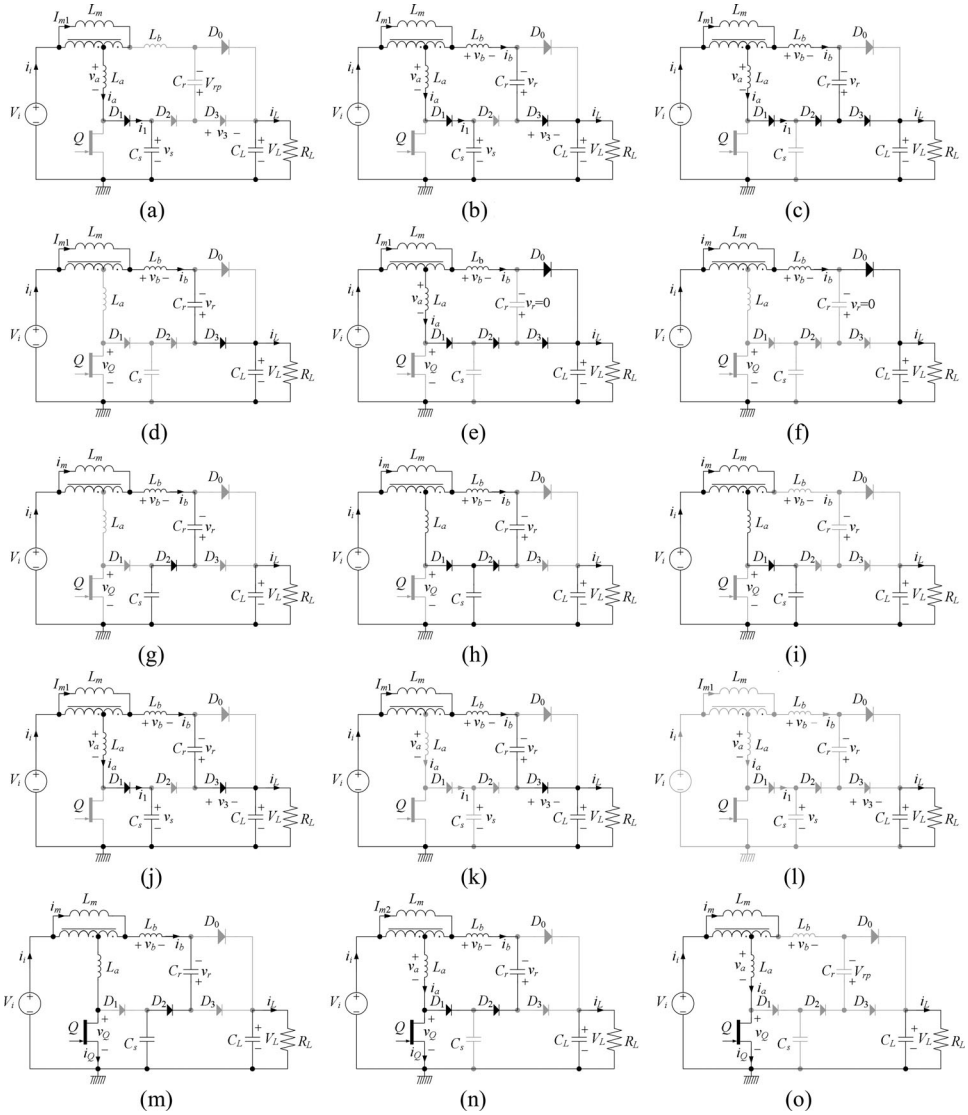

Fig. 2. Operating modes of the proposed converter including DCM (a) Mode 1 (b) Mode 2 (c) Mode 3 (d) Mode 4A (e) Mode 4B (f) Mode 5 (g) Mode 6 (h) Mode 7 (i) Mode 8 (j) Mode 9 (k) Mode 10 (l) Mode 11 (m) Mode 12 (n) Mode 13 (o) Mode 14.

in [57], is described in detail, and experimentally verified by a SiC JFET based 450-W prototype at 50-kHz switching frequency. Moreover, the extension of the proposed ZVZCS scheme to general nonisolated type converters is achieved for a tapped buck–boost converter case, and the ZVZCS operation is also experimentally verified with the same 450-W prototype at 50-kHz switching frequency.

II. Circuit Analysis for DCM Operation

The DCM operating modes of the proposed converter for a switching period T_s can be classified into 14 modes, as shown in Fig. 2, where the switching waveforms are shown in Fig. 3. The turning-off transition of the active switch is for Modes 1–4, the off-mode is Mode 5, whereas the turning-on transition is for Modes 12–13, and the on-mode is Mode 14, as shown in Fig. 4. Between the off-mode and the turning-on transition, there is the DCM transient, which consists of several repetitive *LC* resonances after the magnetizing current i_m goes to zero, for Modes 6–11. The averaged static characteristic of the proposed converter in the DCM is determined simply by an averaged duty cycle D like a conventional tapped-inductor boost converter as (1), where $D_{\rm off}$ is the time ratio that the output diode D_0 conducts

$$G_v \equiv \frac{V_L}{V_i} \cong \frac{D(1+1/n)+D_{\rm off}}{D_{\rm off}} = \frac{1+\sqrt{1+4D^2K}}{2} \quad (1a)$$

$$D_{\rm off} = \frac{n+1}{n}\frac{D}{G_v-1} \text{ where } K = \frac{T_s R_L}{2L_m}\left(\frac{n+1}{n}\right)^2. \quad (1b)$$

Mode 1 [t_0, t_1]: At t_0, the switch Q is just turned OFF, as shown in Fig. 2(a). The leakage current i_a flows to the snubber capacitor C_s and the voltage v_s across C_s increases from zero, which results in the ZVS switching of Q. The voltage v_3 across D_3, when it is turned OFF, is derived as follows:

$$v_3 = V_i + \frac{n+1}{n}(v_s - V_i) + V_{\rm rp} - V_L \quad (2)$$

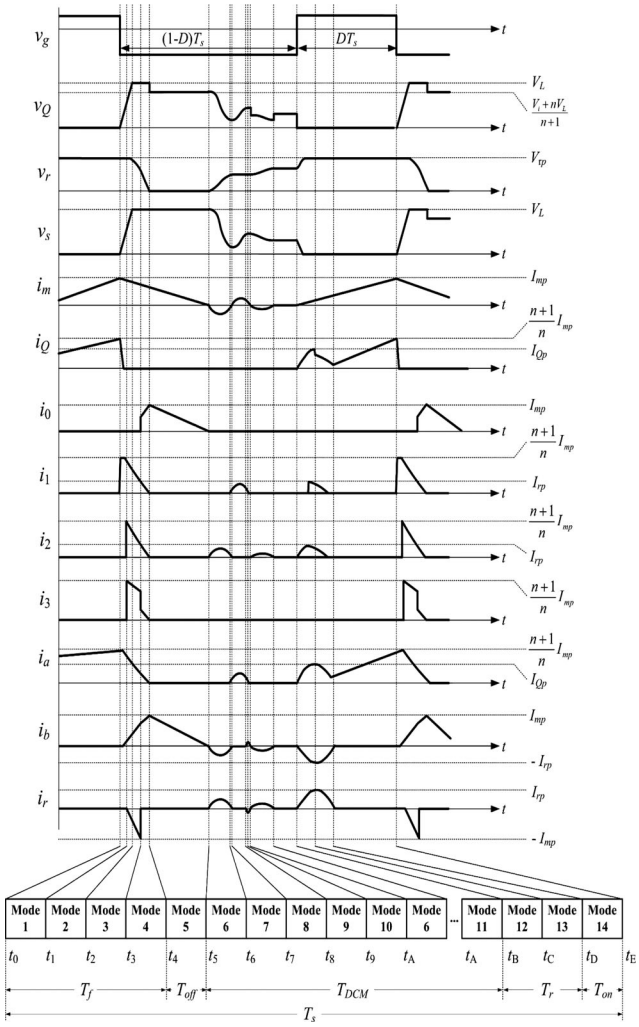

Fig. 3. Waveform diagrams of the proposed converter.

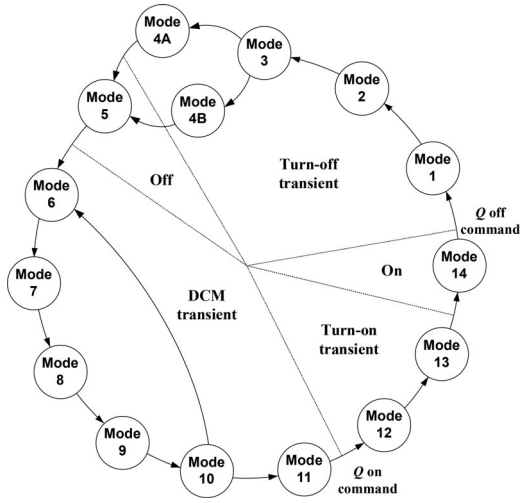

Fig. 4. State diagrams of the proposed converter.

where $V_{\rm rp}$ is the recovery capacitor voltage determined from (34), and the magnetizing current i_m is assumed to be constant for a short time period of this mode. The time interval t_{10}, where the voltage slope of v_s is linear, as shown in Fig. 3, is determined as follows:

$$t_{10} = \frac{nC_s v_s(t_1)}{(n+1)I_{\rm mp}} = \frac{nC_s}{(n+1)I_{\rm mp}} \left\{ \frac{n\left(V_L - V_{\rm rp}\right) + V_i}{n+1} \right\} \tag{3}$$

where $v_s(t_1)$ is the voltage to turn-on the clamp diode D_3 at t_1.

Mode 2 [t_1, t_2]: As the clamp diode D_3 is turned ON, the recovery capacitor voltage v_r starts to decrease while the snubber capacitor voltage v_s is increasing. Considering the fact that Mode 2 is very short compared to a resonant time period ω_1, which is governed during this mode as in (4), and that $i_m \cong I_{\rm mp}$, the sinusoidal changes can be neglected and C_s has been charged linearly since Mode 1, as shown in Fig. 3

$$\omega_1 = 1 \Bigg/ \sqrt{\left\{ \left(\frac{n+1}{n} \right)^2 L_a + L_b \right\} \left\{ \frac{n^2 C_s C_r}{n^2 C_s + (n+1)^2 C_r} \right\}}. \tag{4}$$

The time interval t_{21} to reach $v_s(i_2) = V_L$, therefore, can be straightforwardly determined as follows:

$$t_{21} \cong \frac{nC_s}{(n+1)I_{\rm mp}} \left\{ V_L - v_s(t_1) \right\}. \tag{5}$$

Mode 3 [t_2, t_3] : At t_2, the link diode D_2 is turned ON as a result of v_s increasing up to V_L, as shown in Fig. 2(c). Then, i_b increases, and i_a and v_r decrease. Eventually, either i_a becomes zero which corresponds to Mode 4A, or v_r becomes zero which corresponds to Mode 4B, depending on the load conditions. Assuming that the magnetizing current is still kept constant, the governing frequency of Mode 3 becomes

$$\omega_2 = 1 \Bigg/ \sqrt{\left\{ \left(\frac{n+1}{n} \right)^2 L_a + L_b \right\} C_r}. \tag{6}$$

The general solutions of v_r and i_b for Mode 3 can be written as follows:

$$v_r = \left(V_{\rm rp} + \frac{V_L - V_i}{n} \right) \cos \omega_2 (t - t_2) + \frac{V_i - V_L}{n} \tag{7a}$$

$$i_b = -C_r \frac{dv_r}{dt} = \omega_2 C_r \left(V_{\rm rp} + \frac{V_L - V_i}{n} \right) \sin \omega_2 (t - t_2). \tag{7b}$$

This mode ends at $t_{3\rm A}$ when i_b reaches $I_{\rm mp}$, at which Mode 4A will start, and the time interval $t_{32\rm A}$ becomes

$$t_{32\rm A} \equiv t_{3\rm A} - t_2 \cong \frac{1}{\omega_2} \sin^{-1} \left\{ \frac{I_{\rm mp}}{\omega_2 C_r V_{\rm rp} \left(1 + \frac{V_L - V_i}{n V_{\rm rp}} \right)} \right\}. \tag{8}$$

Mode 4A exists only for a light load condition when $I_{\rm mp}$ is small. For a heavier load condition, where v_r becomes zero before i_b reaches $I_{\rm mp}$, Mode 3 ends at $t_{3\rm B}$, at which Mode 4B will start, and the time interval $t_{32\rm B}$ becomes

$$t_{32\rm B} \equiv t_{3\rm B} - t_2 \cong \frac{1}{\omega_2} \cos^{-1} \left\{ \frac{1}{1 + \frac{n V_{\rm rp}}{V_L - V_i}} \right\}. \tag{9}$$

Mode 4A [t_{3A}, t_4]: At t_{3A}, the diodes D_1 and D_2 are just turned OFF and the magnetizing current i_m, which is still kept constant as I_{mp}, flows to C_r until v_r becomes zero, as shown in Fig. 2(d). Therefore, the time interval t_{43A} can be straightforwardly determined, considering linear charging as follows:

$$t_{43A} \equiv t_4 - t_{3A} = C_r \frac{v_r(t_{3A})}{I_{mp}} = \frac{C_r}{I_{mp}} \left\{ \left(V_{rp} + \frac{V_L - V_i}{n} \right) \cos \omega_2 t_{32A} - \frac{V_L - V_i}{n} \right\} \quad (10)$$

where t_{32A} is determined from (8).

Mode 4B [t_{3B}, t_4]: At t_{3B}, the recovery capacitor voltage v_r becomes zero and the output diode D_0 is just turned ON, as shown in Fig. 2(e). While the magnetizing current i_m is still kept as its maximum value of I_{mp}, i_a and i_b can be solved, as follows:

$$L_l \frac{di_b}{dt} = -L_l \frac{n}{n+1} \frac{di_a}{dt} = \frac{V_L - V_i}{n} \quad \because\ i_a = \frac{n+1}{n} (I_{mp} - i_b). \quad (11)$$

The time interval t_{43B}, at which i_a becomes zero, can be determined from (11), using (7b) and (9) as follows:

$$t_{43B} \equiv t_4 - t_{3B} = \left\{ \left(\frac{n+1}{n} \right)^2 L_a + L_b \right\} \cdot \frac{n^2}{n+1} \cdot \frac{i_a(t_{3B})}{V_L - V_i} = n \left\{ \left(\frac{n+1}{n} \right)^2 L_a + L_b \right\} \frac{I_{mp} - \omega_2 C_r \left(V_{rp} + \frac{V_L - V_i}{n} \right) \sin \omega_2 t_{32B}}{V_L - V_i}. \quad (12)$$

Mode 5 [t_4, t_5]: At t_4, all the turn-off transition is finished, and the output diode D_0 is maintained at turn-on, which delivers the magnetizing current i_m to the load side, as shown in Fig. 2(f). This period of Mode 5 is relatively very long, as in (13), compared to previous transition modes; therefore, i_m is no longer constant but linearly decreases to zero like a conventional DCM operated boost converter, which results in the soft switching of D_0, as in (14)

$$t_{54} = \frac{I_{mp} L_m}{V_L - V_i} \quad (13)$$

$$i_b = i_m \cong \frac{1}{L_m} \int_{t_4}^{t} (V_i - V_L)\, dt + I_{mp} = \frac{V_i - V_L}{L_m} (t - t_4) + I_{mp}. \quad (14)$$

Mode 6 [t_5, t_6]: At t_5, the output diode D_0 is turned OFF as a result of i_b decrease up to zero, and the link diode D_2 is turned ON, which results in a series resonant circuit composed of the magnetizing inductance L_m, leakage inductance L_b and capacitors C_s, C_r, as shown in Fig. 2(g). The governing frequency of Mode 6 becomes

$$\omega_3 = 1 \Big/ \sqrt{(L_m + L_b) \cdot \left(\frac{C_s C_r}{C_s + C_r} \right)}. \quad (15)$$

The snubber capacitor voltage v_s decreases from V_L and its current i_b increases from zero in sinusoidal waveform as follows:

$$v_s = \frac{C_r (V_L - V_i) \cos \omega_3 (t - t_5) + C_s V_L + C_r V_i}{C_s + C_r} \quad (16a)$$

$$i_b = i_m = -C_s \frac{dv_s}{dt} = \frac{\omega_3 C_s C_r (V_L - V_i)}{C_s + C_r} \sin \omega_3 (t - t_5). \quad (16b)$$

The recovery capacitor voltage v_r can be determined from (16a) as follows:

$$v_r = \frac{C_s}{C_r} (V_L - v_s) \because i_r = -i_c. \quad (17)$$

As the voltage v_s increases, the voltage potential of the tap of the tapped inductor v_t is also boosted up to v_s, as in (18), which eventually makes the snubber diode D_1 turned-on at t_6

$$v_t \equiv (v_s - v_r - V_i) \frac{L_m}{L_m + L_b} \cdot \frac{n}{n+1} + V_i \cong (v_s - v_r - V_i) \frac{n}{n+1} + V_i \because L_m >> L_b. \quad (18)$$

The time interval t_{65} is then determined from (16a), using (15) and (18), as follows:

$$t_{65} = \frac{1}{\omega_3} \cos^{-1} \left\{ \frac{2}{\alpha (n/\beta - 1)} \right\} \quad (19)$$

where $\alpha \equiv C_r / C_s$ and $\beta \equiv n V_L / V_i$.

Mode 7 [t_6, t_7]: At t_6, the snubber diode D_1 is turned ON while the link diode D_2 is turned ON, which results in two series resonant loops composed in this mode, as shown in Fig. 2(h). Considering the fact that Mode 7 is very short compared to Mode 6 and that the voltage and current changes are insignificant during this mode, the discharge of C_s is assumed to occur with the same frequency of Mode 6. The time interval t_{76}, at which i_b becomes zero, is then determined from (16b) and (19), as follows:

$$t_{76} \cong \frac{1}{\omega_3} \left[\pi - \cos^{-1} \left\{ \frac{2}{\alpha (n/\beta - 1)} \right\} \right] \to t_{75} \equiv t_{76} + t_{65} \cong \frac{\pi}{\omega_3}. \quad (20)$$

At t_7, Mode 8 starts when $V_i > v_s$, or Mode 11 starts when $V_i < v_s$, depending on load conditions and *LC* component values.

Mode 8 [t_7, t_8]: At t_7, the link diode D_2 is turned OFF as a result of i_b decreasing to zero, and the snubber diode D_1 is still turned ON, which results in a series resonant circuit composed of the magnetizing inductance L_m, leakage inductance L_a, and snubber capacitor C_s, as shown in Fig. 2(i). The governing frequency of Mode 6 then becomes

$$\omega_4 = 1 \Big/ \sqrt{\left\{ \left(\frac{n}{n+1} \right)^2 L_m + L_a \right\} C_s}. \quad (21)$$

The snubber capacitor voltage v_s increases from $v_s(t_7)$, and its current i_a is assumed to be increased from zero in sinusoidal

waveform as follows:

$$v_s = \frac{1-\alpha}{1+\alpha}(V_L - V_i)\cos\omega_4(t-t_7) + V_i \quad (22a)$$

$$i_a = \frac{1-\alpha}{1+\alpha}C_s\omega_4(V_L - V_i)\sin\omega_4(t-t_7) \quad (22b)$$

where the particular solution and initial conditions of the circuit are derived from (16) and (20).

The voltage v_3 across D_3, when it is turned OFF, is derived as follows:

$$\begin{aligned} v_3 &= V_i + \frac{n+1}{n}(v_t - V_i) + v_r(t_7) - V_L \\ &\cong V_i + \frac{n+1}{n}(v_s - V_i) + \frac{2(V_L - V_i)}{1+\alpha} - V_L \\ &\quad (L_m >> L_a). \end{aligned} \quad (23)$$

v_3 becomes zero at $t = t_8$; hence, the time interval t_{87} is then determined from (22a) and (23) as follows:

$$t_{87} = \frac{1}{\omega_4}\cos^{-1}\left\{\frac{n}{n+1}\cdot\frac{\alpha\beta - \beta - n\alpha + n}{(1-\alpha)(\beta - n)}\right\}. \quad (24)$$

Mode 9 [t_8, t_9]: At t_8, the clamp diode D_3 is turned ON as a result of v_3 reaching zero. The recovery capacitor voltage v_r starts to decrease while the snubber capacitor voltage v_s is increasing during Mode 9, as shown in Fig. 2(j). Considering the fact that Mode 9 is very short and insignificant against overall operation compared to Mode 8, the charge of C_s is assumed to have the same frequency as that of Mode 8, as in the Mode 7 analysis. The time interval t_{98}, at which i_a becomes zero, is then determined from (22b) and (24) as follows:

$$\begin{aligned} t_{98} &\cong \frac{1}{\omega_4}\left[\pi - \cos^{-1}\left\{\frac{n}{n+1}\cdot\frac{\alpha\beta - \beta - n\alpha + n}{(1-\alpha)(\beta - n)}\right\}\right] \rightarrow t_{97} \\ &\equiv t_{98} + t_{87} \cong \frac{\pi}{\omega_4}. \end{aligned} \quad (25)$$

Mode 10 [t_9, $t_{\rm A}$]: At t_9, the snubber diode D_1 is turned OFF as a result of i_a decreases to zero, as shown in Fig. 2(k). The recovery capacitor voltage v_r decreases until the recovery capacitor current $i_r (= i_b)$ becomes zero with a governing frequency of ω_5, as in (26). Due to the fact that the initial conditions of Mode 10 are omitted from the previous analysis, the time interval $t_{\rm A9}$ also can be neglected, considering its unimportance compared to the overall operation

$$\omega_5 = 1/\sqrt{(L_m + L_b)C_r}. \quad (26)$$

At $t_{\rm A}$, Mode 11 starts when $v_s < v_r + V_i$; otherwise, a cycle from Mode 6 to Mode 10 continues to repeat.

Mode 11 [$t_{\rm A}$, $t_{\rm B}$]: At $t_{\rm A}$, every diode and the switch Q are completely turned OFF unless there is an external turn-on command for Q, as shown in Fig. 2(l).

Mode 12 [$t_{\rm B}$, $t_{\rm C}$]: At $t_{\rm B}$, the switch Q is turned ON by an external turn-on command and the link diode D_2 is turned ON, which results in a series resonant circuit composed of the leakage inductances L_a, L_b and capacitors C_s, C_r, as shown in Fig. 2(m). The switch current i_Q, which is the sum of magnetizing current and resonant current, increases from zero, which results in a ZCS turn-on of Q. The governing frequency of Mode 12 becomes

$$\omega_6 = 1\Big/\sqrt{\left\{\left(\frac{n+1}{n}\right)^2 L_a + L_b\right\}\left(\frac{C_s C_r}{C_s + C_r}\right)}. \quad (27)$$

Assuming the cycle from Mode 6 to Mode 10 has occurred once before this mode, the snubber capacitor voltage v_s decreases from $v_s(t_{\rm B})$ and its current i_b increases from zero in sinusoidal waveform as follows:

$$v_s = a_1\cos\omega_6(t-t_{\rm B}) + a_2\sin\omega_6(t-t_{\rm B}) + a_3 \quad (28a)$$

$$\begin{aligned} i_b &= C_s\frac{dv_s}{dt} = \omega_6 C_s\{-a_1\sin\omega_6(t-t_{\rm B}) \\ &\quad + a_2\cos\omega_6(t-t_{\rm B})\} \end{aligned} \quad (28b)$$

where the coefficients $\{a_k\}$ can be determined as follows:

$$a_1 = \frac{\alpha\{4n+1+\alpha+\beta(\alpha-3)\}}{(1+\alpha)^2\beta}V_L \quad (29a)$$

$$a_2 = 0 \quad (29b)$$

$$a_3 = \frac{2n(1-\alpha) - \alpha(1+\alpha) + \beta(3\alpha-1)}{(1+\alpha)^2\beta}V_L. \quad (29c)$$

This mode ends at $t_{\rm C}$ when v_s reaches to zero, at which D_1 is turned ON and Mode 13 starts. The time interval $t_{\rm CB}$ is then determined as follows:

$$t_{CB} = \frac{1}{\omega_6}\cos^{-1}\left\{-\frac{a_3}{a_1}\right\}. \quad (30)$$

Mode 13 [$t_{\rm C}$, $t_{\rm D}$]: At $t_{\rm C}$, the snubber diode D_1 is turned ON and the snubber capacitor C_s is excluded from the resonant loop, as shown in Fig. 2(n). The recovery capacitor voltage v_r increases continuously and its current i_r begins to decrease, and they can be determined using the same governing frequency of (6) as follows:

$$v_r = b_1\cos\omega_2(t-t_C) + b_2\sin\omega_2(t-t_C) + b_3 \quad (31a)$$

$$\begin{aligned} i_r &= C_r\frac{dv_r}{dt} = \omega_2 C_r\{-b_1\sin\omega_2(t-t_C) \\ &\quad + b_2\cos\omega_2(t-t_C)\} \end{aligned} \quad (31b)$$

where the coefficients $\{b_k\}$ can be determined as follows:

$$b_1 = \left\{\frac{(3\alpha-1)\beta + 2n(1-\alpha)}{\alpha\beta(1+\alpha)} - \frac{1}{\beta}\right\}V_L \quad (32a)$$

$$b_2 = \frac{4n+1+\alpha+\beta(\alpha-3)}{(1+\alpha)^{3/2}\beta}V_L\sin\omega_6 t_{CB} \quad (32b)$$

$$b_3 = \frac{V_i}{n}. \quad (32c)$$

This mode ends when the recovery capacitor current i_r becomes zero, and the time interval $t_{\rm DC}$ is then determined as follows:

$$t_{DC} = \frac{1}{\omega_2}\left(\frac{\pi}{2} - \tan^{-1}\frac{b_1}{b_2}\right). \quad (33)$$

The recovery capacitor is fully charged at the time $t_{\rm D}$ as follows:

$$v_r(t_D) = b_1 \cos\omega_2 t_{DC} + b_2 \sin\omega_2 t_{DC} + b_3 \equiv V_{\rm rp} \rightarrow V_{\rm rp,max} = \sqrt{b_1^2 + b_2^2} + b_3. \quad (34)$$

Mode 14 [$t_{\rm D}$, $t_{\rm E}$]: At $t_{\rm D}$, the resonant current i_r reaches zero and the ZCS is achieved for D_1 and D_2. Now, Q is solely turned ON, and all the other diodes are completely turned OFF for a while, as shown in Fig. 2(o). Considering the fact that $L_a << L_m$, the magnetizing current i_m is finally determined as follows:

$$i_Q = i_a = \frac{n+1}{n} i_m \cong \frac{n+1}{nL_m}\left(\int_{t_D}^{t} \frac{n+1}{n} V_i dt\right) = \left(\frac{n+1}{n}\right)^2 \frac{V_i}{L_m}(t - t_D). \quad (35)$$

III. Voltage and Current Stress of Each Component

For practical applications of the proposed converter, the voltage and current stress of each component, which are determined based on the circuit analysis results of the previous section, should be within reasonable ranges. As identified from Figs. 2 and 3, the maximum voltages of the switch Q, diodes D_1, D_2, D_3, and snubber capacitor C_s are always bounded to the load voltage V_L. One exception is the output diode D_0, which suffers the disadvantage of higher voltage stress caused by the recovery capacitor voltage $V_{\rm rp}$ during Mode 13, as determined by (34) as follows:

$$V_{0,\max} = V_L + V_{rp,\max}. \quad (36)$$

As identified from Figs. 2 and 3 again, $I_{\rm Qp}$, which is the peak current of the switch Q, is determined by either $I_{\rm Qp}$ of Mode 12 or $I_{\rm mp}$ contribution of Mode 14. From (27b) and (28a), $I_{\rm Qp}$ is obtained as follows:

$$I_{\rm Qp} \equiv \frac{n+1}{n}(-I_{b,\min}) \equiv \frac{n+1}{n} I_{\rm rp} = \frac{n+1}{n}\omega_6 C_s a_1 = \omega_6 C_s V_L \frac{n+1}{n}\frac{\alpha\{4n+1+\alpha+\beta(\alpha-3)\}}{(1+\alpha)^2\beta}. \quad (37)$$

Similarly, the peak current rating of the snubber diode and link diode D_1 and D_2 are determined by either the $I_{\rm mp}$ of the turn-off transient modes or the $I_{\rm rp}$ of the turn-on transient modes, which is defined in (37).

As identified from Figs. 2(b) and 3, the peak current rating of the clamp diode D_3 is involved in Mode 2; however, the current change during Mode 2 is negligible, so only Mode 3 is examined as follows:

$$I_{3,\max} = \text{Max}\{i_a + i_b\} = \text{Max}\left\{\frac{n+1}{n}(I_{\rm mp} - i_b) + i_b\right\} = \text{Max}\left\{\frac{n+1}{n} I_{\rm mp} - \frac{i_b}{n}\right\} = \frac{n+1}{n} I_{\rm mp} \because i_b > 0. \quad (38)$$

The peak voltage ratings and peak current ratings for all the components of the proposed converter are listed in Table I.

TABLE I
Peak Component Ratings of the Proposed Converter

	Peak voltage [V]	Peak current [A]
Switch Q	V_L	$\text{Max}\left\{I_{\rm Qp}, I_{\rm mp}\frac{n+1}{n}\right\}$
Output diode D_0	$V_L + V_{rp}$	$I_{\rm mp}$
Snubber diode D_1	V_L	$\text{Max}\left\{I_{\rm rp}, I_{\rm mp}\frac{n+1}{n}\right\}$
Link diode D_2	$V_{\rm rp} - \frac{V_i}{n}$	$\text{Max}\left\{I_{\rm rp}, I_{\rm mp}\frac{n+1}{n}\right\}$
Clamp diode D_3	V_L	$\frac{n+1}{n} I_{\rm mp}$
Snubber capacitor C_s	V_L	$\frac{n+1}{n} I_{\rm mp}$
Recovery capacitor C_r	$V_{\rm rp}$	$I_{\rm rp}$

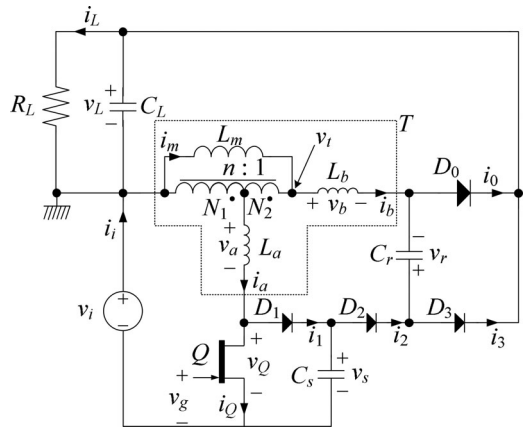

Fig. 5. Circuit diagram of the proposed single-switch-based ZVZCS tapped buck–boost converter.

IV. Extension of the Proposed ZVZCS Scheme: Buck–Boost Converter Case

The proposed ZVZCS scheme, which is a lossless snubber circuit consisting of three small size diode and two capacitors, can be applied to not only boost-type but also other converter types. The proposed idea is extended to a single-switch-based ZVZCS tapped buck–boost converter, as shown in Fig. 5. The averaged static characteristic of the proposed buck–boost converter in the CCM is determined simply by an averaged duty cycle D like a conventional tapped-inductor buck–boost converter as follows [58]:

$$G_{v,\rm CCM} \equiv \frac{V_L}{V_i} \cong \frac{D}{1-D}\cdot\frac{n+1}{n} \quad (39a)$$

$$I_m \cong \frac{I_L}{1-D}. \quad (39b)$$

Similarly, the averaged static characteristics of the proposed buck–boost converter in the DCM are determined as (40), where $D_{\rm off}$ is the time ratio that the output diode D_0 conducts

$$G_{v,\rm DCM} \equiv \frac{V_L}{V_i} \cong \frac{D}{1-D_{\rm off}}\frac{n+1}{n} = \frac{D(n+1)}{n}\sqrt{\frac{T_s R_L}{2L_m}} \quad (40a)$$

$$D_{\rm off} = \frac{D}{G_{v,\rm DCM}}\frac{n+1}{n}. \quad (40b)$$

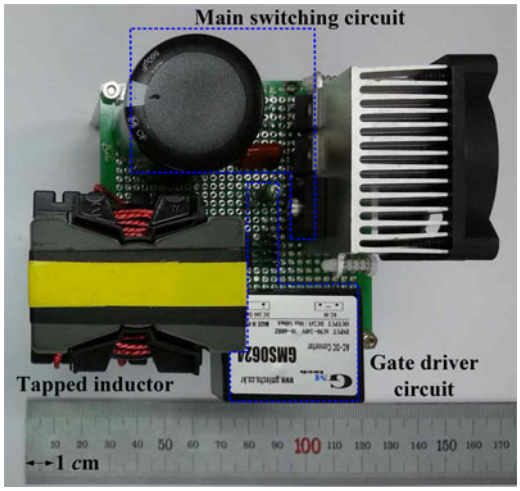

Fig. 6. Photo of a prototype of the proposed ZVZCS tapped boost converter.

TABLE II
SELECTED PARAMETERS OF THE PROPOSED CONVERTER

Parameters	Values
n	2
$L_m\,[\mu\mathrm{H}]$	238
$L_a\,[\mu\mathrm{H}]$	3.80
$L_b\,[\mu\mathrm{H}]$	7.45
$C_s\,[\mathrm{nF}]$	1
$C_r\,[\mathrm{nF}]$	4

The operating principle of the proposed ZVZCS buck–boost converter is the same as that of the previous boost converter case. The ZCS turn-on and ZVS turn-off are achieved for an active switch by means of leakage inductances and snubber capacitor. The energy retrieving process, which is the energy transferring from the snubber capacitor to the recovery capacitor, is conducted by the *LC* resonance during the switch turn-on time to prepare for the next ZVS operation. The operating modes and detailed analyses of the buck–boost are omitted in this paper because the exact circuit analyses for both CCM and DCM of the boost converter have already been provided in [57] and the previous section, respectively. The maximum voltage stress across the active switch, which is one of the most important design factors, is clamped as $V_i + V_L$ during the operation, as in the boost converter case. The ZVZCS operation and the gain characteristic will be validated with a prototype in the subsequent section.

V. EXPERIMENTAL VERIFICATIONS

The design principle introduced in [57] and the component stress analysis in the previous section have been applied to a prototype ZVZCS tapped boost converter in the DCM, operating at 50-kHz switching frequency. A SiC JFET (SJEP120R063), having turn-on and turn-off switching times of 20 ns, was selected because it is a common mid-to-high performance switching device that is affordable. A set of Mn-Zn-type ferrite PQ core was

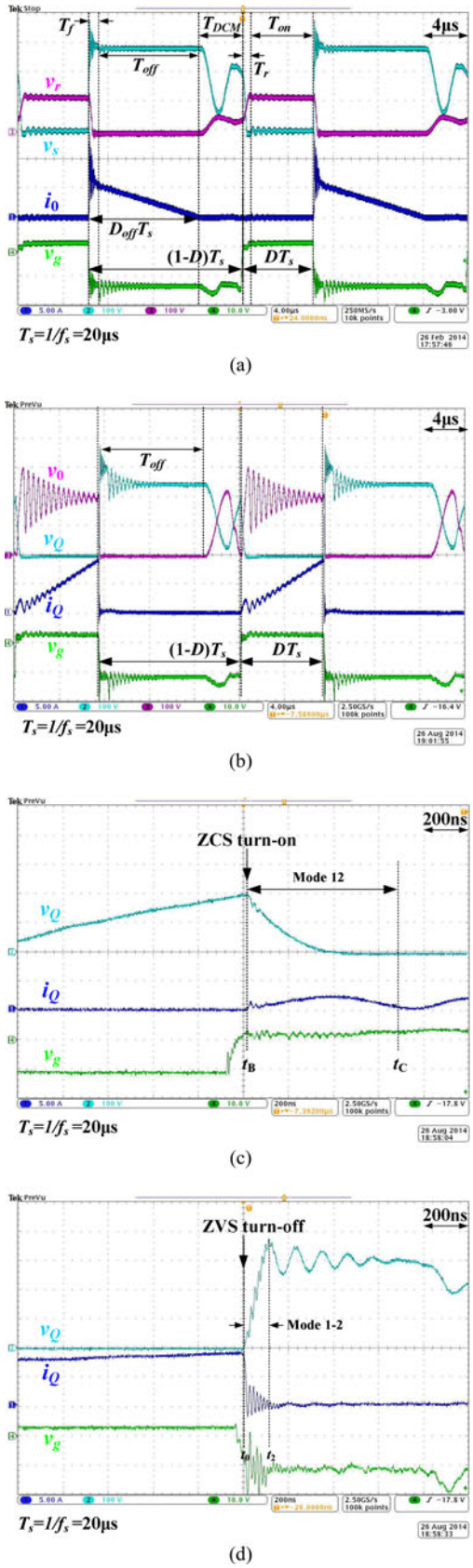

Fig. 7. Measured waveforms for the ZVZCS boost converter in the DCM operation when $D = 0.35$, $V_L = 300$ V. (a) v_r, v_s, i_0, and v_g. (b) v_0, v_Q, i_Q, and v_g. (c) Zoomed-in waveforms for ZCS turn-on. (d) Zoomed-in waveforms for ZVS turn-off.

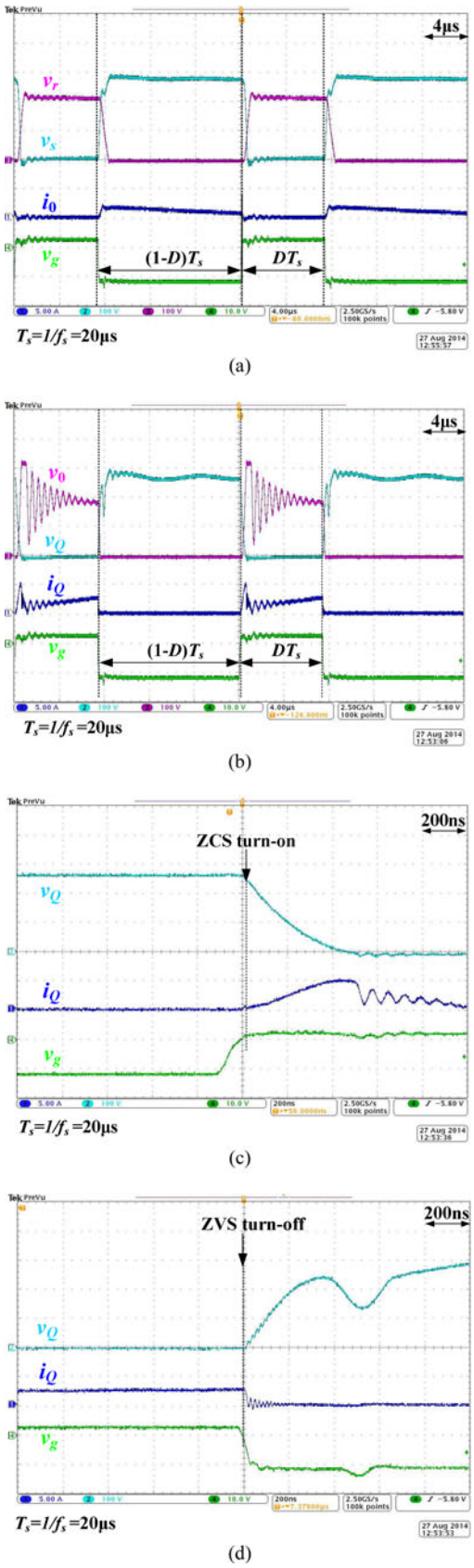

Fig. 8. Measured waveforms for the ZVZCS buck–boost converter in the CCM operation when $D = 0.35$, $V_L = 150$ V. (a) v_r, v_s, i_0, and v_g. (b) v_0, v_Q, i_Q, and v_g. (c) Zoomed-in waveforms for ZCS turn-on. (d) Zoomed-in waveforms for ZVS turn-off.

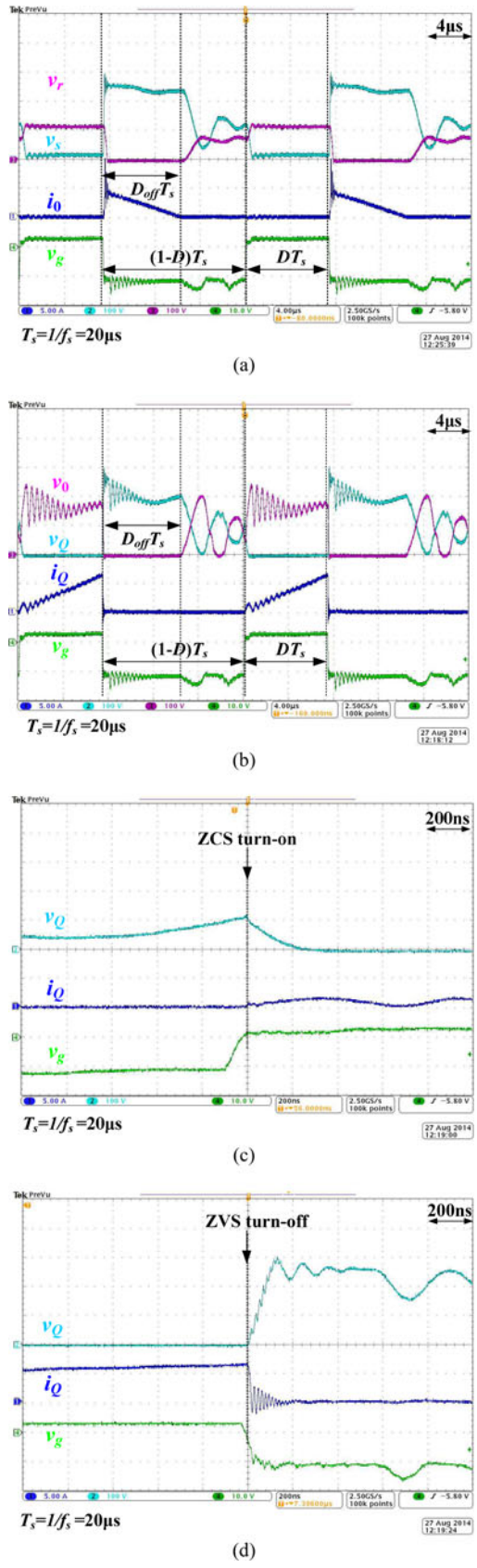

Fig. 9. Measured waveforms for the ZVZCS buck–boost converter in the DCM operation when $D = 0.35$, $V_L = 150$ V. (a) v_r, v_s, i_0 and v_g. (b) v_0, v_Q, i_Q and v_g. (c) Zoomed-in waveforms for ZCS turn-on. (d) Zoomed-in waveforms for ZVS turn-off.

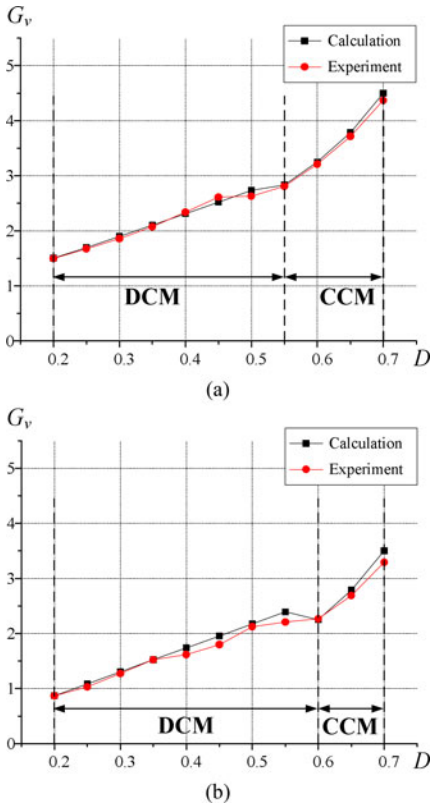

Fig. 10. Measured output voltage gain G_v for an input voltage of 50 V. (a) Boost converter case. (b) Buck–boost converter case.

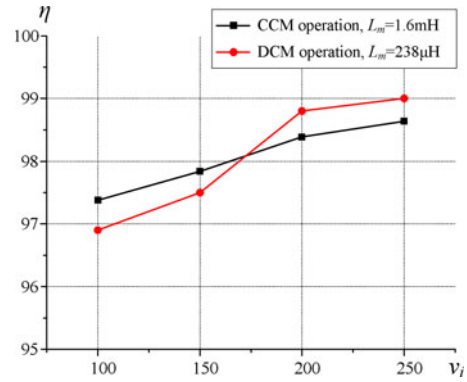

Fig. 11. Measured efficiency η for a load voltage of 300 V.

used to fabricate a tapped inductor where the magnetizing inductance L_m and the turn ratio n are 238 μH and 2, respectively. The proposed converter was fabricated, as shown in Fig. 6, and the circuit parameters are tabulated in Table II. By reconnecting the ground port of the load to the positive side of the input voltage source, a prototype ZVZCS tapped buck–boost converter was simply achieved with the same component values as those of the boost prototype.

The experimental waveforms of the proposed ZVZCS tapped boost converter are illustrated in Fig. 7, where the voltage and current stresses of the components are well mitigated in accordance with the analyses. The ZCS turn-on and ZVS turn-off for DCM operation were successfully verified, as shown in Fig. 7(c) and (d). Moreover, the experimental waveforms of the ZVZCS tapped buck–boost converter for both CCM and DCM operations are illustrated in Figs. 8 and 9, respectively. From the detailed waveforms, as shown in Fig. 8(c) and (d) and Fig. 9(c) and (d), the proposed ZVZCS tapped buck–boost scheme were clearly verified.

The input-to-output voltage gain G_v, for both ZVZCS tapped boost and buck–boost converters, were measured w.r.t. D and compared with the ideal case of (1), (39), and (40), as shown in Fig. 10(a) and (b). It is verified that the experimental results coincide with the theory for a wide operating range of D from 0.2 to 0.7. Two digital power meters (Yokogawa WT1600 and WT210) were used at the input and load sides for the efficiency measurement. As shown in Fig. 11, the maximum efficiency η of the proposed ZVZCS tapped boost converter for the fixed load voltage of 300 V at the switching frequency of 50 kHz, neglecting the gate driver power consumption, was measured as 99.0% in the DCM operation when $L_m = 238$ μH and 98.6% in the CCM operation when $L_m = 1.6$ mH, respectively. From the temperature measurement by a thermo-graphic camera (Fluke Ti10), it was found that the efficiency drop was mainly due to the core loss and conduction loss of the inductor. The temperature of a tapped inductor increased up to 41 °C during the efficiency measurement, whereas the other components, such as the snubber and recovery capacitors, had lower temperature profiles of under 35 °C when the ambient temperature was 23 °C. The load power was fixed to 450 W for the input voltage range of 100–250 V during the efficiency measurement. The efficiency evaluation was not conducted for the buck–boost converter case in this paper because of an excessive voltage rating of the prototype.

VI. Conclusion

A complete mode analysis and design of a single-SiC-switch-based ZVZCS tapped boost converter have been performed and verified both by theory and experiment. The proposed converter has a wide ZVZCS operating range with no severe voltage and current stresses, or cumbersome parasitic ringing. Moreover, high efficiencies of 98.6% and 99.0% were achieved by a prototype converter for the CCM and DCM operations, respectively. The extension of the proposed ZVZCS scheme to other converter types is introduced and experimentally verified for an example buck–boost type. Due to its wide ZVZCS operating range regardless of DCM or CCM operation with simple circuit structure, the proposed converter can be a suitable candidate for the power factor correction circuits with high efficiency, where the load voltage is fixed and input voltage is rapidly varying in time. A detail design of the tapped inductor of the proposed converter is left for future work.

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