Bidirectional Operation of High Step-Down Converter

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***Abstract*—In this paper, a high step-down bidirectional converter, utilizing one coupled inductor and two energy-transferring capacitors, is presented. In the step-down mode, the capacitor is connected between input voltage and coupled inductor, which plays a role to step down the input voltage. Therefore, the corresponding voltage conversion ratio is much lower than that of the traditional buck converter and also can be lower than that of the tapped-inductor buck converter. Moreover, the output voltage varies with the duty cycle linearly, making control easier. In the step-up mode, one capacitor is first charged by the coupled inductor, and then releases the energy along with the coupled inductor and the other capacitor connected in series. Therefore, a higher voltage gain can be obtained. Furthermore, the leakage inductance energy can be recycled. Therefore, the switching losses can be reduced and the efficiency can be improved. In this study, the operating principles and experimental results are provided to verify the effectiveness and performance of the proposed converter.**

***Index Terms*—Bidirectional converter, coupled inductor, energy-transferring capacitor, step-down converter.**

I. Introduction

With the development of technology, step-down converters are widely used in digital circuit power systems, which needs lower input voltages. In general, a 48 V voltage source generated from the ac–dc converter is used for communication systems in the network communication room. Traditionally, the buck converter is used to step down the high voltage to a lower voltage. However, for the device which needs an input voltage of 3.3 V or less, an extremely low duty cycle is necessary for the buck converter if the input voltage is 48 V, thereby causing the control design to be tough and the accompanying power loss to be relatively high. Up to now, the two-stage step-down structure has been widely employed in the applications which need much lower voltage conversion ratio. For example, in order to power the CPU, the DRAM and the hard disk, the first stage transfers 48 to 12 V to power the point of load (POL), and then the POL, called the second stage, transfers 12 to 3.3, 2.5, 1.8, 1.5, 1.2 or 1 V.

The methods described in [1]–[4] are based on the two-stage buck converter. But these methods need relatively many active switches and components, PWM gate driving circuits and signals, etc. Obviously, its overall efficiency is the product of the efficiencies of two stages. Hence, the two-stage buck converter is not suitable for low-power applications. In [5], a high-efficiency open-loop bus converter is presented. In this converter, the input voltage of 48 V voltage is first stepped down to 12 V, which is converted into a lower output voltage of 3.3 V or less to supply the load via a second stage, named POL. Basically, such a topology belongs to a two-stage converter. But, this bus converter along with the accompanying POL needs six active switches and three magnetic devices, along with individual control integrated circuits (ICs). The methods described in [6]–[10] are based on multiple voltage regulators connected in parallel and coupled inductors, and accordingly by using interleaved PWM signals, the ratio of output voltage to input voltage can be enhanced. As compared with the traditional buck converter, under the condition of the same input and output voltages, this converter can operate under a relatively large duty cycle, thereby reducing the problem in a relatively small duty cycle. However, the aforementioned structure needs at least two phases operating simultaneously, so it is suitable for high output current applications. The methods described in [7], [11]–[18] are based on coupled inductors so as to achieve high step-down voltage conversion ratios. Even though these circuits are simple, the leakage inductances of the coupled inductors would cause high voltage spikes to tend to break down the switches, and hence additional passive snubbers are required to protect the switches from being destroyed, thereby tending to reduce the corresponding efficiency. Although the active snubbers presented by the literatures [18]–[20] can recycle the energy stored in leakage inductances, the accompanying circuits are too complex. In [6], [12], [21]–[24], too many switches and magnetic devices are needed, resulting in high cost and complex structures, hence they are not suitable for low- or middle-power applications. In [25], in order to achieve the fast transient response, the switching capacitor along with the transformer is employed to transfer the energy to the output terminal. In [7], [10], [12], [17], [19], [21], [22], [26], the switches require floating gate drivers instead of low-cost half-bridge gate drivers. In this case, if the pulse transformer is adopted, the PCB space will become relatively large, leading to difficulty in applications. The method described in [4] possesses the floating output, which limits the applications. The method described in [8], [11]–[13], [15], [19], [20], [26], [27]–[29] possesses nonlinearity in voltage conversion ratio, thereby making the controller design difficult. The method described in [30] needs many inductors, capacitors, and diode arrays, leading to too many components used and relatively low efficiency.

Based on the aforementioned, a high step-down converter is presented, which utilizes one coupled inductor, two

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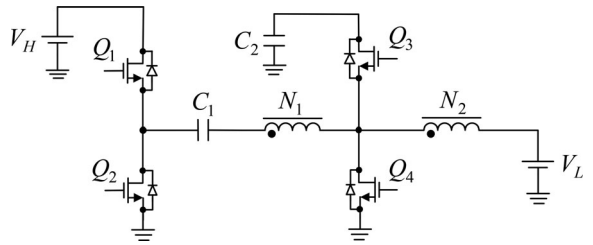

Fig. 1. Proposed bidirectional step-down converter.

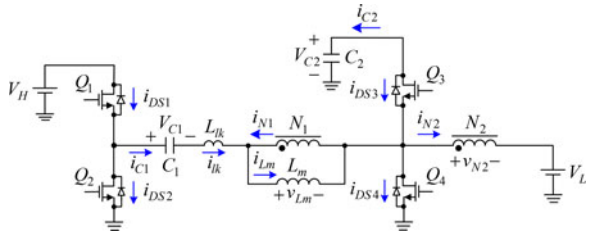

Fig. 2. Equivalent circuit model of the proposed converter.

energy-transferring capacitors with small capacitances, and the proposed converter can be driven using existing buck PWM control ICs. Furthermore, the voltage conversion ratio of this converter is much lower than that of the traditional buck converter. Above all, its output voltage varies with the duty cycle linearly. In addition, the proposed high step-down converter can be operated in the step-up mode. Therefore, the proposed converter can be used in the energy harvesting applications, such as thermoelectric generation system, which can convert heat energy into electricity. As generally recognized, the output voltage of the thermoelectric generator is very sensitive to temperature variations. Therefore, a converter with high voltage gain is preferable in this application [31]–[33]. Since the proposed converter can be operated in a bidirectional way, it can be used in the burn-in test applications [34]–[36].

II. Overall System Configuration

Fig. 1 shows the proposed bidirectional converter, which contains four switches Q_1, Q_2, Q_3, and Q_4, two energy-transferring capacitors C_1 and C_2, and one coupled inductor composed of the primary winding N_1 and the secondary winding N_2. Moreover, Q_1 and Q_3 are driven simultaneously, whereas Q_2 and Q_4 are driven simultaneously. Although there are four switches in this circuit, only two half-gate drivers are required to drive them. In addition, the high-voltage side is denoted by V_H, and the low-voltage side is signified by V_L.

III. Basic Converter Analysis

The equivalent circuit of the proposed converter is shown in Fig. 2. The coupled inductor is modeled as an ideal transformer with the primary winding N_1 and the secondary winding N_2, a magnetizing inductor L_m connected in parallel with the N_1 winding, and a leakage inductor L_{lk}. Besides, in order to make the analysis of the proposed converter easier, there are some assumptions to be made as follows:

1) the proposed converter operates in the positive current region, that is, the current flowing through the magnetizing inductor L_m is always positive;
2) all the switches and diodes are assumed to be ideal components;
3) the values of all the capacitors are large enough such that the voltages across them are kept constant at some values.

The following analysis contains the operating principles, voltage gains, boundary conditions of the magnetizing inductor in step-down and step-up modes, influence of leakage inductance, and performance comparison with different step-down converters. In addition, the currents flowing through Q_1, Q_2, Q_3, Q_4, C_1, C_2, L_{lk}, N_1, N_2, and L_m are signified by i_{DS1}, i_{DS2}, i_{DS3}, i_{DS4}, i_{C1}, i_{C2}, i_{lk}, i_{N1}, i_{N2}, and i_{Lm}, respectively. Furthermore, the voltage across L_m or the voltage across the N_1 winding is signified by v_{Lm}, the voltage across the N_2 winding is represented by v_{N2}, and the voltages across C_1 and C_2 are indicated by V_{C1} and V_{C2}.

A. Step-Down Mode Operation

For the proposed converter operating in the positive current region, there are ten operating states, to be described as follows. Fig. 3 shows the illustrated waveforms over one switching period. It is noted that the current i_{N1} is the same as the current i_{N2} except that there is a difference in amplitude between the two.

1) *State 1 [t_0, t_1]:* As shown in Fig. 4(a), the switches Q_1 and Q_3 are turned ON, but the switches Q_2 and Q_4 are turned OFF. During this state, a positive voltage is imposed on the magnetizing inductor L_m and the leakage inductor L_{lk}, making both L_m and L_{lk} magnetized. In the meantime, the capacitor C_1 is charged, and the currents in the N_1 winding and the capacitor C_2, i.e., i_{N1} and i_{C2}, are decreasing slowly, providing energy to the load. This state comes to an end once i_{C2} reaches zero at t_1.
2) *State 2 [t_1, t_2]:* As shown in Fig. 4(b), the switches Q_1 and Q_3 keep turned ON, but the switches Q_2 and Q_4 keep turned OFF. During this state, the capacitor C_2 is charged, so the current i_{C2} is increasing continuously. Meanwhile, the current i_{N1} is continuously decreasing. This mode ends when i_{N1} drops to zero at t_2.
3) *State 3 [t_2, t_3]:* As shown in Fig. 4(c), the switches Q_1 and Q_3 still keep turned ON, but the switches Q_2 and Q_4 still keep turned OFF. During this state, the currents i_{lk} and i_{Lm} keep increasing, and the current i_{N2} is also increasing in the opposite direction. As a result, the current i_{C2} is the sum of i_{lk} and $-i_{N2}$. This state ends as Q_1 and Q_3 are turned OFF at t_3.
4) *State 4 [t_3, t_4]:* As shown in Fig. 4(d), the switches Q_1 and Q_3 become turned OFF, and the switches Q_2 and Q_4 keep turned OFF. During this blanking time period, the body diodes of Q_2 and Q_3 are forward biased by the leakage inductance current i_{lk}. Meanwhile, the voltage $(V_{C2} - V_L) \times N_1/N_2$ is imposed on the magnetizing inductor L_m, causing L_m to be continuously

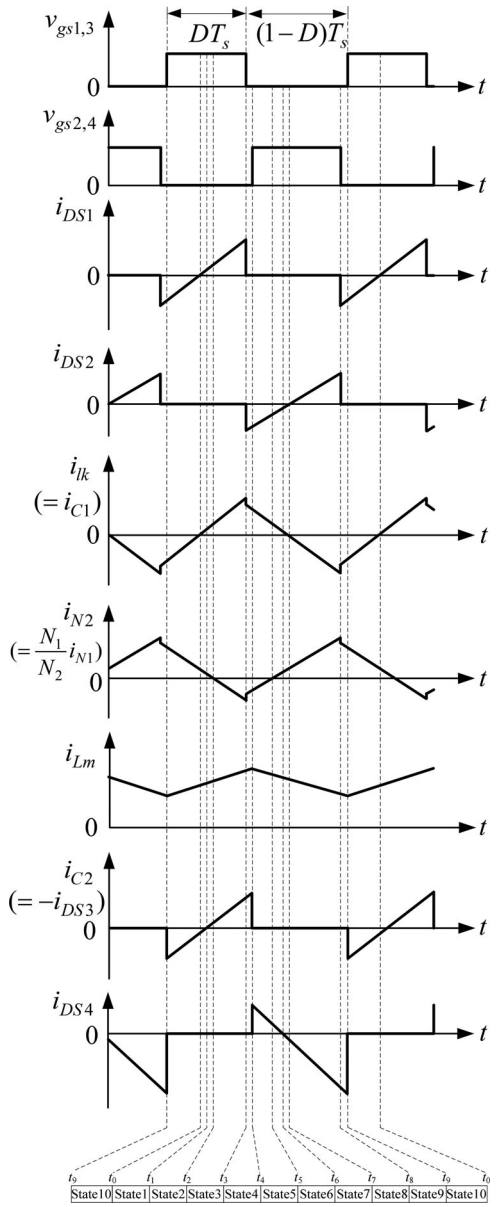

Fig. 3. Illustrated waveforms for the proposed converter in the step-down mode.

magnetized, and the current i_{lk} is gradually declining. This state comes to an end while Q_2 and Q_4 become turned ON at t_4.

5) *State 5 [t_4, t_5]:* As shown in Fig. 4(e), the switches Q_1 and Q_3 keep turned OFF, but the switches Q_2 and Q_4 become turned ON. Since there is a current flowing through the body diode of Q_2 before state 5 begins, Q_2 can achieve ZVS turn-on. Meanwhile, the voltage $-V_{C1}$ is imposed on the magnetizing inductor L_m, thereby causing L_m to be demagnetized, and the current i_{lk} is gradually declining. The current i_{N2} is decreasing until it reaches zero at t_5, and this state ends.
6) *State 6 [t_5, t_6]:* As shown in Fig. 4(f), the switches Q_1 and Q_3 still keep turned OFF, and Q_2 and Q_4 still keep turned ON. During this state, the current i_{lk} is decreasing and the current i_{N2} is increasing. L_m keeps demagnetized. As soon as i_{lk} is smaller than i_{N2}, the current i_{ds4} will change the current direction. As i_{ds4} drops to zero, this state ends at t_6.
7) *State 7 [t_6, t_7]:* As shown in Fig. 4(g), the switches Q_1 and Q_3 are still turned OFF, but Q_2 and Q_4 are still turned ON. During this state, the magnetizing inductor L_m still keeps demagnetized, the current i_{lk} is still decreasing, the current i_{N2} is still increasing, and the current i_{ds4} is increasing in the opposite direction. This state comes to an end once i_{lk} reaches zero at t_7.
8) *State 8 [t_7, t_8]:* As shown in Fig. 4(h), the switches Q_1 and Q_3 are still in the turn-off state, but Q_2 and Q_4 are still in the turn-on state. During this state, the magnetizing inductor L_m still keeps demagnetized, the current i_{lk} is increasing in the opposite direction, the current i_{N2} is still increasing, and the current i_{ds4} is increasing in the opposite direction. This state ends when Q_2 and Q_4 are turned OFF at t_8.
9) *State 9 [t_8, t_9]:* As shown in Fig. 4(i), the switches Q_1 and Q_3 still keep turned OFF, and the switches Q_2 and Q_4 become turned OFF. During this blanking time period, the body diodes of Q_1 and Q_4 are forward biased by the current i_{lk}, and also, the magnetizing inductor L_m keeps demagnetized. Meanwhile, the leakage inductor L_{lk} is demagnetized, and i_{N2} is decreasing. This state comes to an end when Q_1 and Q_3 are turned ON at t_9.
10) *State 10 [t_9, t_0]:* As shown in Fig. 4(j), the switches Q_2 and Q_4 keep turned OFF, but the switches Q_1 and Q_3 become turned ON. Before the state 10 begins, there is a current flowing through the body diode of Q_1, and hence, Q_1 can be turned ON with ZVS. On the other hand, the leakage inductor L_{lk} is still demagnetized, and C_2 is discharging energy to the load. This state ends when the current i_{lk} reaches zero at t_0, and the next cycle is repeated.

B. Step-Up Mode Operation

For the proposed converter operating in the positive current region, there are ten operating states, to be described as follows. Fig. 5 shows the illustrated waveforms over one switching period.

1) *State 1 [t_0, t_1]:* As shown in Fig. 6(a), Q_1 and Q_3 are turned ON, but Q_2 and Q_4 are turned OFF. During this state, the voltage $(V_{C2}-V_o)\times N_1/N_2$ is imposed on L_m, thereby causing L_m to be magnetized. Meanwhile, i_{lk} is increasing but i_{N1} is decreasing, whereas C_2 is charged but C_1 is discharged. This state ends when i_{C2} reaches zero at t_1.
2) *State 2 [t_1, t_2]:* As shown in Fig. 6(b), Q_1 and Q_3 keep turned ON, but Q_2 and Q_4 keep turned OFF. This state is the same as the state 1 except that C_2 is discharged. This state comes to an end as i_{N1} reaches zero at t_2.
3) *State 3 [t_2, t_3]:* As shown in Fig. 6(c), Q_1 and Q_3 keep turned ON, but Q_2 and Q_4 keep turned OFF. During this state, L_m keeps demagnetized. At the same time,

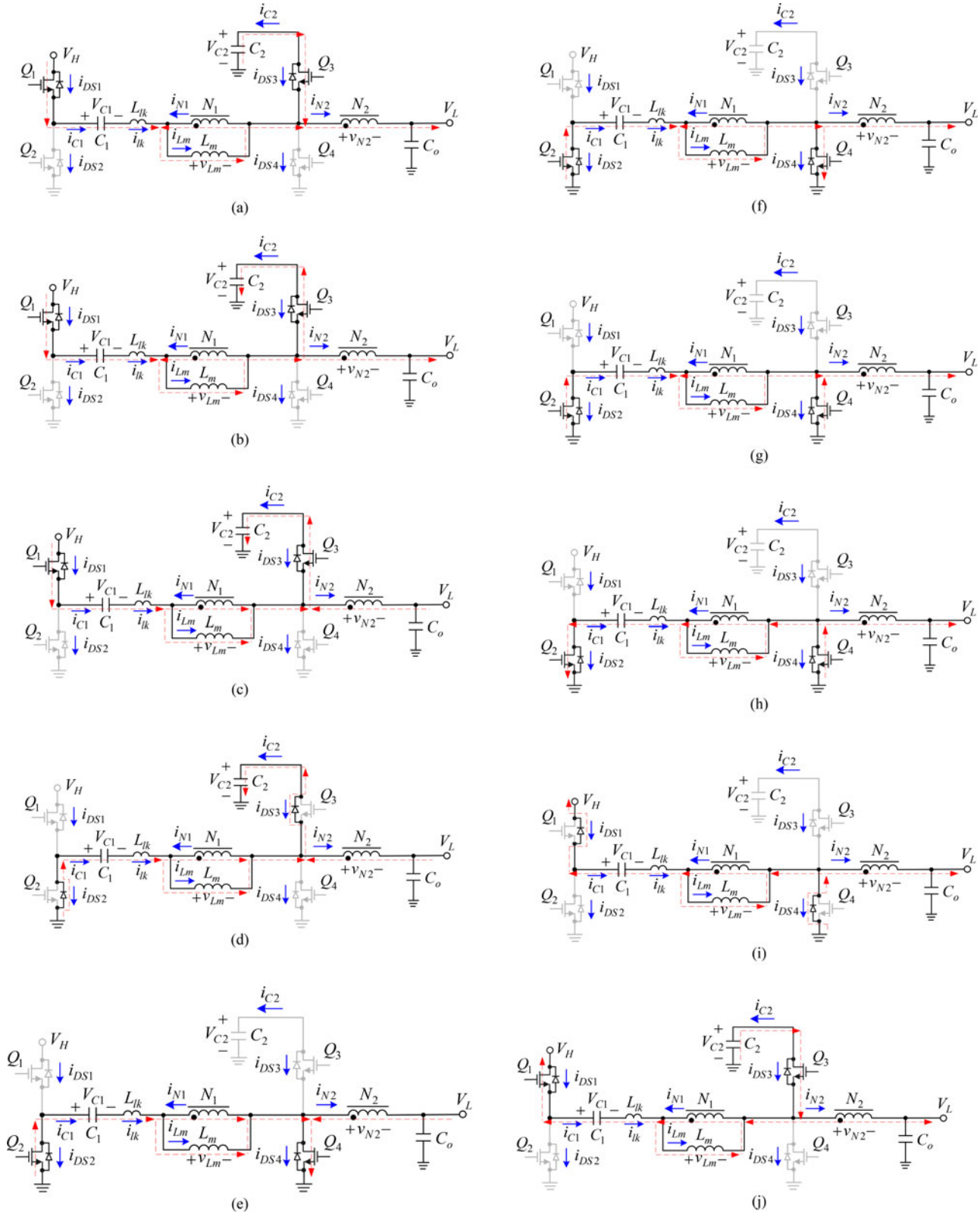

Fig. 4. Power flow paths over one switching period in the step-down mode: (a) state 1; (b) state 2; (c) state 3; (d) state 4; (e) state 5; (f) state 6; (g) state 7; (h) state 8; (i) state 9; and (j) state 10.

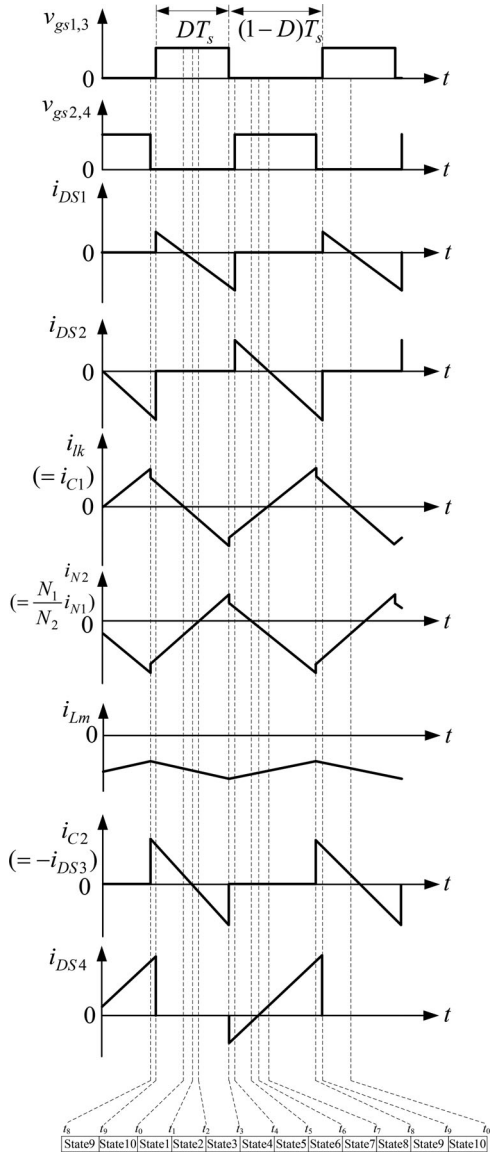

Fig. 5. Illustrated waveforms for the proposed converter in the step-up mode.

i_{N1} is increasing in the positive direction, whereas i_{lk} is increasing in the opposite direction. Also, C_2 is continuously discharged energy. This state ends when Q_1 and Q_3 are turned OFF at t_3.

4) *State 4 [t_3, t_4]:* As shown in Fig. 6(d), Q_1 and Q_3 become turned OFF, and Q_2 and Q_4 keep turned OFF. During this blanking time period, the body diodes of the switches Q_1 and Q_4 are forward biased. In the meantime, the voltage $-V_o \times N_1/N_2$ is imposed on L_m, thereby causing L_m to be demagnetized. Also, i_{lk} is declining. This state comes to an end as Q_2 and Q_4 are turned ON at t_4.
5) *State 5 [t_4, t_5]:* As shown in Fig. 6(e), Q_1 and Q_3 keep turned OFF, but Q_2 and Q_4 become turned ON. Since there is a current flowing through the body diode of Q_4 before state 5 begins, Q_4 can achieve ZVS turn-on. Also, L_m is still demagnetized. Once i_{N1} falls to zero, this state ends at t_5.

TABLE I
SUMMARIZATION OF ZVS ACHIEVEMENT

Switch Mode	Q_1	Q_2	Q_3	Q_4
Step-down	ZVS turn-on	ZVS turn-on	ZVS turn-off	ZVS turn-off
Step-up	ZVS turn-off	ZVS turn-off	ZVS turn-on	ZVS turn-on

6) *State 6 [t_5, t_6]:* As shown in Fig. 6(f), Q_1 and Q_3 still keep turned OFF, but Q_2 and Q_4 still keep turned ON. During this state, i_{N1} and i_{N2} are increasing. Meanwhile, L_m is still demagnetized, and i_{lk} is continuously declining. As soon as i_{N2} is equal to i_{lk}, thereby causing i_{ds4} to reach to zero, this state comes to an end at t_6.
7) *State 7 [t_6, t_7]:* As shown in Fig. 6(g), Q_1 and Q_3 are still in the turn-off state, but Q_2 and Q_4 are still in the turn-on state. During this state, L_m is still demagnetized, and i_{lk} is still decreasing. Once i_{lk} drops to zero, this state ends at t_7.
8) *State 8 [t_7, t_8]:* As shown in Fig. 6(h), Q_1 and Q_3 are still turned OFF, but Q_2 and Q_4 are still turned ON. During this state, L_m is still demagnetized, and i_{lk} starts to increase. This state ends as Q_2 and Q_4 are turned OFF at t_8.
9) *State 9 [t_8, t_9]:* As shown in Fig. 6(i), the switches Q_1 and Q_3 still keeps turned OFF, and Q_2 and Q_4 become turned OFF. During this blanking time period, the body diodes of the switches Q_2 and Q_3 are forward biased. In the meantime, L_m starts to be magnetized by the voltage $(V_{C2} - V_L) \times N_1/N_2$. This state ends when Q_1 and Q_3 are turned ON at t_9.
10) *State 10 [t_9, t_0]:* As shown in Fig. 6(j), Q_2 and Q_4 keep turned OFF, but Q_1 and Q_3 become turned ON, and Q_3 achieves ZVS turn-on. During this state, L_m is still magnetized by the voltage $(V_{C2} - V_L) \times N_1/N_2$, and i_{lk} is continuously demagnetized. This state ends once i_{lk} reaches zero at t_0, and the next cycle is repeated.

C. ZVS Achievement

From the above analyses of the step-down mode and step-up mode, the ZVS states can be summarized in Table I.

D. Voltage Gain in Step-Down Mode

To attain the voltages across C_1 and C_2, and the voltage gain, only states 2 and 5 as shown in Fig. 4(b) and (e) are considered herein with the blanking times and the leakage inductor L_{lk} ignored. From state 5, V_{C1} can be found to be

$$V_{C1} = -v_{Lm} = V_L \cdot \left(\frac{N_1}{N_2}\right). \tag{1}$$

Furthermore, from state 2, V_{C2} can be described to be

$$V_{C2} = V_L + (V_H - V_{C1} - V_L) \cdot \left(\frac{N_2}{N_1 + N_2}\right). \tag{2}$$

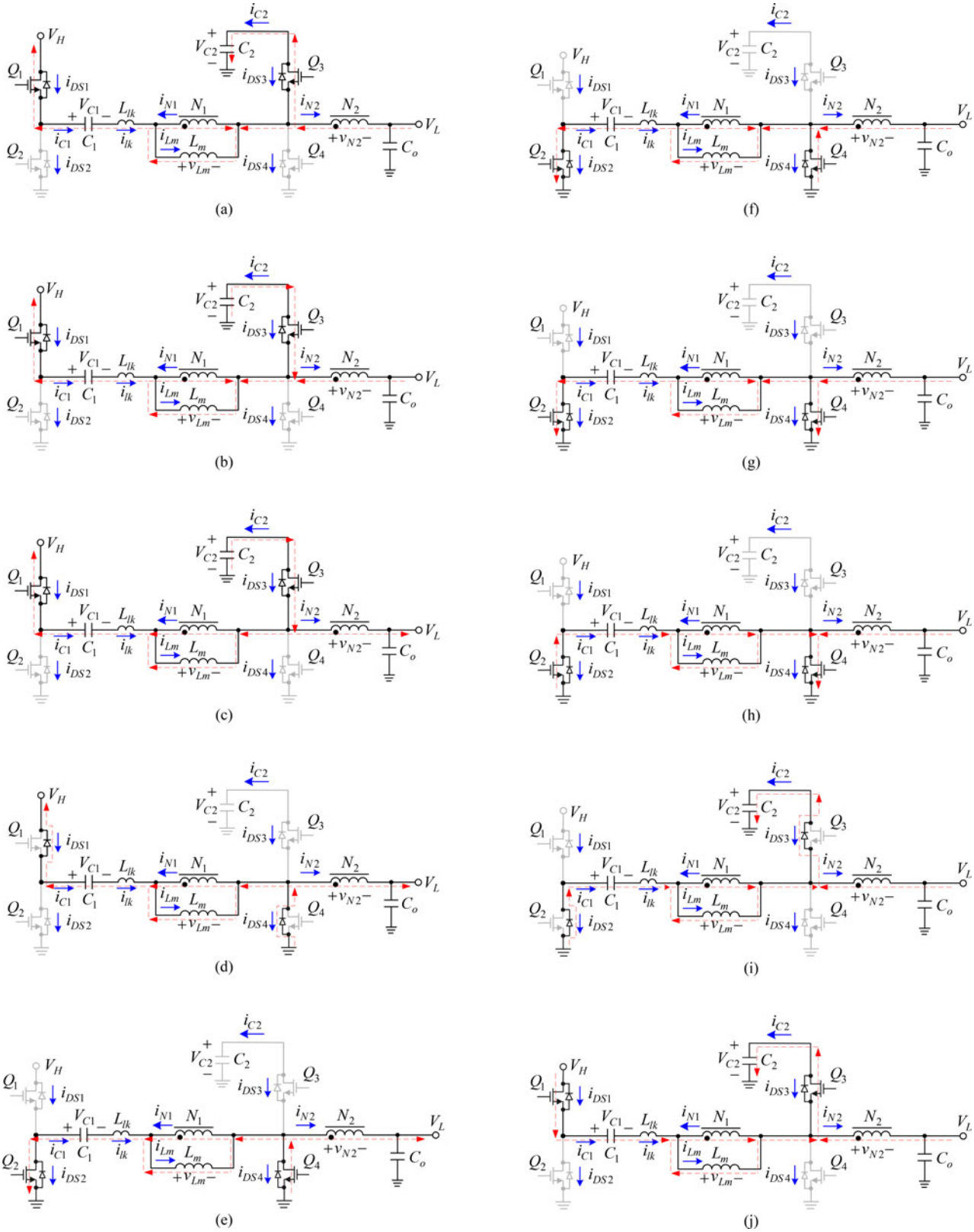

Fig. 6. Power flow paths over one switching period in the step-up mode: (a) state 1; (b) state 2; (c) state 3; (d) state 4; (e) state 5; (f) state 6; (g) state 7; (h) state 8; (i) state 9; and (j) state 10.

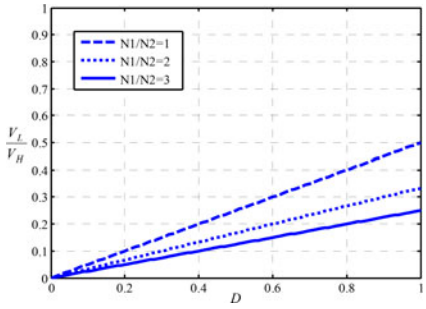

Fig. 7. Curves of voltage gain versus duty cycle for the proposed converter in the step-down mode with different values of turns ratio.

In addition, by applying the voltage–second balance principle to L_m over one switching period, the following equation can be obtained to be

$$D\cdot(V_H - V_{C1} - V_L)\cdot\left(\frac{N_1}{N_1+N_2}\right) = (1-D)\cdot V_L\cdot\left(\frac{N_1}{N_2}\right). \tag{3}$$

Next, based on (1) and (3), the corresponding voltage gain can be expressed by

$$\frac{V_L}{V_H} = D\cdot\left(\frac{N_2}{N_1+N_2}\right). \tag{4}$$

From (4), it can be seen that the voltage gain of the proposed converter can be adjusted not only by the duty cycle but also by the primary and secondary turns. Fig. 7 shows the curves of voltage gain versus duty cycle of the proposed converter, considering different values of turns ratio.

E. Boundary Condition for Magnetizing Inductor in Step-Down Mode

The condition for the magnetizing inductor L_m operating in what region will be described as follows: equation (5) as shown on the bottom of the page where I_{Lm} and Δi_{Lm} are the dc and ac components of i_{Lm}, respectively.

The expression of I_{Lm} can be obtained from (6) and (7). For analysis convenience, it is assumed that the input power is equal to the output power. According to the voltage–second balance for the inductor and the ampere–second balance for the capacitor, the dc component of the inductor voltage and the dc component of the capacitor current are zero. Therefore, as shown in Fig. 8, the dc component of i_{N2}, I_{N2}, is equal to $I_{o,L}$, which is the dc component of the output current $i_{o,L}$; likewise, as shown in Fig. 9, the dc component of current i_{Lm}, I_{Lm}, is equal to the dc component of i_{N1}, I_{N1}. Therefore

$$I_{N1} = \frac{N_2}{N_1}I_{N2} = \frac{N_2}{N_1}I_{o,L} \tag{6}$$

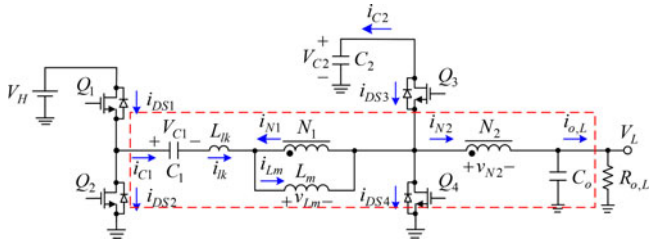

Fig. 8. Marked area in the proposed converter used to explain the relationship between I_{Lm} and $I_{o,L}$.

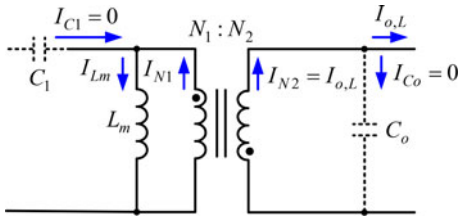

Fig. 9. Equivalent model for dc analysis of the coupled inductor.

$$I_{Lm} = I_{N1} = \frac{N_2}{N_1}I_{o,L}. \tag{7}$$

In Fig. 8, $I_{o,L}$ can be expressed as $V_L/R_{o,L}$. Substituting $V_L/R_{o,L}$ into $I_{o,L}$ in (7) yield the following:

$$I_{Lm} = I_{N1} = \frac{N_2}{N_1}\times\frac{V_L}{R_{o,L}}. \tag{8}$$

Also, Δi_{Lm} can be represented by

$$\begin{aligned}\Delta i_{Lm} &= \frac{v_{Lm}\Delta t}{L_m} = \frac{\frac{N_1}{N_2}\times V_L\times(1-D)T_s}{L_m}\\ &= \frac{\frac{N_1}{N_1+N_2}\times V_H\times D(1-D)T_s}{L_m}.\end{aligned} \tag{9}$$

As $2I_{Lm}\geq\Delta i_{Lm}$, L_m operates in the positive current region. Moreover, the further deduction is shown as follows:

$$\begin{aligned}&2I_{Lm}\geq\Delta i_{Lm}\\ &\Rightarrow 2\times\frac{N_2}{N_1}\times\frac{V_L}{R_{o,L}}\geq\frac{\frac{N_1}{N_1+N_2}V_H\times D(1-D)T_s}{L_m}\\ &\Rightarrow\frac{2L_m}{R_{o,L}T_s}\geq\left(\frac{N_1}{N_2}\right)^2(1-D)\\ &\Rightarrow K_1\geq K_{crit1}(D)\end{aligned} \tag{10}$$

where $K_1=\frac{2L_m}{R_{o,L}T_s}$ and $K_{crit1}(D)=\left(\frac{N_1}{N_2}\right)^2(1-D)$.

From (10), the relationship between $K_{crit1}(D)$ and D is shown in Fig. 10 under the condition that N_1/N_2 is set at 3. From Fig. 10, it can be seen that if K_1 is larger than $K_{crit1}(D)$,

$$\begin{cases}2I_{Lm}\geq\Delta i_{Lm}, & \text{for all current values in the positive current region}\\ 2I_{Lm}<\Delta i_{Lm}, & \text{for part of current values in the negative current region}\end{cases} \tag{5}$$

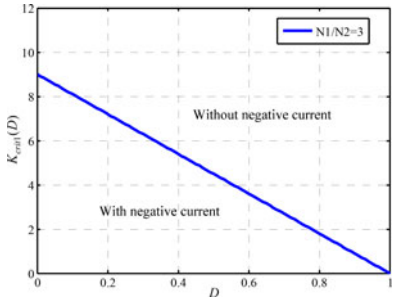

Fig. 10. Boundary condition for magnetizing inductor L_m in the step-down mode.

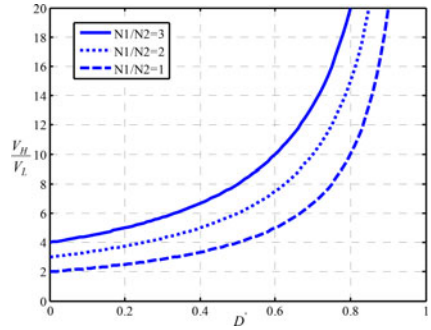

Fig. 11. Curves of voltage gain versus duty cycle for the proposed converter in the step-up mode with different values of turns ratio.

L_m will operate in the positive current region; otherwise, part of i_{Lm} will enter the negative current region.

F. Voltage Gain in Step-Up Mode

To attain the voltages across C_1 and C_2, and the voltage gain, only states 2 and 8 as shown in Fig. 6(b) and (h) are considered herein with the blanking times and the leakage inductor L_{lk} ignored. From state 2, V_H can be found to be

$$V_H = V_{C1} + v_{Lm} + V_{C2}. \tag{11}$$

Furthermore, from state 8, V_{C1} can be found to be

$$V_{C1} = \frac{N_1}{N_2} \cdot V_L. \tag{12}$$

In addition, by applying the voltage–second balance principle to L_m over one switching period, the following equation can be obtained:

$$D \cdot (V_{C2} - V_L) \cdot \left(\frac{N_1}{N_2}\right) = (1-D) \cdot V_L \cdot \left(\frac{N_1}{N_2}\right). \tag{13}$$

V_{C2} can be found to be

$$V_{C2} = \frac{1}{D} \cdot V_L. \tag{14}$$

Next, in state 2, v_{Lm} can be found to be

$$v_{Lm} = \left(\frac{N_1}{N_2}\right) \cdot \left(\frac{1-D}{D}\right) \cdot V_L. \tag{15}$$

Based on (11), (12), (14), and (15), V_H can be expressed to be

$$\begin{aligned} V_H &= \frac{N_1}{N_2} \cdot V_L + \left(\frac{N_1}{N_2}\right) \cdot \left(\frac{1-D}{D}\right) \cdot V_L + \frac{1}{D} \cdot V_L \\ &= \left(1 + \frac{N_1}{N_2}\right) \cdot \frac{1}{D} \cdot V_L. \end{aligned} \tag{16}$$

The corresponding voltage gain can be expressed to be

$$\frac{V_H}{V_L} = \left(1 + \frac{N_1}{N_2}\right) \cdot \frac{1}{D}. \tag{17}$$

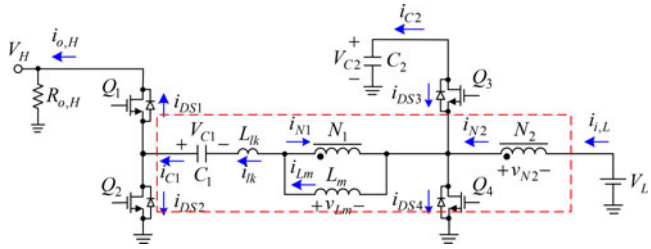

Fig. 12. Marked area in the proposed converter used to explain the relationship between I_{Lm} and $I_{o,H}$.

If $1 - D$ is defined as D', the corresponding voltage gain can be rewritten to be

$$\frac{V_H}{V_L} = \left(1 + \frac{N_1}{N_2}\right) \cdot \frac{1}{1-D'} \cdot V_L. \tag{18}$$

From (18), it can be seen that the voltage gain of the proposed converter can be adjusted not only by the duty cycle but also by the primary and secondary turns. Fig. 11 shows the curves of voltage gain versus duty cycle of the proposed converter, considering different values of turns ratio.

G. Boundary Condition for Magnetizing Inductor in Step-Up Mode

The condition for the magnetizing inductor L_m operating in what region will be described as follows: equation (19) as shown on the bottom of the page where I_{Lm} and Δi_{Lm} are the dc and ac components of i_{Lm}, respectively.

The expression of I_{Lm} can be obtained from (20) and (21). For analysis convenience, it is assumed that the input power is equal to the output power. According to the voltage–second balance for the inductor and the ampere–second balance for the capacitor, the dc component of the inductor voltage and the dc component of the capacitor current are zero. Therefore, as shown in Fig. 12, the dc component of i_{N2}, I_{N2}, is equal to $I_{i,L}$, which is the dc component of the input current $i_{i,L}$; likewise, as shown in Fig. 13, the dc component of current i_{Lm}, I_{Lm}, is equal to the dc component of i_{N1}, I_{N1}.

$$\begin{cases} 2I_{Lm} \geq \Delta i_{Lm}, & \text{for all current values in the positive current region} \\ 2I_{Lm} < \Delta i_{Lm}, & \text{for part of current values in the negative current region} \end{cases} \tag{19}$$

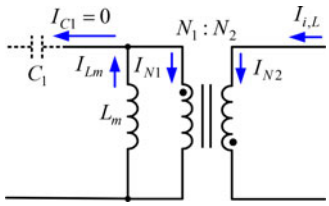

Fig. 13. Equivalent model for dc analysis of the coupled inductor.

Therefore

$$I_{N1} = \frac{N_1}{N_2} I_{N2} = \frac{N_1}{N_2} I_{i,L} \tag{20}$$

$$I_{Lm} = I_{N1} = \frac{N_2}{N_1} I_{i,L}. \tag{21}$$

Since $I_{i,L}$ can be expressed as $\left(1+\frac{N_1}{N_2}\right)\cdot\frac{1}{D}\cdot I_{o,H}$, (21) can be rewritten as

$$\begin{aligned} I_{Lm} &= \frac{N_2}{N_1}\cdot\left(1+\frac{N_1}{N_2}\right)\cdot\frac{1}{D}\cdot I_{o,H} \\ &= \left(1+\frac{N_2}{N_1}\right)\cdot\frac{1}{D}\cdot I_{o,H}. \end{aligned} \tag{22}$$

In Fig. 12, $I_{o,H}$ can be expressed as $V_H/R_{o,H}$. Substituting $V_H/R_{o,H}$ into $I_{o,H}$ in (22) yield the following:

$$I_{Lm} = \left(1+\frac{N_2}{N_1}\right)\cdot\frac{1}{D}\cdot\frac{V_H}{R_{o,H}}. \tag{23}$$

Also, Δi_{Lm} can be represented by

$$\Delta i_{Lm} = \frac{v_{Lm}\Delta t}{L_m} = \frac{\frac{N_1}{N_2}\cdot V_L\cdot(1-D)\cdot T_s}{L_m}. \tag{24}$$

As $2I_{Lm} \geq \Delta i_{Lm}$, L_m operates in the positive current region. Moreover, the further deduction is shown as follows:

$$\begin{aligned} &2I_{Lm} \geq \Delta i_{Lm} \\ &\Rightarrow 2\cdot\left(1+\frac{N_2}{N_1}\right)\cdot\frac{1}{D}\cdot\frac{V_H}{R_{o,H}} \geq \frac{\frac{N_1}{N_2}\cdot V_L\cdot(1-D)\cdot T_s}{L_m} \\ &\Rightarrow \frac{2L_m}{R_{o,H}T_s} \geq \left(\frac{D}{1+\frac{N_2}{N_1}}\right)^2(1-D) \\ &\Rightarrow \frac{2L_m}{R_{o,H}T_s} \geq \left(\frac{1-D'}{1+\frac{N_2}{N_1}}\right)^2 D' \\ &\Rightarrow K_2 \geq K_{crit2}(D') \end{aligned} \tag{25}$$

where $K_2 = \dfrac{2L_m}{R_{o,H}T_s}$ and $K_{crit2}(D') = \left(\dfrac{1-D'}{1+\frac{N_2}{N_1}}\right)^2 D'$.

From (25), the relationship between $K_{crit2}(D')$ and D' is shown in Fig. 14 under the condition that N_1/N_2 is set at 3. From Fig. 14, it can be seen that if K_2 is larger than $K_{crit2}(D')$, L_m will operate in the positive current region; otherwise, part of i_{Lm} will enter the negative current region.

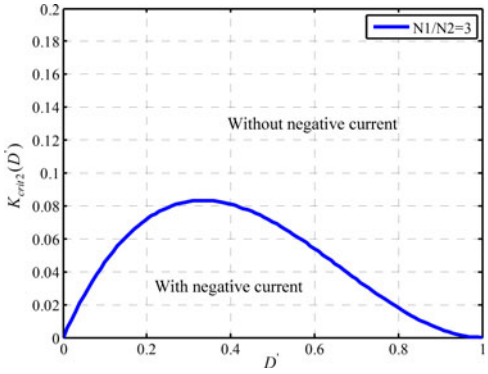

Fig. 14. Boundary condition for magnetizing inductor L_m in the step-up mode.

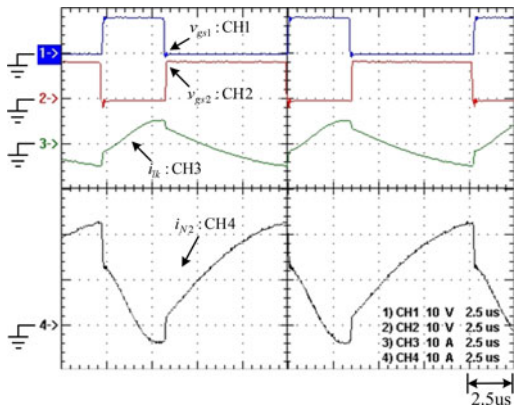

Fig. 15. Waveforms at rated load in step-down mode: (1) v_{gs1} [10 V/div]; (2) v_{gs2} [10 V/div]; (3) i_{lk} [10 A/div]; (4) i_{N2} [10 A/div].

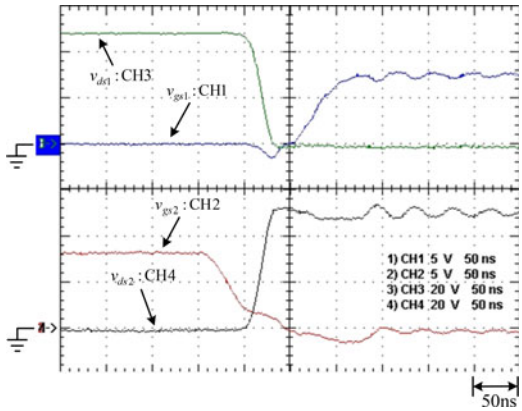

Fig. 16. Waveforms at rated load due to rising edge of v_{gs1} in step-down mode: (1) v_{gs1} [5 V/div]; (2) v_{gs2} [5 V/div]; (3) v_{ds1} [20 V/div]; (4) v_{ds2} [20 V/div].

H. Influence of the Leakage Inductance

In practice, the voltage of C_1 will be affected by the leakage inductance. This can be seen in the step-down mode in state 7 shown in Fig. 4(g), and in the step-up mode in state 8 shown in Fig. 6(h). Hence, the voltage across C_1, V_{C1}, with the leakage inductance considered, can be found as follows.

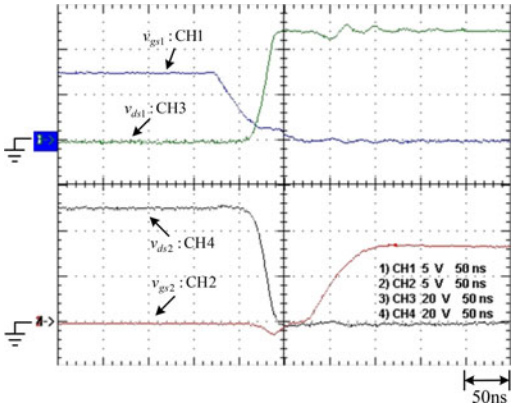

Fig. 17. Waveforms at rated load due to rising edge of v_{gs2} in step-down mode: (1) v_{gs1} [5 V/div]; (2) v_{gs2} [5 V/div]; (3) v_{ds1} [20 V/div]; (4) v_{ds2} [20 V/div].

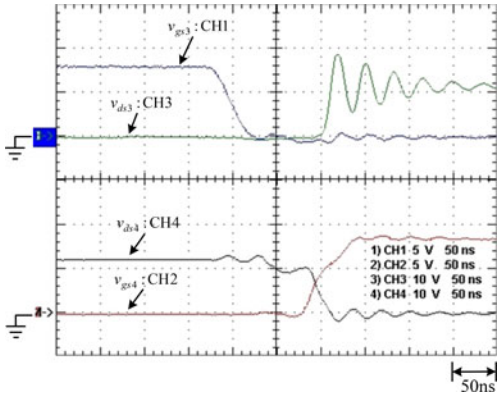

Fig. 19. Waveforms at rated load due to rising edge of v_{gs4} in step-down mode: (1) v_{gs3} [5 V/div]; (2) v_{gs4} [5 V/div]; (3) v_{ds3} [10 V/div]; (4) v_{ds4} [10 V/div].

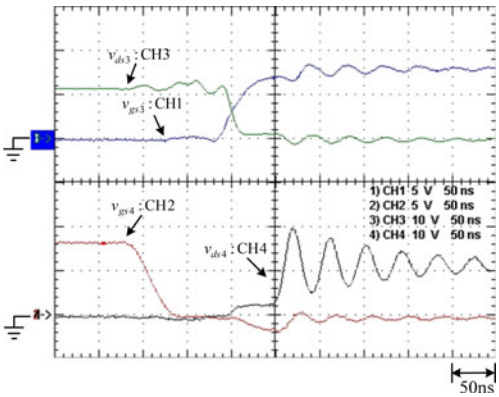

Fig. 18. Waveforms at rated load due to rising edge of v_{gs3} in step-down mode: (1) v_{gs3} [5 V/div]; (2) v_{gs4} [5 V/div]; (3) v_{ds3} [10 V/div]; (4) v_{ds4} [10 V/div].

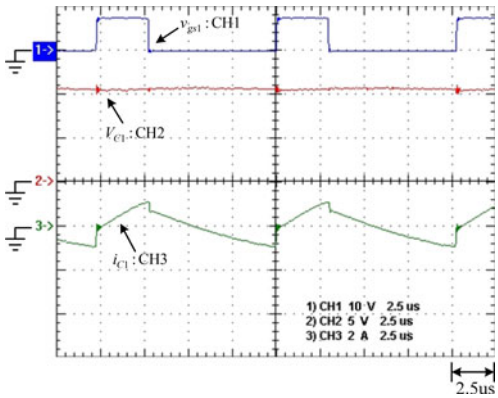

Fig. 20. Waveforms at light load in step-down mode: (1) v_{gs1} [10 V/div]; (2) V_{C1} [5 V/div]; (3) i_{C1} [2 A/div].

1) Step-Down Mode

$$V_{C1} = -\left(v_{lk}^{(7)} + v_{Lm}^{(7)}\right) = -\left[L_{lk}\frac{di_{lk}^{(7)}}{dt} + \frac{N_1}{N_2} \times (-V_L)\right]$$
$$= \frac{N_1}{N_2} \times V_L - L_{lk}\frac{di_{lk}^{(7)}}{dt} \quad (26)$$

where $v_{lk}^{(7)}$, $v_{Lm}^{(7)}$, and $i_{lk}^{(7)}$ are the leakage inductance voltage, magnetizing inductance voltage, and primary-side current in state 7, respectively.

2) Step-Up Mode

$$V_{C1} = -\left(v_{lk}^{(8)} + v_{Lm}^{(8)}\right) = -\left[L_{lk}\frac{di_{lk}^{(8)}}{dt} + \frac{N_1}{N_2} \times (-V_L)\right]$$
$$= \frac{N_1}{N_2} \times V_L - L_{lk}\frac{di_{lk}^{(8)}}{dt} \quad (27)$$

where $v_{lk}^{(8)}$, $v_{Lm}^{(8)}$, and $i_{lk}^{(8)}$ are the leakage inductance voltage, magnetizing inductance voltage, and primary-side current in state 8, respectively.

From (26) and (27), it can be seen that the voltage across C_1 is practically affected by the leakage inductance. Moreover, if the leakage inductance is ignored, the equations shown in (26) and (27) will be rewritten to be $V_{C1} = (N_1/N_2) \cdot V_L$, as shown in (1) of the step-down mode and in (12) of the step-upmode. Moreover, the experimental waveforms of V_{C1} in the step-down and step-up modes are to be shown in Figs. 20 and 21, and Figs. 27 and 28, respectively.

I. Performance Comparison With Different Step-Down Converters

The proposed converter is compared with four step-down type converters as shown in Table II. There are traditional buck converter, two-stage buck converter, tapped-inductor buck converter, full-bridge converter, and the proposed converter. For the voltage gain, under the same duty cycle and turns ratio, the proposed converter has a higher step-down value, and the voltage stresses are smaller than the tapped-inductor buck converter, which also uses a coupled inductor. Moreover, the number of components of the proposed converter is lower than that of the full-bridge converter.

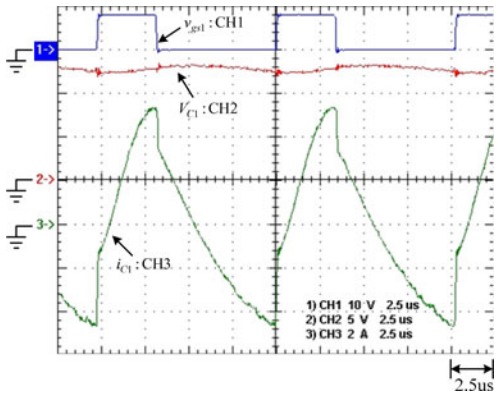

Fig. 21. Waveforms at rated load in step-down mode: (1) v_{gs1} [10 V/div]; (2) V_{C1} [5 V/div]; (3) i_{C1} [2 A/div].

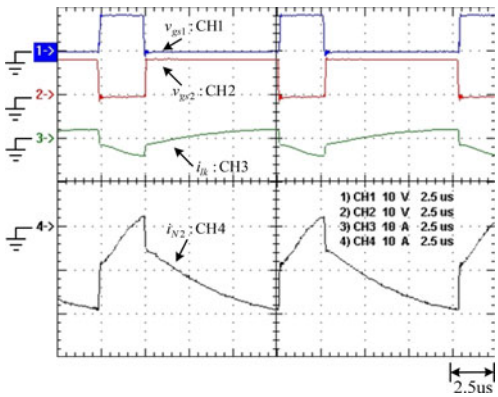

Fig. 22. Waveforms at rated load in step-up mode: (1) v_{gs1} [10 V/div]; (2) v_{gs2} [10 V/div]; (3) i_{lk} [10 A/div]; (4) i_{N2} [10 A/div].

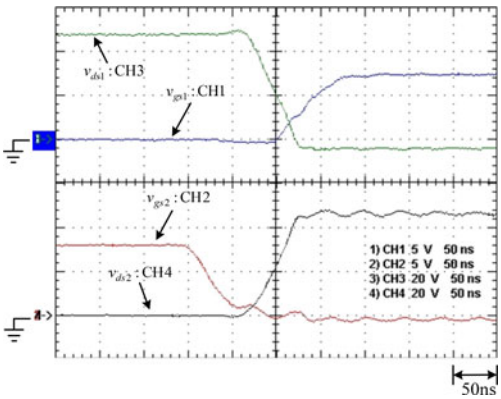

Fig. 23. Waveforms at half load due to rising edge of v_{gs1} in step-up mode: (1) v_{gs1} [5 V/div]; (2) v_{gs2} [5 V/div]; (3) v_{ds1} [20 V/div]; (4) v_{ds2} [20 V/div].

IV. Design Considerations

To verify the effectiveness of the proposed converter, a prototype is built up and tested. Table III shows the specifications of the proposed converter, and Table IV shows the components used in the proposed converter. Since the proposed converter is originally operated in the step-down mode, the following designs are based on the step-down operation.

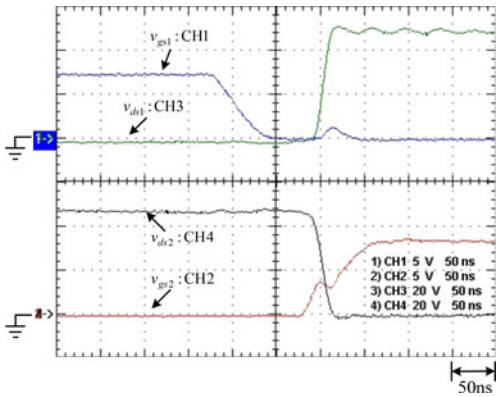

Fig. 24. Waveforms at rated load due to rising edge of v_{gs2} in step-up mode: (1) v_{gs1} [5 V/div]; (2) v_{gs2} [5 V/div]; (3) v_{ds1} [20 V/div]; (4) v_{ds2} [20 V/div].

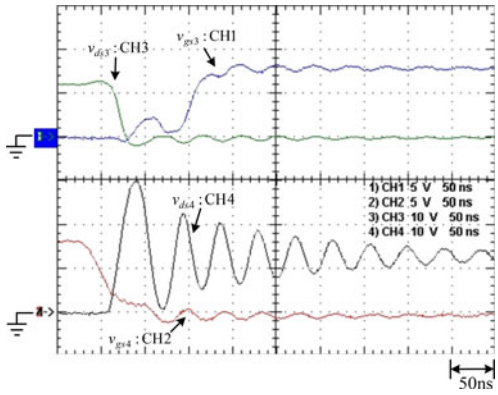

Fig. 25. Waveforms at rated load due to rising edge of v_{gs3} in step-up mode: (1) v_{gs3} [5 V/div]; (2) v_{gs4} [5 V/div]; (3) v_{ds3} [10 V/div]; (4) v_{ds4} [10 V/div].

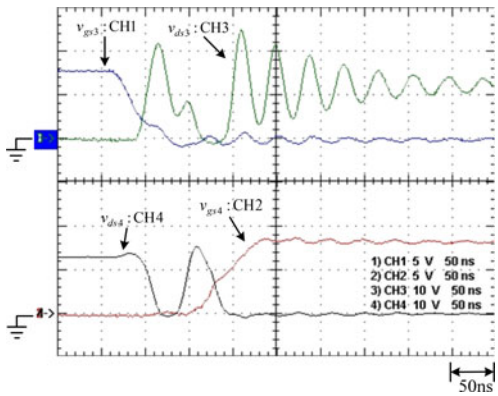

Fig. 26. Waveforms at rated load due to rising edge of v_{gs4} in step-up mode: (1) v_{gs3} [5 V/div]; (2) v_{gs4} [5 V/div]; (3) v_{ds3} [10 V/div]; (4) v_{ds4} [10 V/div].

A. Determination of Duty Cycle and Turns Ratio

In this study, the voltage conversion ratio under step-down mode is set at $3.3/48 = 0.06875$. Therefore, according to (4), there are many different possibilities of choosing the duty cycle D and turns ratio. If $N_1/N_2 = 1$, D will be 13.75%, which is too small and not a suitable duty cycle. If $N_1/N_2 = 4$, D will be 34.38%. However, this turns ratio will increase the volume of the coupled inductor and enlarge the leakage inductance.

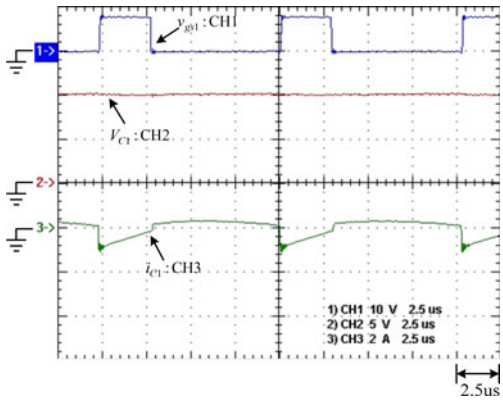

Fig. 27. Waveforms at light load in step-up mode: (1) v_{gs1} [10 V/div]; (2) V_{C1} [5 V/div]; (3) i_{C1} [2 A/div].

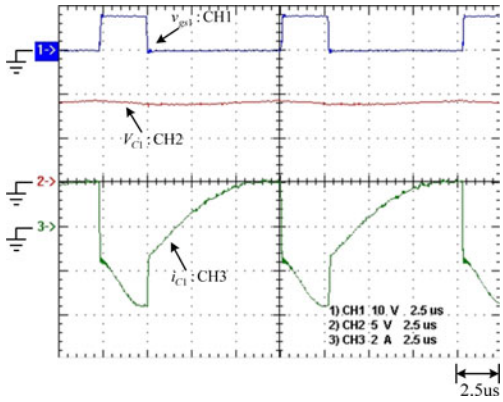

Fig. 28. Waveforms at rated load in step-up mode: (1) v_{gs1} [10 V/div]; (2) V_{C1} [5 V/div]; (3) i_{C1} [2 A/div].

Eventually, the combination of $N_1/N_2 = 3$ and $D = 27.5\%$ will be a preferred choice.

B. Magnetizing Inductor Design

What current region the proposed converter operates in is determined by the current flowing through the magnetizing inductor L_m. To make sure that L_m always operates in the positive current region, the required equation is as follows:

$$I_{Lm,\min} = \frac{N_2}{N_1} I_{o,L,\min} = \frac{1}{3} \times 1.6 = 0.533\,\text{A} \quad (28)$$

$$\begin{aligned} L_m &> \frac{v_{Lm}\Delta t}{\Delta i_{Lm}} = \frac{\frac{N_1}{N_2} \cdot V_L \cdot (1-D)T_s}{2I_{Lm,\min}} \\ &= \frac{3 \times 3.3 \times (1-0.275) \times 10\mu}{2 \times 0.533} \\ &\approx 67.3\,\mu\text{H} \end{aligned} \quad (29)$$

where $I_{Lm,\min}$ is the minimum dc current in L_m, and finally, the value of L_m is set to 86 μH.

Next, based on (10) and the parameters shown in Tables III and IV, it can be seen that in the step-down mode if the output current $I_{o,L}$ is higher than 1.25 A, the converter will always operates in the positive current region as follows:

$$\begin{aligned} &\frac{2L_m}{R_{o,L}T_s} \geq \left(\frac{N_1}{N_2}\right)^2 (1-D) \\ &\Rightarrow \frac{1}{R_{o,L}} \geq \left(\frac{N_1}{N_2}\right)^2 (1-D)\left(\frac{T_s}{2L_m}\right) \\ &\Rightarrow I_{o,L} \geq \left(\frac{N_1}{N_2}\right)^2 (1-D)\left(\frac{T_s}{2L_m}\right) V_L \\ &\Rightarrow I_{o,L} \geq (3)^2(1-0.275)\left(\frac{10\mu}{2\times 86\mu}\right) \times 3.3 \\ &\Rightarrow I_{o,L} \geq 1.25\,\text{A}. \end{aligned} \quad (30)$$

C. Energy-Transferring Capacitor Design

The capacitors C_1 and C_2 are used to transfer the energy from the input to the output. Thus, the capacitances of C_1 and C_2 can be estimated by using the following equations:

$$C_1 > \frac{2P_{o,\text{rated}}}{V_{C1}^2 \cdot f_s} = \frac{2 \times 26.4}{(9.9)^2 \times 100 \times 10^3} \approx 5.38\,\mu\text{F} \quad (31)$$

$$C_2 > \frac{2P_{o,\text{rated}}}{V_{C2}^2 \cdot f_s} = \frac{2 \times 26.4}{(12)^2 \times 100 \times 10^3} \approx 3.67\,\mu\text{F}. \quad (32)$$

In practice, the actual capacitance decreases with frequency. The actual capacitance is smaller than its rated capacitance when operated at a high switching frequency. Hence, the capacitance should be selected to be larger than the theoretical value. Also, based on (1) and (2), and Tables III and IV, the voltage across C_1 and C_2 are 9.9 and 12 V, respectively. Moreover, other criteria of selecting capacitors are that the values of the capacitors C_1 and C_2 should be larger enough to avoid resonance with leakage inductors, the capacitors C_1 and C_2 have to endure high current ripples, and the ESRs of C_1 and C_2 should be as small as possible. Therefore, the SMD MLCC capacitor would be a good candidate to satisfy these conditions. Eventually, two 10 μF MLCC capacitors connected in parallel are selected for C_1 and C_2.

D. Switch Voltage Stress Analysis

The ideal voltage stresses without considering spikes across Q_1, Q_2, Q_3, and Q_4 can be estimated as follows:

$$V_{ds1} = V_{ds2} = V_H = 48\,\text{V} \quad (33)$$

$$\begin{aligned} V_{ds3} &= V_{ds4} = V_L + (V_H - V_{C1} - V_L) \cdot \left(\frac{N_2}{N_1 + N_2}\right) \\ &= 3.3 + (48 - 9.9 - 3.3) \cdot \frac{1}{4} = 12\,\text{V}. \end{aligned} \quad (34)$$

Practically, considering the effect of noises and the voltage spikes caused by the parasitic and leakage inductances, the specifications of the drain-source voltage rating of the MOSFET, used as the switch, should be appropriately chosen to ensure that the MOSEFET can operate without being damaged. The voltage rating of the MOSFET should be higher than its theoretical values. Finally, two PHB34NQ10T MOSFETs with drain-source voltage ratings of 100 V are selected for Q_1 and Q_2, and two

TABLE II
COMPARISON OF OTHER STEP-DOWN CONVERTERS IN TERMS OF VOLTAGE GAIN, EACH COMPONENT NUMBER, SWITCH VOLTAGE STRESS, AND ISOLATION

Converter	Traditional buck	Two-stage buck	Tapped-inductor buck	Full-bridge	Proposed
Voltage gain	D	D^2	$\frac{D}{1+\frac{N_1}{N_2}\cdot(1-D)}$	$D\cdot\left(\frac{N_2}{N_1}\right)$	$D\cdot\left(\frac{N_2}{N_1+N_2}\right)$
Number of switch	1	2	1	4	4
Number of diode	1	2	1	4	0
Number of coupled inductor or transformer	0	0	1	1	1
Number of capacitor	1	2	1	2	3
Number of output inductor	1	2	0	1	0
Switch voltage stress	$V_{ds1}=V_{\rm in}$	$V_{ds1}=V_{\rm in}$ $V_{ds2}=DV_{\rm in}$	$V_{ds1}=\left(\frac{1+\frac{N_1}{N_2}}{D}\right)\cdot V_o$	$V_{ds1}=V_{ds2}=$ $V_{ds3}=V_{ds4}=$ $V_{\rm in}$	$V_{ds1}=V_{ds2}:$ (33) $V_{ds3}=$ $V_{ds4}:$ (34)
Isolation	No	No	No	Yes	No

IRL8113 MOSFETs with drain-source voltage ratings of 30 V are chosen for Q_3 and Q_4.

V. EXPERIMENTAL RESULTS

Figs. 15–21 show waveforms in the step-down mode. Fig. 15 shows the gate driving signals v_{gs1} and v_{gs2} for the switches Q_1 and Q_2, respectively, the primary-side current i_{lk}, and the secondary-side current i_{N2}. From Fig. 15, it can seen that the actual duty cycle for Q_1 is about 0.28, which is somewhat deviated from the ideal duty cycle of 0.275. Fig. 16 shows the rising edge of v_{gs1}, the voltage across Q_1, v_{ds1}, the falling edge of v_{gs2}, and the voltage across Q_2, v_{ds2}. Fig. 17 shows the falling edge of v_{gs1}, the voltage across Q_1, v_{ds1}, the rising edge of v_{gs2}, and the voltage across Q_2, v_{ds2}. From these figures, it can be seen that the switches Q_1 and Q_2 possess ZVS turn-on. Fig. 18 shows the rising edge of v_{gs3}, the voltage across Q_3, v_{ds3}, the falling edge of v_{gs4}, and the voltage across Q_4, v_{ds4}. Fig. 19 shows the falling edge of v_{gs3}, the voltage across Q_3, v_{ds3}, the rising edge of v_{gs4}, and the voltage across Q_4, v_{ds4}. From these figures, it can be seen that the switches Q_3 and Q_4 possess ZVS turn-OFF. Figs. 20 and 21 show the gate driving signals v_{gs1}, the voltage across C_1, V_{C1}, and the current flowing through C_1, i_{C1}, in the step-down mode, at light load, and rated load, respectively. Based on (26), when Q_1 is turned OFF, the slope of $i_{lk}(=i_{C1})$ is negative. Therefore, the voltage V_{C1} is higher than the ideal value, and when the converter is operated at rated load, the slope of $i_{lk}(=i_{C1})$ is more negative, the voltage V_{C1} is much higher than the ideal value.

Figs. 22–28 show waveforms in the step-up mode. Fig. 22 shows the gate driving signals v_{gs1} and v_{gs2} for the switches Q_1 and Q_2, respectively, the primary-side current i_{lk}, and the secondary-side current i_{N2}. Fig. 23 shows the rising edge of v_{gs1}, the voltage across Q_1, v_{ds1}, the falling edge of v_{gs2}, and the voltage across Q_2, v_{ds2}. Fig. 24 shows the falling edge of v_{gs1}, the voltage across Q_1, v_{ds1}, the rising edge of v_{gs2}, and the voltage across Q_2, v_{ds2}. From these figures, it can be seen that the switches Q_1 and Q_2 possess ZVS turn-off. Fig. 25 shows the rising edge of v_{gs3}, the voltage across Q_3, v_{ds3}, the falling edge of v_{gs4}, and the voltage across Q_4, v_{ds4}. Fig. 26 shows the falling edge of v_{gs3}, the voltage across Q_3, v_{ds3}, the rising edge of v_{gs4}, and the voltage across Q_4, v_{ds4}. From these figures, it can be seen that the switches Q_3 and Q_4 possess ZVS turn-on. Figs. 27 and 28 show the gate driving signals v_{gs1}, the voltage across C_1, V_{C1}, and the current flowing through C_1, i_{C1}, in the step-up mode, at the light load and rated load, respectively. Based on (27), when Q_1 is turned OFF, the slope of $i_{lk}(=i_{C1})$ is positive. Therefore, the voltage V_{C1} is lower than the ideal value, and when the converter is operated at rated load, the slope of $i_{lk}(=i_{C1})$ is more positive, the voltage V_{C1} is much lower than the ideal value.

TABLE III
SYSTEM SPECIFICATIONS OF THE PROPOSED CONVERTER

System parameters	Specifications
High-side voltage (V_H)	48 V
Low-side voltage (V_L)	3.3 V
Rated output current ($I_{o,\rm rated}$)	8 A
Minimum output current ($I_{o,\rm min}$)	1.6 A
Switching frequency (f_s)	100 kHz

From figures mentioned above, it can be seen that there are voltage spikes and severe oscillations across Q_3 and Q_4. Hence, there are two reasons used to describe these phenomena in the following: 1) In this converter, the switches Q_1 and Q_3 are turned ON/OFF simultaneously, whereas the switches Q_2 and Q_4 are turned ON/OFF simultaneously. However, the blanking times between Q_1 and Q_2 are tuned in the step-down mode, so as to obtain the optimal performance of efficiency. Hence, the voltages across Q_3 and Q_4 will have some voltage spikes during the turn-on period in the step-up mode; and 2) the distance between C_2 and Q_3 is too long, thereby causing the parasitic inductance to be relatively large. In addition, the current in the low-voltage side is much higher than that in the high-voltage side. Hence, the voltage across Q_3 and Q_4 will oscillate severely during the turn-off period.

TABLE IV
COMPONENTS USED IN THE PROPOSED CONVERTER

Components		Product name
MOSFET switches	Q_1, Q_2	PHB34NQ10T
	Q_3, Q_4	IRL8113
Energy-transferring capacitor C_1 and C_2		TDK C3225X7S1H106K
Output capacitor C_o		10 μF MLCC × 2, 470 μF Rubycon × 1, 330 μF OSCON × 1, 10 μF MLCC × 1
Coupled inductor		Core: T106-M125, $N_1 : N_2 = 3 : 1$, $L_m = 86$ μH, $L_{lk} = 1.5$ μH
Gate driver		HIP2101
ADC		ADC7476

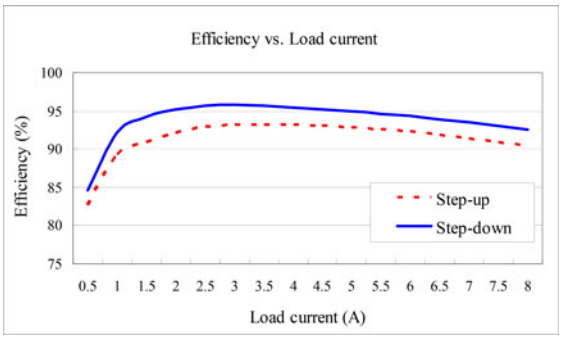

Fig. 29. Efficiency versus load current.

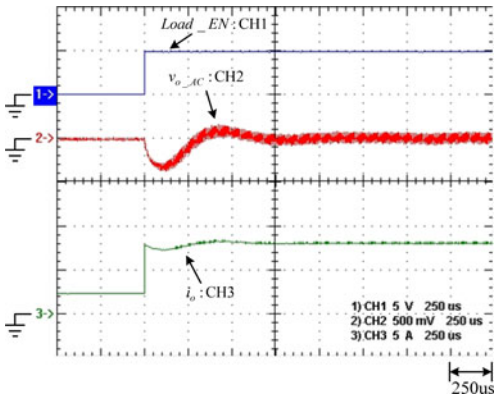

Fig. 30. Load transient responses due to step load change from light load to rated load: (1) *Load_EN* [5 V/div]; (2) v_{o_AC} [500 mV/div]; (3) i_o [5 A/div].

Furthermore, Fig. 29 shows the efficiency under step-down mode and step-up mode. It can be seen that, under step-down mode, the maximum efficiency is about 96% and the rated load efficiency is about 92%, whereas under step-up mode, the maximum efficiency is about 92% and the rated load efficiency is about 90.5%. The reason that the efficiency in the step-down mode is higher than that in the step-up mode is that in the step-up mode, there are oscillations across Q_3 and Q_4; thus, the switching losses will be higher than those in the step-down mode. Moreover, due to the oscillations across them, the soft switching cannot be achieved well. There are still some cross-

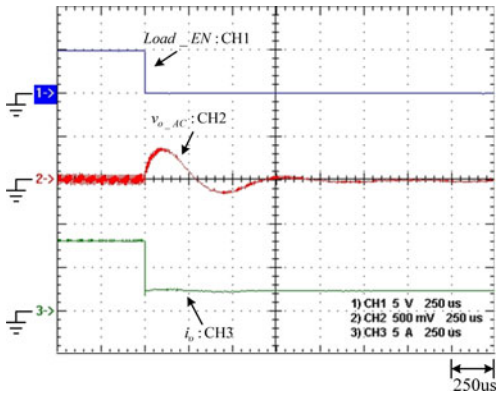

Fig. 31. Load transient responses due to step load change from rated load to light load: (1) *Load_EN* [5 V/div]; (2) v_{o_AC} [500 mV/div]; (3) i_o [5 A/div].

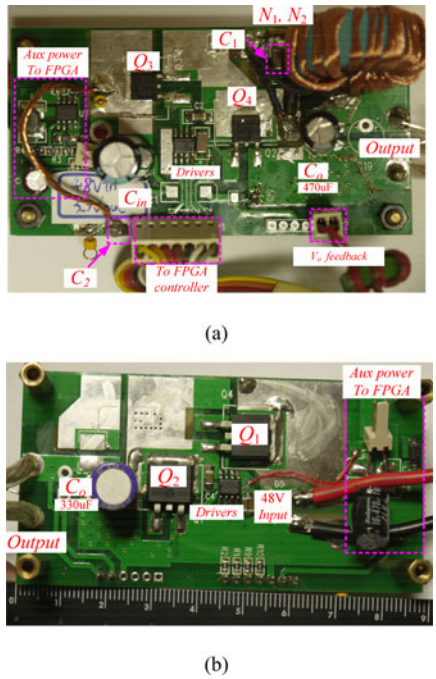

Fig. 32. Photos of the proposed converter from: (a) the top; (b) the bottom.

ing areas, which leads to increasing switching losses. Therefore, the efficiency in the step-down mode is higher than that in the step-up mode.

In addition, Fig. 30 shows the load transient responses due to step load change from light load to rated load, whereas Fig. 31 shows the load transient responses due to step load change from rated load to light load. From Figs. 30 and 31, it can be seen that the corresponding undershoot or overshoot is about 350 mV within 750 μs. Also, Fig. 32 shows the pictures of the proposed converter.

VI. CONCLUSION

First of all, a high step-down bidirectional converter, utilizing a coupled inductor and two energy-transferring capacitors is presented. In the step-down mode, the corresponding voltage conversion ratio is much lower than that of the traditional buck converter. Furthermore, the output voltage varies with the duty

cycle linearly. In the step-up mode, the voltage gain is much higher than that of the traditional boost converter. Moreover, in the step-down mode, the switches Q_1 and Q_2 can achieve ZVS turn-on and the switches Q_3 and Q_4 can achieve ZVS turn-off, whereas in the step-up mode, the switches Q_1 and Q_2 can achieve ZVS turn-off and the switches Q_3 and Q_4 can achieve ZVS turn-on. The leakage inductance energy can be recycled. In addition, the four switches can be driven by using two half-bridge gate drivers, without any isolated gate drivers. The proposed converter can be operated in the step-up mode; thus, it can be used in the energy-harvesting applications, such as thermoelectric generation system. Since the proposed converter can be operated in a bidirectional way, it can also be used in the burn-in test applications. To sum up, the structure of the proposed converter is quite simple and very suitable for different applications in the industry.

REFERENCES

[1] Y. Ren, M. Xu, K. Yao, Y. Meng, F. C. Lee, J. Guo, and Y. Ren, "Two-stage approach for 12 V VR," in *Proc. IEEE Appl. Power Electron. Conf.*, 2004, vol. 2, pp. 1306–1312.

[2] Y. Ren, M. Xu, K. Yao, and F. C. Lee, "Two-stage 48 V power pod exploration for 64-bit microprocessor," in *Proc. IEEE Appl. Power Electron. Conf.*, 2003, vol. 1, pp. 426–431.

[3] Y. Ren, M. Xu, Y. Meng, and F. C. Lee, "12V VR efficiency improvement based on two-stage approach and a novel gate driver," in *Proc. IEEE Power Electron. Spec. Conf.*, 2005, pp. 2635–2641.

[4] H. Mao, J. A. Abu-Qahouq, S. Luo, and I. Batarseh, "Zero-voltage-switching (ZVS) two-stage approaches with output current sharing for 48 V input DC-DC converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2004, vol. 2, pp. 1078–1082.

[5] K. I. Hwu and Y. T. Yau, "Resonant voltage divider with bidirectional operation and startup considered," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1996–2006, Apr. 2012.

[6] W. Li, J. Xiao, J. Wu, J. Liu, and X. He, "Application summarization of coupled Inductors in DC-DC converters," in *Proc. IEEE Appl. Power Electron. Conf.*, 2009, pp. 1487–1492.

[7] W. Li and X. He, "A family of interleaved DC-DC converters deduced from a basic cell with winding-cross-coupled inductors (WCCIs) for high step-up or step-down conversions," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1791–1801, Jul. 2008.

[8] C.-T. Tsai and C.-L. Shen, "Interleaved soft-switching buck converter with coupled inductors," in *Proc. IEEE Int. Conf. Sustainable Energy Technol.*, 2008, pp. 877–882.

[9] Z. Zhang, E. Meyer, Y.-F. Liu, and P. C. Sen, "A non-isolated ZVS self-driven current tripler topology for low voltage and high current applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 1983–1990.

[10] Y. Jang, M. M. Jovanovic, and Y. Panov, "Multiphase buck converters with extended duty cycle," in *Proc. IEEE Appl. Power Electron. Conf.*, 2006, pp. 38–44.

[11] D. A. Grant, Y. Darroman, and J. Suter, "Synthesis of tapped-inductor switched-mode converters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1964–1969, Sep. 2007.

[12] S. Ye, W. Eberle, and Y.-F. Liu, "A novel non-isolated full bridge topology for VRM applications," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 427–437, Jan. 2008.

[13] H. Cheng, K. M. Smedley, and A. Abramovitz, "A wide-input–wide-output (WIWO) DC–DC converter," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 280–289, Feb. 2010.

[14] M. Batarseh, X. Wang, and I. Batarseh, "Non-isolated half bridge buck based converter for VRM application," in *Proc. IEEE Power Electron. Spec. Conf.*, 2007, pp. 2393–2398.

[15] K. Nishijima, D. Ishida, K. Harada, T. Nabeshima, T. Sato, and T. Nakano, "A novel two-phase buck converter with two cores and four windings," in *Proc. IEEE Int. Telecommun. Energy Conf.*, 2007, pp. 861–866.

[16] K. Yao, Y. Ren, J. Wei, M. Xu, and F C. Lee, "A family of buck-type DC-DC converters with autotransformers," in *Proc. IEEE Appl. Power Electron. Conf.*, 2003, vol. 1, pp. 114–120.

[17] Z. Yang, S. Ye, and Y.-F. Liu, "A new transformer-based non-isolated topology optimized for VRM application," in *Proc. IEEE Power Electron. Spec. Conf.*, 2005, pp. 447–453.

[18] M. H. Vafaie, E. Adib, and H. Farzanehfard, "A self powered gate drive circuit for tapped inductor buck converter," in *Proc. IEEE Power Electron. Drive Syst. Technol. Conf.*, 2012, pp. 379–384.

[19] P. Xu, J. Wei, and F. C. Lee, "The active-clamp couple-buck converter-a novel high efficiency voltage regulator modules," in *Proc. IEEE Appl. Power Electron. Conf.*, 2001, vol. 1, pp. 252–257.

[20] B.-R. Lin, J.-J. Chen, and F.-Y. Hsieh, "Analysis and implementation of a bidirectional converter with high conversion ratio," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2008, pp. 1–6.

[21] Z. Zhang, W. Eberle, Y.-F. Liu, and P. C. Sen, "A novel non-isolated ZVS asymmetrical buck converter for 12V voltage regulators," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 974–978.

[22] S. Ye, E. Meyer, Y.-F. Liu, and L. X. Dong, "A novel non-isolated two-phase full bridge topology for VRM applications," in *Proc. IEEE Appl. Power Electron. Conf.*, 2008, pp. 24–30.

[23] Z. Zhang, E. Meyer, Y.-F. Liu, and P. C. Sen, "A 1-MHz, 12-V ZVS nonisolated full-bridge VRM with gate energy recovery," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 624–636, Mar. 2010.

[24] H. Jang, T. Ahn, and B. Choi, "New half-bridge dc-to-dc converters for wide input voltage applications," in *Proc. IEEE Int. Telecommun. Energy Conf.*, 2009, pp. 1–6.

[25] L. Gu, K. Jin, X. Ruan, M. Xu, and F. Lee, "A family of switching capacitor regulators," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 740–749, Feb. 2014.

[26] S. Xiong, S.-C. Wong, S.-C. Tan, and C. K. Tse, "A family of exponential step-down switched-capacitor converters and their applications in two-stage converters," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1870–1880, Apr. 2014.

[27] Z. Zhang, W. Eberle, Y.-F. Liu, and P. C. Sen, "A nonisolated ZVS asymmetrical buck voltage regulator module with direct energy transfer," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3096–3105, Aug. 2009.

[28] K. W. E. Cheng, "Tapped inductor for switched-mode power converters," in *Proc. IEEE Int. Conf. Power Electron. Syst. Appl.*, 2006, pp. 14–20.

[29] Z. Yang, S. Ye, and Y. Liu, "A novel nonisolated half bridge DC-DC converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 2005, vol. 1, pp. 301–307.

[30] J. Leyva-Ramos, L. H. Diaz-Saldierna, and M. G. Ortiz-Lopez, "Control of high-step down voltage converters for voltage regulator modules," in *Proc. IEEE Conf. Control Appl. Intell. Control*, 2011, pp. 1–6.

[31] J. A. B. Vieira and A.M. Mota, "Thermoelectric generator using water gas heater energy for battery charging," in *Proc. IEEE Conf. Control Appl. Intell. Control*, 2009, pp. 1477–1482.

[32] Y. Fang, L. Ge, and W. Hua, "Multiple-input dc-dc converter for the thermoelectric-photovoltaic energy system in hybrid electric vehicles," in *Proc. IEEE Vehicle Power Propulsion Conf.*, 2010, pp. 1–5.

[33] I. Laird and D. D. C. Lu, "High step-up dc/dc topology and MPPT algorithm for use with a thermoelectric generator," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3147–3157, Jul. 2013.

[34] B. O'Sullivan, R. Morrison, M. G. Egan, J. Slowey, and B. Barry, "A lossless commutated boost converter as an active load for burn-in application," in *Proc. IEEE Appl. Power Electron. Conf.*, 2001, pp. 953–958.

[35] B. O'Sullivan, R. Morrison, M. G. Egan, J. Slowey, and B. Barry, "A regenerative load system for the test of intel VRM 9.1 compliant modules," in *Proc. IEEE Appl. Power Electron. Conf.*, 2004, pp. 298–303.

[36] K. I. Hwu and Y. T. Yau, "Active load for burn-in test of buck-type dc-dc converter with ultra-low output voltage," in *Proc. IEEE Appl. Power Electron. Conf.*, 2008, pp. 635–638.

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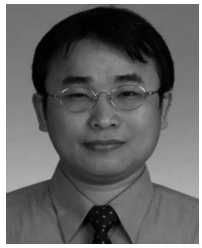

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