A Cell-Level Differential Power Processing IC for Concentrating-PV Systems With Bidirectional Hysteretic Current-Mode Control and Closed-Loop Frequency Regulation

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***Abstract*—This paper describes an integrated power management IC with bidirectional current capability, aimed at compensating differences in output current between series-connected cells in concentrating photovoltaic (CPV) systems. The integrated 3.6-MHz power stage allows building a small-form-factor converter per cell. A hysteretic current-mode controller regulates the bidirectional converter's current to equalize neighboring cell voltages. A phase-locked loop controls the inductor current ripple around the average value to stabilize the switching frequency. The use of hysteretic current-mode control with a novel bidirectional senseFET scheme provides inherent current protection and high reliability. The converter can operate from an input voltage as low as 1.8 V and with an inductor current up to $\pm$1.5 A, while achieving a system efficiency above 90% for current mismatches between cells up to 60%. Measurement results show that the converter maximizes the output power of series-connected CPV cells with mismatched output currents.**

***Index Terms*—Analog integrated circuits, current-mode control, dc–dc power conversion, energy harvesting, integrated circuit design, photovoltaic power systems, power converter, power electronics.**

I. Introduction

EMERGING concentrating photovoltaic (CPV) technology provides an attractive alternative to conventional thin-film and crystalline-silicon (c-Si) PV modules, especially in dry environments with high solar yields. CPV systems use 500–1000$\times$ less semiconductor material than c-Si PV modules, while requiring two-axis mechanical trackers. CPV cells are typically made using multijunction III–V semiconductors having a high responsivity over a broad range of wavelengths from 300–1800 nm, resulting in cell-level efficiencies in excess of 40% [1]. The cell-level power management IC presented in this paper has been optimized for the unique light-guide solar optic (LSO) technology under development by Morgan Solar [2]. The LSO is a low-profile, lightweight waveguide that uses total internal reflection to transfer the direct normal irradiance onto a center-mounted triple-junction cell, as shown in Fig. 1(a). Four LSO prototypes connected to a mechanical tracker are shown in Fig. 1(b) and a more typical large-scale array is shown in Fig. 1(c).

In typical grid-tied CPV systems, dozens of CPV cells are connected in series to form high-voltage strings, and multiple strings are connected in parallel to build modules with desired output ratings. The module voltage/current is regulated by a central inverter in order to achieve maximum power point tracking (MPPT). A relatively large current mismatch between the component cells of a module is common, due to nonuniform cell optical characteristics, misalignment in the concentrators, electrical and thermal parameter variations, nonuniform aging, as well as partial shading. The more complex cell structure compared to c-Si PV, as well as the need for optical concentration and mechanical tracking, implies that CPV systems suffer more from small, randomly distributed mismatches. At the same time, since they are installed in near-ideal harvesting locations such as deserts, the partial shading problem is limited to dusk and dawn, when nearby trackers may cast a shadow on their neighbors.

As a result, the harvested power in a series-connected CPV system can be reduced by up to 30%. A sample measurement of normalized short-circuit currents for six individual CPV cells over 192 h is shown in Fig. 2(a) [3]. The resulting maximum mismatch in both the short-circuit current I_{sc} and open-circuit voltage V_{oc} for the six cells is plotted versus time in Fig. 2(b). It is clear from Fig. 2(b) that current mismatches are more significant than voltage mismatches in practical CPV systems. The objective of this paper is to demonstrate a low-cost cell-level power management IC with fully integrated bidirectional hysteretic current control to alleviate the energy loss that occurs due to current-domain mismatches in CPV systems.

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II. Cell-Level Power Management

In order to mitigate the negative impact of differences in output power between PV modules, submodules, and cells on

Fig. 1. (a) Ray-trace simulation of the low-profile LSO. Each packaged LSO includes an optical concentrator and a multijunction cell. (b) Four LSO prototypes installed on a mechanical tracker. (c) Large-scale LSO array on a dual-axis mechanical tracking system.

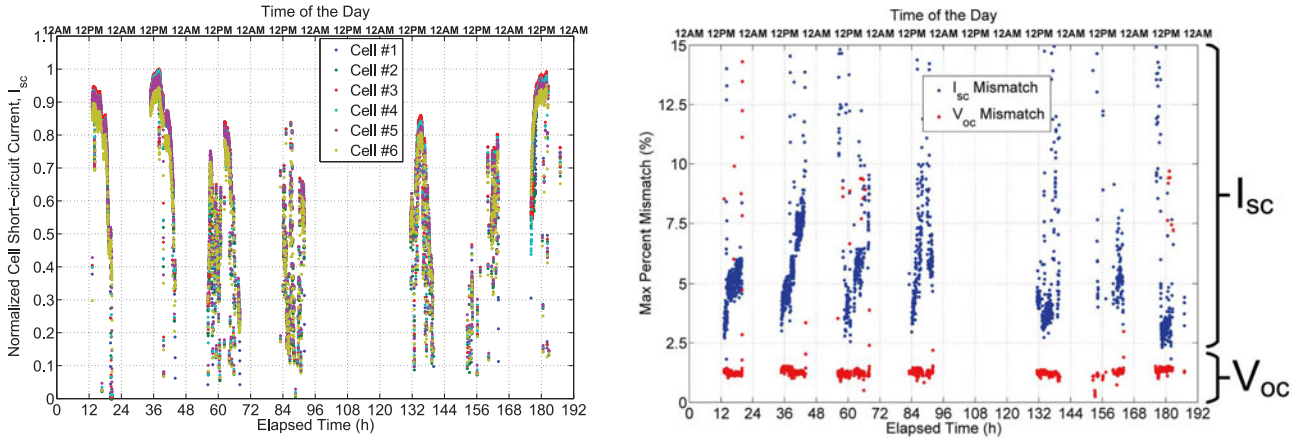


Fig. 2. (a) Measured short-circuit current (normalized), and (b) maximum percent mismatch in short-circuit currents and open-circuit voltages over time, for six LSO cells without any distributed dc–dc converters.

the total harvested output power of a PV system, many efforts have been documented in the literature regarding distributed MPPT (DMPPT) at various levels of granularity [4]–[10]. Theoretical studies show that DMPPT at the cell-level granularity yields the highest energy [11], [12]. In contrast to c-Si cells, whose harvested power does not increase significantly beyond the substring granularity level [12], the cell-level entities in CPV systems produce much greater power (≈10 W) and are more likely to be mismatched. Thus, the improvements from going to cell-level power processing in CPV systems are expected to be higher as well. Furthermore, when implementing DMPPT at the cell level, microinverters as in [9] become impractical. A conventional implementation of cell-level DMPPT using dc–dc converters is shown in Fig. 3(a). In this case, the dc–dc converters are known as power optimizers or microconverters, and they regulate their input voltage to ensure that each cell operates at its respective MPP, regardless of the presence of mismatches in the system. However, as the cost of PV cells has fallen well below \$1/W, it is very challenging to cost-effectively deploy the conventional power-optimizer architecture, as shown in Fig. 3(a), at the cell level of granularity. This is mainly due to the high efficiency requirement (>95%), since the efficiency of the power optimizers directly affects the system efficiency. Furthermore, the additional components should cost no more than the amount of additional power they help harvest. In order to balance the added system cost with the improved performance and robustness, the complete dc–dc DMPPT system, including the IC, the passive components, and the packaging, should cost less than \$0.1/W of peak generated PV power.

An alternative and arguably more cost-effective distributed power management approach is shown in Fig. 3(b). This concept is known as *partial* or *differential power processing*, or Δ-conversion [13]–[26]. Various topologies have been proposed [26], ranging from buck-boost converters [13]–[15], [17], [21], [25] or switched-capacitor converters [16], [20], [24] operating between neighboring PV modules, submodules or cells, to buck–boost converters or isolated flyback converters operating between submodules and the complete string or an individual port [19], [22], [23]. Control methodologies can be subdivided between applying voltage equalization between neighboring (sub) modules or cells [14]–[16], [18], [20], [24], and applying MPPT to individual (sub) modules. In the latter case, a distinction can be made between applying central

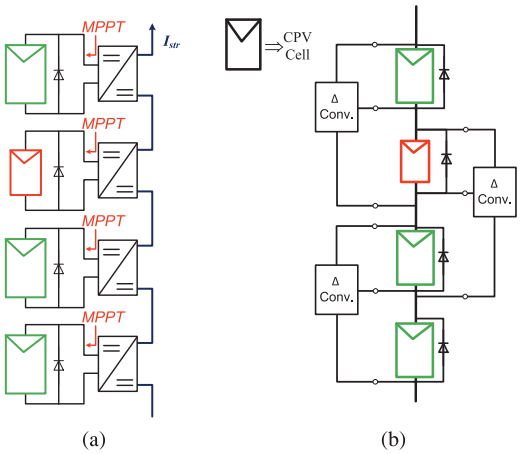


Fig. 3. (a) Conventional dc–dc power optimizer, where each converter performs MPPT locally and requires the same power rating as the cell. (b) Δ-converter architecture with voltage equalization; for the same system efficiency, each converter can have a lower power rating and efficiency.

[13] or distributed control [17], [19], [21], [22], [25]. The highest granularity examples are a hybrid inductive-capacitive converter between neighboring groups of six c-Si cells [20] and a capacitive converter using the implicit cell diffusion capacitances to equalize cell voltages in a string [24]. The utility of the Δ-conversion concept in cost-sensitive CPV applications was demonstrated in [3] at the system level with off-the-shelf components, whereas this paper focuses on monolithic integration of said design and the associated challenges. In contrast to [20], the inductor current is explicitly controlled in this design using bidirectional hysteretic current-mode control (HCMC) with closed-loop frequency regulation, as discussed in Section IV. Precise knowledge of the current carried by each Δ-converter enables more detailed system monitoring and the ability to intelligently control the converters in situations where the compensation currents become too low or too high (see Section IV). Furthermore, our design incorporates all necessary supply generation and protection functions on-chip, unlike the external regulators used in [20]. The converter presented in [24] does not use dedicated integrated circuits, and requires the power stages to process part of the bulk system power as well, as opposed to this paper and [20], where only power mismatches are processed.

Since the Δ-converters only process, on average, the differences between corresponding cell currents and the string current, they have a reduced power rating and a lower efficiency requirement compared to conventional dc–dc optimizers [13]–[26]. When the cells in the system are completely matched, the Δ-converters process no power (and can be switched off), resulting in near-zero losses. A more detailed system configuration is shown in Fig. 4(a), where each Δ-converter is lumped with one CPV cell for ease of packaging. There are two possible ways to bundle and associate the Δ-converters with the corresponding LSOs, which leaves either the top or the bottom cell of the string without a converter, as in Fig. 4(a) where the bottom cell is left unbundled. A string of n cells, therefore, requires $(n-1)$ active converters, and an additional wire per bundled unit, compared

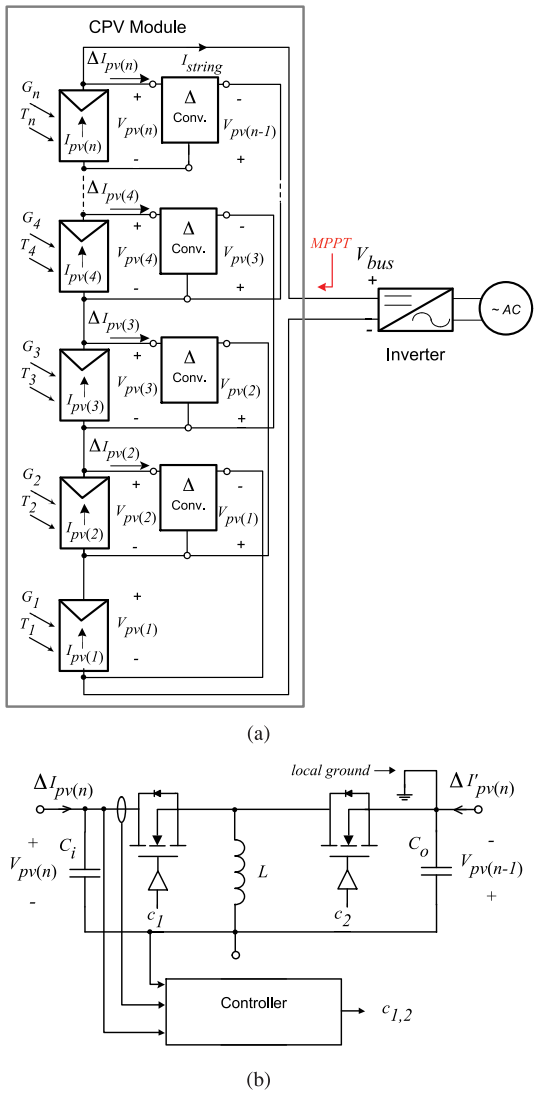
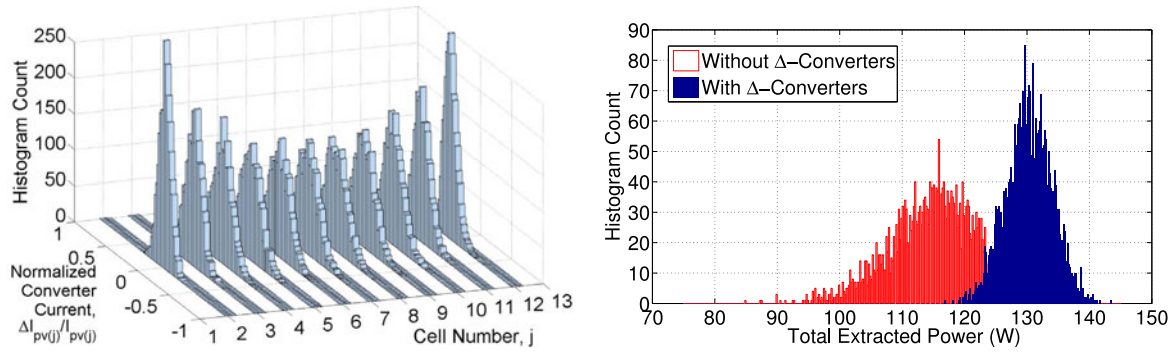


Fig. 4. (a) Architecture for a grid-tied distributed Δ-converter system showing how one converter is bundled with each LSO. G_n and T_n represent the local irradiance and temperature, respectively, for each LSO. (b) Implementation of the Δ-converter using a half-bridge topology, allowing bidirectional power flow.

to that in Fig. 3(a). Note that in practical systems, all LSOs will likely be bundled with a converter for simplicity, and the unused converter in an assembled string will be kept permanently off.

Unlike the conventional approach, the Δ-converters need to handle bidirectional power flow, which is achieved most simply with a synchronous half-bridge topology, configured as a buck–boost converter, as shown in Fig. 4(b). While the duty cycle of each converter can be controlled to place each cell at its MPP, the DMPPT process in a Δ-conversion system is inherently more complex than in the conventional power optimizer system, since the converter currents have a high degree of coupling. While performing DMPPT without a central controller is possible [17], [19], [21], [22], [25], neighbor-to-neighbor communication is required, which adds to the system cost and impacts reliability. Moreover, previous work has demonstrated that applying voltage equalization on the submodule level in c-Si systems can



(a) (b)

Fig. 5. (a) Δ-converter current distributions. (b) String power distributions with and without Δ-converters, with uniform irradiance and 10% variation in I_{sc} [3].

recover up to 98% of the true MPP power, even in the presence of worst-case MPP voltage variations due to irradiance or temperature mismatches [23]. Therefore, voltage equalization between neighboring CPV cells is applied in this paper, similar to [14]–[16], [18], [20], [24]. The external MPPT controller [such as the inverter in Fig. 4(a)] regulates the string current I_{string} (or the voltage, V_{bus}) to achieve maximum power. This results in the cells operating near their MPP voltage V_{mpp} assuming their voltage-domain parameters are matched. Given that the V_{mpp} of different cells (which is a linear function of their V_{oc}) vary by only 1% throughout most of the day, as measured in Fig. 2(b), the added complexity of performing full DMPPT, as opposed to voltage equalization, is not justified in this particular system [3]. Furthermore, voltage equalization causes the elimination of multiple local maxima in the power versus voltage characteristics of the string, giving rise to a unique string MPP. This reduces the complexity of the external MPPT controller, since a simpler MPPT algorithm can be used.

III. Δ-Converter System Challenge: Current Cascading

Finding the actual current distribution in a string of Δ-converters under various irradiance conditions is complex due to the phenomenon known as *current cascading*. Assuming that the jth converter has an efficiency of η_j, its current is given recursively by (1) from [3]

$$\Delta I_{\mathrm{pv}(j)} = \left(1 + k_j \frac{V_{\mathrm{pv}(j)}}{V_{\mathrm{pv}(j-1)}}\right)^{-1} \times \left(I_{\mathrm{pv}(j)} - I_{\mathrm{pv}(j-1)} + \Delta I_{\mathrm{pv}(j-1)} + k_{j+1} \frac{V_{\mathrm{pv}(j+1)}}{V_{\mathrm{pv}(j)}} \Delta I_{\mathrm{pv}(j+1)}\right)$$

$$\text{where } k_j = \begin{cases} \eta_j, & \text{if } \Delta I_{\mathrm{pv}(j)} \geq 0 \\ \frac{1}{\eta_j}, & \text{if } \Delta I_{\mathrm{pv}(j)} < 0. \end{cases} \quad (1)$$

Note that for the bundling scheme shown in Fig. 4(a), the bottom cell ($n = 1$) has no associated converters, and therefore, $\Delta I_{\mathrm{pv}(1)} = 0$. In this paper, an averaged model of the dc–dc converters and CPV cells is used to obtain the steady-state operating points using transient simulations. The current-dependent efficiency of each converter is modeled, and I_{string} is set using an external MPPT block.

As each converter transfers current to its neighbors in order to equalize the voltages, each successive Δ-converter has a larger current variability, leading to the phenomenon termed *current cascading*. A statistical system simulation for $n = 12$, reflecting the intended string length in the Morgan Solar system targeted by this paper, was run in `Simulink` to illustrate the current cascading phenomenon [3]. The simulation was run with a fixed irradiance input for each of the 12 LSOs, and repeated 3000 times. In each simulation run, the LSOs were randomly selected from a batch of cells with a normal distribution in I_{sc} in order to simulate process variations. The I_{sc} parameter was normally distributed with a standard deviation of $\sigma_I/\mu_I = 10\%$. Although the chosen quantity is comparatively large in the context of PV systems, this was the worst-case variation expected from the target system (including not only triple-cell junction mismatches, but also optical and mechanical parameter variations in the CPV system), and therefore defined the design parameters. The resulting statistical distribution of converter currents $\Delta I_{pv(j)}/I_{pv(j)}$ is shown in Fig. 5(a).

The quantity $\Delta I_{pv(j)}/I_{pv(j)}$ is a measure of the relative current spread in the converters, which is useful for designing the current-limiting strategy and sizing the power stage based on economic considerations. The simulation shows that the spread in $\Delta I_{pv(j)}/I_{pv(j)}$ is lowest at the top and bottom of the string and gradually increases toward the middle of the string. The middle Δ-converters are, therefore, more likely to carry substantially higher currents over their lifetime, and have reduced reliability. For some rare cases, where $\Delta I_{pv(j)}/I_{pv(j)} > 0.5$, the Δ-converters can carry more than half of the current as the associated CPV cell. High currents lead to low efficiency and reduced energy yield. The Δ-converter concept is, therefore, generally more suitable for systems having relatively small statistical variations, such as CPV systems. The statistical distribution for the total extracted power with and without the converters added to the system is shown in Fig. 5(b), which clearly demonstrates the benefit of the Δ-conversion scheme. Despite the limited efficiency of the dc–dc converters, with $\eta_{peak} \approx 90\%$ (similar to Fig. 16), the mean power μ_P increases by 13% from 115 to 130 W, while the spread σ_P/μ_P is reduced by 52%. While the numerical results will certainly vary as function of the chosen string length (n) and the coefficient of variation (σ_I/μ_I), these results are used to set the experimental Δ-converter power rating based on the expected parameters of the LSOs.

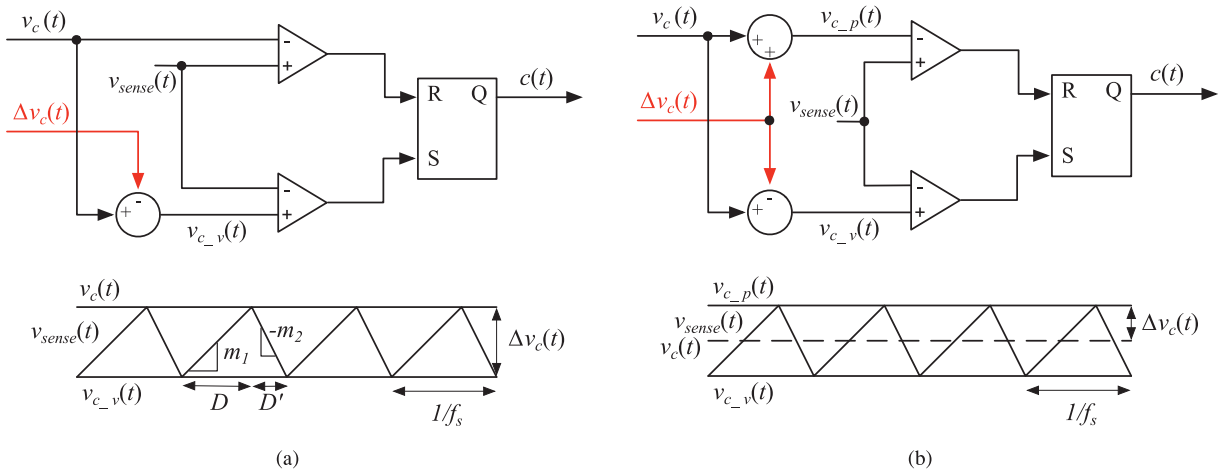


Fig. 6. Current-programmed controllers and ideal switching waveforms for (a) peak HCMC with fixed hysteretic window, and (b) ripple HCMC.

IV. Current-Mode Control Schemes and Frequency Regulation Schemes

Due to the cost-sensitive nature of PV generation, the power management IC must be implemented in a mature low-cost Bipolar-CMOS-DMOS (BCD) technology, with the highest possible switching frequency in order to reduce the size of the passive components. The voltage equalization scheme can be implemented at a very low cost with simple duty-cycle control. However, operating a large coupled Δ-converter system without explicitly controlling the inductor currents leads to several issues:

1) the inductor must be oversized to handle large peak currents during transients;
2) the lack of cycle-by-cycle current protection on both switches is a major reliability concern, especially in this industrial application with a targeted lifetime above ten years;
3) the system does not have the capability of operating in a constant-current mode to limit the total processed power under large shading gradients.

For these reasons, the proposed IC implements an inner current control loop within the voltage equalization scheme. This paper presents the first on-chip implementation of a particular form of current-mode control, which is well suited to this CPV application, as described in the following sections.

A. Hysteretic Current-Mode Control (HCMC)

HCMC is used to eliminate the need for slope compensation by relying on the principle of self-oscillation. As with peak and valley current-mode control, there are two natural variations of HCMC: peak and valley HCMC. In the peak HCMC implementation shown in Fig. 6(a) [27], there is no need for an external clock. The valley current command $v_{c\_v}(t)$ is simply derived from the peak current command $v_c(t)$ using a fixed offset Δv_c:

$$v_{c\_v}(t) = v_c(t) - \Delta v_c. \tag{2}$$

Unlike peak current-mode control, the switching frequency f_s is no longer fixed and given by

$$f_s = \frac{m_1 D}{\Delta v_c} = \frac{m_2 D'}{\Delta v_c}. \tag{3}$$

In contrast, valley HCMC works by simply treating $v_c(t)$ as the valley command, and generating the peak current command $v_{c\_p}(t)$ from

$$v_{c\_p}(t) = v_c(t) + \Delta v_c. \tag{4}$$

In either case, the offset Δv_c can be designed to achieve a desired f_s only for a known L, and fixed V_{in} and V_{out}. For systems having a wide range of V_{in} and/or V_{out}, the variation in f_s leads to significant stability and electromagnetic interference issues.

Ripple HCMC control is shown in Fig. 6(b). In this case, the offset $\Delta v_c(t)$ is both added to and subtracted from the current command $v_c(t)$ to obtain the peak and valley current commands, $v_{c\_p}(t)$ and $v_{c\_v}(t)$, respectively [28], [29]. As with peak and valley HCMC, this scheme does not require slope compensation. The circuit complexity is slightly increased with one more summing circuit. However, $v_c(t)$ becomes proportional to the average inductor current, which is highly desirable. An alternative version of ripple HCMC was implemented using the sensed capacitor current in both analog [30] and digital [31] forms.

B. Frequency Regulation Schemes for HCMC

HCMC eliminates the need for slope compensation at the expense of variable frequency operation. In this section, a frequency regulation mechanism is reviewed that can be applied to all three HCMC schemes: a phase-locked loop (PLL), as shown in Fig. 7. The diagram shows the outer voltage loop, which is used to regulate the output voltage $v(t)$ by controlling the inductor current command $v_c(t)$. H and R_f are the output sensing gain and inductor current sensing gain, respectively. A PI compensator $G_c(s)$ is usually sufficient to stabilize the outer loop, since current-mode converters exhibit simple first-order dynamics in the frequency range of interest.

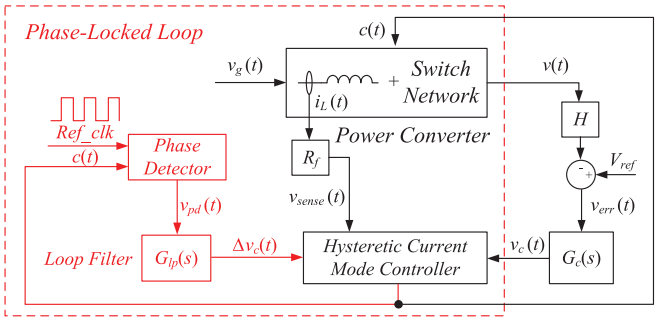


Fig. 7. Conceptual PLL-based frequency regulation techniques, which can be applied to any of peak, valley or ripple HCMC.

Using the PLL, $\Delta v_c(t)$ is adjusted to maintain a fixed frequency. The gating signal $c(t)$ is compared to the reference clock *Ref_clk* by a phase detector and the error is fed to a loop filter. The output of the loop filter is used to control the hysteretic window through $\Delta v_c(t)$ [29], [32], [33]. Since f_s is only locked during steady state, this method is commonly referred to as a quasi-fixed frequency technique. The operation of the frequency regulation loop is very similar to a standard PLL, where the power converter behaves as a voltage-controlled oscillator, with $\Delta v_c(t)$ acting as the control voltage. The small-signal modeling and detailed system-level evaluation of HCMC with frequency regulation is covered in [34].

The PLL scheme of Fig. 7, as well as the voltage regulation loop, can be implemented in either analog or digital form. This leads to an array of possible mixed-signal implementations, with various performance tradeoffs and challenges, especially for on-chip implementation. There is also a class of hysteretic voltage-mode controllers that incorporate switching frequency regulation [35]–[37]. These hysteretic controllers operate on the small output voltage ripple, rather than the relatively large inductor current ripple used in HCMC.

To the best of the authors' knowledge, the first frequency control scheme for HCMC was demonstrated using a PLL approach on ripple HCMC by [28]. Another PLL approach, combined with peak HCMC, was outlined in [38]. Both of these works have fully analog realizations. More recently, [30] demonstrated another off-chip frequency regulation mechanism based on a frequency-to-voltage converter applied to a modified form of ripple HCMC.

V. Power Management IC Implementation

The simplified architecture of the CPV IC is shown in Fig. 8 and the main system specifications are listed in Table I. The IC performs two major functions: 1) the controller actively redistributes the cell currents to equalize the voltages of two neighboring CPV cells (i.e., to make $V_{mid} = V_{pv}/2$), without requiring any form of central control or communication, and 2) the IC provides all the protection, monitoring, and auxiliary power supply functions, since it is directly supplied from the CPV cell pair without any external power available. The specifications of the triple-junction CPV cell under nominal conditions are given in Table I. The IC is capable of starting up with a supply voltage as low as $V_{pv} = 1.8$ V, where V_{pv} is the voltage across the two CPV cells to which the IC is connected. This low-voltage condition may occur at startup, where one of the cells is bypassed through the anti-parallel diode due to a large difference between the cell output current and the string current, as shown in Fig. 3(b).

The internal power supply scheme is shown in Fig. 9. An on-chip auxiliary boost converter provides V_{aux}, a regulated 10-V supply for the main-stage gate drivers, as well as two linear voltage regulators (LVR) that power the controller and internal protection blocks. An input-supply switching scheme enables the LVRs to dynamically switch their input supply from V_{aux} to V_{pv} when V_{pv} is greater than 4.7 V to reduce power consumption. Burst-mode control is implemented in both the auxiliary and main-stage converters to improve the light-load efficiency. The main converter uses a synchronous half-bridge power stage with 12-V-compatible 300-mΩ n-channel DMOS devices switching at up to 4 MHz. The 10-V drive voltage allows the high-side switch to operate without the need for a bootstrap capacitor, since the driver can be referenced to ground. This reduction in the number of external components is beneficial from both volume/cost and reliability perspectives. The choice of 10 V also provides a suitable tradeoff between increasing the drive voltage (and reducing switch sizes), and leaving sufficient voltage margin for the 12-V-compatible devices to satisfy reliability requirements. Under nominal conditions, the high-side switch, therefore, has an effective drive voltage of $V_{gs} = 10\text{ V} - 2(2.5\text{ V}) = 5$ V, while the low-side switch operates with $V_{gs} = 10$ V. The two power transistors are sized to achieve the same on-resistance in the worst-case corner ($V_{pv} = 6$ V) despite their different drive voltages, so that startup can be guaranteed under all conditions.

A. Control-Loop Architecture and Design

The HCMC scheme leads to a self-oscillating power stage, avoiding the need for slope compensation. The simplified control architecture is shown in Fig. 10. Using a digital compensator has many well-known benefits, including robustness to temperature and process variations, elimination of off-chip compensation components, and programmable compensator coefficients. The digital voltage loop compensator $G_c(z)$ generates the digital average current command $I[n]$ in order to perform voltage equalization. This corresponds to $V_{mid} = V_{pv}/2$, where V_{pv} is the voltage across two CPV cells. The voltages V_{mid} and V_{pv} are sampled using a low-power windowed analog-to-digital converter (ADC), as described in Section V-B. The average current command is converted into an analog current I_L using a 9-bit current-mode flash digital-to-analog converter (DAC). The DAC uses a combination of 4-bit binary-weighted and 5-bit thermometer-coded current sources to achieve the necessary linearity in this application.

The frequency regulation loop has been implemented in the analog domain. The integrated PLL adjusts Δi_L such that the switching frequency f_s equals reference frequency, $f_{ref} = 3.6$ MHz, independent of the chosen inductance L or variations in input/output voltages. The reference frequency is generated using an internal RC oscillator. The PLL includes a

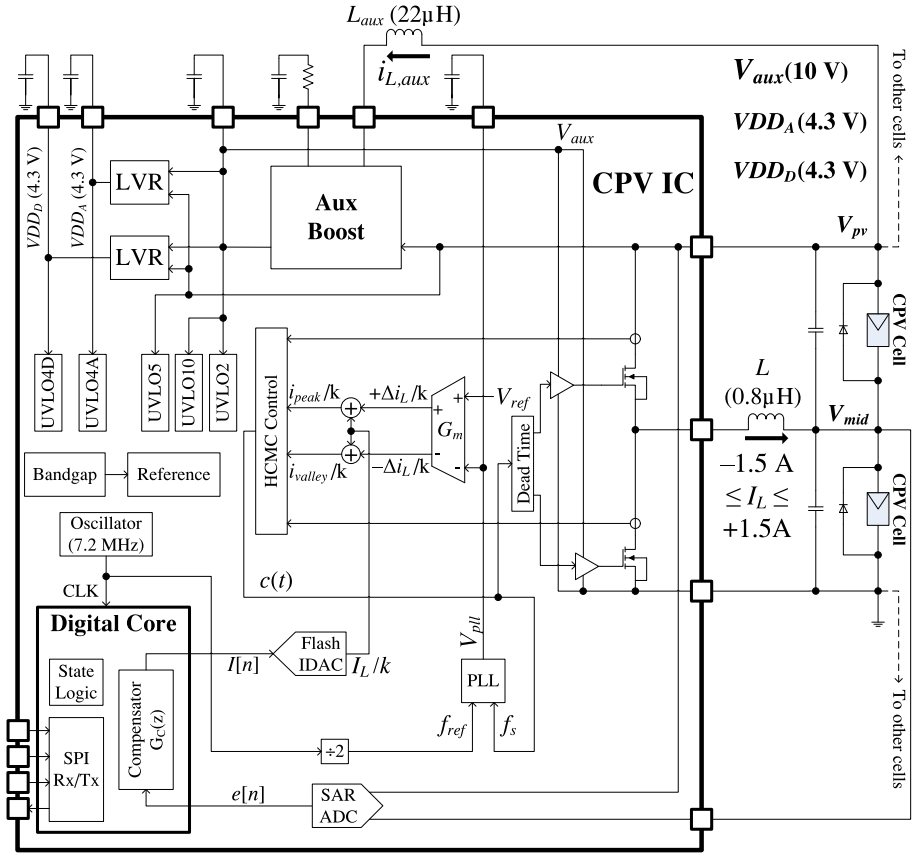


Fig. 8. CPV IC system architecture with digitally-controlled Δ-converter and on-chip auxiliary power supply.

TABLE I
Δ-CONVERTER PARAMETERS

Parameter	Value	Unit
CPV Cell Open-circuit voltage, V_{oc}	3.0	V
CPV Cell Short-circuit current, $I_{\rm sc}$	3.2	A
CPV Cell MPP voltage, $V_{m\,pp}$	2.5	V
CPV Cell MPP current, $I_{\rm m\,pp}$	3.0	A
Fabrication Process	1-μm BCD	
Chip Size	2.7×3.7	$\rm mm^2$
Closed-loop Switching Frequency, f_s	3.6	MHz
Control Mode	Hyst. Current-Mode	
Operating Voltage at V_{pv}	1.8–6.0	V
Max. Average Inductor Current, I_L	±1.5	A
Auxiliary Boost Voltage, V_{aux}	10	V
Power FET On-resistance, R_{on}	300	mΩ
Main Converter Inductance, L	0.8	μH
Auxiliary Boost Inductance, $L_{\rm aux}$	22	μH

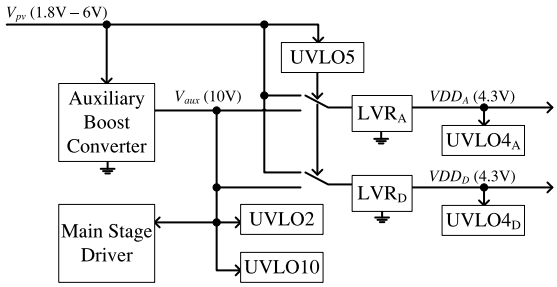


Fig. 9. On-chip power-supply scheme.

phase-detector and charge-pump circuit and a loop filter. The PLL bandwidth is designed to be significantly higher than that of the voltage loop, in order to avoid interactions. Similar to Fig. 6(b), the peak and valley current references are generated by adding and subtracting the ripple current to and from the average current command, respectively, such that $i_{peak} = I_L + \Delta i_L$ and $i_{valley} = I_L - \Delta i_L$. The switching signal $c(t)$ is generated based on comparing the sensed inductor current with i_{peak} and i_{valley}, which are defined for both positive and negative I_L as shown in Fig. 11.

Unlike [33], [39], a bidirectional HCMC with frequency regulation and a digital voltage loop is used in this paper, with digitized I_L. With the optional implementation of wireless or power-line communication (PLC) in the future, the sampled value of I_L for each converter can be used on system level to monitor health and optimize efficiency. A stability analysis of the voltage loop in the context of the highly coupled Δ-conversion system is inherently complex, but has been addressed in [40] and thus is not discussed here.

One of the main challenges of implementing HCMC beyond several megahertz in a mature BCD process is the high-bandwidth requirement for both peak and valley current sensing.

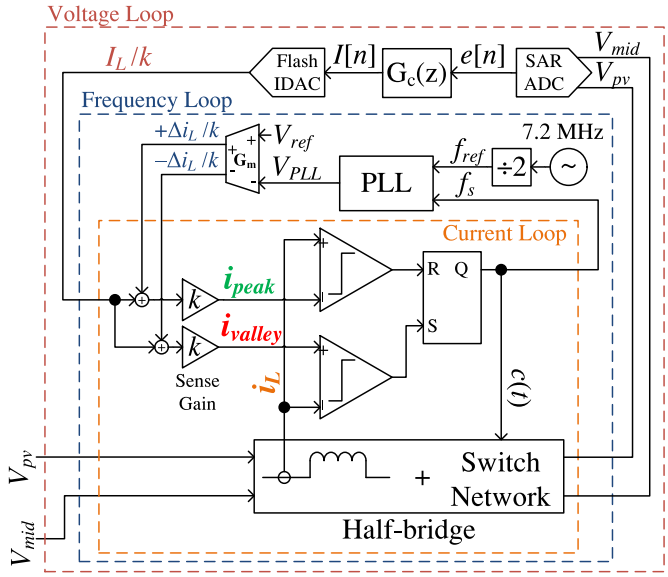


Fig. 10. Control-loop architecture.

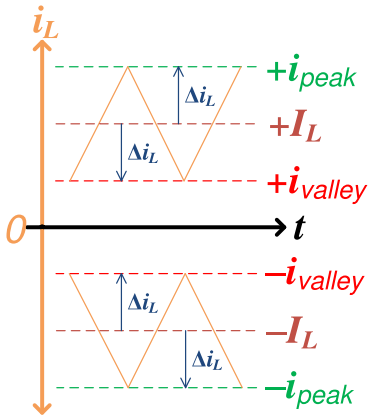


Fig. 11. Peak and valley current for positive and negative I_L.

This is further complicated by the need for bidirectional current sensing. A simplified diagram of the sensing scheme is shown in Fig. 12. The power stage includes the two power transistors, as well as four senseFET transistors, used for bidirectional operation. The powerFET to senseFET ratio k is taken to be 876.

Current sources i_{peak} and i_{valley} are fed to one of the two senseFETs matched to each power MOSFET, depending on the direction of i_L. The direction bit is used for two purposes: 1) it directs i_{peak} and i_{valley} into the appropriate senseFET transistor and 2) it configures the input of the two high-speed comparators using an analog multiplexer. The comparators are blanked for $t_{blank} = 30$ ns following the power stage switching instant (known as leading-edge blanking). During the blanking time, the analog multiplexers disconnect the comparator inputs from the power stage for reliable operation. Moreover, a small offset is applied at the comparator inputs to ensure known states as well as fast recovery following the blanking time.

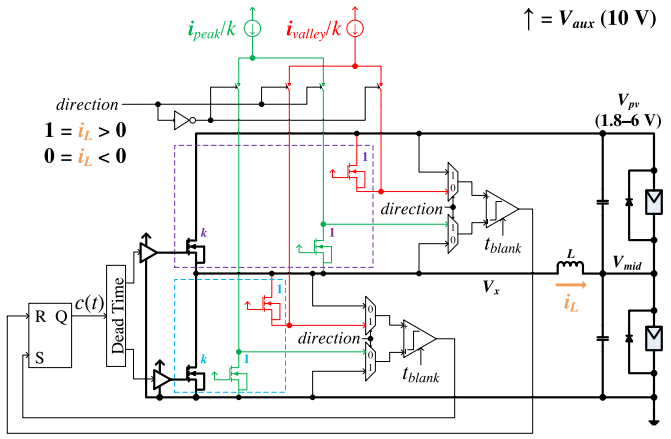


Fig. 12. Bidirectional control-loop implementation.

The current sources i_{peak} and i_{valley} always have the same direction, and zero crossings of i_L are avoided for low I_L values (which would lead to $i_{peak} > 0$, $i_{valley} < 0$ for small positive I_L), since this would require changing the comparator inputs at the speed of f_s. Instead, burst mode is employed when I_L is low, and the converter only switches to continuous conduction mode (CCM) when the average current has exceeded a predefined limit. Burst-mode and CCM operation and transitions between the two modes are described in further detail in Section VI.

B. Analog-to-Digital Converter

The ADC used for the voltage loop utilizes a differential successive-approximation register (SAR) topology to resolve a window of 3 bits (signed) of differential voltage, as shown in Fig. 13(a). The inputs to the ADC are V_{pv}, and V_{mid}. The ADC quantizes their difference, $V_{error} = V_{pv}/2 - V_{mid}$, in 50-mV bins to produce $e[n]$. The ADC has an operating clock of 7.2 MHz and uses 16 cycles to complete a conversion. As such, the effective sampling rate is 450 kHz. The architecture of the differential SAR is based on using two 3-bit switched capacitor arrays to track, hold and bit-cycle each input. A sample conversion is shown in Fig. 13(b), demonstrating the processing steps of a full-range differential voltage with the associated switches (S_{a3-0}, S_{b3-0}, S_{c1-0}, S_{d1-0}) and node voltages ($V_{sa} - V_{sb}$, V_{comp}). In particular, switches S_{a3} and S_{b3} are used to offset the zero error bin to create a mid-tread quantization. Two cycles are used for each comparison to allow for greater settling time for the reference, which is possible due to the high-operating frequency. During the hold operation, a voltage of $V_{x(k)} = 4.3 - V_{in(k)}$ is produced on each comparator input, which creates a positive common-mode voltage regardless of the sign of the input voltages. During bit-cycling, in the first two cycles, the sign of the signal is determined by comparing which capacitor array sampled the smaller held voltage. In the next six cycles that capacitor array is switched in successive approximation to create the condition that $V_{xa} = V_{xb}$, while the opposing array is held constant. To facilitate a low-impedance input and low offset, the CPV voltages are sampled through a BJT common-emitter buffer. A reference voltage of 0.2 V is buffered through a two-

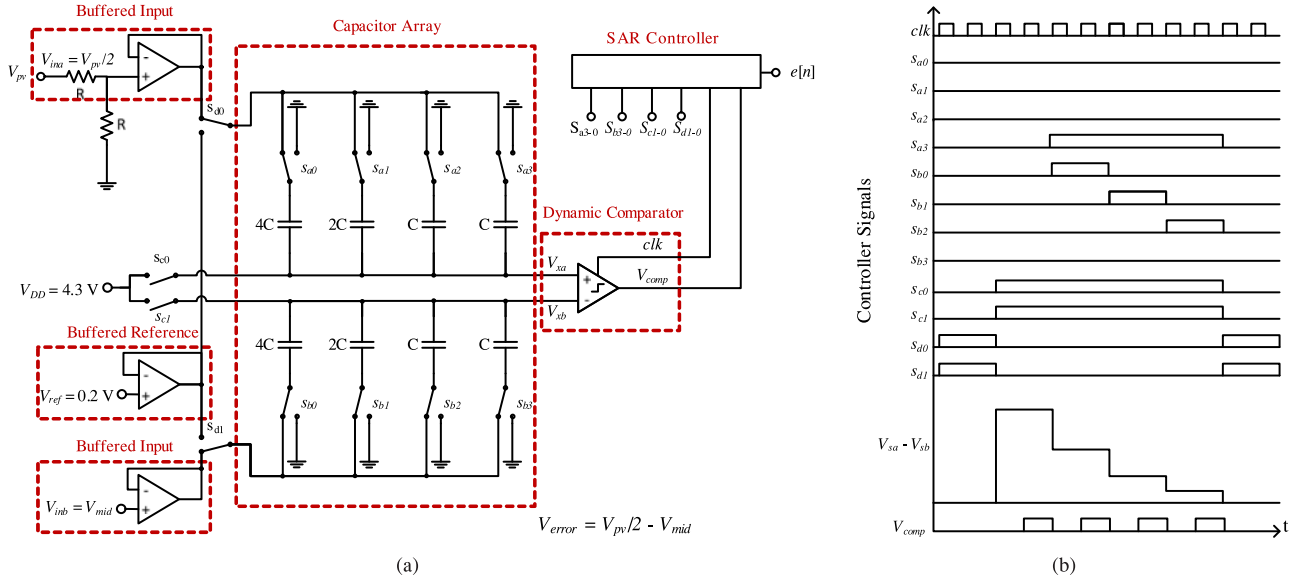


Fig. 13. Differential A-D converter: (a) block diagram; (b) sample conversion waveform.

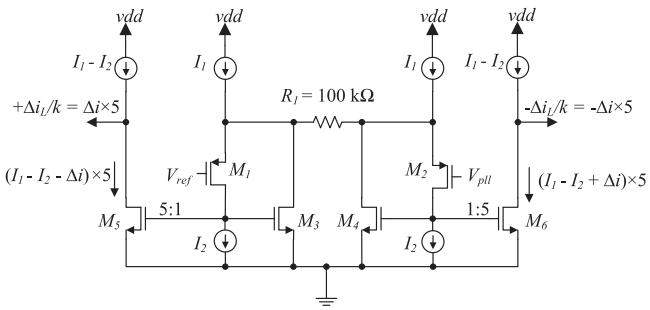


Fig. 14. Transconductor architecture.

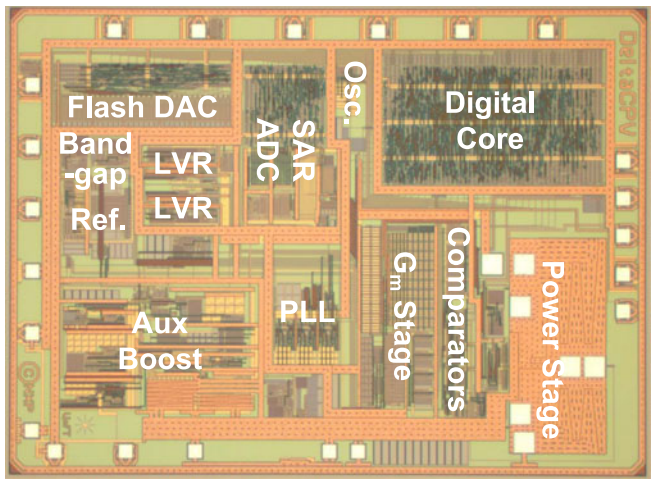


Fig. 15. Chip micrograph. The die measures 2.7 mm × 3.7 mm.

stage op-amp followed by a PMOS pass transistor, which is a conventional linear regulator configuration, allowing for flexible reference levels. A dynamic comparator is created using a preamplifier, two-stage positive feedback, and an SR latch. A digital SAR controller is implemented using a finite state machine to control the switches for the track, hold and bit-cycling operations.

C. Transconductor

A transconductor is used in the frequency loop, as shown in Fig. 8, to produce the ripple inductor current command $\Delta i_L/k$ from the output of the PLL V_{pll}. The architecture of the transconductor is shown in Fig. 14 [41]. The transconductance G_m is given by

$$G_m = \frac{\Delta i}{V_{\text{ref}} - V_{\text{pll}}} = \frac{1}{R_1}. \tag{5}$$

The transconductor has a PMOS input pair, so that it will produce the maximum Δi_L and minimum switching frequency when $V_{pll} = 0$ V, before the PLL is turned ON. This ensures that switching-frequency-dependent blocks, such as the current-sensing circuit, are clocked below their maximum operational frequency before the PLL is locked.

VI. Experimental Results

The IC was implemented in NXP's 1-μm automotive BCD-SOI process, as shown in Fig. 15. By taking advantage of the relaxed efficiency requirement of the Δ-converter, the power stage has been implemented with relatively high-ohmic switches, which reduces the area, and thus cost, of the IC [2].

A. Open-Loop Efficiency of the Power Stage

The measured open-loop efficiency of the main power stage under different voltages and switching frequency conditions is

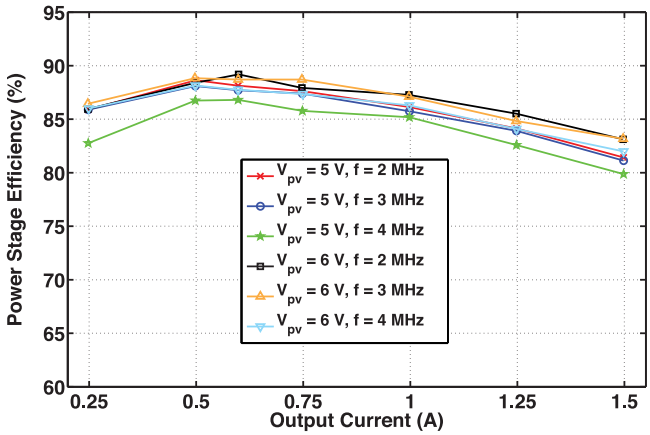


Fig. 16. Measured open-loop main converter efficiency in CCM with $V_{mid} = 0.5V_{pv}$.

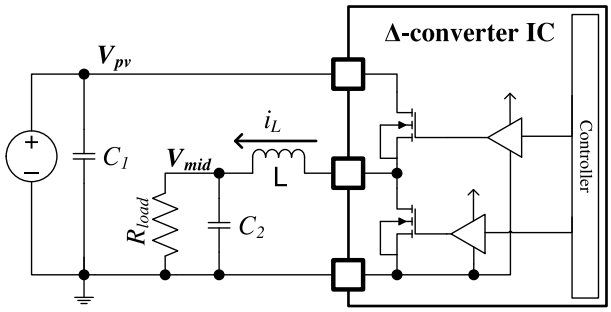


Fig. 17. Main converter test setup.

shown in Fig. 16. The main power stage has a peak efficiency of 89% and a maximum current of 1.5 A.

B. Verification of Converter Operation

In order to test the IC under consistent and controlled operating conditions, the converter was installed in a buck converter setup, with a voltage source at the V_{pv} node, and a resistive load at V_{mid}, as shown in Fig. 17. IC operation in this setup is similar to the case where the lower of the CPV cells is underperforming, so that the converter will supply current to the V_{mid} node. Clearly, it is also possible to install the IC in a boost setup, with a voltage source at V_{mid} and a load at V_{pv}, corresponding to an underperforming top cell, where the converter will draw current from the V_{mid} node. Since the two setups are functionally very similar, only results from the buck setup will be presented in this section for the sake of brevity.

The measured startup process of the internal supplies is shown in Fig. 18. When the input voltage is low, the auxiliary boost converter relies on open-loop, oscillator-based operation to charge its output and thereby enable the internal LVRs. Subsequently, the control loop of the auxiliary boost is activated and the 10-V rail fully regulated. All supply rails are fully regulated within 6 ms.

The startup of the main converter is shown in Fig. 19(a). The converter is first operated with an open-loop 50% duty cycle for

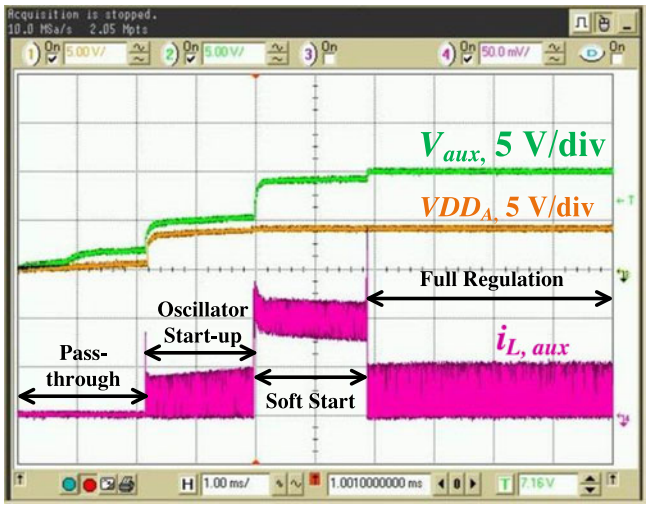
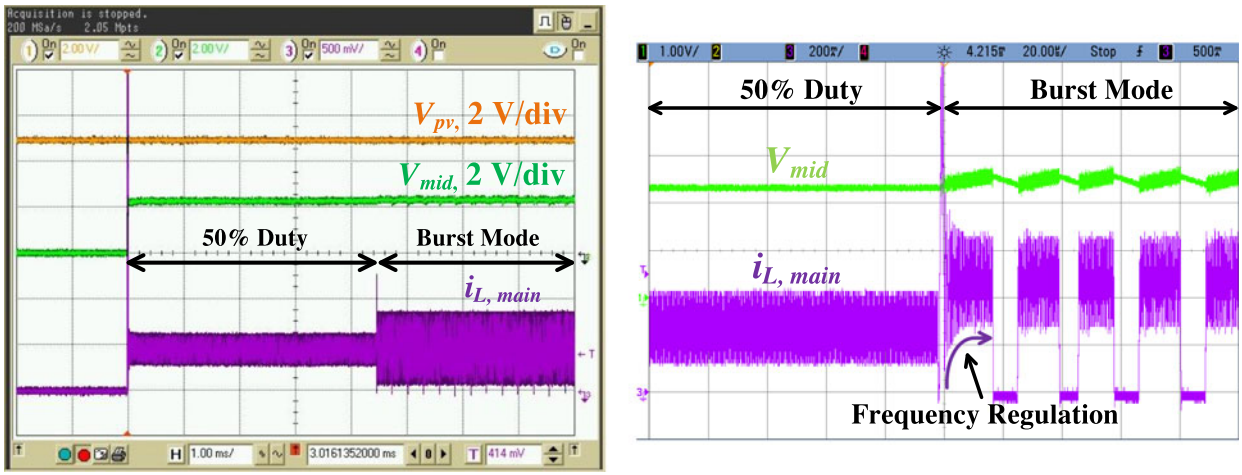


Fig. 18. Measured startup process of the internal supplies.

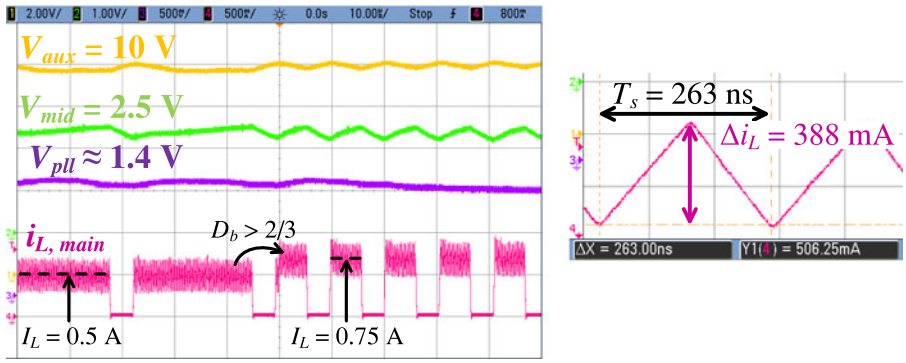
coarse regulation, which brings the operating conditions close to nominal and eases the requirements of the current control loop. The inrush current that occurs when the converter switches ON is self-limited by the combination of R_{on} of the power switches and the inductor's parasitic series resistance, both of which are relatively high in this design. After a fixed duration (4 ms) in fixed duty-cycle mode, the converter transitions to closed-loop current-mode control for more accurate voltage equalization. The voltage of the V_{mid} node is properly regulated to $V_{pv}/2$ after the converter turns ON, while the controller automatically transitions to burst mode to improve efficiency at low-output power. When the converter enters current-mode control for the first time, the inductor current ripple Δi_L is at maximum, but the frequency regulation loop quickly regulates it to achieve $f_s = 3.6$ MHz during the active periods, as shown in Fig. 19(b).

The converter employs both burst mode and CCM. In burst mode, shown in Fig. 20(a), the power stage is operated in periodic bursts, the duration of which is controlled by a hysteretic voltage window around V_{mid}. During the bursts, the average inductor current I_L is fixed at 0.5, 0.75 or 1 A, chosen by the digital controller in order to maintain the ratio of burst on and off times D_b between 1/3 and 2/3. An example of this is shown in Fig. 20(a), where D_b becomes higher than 2/3 due to a load step, and the converter automatically increases I_L to compensate and bring D_b within the desired range. A short D_b is prevented for technical reasons (primarily the sampling speed limitations of the ADC), while long bursts at lower I_L values are avoided to take advantage of the efficiency profile shown in Fig. 16. Furthermore, the [1/3, 2/3] range provides hysteresis to prevent unstable oscillations between adjacent I_L values. Using burst mode for low-current operations eliminates the need for zero-current detection, and eases the common-mode requirements of the current comparators. Throughout burst mode, Δi_L is regulated by the frequency regulation loop to achieve $f_s \approx 3.8$ MHz, as shown in Fig. 20(b). The deviation of f_s from the nominal value of 3.6 MHz can be attributed to the $\pm 20\%$ tolerance of the RC oscillator used to set the reference for the frequency loop.



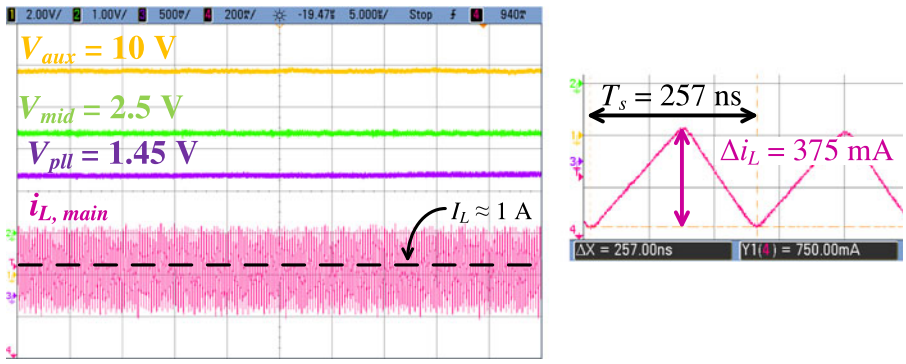
(a) (b)

Fig. 19. (a) Main converter startup and voltage equalization under closed-loop control. (b) Transition between 50% duty-cycle mode and burst mode.



(a) (b)

Fig. 20. (a) Burst-mode operation with $V_{pv} = 5$ V, 10 to 5 Ω step at V_{mid}. (b) Frequency regulation during burst mode.



(a) (b)

Fig. 21. (a) CCM operation with $V_{pv} = 5$ V, 2.5 Ω at V_{mid}. (b) Frequency regulation during CCM.

Additionally, since typical CPV installations are located in remote areas away from human populations, and the Δ-converters handle relatively small amounts of power, no particular care was necessary to avoid audible noise generated during burst-mode operation at low currents. Although the voltage ripple is relatively high in burst mode, it is of similar magnitude as typical variations in V_{mpp} due to environmental factors, and therefore represents a similar degree of reduction in power extraction (2–3%) [23]. Future designs should improve the regulation accuracy for better processing efficiency.

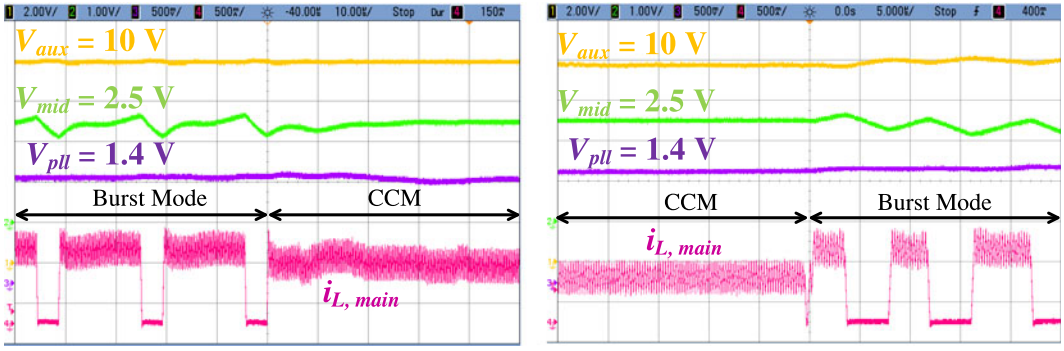


Fig. 22. Transition from (a) burst mode to CCM (4 to 3 Ω step at V_{mid}), and (b) CCM to burst mode (4 to 5 Ω step at V_{mid}), with $V_{pv} = 5$ V.

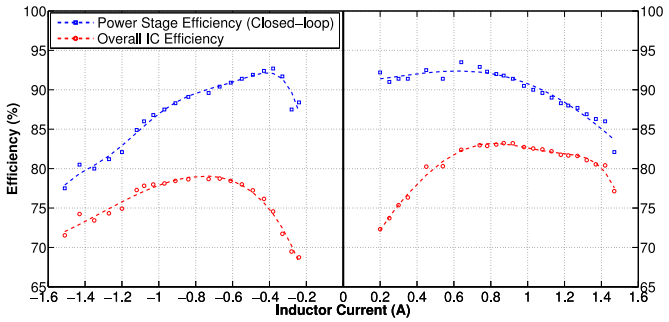


Fig. 23. Measured converter efficiency with $V_{mid} = 0.5V_{pv} = 2.5$ V. Dashed lines are only for demonstrating trends.

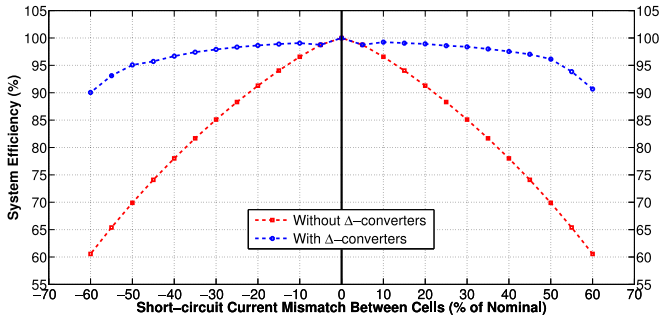


Fig. 24. Measured system efficiency for various mismatches in a two-cell string. Mismatch measurement is referenced to the parameters of the lower cell.

When $D_b > 2/3$ with $I_L = 1$ A in burst mode, the converter switches to CCM, where the power stage is operated continuously, shown in Fig. 21(a). In this mode, I_L is set by a digital PI controller in order to equalize the cell voltages, and Δi_L is adjusted by the frequency regulation loop to obtain $f_s \approx 3.9$ MHz, as shown in Fig. 21(b), within tolerance of the nominal target of 3.6 MHz. However, the value of I_L in CCM is kept between approximately 0.6 and 1.5 A. The maximum I_L is limited at 1.5 A in order to protect the power stage and avoid operating beyond the low-efficiency region in Fig. 16, while below 0.6 A, the converter switches to burst-mode operation to reduce gate-drive losses.

Transitions between burst mode and CCM operation, shown in Fig. 22, are handled automatically. Switching to CCM improves the voltage regulation at V_{mid}, as shown in Fig. 22(a), since the converter can regulate the current more accurately through the digital PI loop. In contrast, the ripple at V_{mid} increases in burst mode due to the noncontinuous operation; however, the power stage losses, drawn from V_{aux}, are also reduced, which allows the auxiliary boost converter to operate in burst mode, as evidenced by the increased ripple at V_{aux} in Fig. 22(b).

C. Converter Efficiency

The measured efficiencies of the main power stage (under closed-loop control and including drive losses) and the overall converter (including controller losses as well) is shown in Fig. 23 as a function of the inductor current. By employing burst-mode operation, the main power stage obtains efficiencies above 90% for low-current regions. Operation below ∼200 mA is avoided since the power improvement in such scenarios is negligible, while maximum current is limited to 1.5 A, as noted elsewhere. The asymmetric efficiency results from the fact that the power devices were sized to guarantee startup in the worst case ($V_{pv} = 6$ V), which results in a slightly weaker low-side device in the nominal case ($V_{pv} = 5$ V). Since the IC integrates all supply generation and protection functions on-chip, the overall efficiency of the converter is less than outstanding, unlike [20], where external LVRs are used (whose impact is not mentioned). Nonetheless, the impact of converter efficiency on the overall system is low thanks to the Δ-conversion architecture, as shown in Section VI-D.

D. System Efficiency

To quantify the impact of the Δ-converter efficiency on the power harvested from the system, the simulation setup described in Section III was utilized to simulate a two-cell CPV system with one Δ-converter (as shown in Fig. 25) with varying degrees of I_{scn} mismatches between the two cells and a converter efficiency profile identical to that in Fig. 23. Fig. 24 shows the resulting *system efficiency* with and without the Δ-converter. Here, system efficiency is defined as the ratio of the harvested power (from the two-cell string) to the theoretical maximum available from the two cells. Clearly, despite the modest

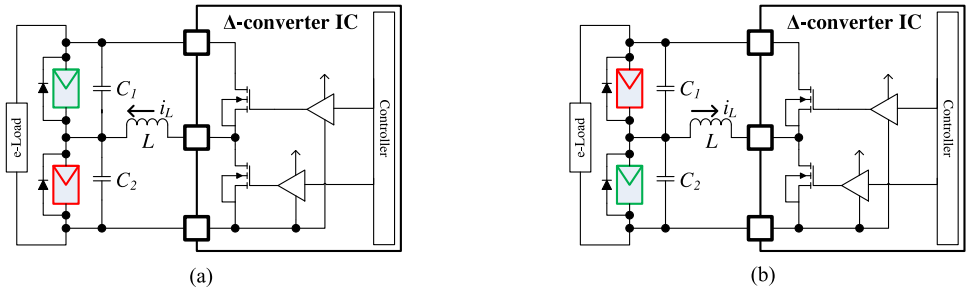


Fig. 25. Δ-converter test setup. (a) Buck mode and (b) boost mode.

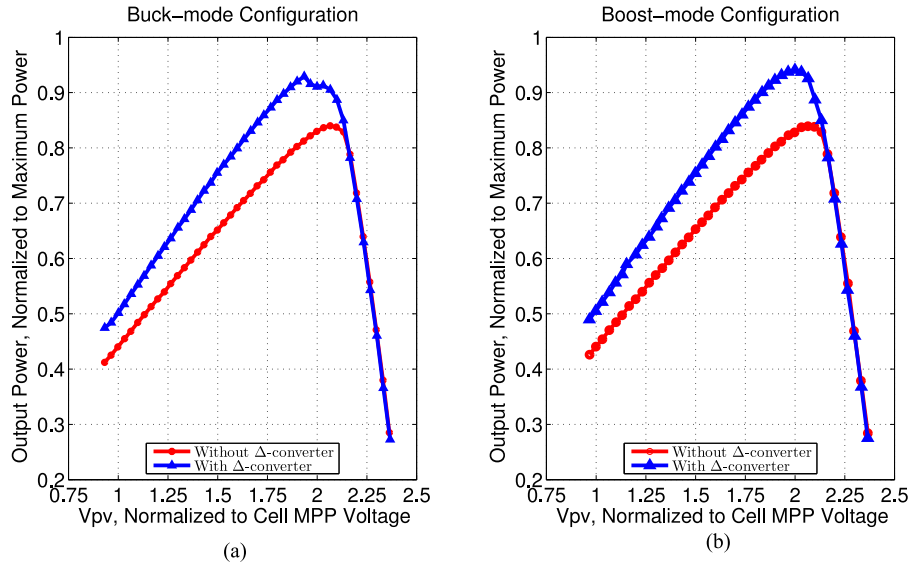


Fig. 26. Increase of system power using Δ-converter in (a) buck mode and (b) boost mode.

converter efficiency, the system efficiency remains above 95% for up to 50% mismatch between the cells, and certainly obtains significant improvements over the string setup. For low mismatches (and, thus, low currents), the converter shuts down, as described in Section VI-C, without significantly deteriorating the system efficiency. Consequently, the range of mismatches that the converters can handle in a practical system depends on the required system efficiency, as well as the string length. As discussed in Section III, converters in longer strings process higher amounts of powers on average due to current cascading, and can, therefore, only handle a lower degree of mismatches for the same system efficiency target, as compared to shorter strings.

E. Validation of Δ-Conversion Benefits

To verify the effectiveness of the IC in a realistic Δ-conversion setup and quantify the benefits, a two-cell CPV string was built using an Agilent solar array simulator. The string was biased at a fixed voltage using an electronic load, and the IC was connected across the cells as a Δ-converter, as shown in Fig. 25. During the measurements, the bottom cell was made 30% weaker (in output current) than the top one in one setup, and vice versa in another. These setups are referred to as buck mode [see Fig. 25(a)] and boost mode [see Fig. 25(b)], respectively.

The resulting string output power, with and without the Δ-converter, is shown in Fig. 26, normalized to the sum total of the maximum power of the two cells. While the two-cell string can only deliver approximately 84% of its maximum power on its own, up to 94% of the total can be extracted when the Δ-converter is active. Furthermore, the benefits will be more pronounced with realistic string sizes and over longer periods as the CPV cells age and become more mismatched, as demonstrated in the system simulations [3].

VII. Conclusion

This paper presents the first power management IC using bidirectional current control for mitigating current-domain mismatches in CPV systems using the Δ-converter approach. Taking advantage of the relaxed requirements for a Δ-converter, the IC employs a high-switching frequency above 3 MHz and integrated supply and protection functions to reduce the size and number of external components. The use of HCMC with a novel bidirectional senseFET scheme provides inherent current protection and high reliability. The high level of integration and lower cost compared to conventional power optimizers make

the IC ideally suited for integration with CPV cells for active mismatch mitigation.

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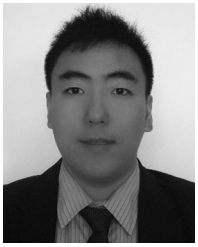

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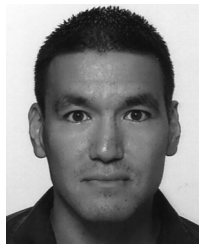

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