Technical Assessment of Load Commutation Switch in Hybrid HVDC Breaker

Arman Hassanpoor, *Student Member, IEEE*, Jürgen Häfner, and Björn Jacobson

***Abstract*—The development of a large-scale high-voltage direct current (HVDC) power grid requires a reliable, fast, and low-loss circuit breaker. The load commutation switch (LCS) is an essential part of ABB's 1200-MW hybrid HVDC breaker concept, which builds up a low-loss conducting path for the load current. The technical requirements for the LCS are expressed in this paper by studying the operation principle of the hybrid HVDC breaker. The voltage stress over the LCS is determined based on a dc grid with 320 and 2 kA rated voltage and current. A system model of the hybrid HVDC breaker is developed in PSCAD/EMTDC to study the design criteria for snubber circuit and arrester blocks. It is observed that conventional snubber circuits are not suitable for a bidirectional LCS as the current of snubber capacitors prevent the fast interruption action. A modified snubber circuit is proposed in this paper along with two more alternatives for the LCS to overcome this problem. Moreover, the power loss model for a semiconductor device is discussed in this paper based on the 4.5-kV StakPak IGBT. The model is used to calculate the conduction power losses for different LCS topologies. Ultimately, a matrix of 3 $\times$ 3 IGBT modules is selected to provide a reliable LCS design which can handle several internal fault cases with no interruption of operation. A full-scale prototype has been constructed and tested in ABB HVDC Center, Ludvika, Sweden. The experimental test results are also included in the paper in order to verify the calculation and simulation study.**

***Index Terms*—HVDC grid, semiconductor breaker, solid-state circuit breaker.**

I. Introduction

TRANSPORTING power electricity from distant renewable resources to load centers with high efficiency and low visibility environmental impact, are important features which can be achieved with a high-voltage direct current (HVDC) grid. The evolution of the power electricity network leads to a demand for advanced power transmission methods and more dc grids. The key equipment for developing the dc grid and dc switchyards is the dc circuit breaker [1], [2]. The lack of a fast and reliable dc breaker has always been an issue preventing the development of dc grids but this obstacle has now been removed by introducing the hybrid HVDC breaker in [3]. The hybrid HVDC breaker is a stand-alone system, which can independently interrupt the dc current.

The hybrid HVDC breaker consists of three essential components: load commutation switch (LCS), ultrafast disconnector (UFD), and main breaker. The hybrid HVDC breaker is a proactive component, which is able to interrupt the load current either during fault cases or normal steady-state conditions. In the hybrid HVDC breaker, there is a bypass current path over the main breaker in which the UFD and LCS are placed in series. The load current flows through the bypass path during normal operation, while turning off the LCS commutates the current to the main breaker path, so LCS is exposed to the main breaker voltage drop, during the UFD opening time. Since the LCS is conducting the load current, it is necessary to consider the possible failure modes and design a highly reliable bidirectional topology for this switch.

Following Section I, the operation principle of the hybrid HVDC breaker is described in Section II. Section III presents system modeling, design specification, and different LCS topologies. This Section conclude the most reliable, fast, and low-loss LCS through a detailed system study. Section IV is devoted to the experimental results from tests on a full-scale prototype of LCS, and finally, the conclusion is drawn in Section V.

II. Hybrid HVDC Breaker Operation Principle

The concept of hybrid HVDC breaker was first proposed by Häfner and Jacobson in [3]. Fig. 1 demonstrates the operation principle of the hybrid HVDC breaker. The load current flows through the UFD and LCS during normal operation. The green line in Fig. 1(a) shows the load current path during this time. In the case of any fault, the conducting current will increase proportionally to the fault current and, subsequently, the fault mode will be triggered according to grid requirements and protection scenarios. In this study, an increase of 20% in the conducting current above the nominal current has been set as a trigger threshold, so the LCS turn-off signal is initiated at conducting current equal to 2.4 kA, which is followed by decision making time delay. The fault type can be determined during this time delay. As Fig. 1(b) shows the fault current goes through the LCS for a certain period of time. As the LCS is switched OFF, the current will be commutated to the main breaker path, and the UFD will subsequently isolate one side of the LCS. At this time, the main breaker can interrupt the fault current and complete the current interruption. Fig. 1(c) illustrates the commutated current in the main breaker path. In the end, the fault energy will be absorbed by the arrester across the main breaker [see Fig. 1(d)]. Note that a current limiting reactor is placed in series to the

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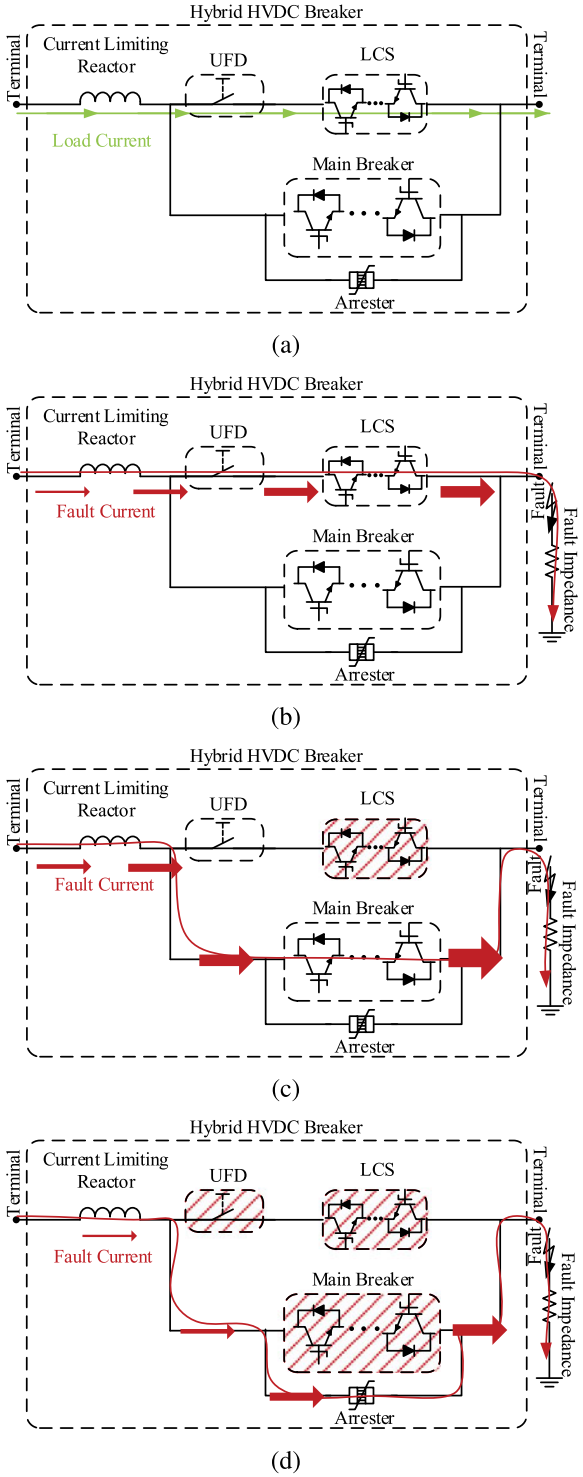

Fig. 1. Hybrid HVDC breaker operation principle. (a) Normal load current path. (b) Fault initiates operation. (c) LCS interrupts and commutates current to main breaker. (d) Main breaker interrupts and commutates current to the arrester.

LCS and main breaker. The purpose of this reactor is to limit the current rate of change during faults. The corresponding current interruption sequence is demonstrated in Fig. 2. Referring to Fig. 2, the fault occurred at $t = 6$ ms when the line carried a current I_c of 2 kA. At the time when the fault is established

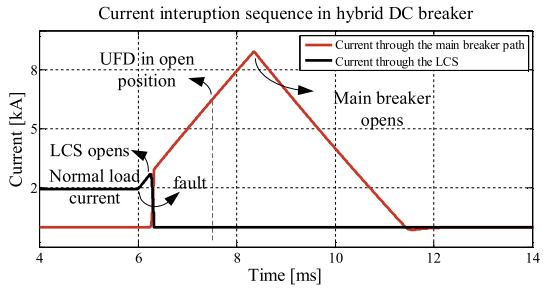

Fig. 2. Current interruption sequence in hybrid HVDC breaker.

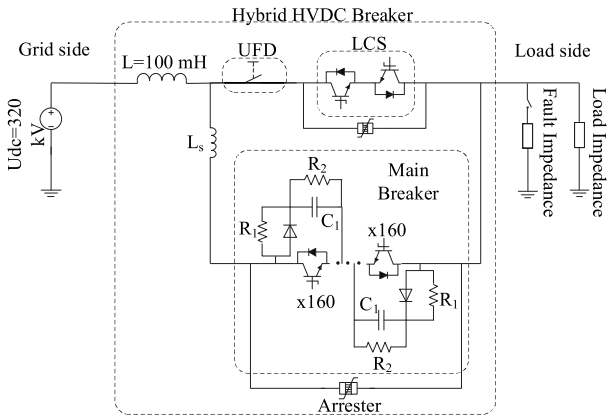

Fig. 3. Simulation model for hybrid HVDC breaker.

(20% above the nominal current in this example, $I_c = 2.4$ kA), the LCS is switched OFF, and the current is commutated to the main breaker branch. Thereafter, the UFD isolates the LCS in the system and enables main breaker operation. The main breaker can either immediately interrupt the current or limit the current based on the protection logics. However, Fig. 2 shows the case that a fault current of 9 kA is interrupted by the main breaker.

III. System Study

The LCS design criteria can be addressed by a detailed study of stresses over this switch in a system model. A simulation model is described in this section, which includes a simplified network model along with the hybrid HVDC breaker model. The network is modeled as a dc voltage source and a resistive load to derive the maximum current of 2 kA in the steady-state operation mode. Since the most severe fault would be a fault at the breaker terminals, then zero fault impedance has been considered for the worst-case scenario in the simulation study. However, different topologies for LCS are introduced later in this section and evaluated for different power loss generation.

A. System Modeling

Fig. 3 demonstrates the studied model of hybrid HVDC breaker including a simplified dc grid, main breaker, UFD, LCS, and arrester banks. The hybrid HVDC breaker is evaluated in a 320-kV dc grid for a rated current of 2 kA. This grid is

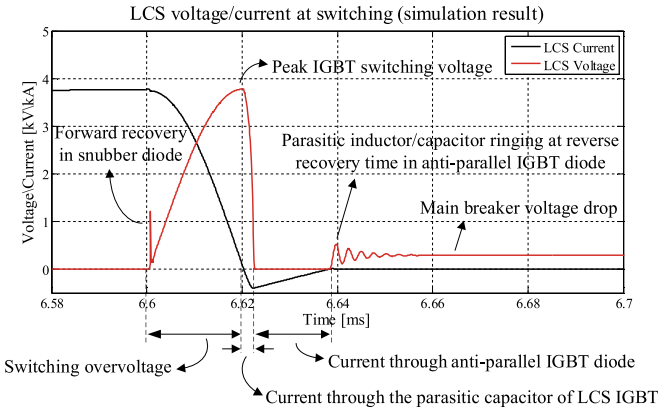

Fig. 4. LCS voltage stress during the fault current interruption interval.

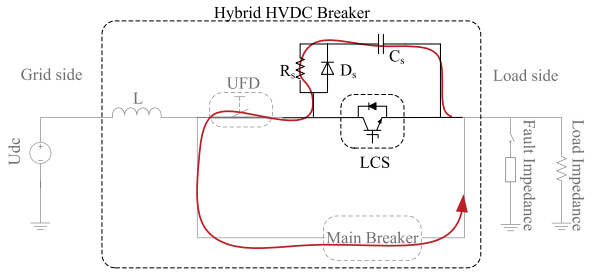

Fig. 5. Standard RCD snubber (the red line highlights the discharging problem with the standard snubber circuit).

represented by a stiff dc source of 320 kV along with a resistive load. The current limiting reactor is selected in a way to limit the current rise rate to 3.5 kA/ms for a low inductance fault at dc switchyard terminals. As it is shown in [3], a dc reactor of 100 mH can fulfill this requirement assuming a breaking time of less than 5 ms. The main breaker consists of four 80-kV modules, which are able to interrupt the current in either direction, employing 40-IGBT modules in each direction. Each module also utilizes an arrester bank to limit the maximum voltage over the corresponding module. Since the internal behavior of the main breaker is not the subject of this study, it is sufficient to model the main breaker using 160 IGBTs in one direction and 160 diodes in the other direction, while an arrester bank is positioned over all semiconductor devices. Furthermore, the equivalent turn-off snubber is available for the main breaker.

The UFD is modeled as an ideal switch which can be operated only at zero current. A delay time of 2 ms is introduced in the operation of this switch in order to model the mechanical time delay [4]. The UFD isolates the LCS from the voltage over the main breaker. Hence, the voltage rating requirement of LCS is relatively low. In this study, the LCS is initially modeled as two IGBT modules, which are connected in opposite directions. The inductance L_s links the bypass path and the main breaker path, this is the stray inductance of the mechanical structure. Since the LCS is the main object under study, the values of the dominating parasitic electrical elements of the mechanical structures and components are roughly estimated and implemented in the simulated model.

B. Design Specification

Fig. 4 shows the voltage stress over the LCS during the interruption interval. This is the time interval when the load current is sequentially commutating from the bypass path to the main breaker path and, then, arrester path, in order to complete the interruption. Referring to Fig. 4, the turn-off signal triggers the LCS at $t = 6.6$ ms, and the IGBT switching voltage is exposed over the LCS at this moment. The LCS switching voltage depends on the number of series IGBTs in the LCS, snubber circuit, and stray inductance between the LCS and the main breaker. The larger the stray inductance, the longer the commutation time and, consequently, the larger the voltage overshoot over the LCS. This shows how mechanical design affects the voltage stress over the LCS. The assumed stray inductance and snubber circuit introduce a peak voltage of 3.9 kV in the case of one IGBT module in the LCS, which is marked as "peak IGBT switching voltage" in Fig. 4 at $t = 6.62$ ms. The parasitic capacitor over the LCS IGBTs completes a loop through both the main breaker and the UFD at the snubber diode reverse recovery time, see black curve after $t = 6.62$ ms. At this moment, the negative LCS IGBT voltage drop makes the corresponding antiparallel diode forward biased. This diode will continue conducting until the positive voltage drop over the main breaker appears over the LCS IGBT and makes the LCS antiparallel diode reverse biased. This current is labeled as "current through antiparallel IGBT diode" in Fig. 4. The parasitic stray inductances and capacitors in the bus bars and cables create an oscillation at the reverse recovery time of the LCS antiparallel diode, which is observed as a ringing in the LCS voltage curve at $t = 6.64$ ms. While the fault current totally commutates to the main breaker path, the forward voltage drop (FVD) in the main breaker would appear over the LCS until the UFD isolates the LCS. Additionally, to protect the LCS against any undesirable overstress, an arrester bank has been placed over the LCS.

In order to lower the *dv/dt* at switching time, a resistor–capacitor diode (RCD) turn-off snubber is placed at each IGBT module in LCS. Standard RCD snubber is shown in Fig. 5. R_s is the turn-on resistor, which controls the discharging behaviour of the snubber capacitor C_s at turn on time. The diode D_s bypasses R_s during the turn-off period in order to reduce the IGBT stress and charge the snubber capacitor as fast as possible. However, using the conventional RCD snubber for LCS prevents fast UFD action, because the snubber capacitor C_s has a low resistive path to be discharged through the R_s, UFD, and main breaker during the breaking action. The discharging current goes through the UFD and precludes fast opening action. The current through the UFD and the main breaker is plotted in Fig. 6, and the discharging path is highlighted in Fig. 5. Three different alternatives are proposed in order to overcome the discharging problem by the conventional RCD snubber. Any design should maintain the following requirements for LCS:

1) bidirectional current interruption;
2) high system reliability;
3) minimize the component's stress;
4) several switching actions of LCS in a short period of time;

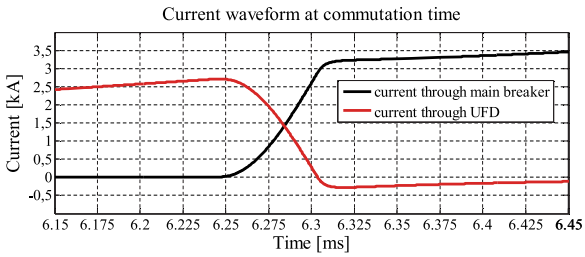

Fig. 6. Current through the main breaker path and bypass path.

5) simple mechanical structure;
6) low-conduction loss.

1) Alternative One (Reversal Connection): Using a diode in series with the LCS will prevent the snubber capacitor to be discharged through the main breaker. In this case, the standard RCD snubber can be used, while the same configuration should be used as an antiparallel connected LCS to enable bidirectional operation of the hybrid HVDC breaker. However, a resistor is used in parallel to the snubber capacitor to discharge the capacitor with a large time constant. This facilitates a more secure maintenance period and lowers risk to personnel. Fig. 7(a) illustrates the topology for this alternative. Another advantage of this topology is that only one IGBT stack will conduct the current in each direction so the conduction losses only include IGBT losses and no diode loss in the antiparallel IGBT diodes. The diode power loss is only generated through the series diodes D_1 and D_2 in this alternative.

2) Alternative Two (Modified Snubber Circuit): A modified snubber circuit is presented in Fig. 7(b). During the turn-off period, C_1 is charged and shapes the switching voltage over the corresponding IGBT. While the current commutation is accomplished, the stored charge in C_1 will be shared by parallel capacitor C_2 through R_2. Thereafter, C_1 can handle another switching action in the corresponding IGBT. The capacitance of C_2 needs to be at least three times higher than C_1 and R_2 resistance also needs to be much smaller than R_1. Moreover, R_1 ensures capacitor discharge with a relatively large time constant. A typical value for this snubber circuit is as follows:

1) $C_1 = 7.5\ \mu$F, $C_2 = 20\ \mu$F;
2) $R_1 = 10\ \text{k}\Omega$, $R_2 = 10\ \Omega$;

3) Alternative Three (Snubber IGBT): In order to unify the mechanical design along with the full functionality of the turn-off snubber, an IGBT module can be placed in the snubber circuit according to Fig. 7(c). All LCS IGBTs, including snubber IGBTs, are switched simultaneously; therefore, no additional firing pulse control logic needs to be implemented for the snubber IGBT. The snubber IGBT will block the discharging current through the snubber resistance at turn-off, while it forms a discharging path through the snubber resistance at the time that LCS IGBT is switched on again. This feature allows fast turn-on turn-off actions for LCS with no excessive over voltage formation over the IGBT modules [5].

C. LCS Topology

Regardless which of the above mentioned snubber configurations is used, the LCS continuously conducts the load current

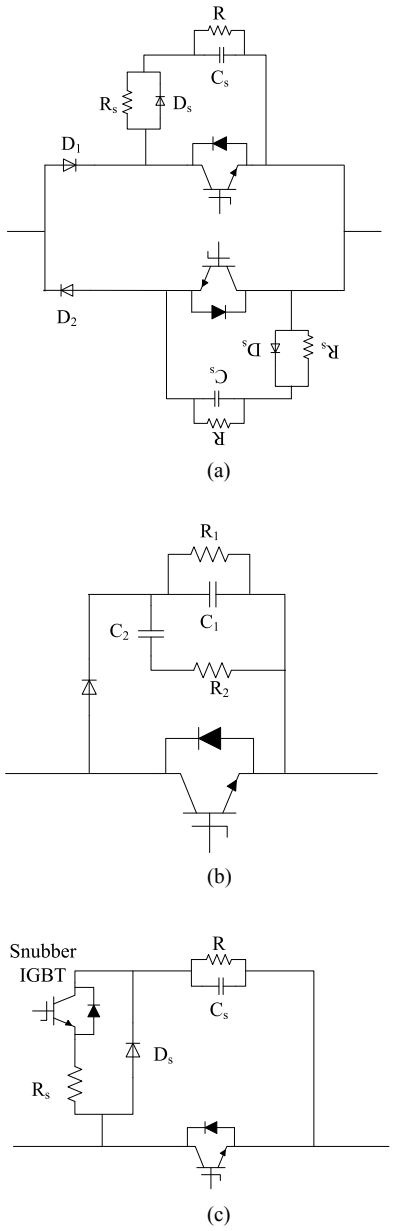

Fig. 7. (a) Alternative one (series diode connection). (b) Alternative two (modified snubber circuit). (c) Alternative three (snubber IGBT).

in steady-state operation. In this section, a reliable and robust design of the LCS is addressed by providing an additional conducting path and also decreasing the stresses on each internal component.

Additional conducting paths can be provided by paralleling the semiconductor devices in the LCS, while series connection results in a lower voltage stress on each device. Therefore, the LCS reliability can be improved through paralleling and series connection of semiconductor devices. On the other hand, each semiconductor device contributes to power losses and also increase the total system complexity, so an optimized design for the LCS is a tradeoff between system reliability, power loss, and system complexity. However, ten different LCS topologies have been studied and evaluated regarding the component stresses and losses. These cases are depicted in Fig. 8. The semiconductor

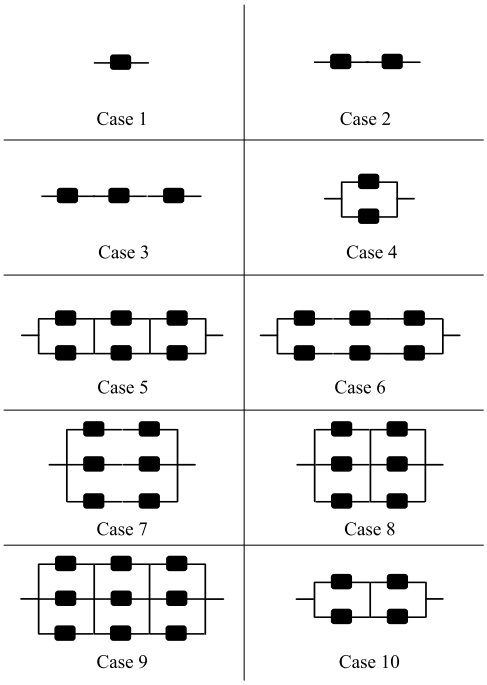

Fig. 8. Topologies for the LCS.

devices and electrical connections are represented by black blocks and plain lines in this figure. Power losses are calculated utilizing the 4.5-kV StakPak IGBT module [6]. IGBT conduction loss can be approximated by modeling the IGBT on-state zero current collector–emitter voltage (V_{CE0}) as a dc source voltage and a collector–emitter on-state resistance (R_{CE0}) in series

$$v_{CE}(t) = V_{CE0} + R_{CE0} i_{CE}(t) \tag{1}$$

where $v_{CE}(t)$ and $i_{CE}(t)$ are the instantaneous collector–emitter voltage and current, respectively. Similarly, the instantaneous voltage drop over the antiparallel diode ($v_D(t)$) can be approximated by employing the FVD and diode on-resistance ($R_{\rm on}$)

$$v_D(t) = FVD + R_{\rm on} i_D(t) \tag{2}$$

in which, $i_D(t)$ is the instantaneous diode current. Furthermore, the instantaneous IGBT and diode conduction loss ($p_{CE}(t)$ and $p_D(t)$) can be, respectively, formulated as

$$\begin{aligned} p_{CE}(t) &= v_{CE}(t) i_{CE}(t) \\ p_D(t) &= v_D(t) i_D(t) \end{aligned} \tag{3}$$

while substituting (1) and (2) into (3) expresses the instantaneous power losses with respect to instantaneous device current

$$\begin{aligned} p_{CE}(t) &= V_{CE0} i_{CE}(t) + R_{CE0} i_{CE}^2(t) \\ p_D(t) &= FVD i_D(t) + R_{\rm on} i_D^2(t). \end{aligned} \tag{4}$$

The maximum conduction losses in each IGBT module and antiparallel diode were calculated by implementing (4) in a PSCAD simulation model utilizing the 4.5-kV StakPak IGBT parameters for V_{CE0}, R_{CE0}, FVD, and $R_{\rm on}$. Results are available in Table I for various LCS topologies. The LCS requirement specifications including the design margins are summarized in Table II, which determines the final design of the LCS according to topology number 9. Two parallel semiconductor devices are required for 2.6-kA continuous current, while a third one ensures redundancy in this set. A second set of three paralleled devices is required to create enough voltage drop across the LCS, which is needed to ensure short-circuit failure mode of a failed device in the main breaker. A third set of three paralleled devices is needed for redundancy if one of the other series devices fails. However, in the case of device failure in any parallel set, there are two more alternative current paths, which can handle the load current. In order to have full operation availability, the cooling system is designed based on the maximum power loss in Case 10.

TABLE I
COMPONENT LOSSES FOR DIFFERENT TOPOLOGIES

Case no.	Nominal component current	Max. IGBT conduction loss	Max. diode conduction loss
1	2.7 kA	6.9 kW	5.8 kW
2	2.7 kA	6.9 kW	5.8 kW
3	2.7 kA	6.9 kW	5.8 kW
4	1.4 kA	2.5 kW	2.2 kW
5	1.4 kA	2.5 kW	2.2 kW
6	1.4 kA	2.5 kW	2.2 kW
7	0.9 kA	1.5 kW	1.3 kW
8	0.9 kA	1.5 kW	1.3 kW
9	0.9 kA	1.5 kW	1.3 kW
10	1.4 kA	2.5 kW	2.2 kW

TABLE II
REQUIREMENT SPECIFICATIONS FOR LCS

Requirements	Dimensions	Values
Nominal current	A_{DC}	2000
Maximum continuous current	A_{DC}	2600
Maximum current level during commutation	kA_{peak}	8
Maximum voltage stress after commutation	kV_{peak}	4.8
Maximum transient voltage stress during commutation	kV_{peak}	9
Repetitive switching capability within one operating cycle (turn-off/turn-on)		10

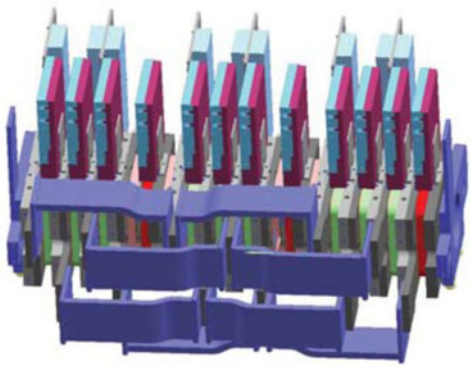

Fig. 9. Stack design for LCS (Blue: Bus bars, Red: Isolators, Green: IGBTs, Purple: Gate units).

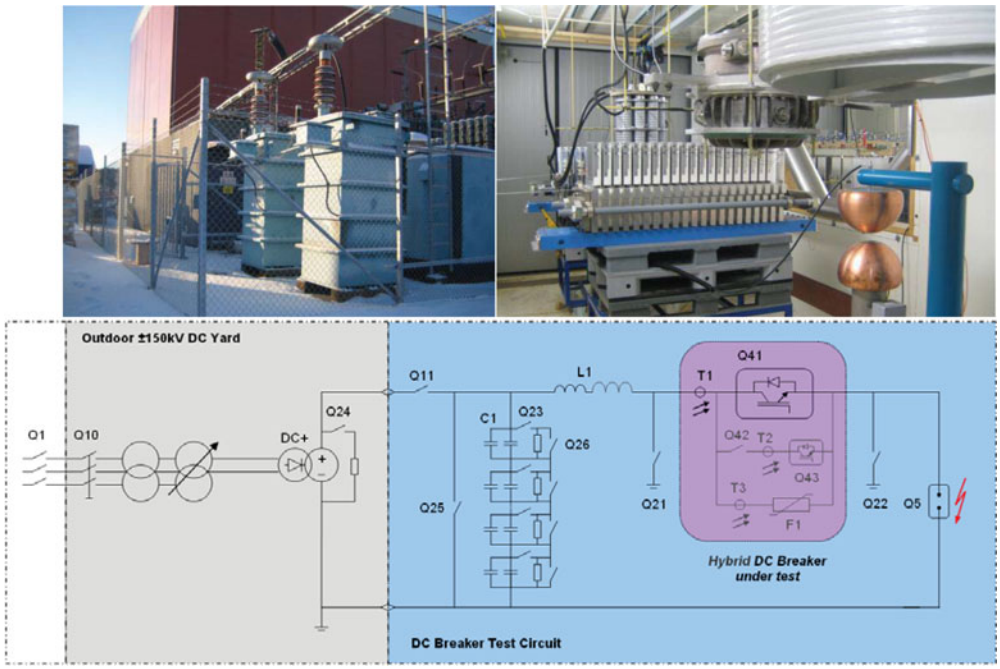

Fig. 10. Hybrid HVDC breaker test circuit.

In this case, all back-up devices in the LCS are fully used. In addition to all above mentioned redundancies in the LCS, an arrester block will protect the LCS against any kind of unexpected stresses, which might occur in internal or external failure cases. This arrester block limits the maximum overvoltage stress to 4.5 kV in the case of 4.5-kV StakPak IGBT module utilization. The final stack design of the LCS is illustrated in Fig. 9. The stack design brings full modularity and easy maintenance. Parallel connections are accomplished through flexible bus bars between each set of three series devices, while insulator plates separate the series sets.

Overall, the LCS is designed in a way that can handle different fault cases not only inside the LCS, but also in the main breaker path. Refereing to Table I, the LCS can withstand the maximum load current of 8 kA in the case of any commutation failure occur in the system. This maxmimum current level corresponds to the 9 kV of transient peak voltage.

IV. Experimental Test Results

An LCS full-scale prototype has been built according to the design specification in Section III-C and the third alternative (snubber IGBT). The designed LCS has been studied in a test circuit including the main breaker, UFD, and arresters in order to illustrate the stresses over the LCS components. The test sequence is similar to the introduced functional logic of the hybrid HVDC breaker in Section II. However, the fault current in this test setup is generated by discharging the capacitor banks and its rate of change (*di/dt*) is regulated by reactors in the loop.

A. Test Setup

Fig. 10 illustrates the hybrid HVDC breaker test circuit. The capacitor bank $C1$ builds up the desired dc voltage level of 40 kV, supplied by a $\pm$150-kV outdoor dc switchyard. Initially, the breaker $Q11$ charges the capacitor bank $C1$. Later, the dc switchyard will be isolated by opening the breaker $Q11$. Thereafter, the capacitor bank $C1$ discharges through the reactor $L1$ and test object, when the spark gap $Q5$ triggers the test. The variable reactor $L1$ can be manipulated to achieve different rates of rise of the current *di/dt*. The object under test including main breaker, UFD, LCS, and arrester bank is represented by $Q41$, $Q42$, $Q43$, and $F1$, respectively, in Fig. 10. The optical current measurement devices are also integrated in the test circuit to measure different quantities during the test procedure. $T1$ measures the total discharging current, $T2$ measures the current through LCS, and $T3$ measures the arrester current. The breakers $Q21$, $Q22$, $Q25$, and $Q26$ are protective breakers ensuring circuit grounding for safety purposes.

B. Test Results

The results from tests are illustrated in Fig. 11. The spark gap $Q5$ initiates the test at $t_0 = 0.0112$ s. In this test, the discharging current is shared between LCS and the main breaker path according to resistance. Note that only one main breaker stack (80-kV module) is used in this test, otherwise there would not be any current flow through the main breaker path in normal operation of the hybrid HVDC breaker. However, the LCS is turned off when the conducting current reaches 3.2 kA. At this moment, the current commutates to the main breaker path, and as is shown in Fig. 11, the LCS current becomes zero. A delay time of 250 μs is assumed for commutation time; therefore, the UFD can be opened after this time delay. Finally, the total current of 9 kA is interrupted by turning off the main breaker. Fig. 11 shows currents in different paths of the hybrid HVDC breaker and also voltage stress over the main breaker during the test interval.

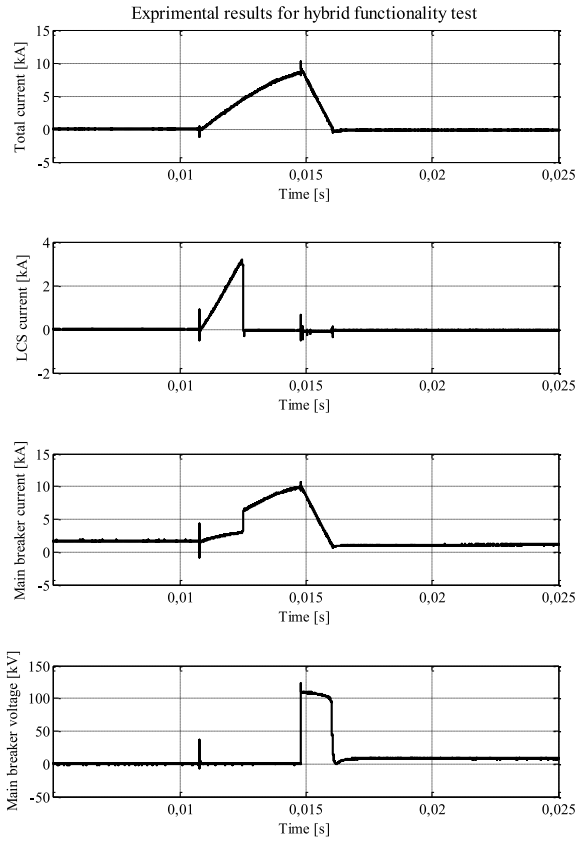

Fig. 11. Experimental results for hybrid functionality test.

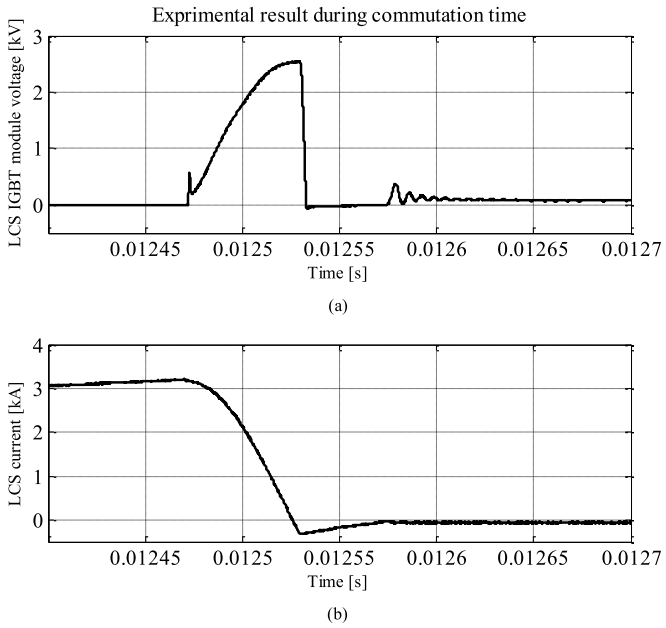

Fig. 12. LCS voltage and current during commutation time.

An expanded view of the LCS IGBT module voltage stress is available in Fig. 12(a). Comparing the test result in this Figure with the simulation result in Fig. 4 validates the simulation model with an acceptable error margin. Similar to Fig. 4, the first overshoot in Fig. 12(a) is due to the forward recovery in the snubber diode. The maximum voltage of 2.7 kV is governed by snubber circuit, LCS topology, and stray inductances in the commutation loop. Hereafter, the zero voltage over the IGBT modules in the LCS explain the current flowing through the antiparallel diode of the IGBT module. And finally, the voltage oscillation appears at the reverse recovery time for the antiparallel diode, which is due to the parasitic components between the LCS and the main breaker. Fig. 12(b) shows the expanded view for the LCS current at the switching time, which matches the simulation results illustrated in Fig. 4.

V. Conclusion

The LCS is one of the key parts of the hybrid HVDC breaker concept. The LCS continuously conducts the load current in the normal steady-state operation of the hybrid HVDC breaker. In this paper, the operating principle of the hybrid HVDC breaker is analyzed primarily toward developing a simulation model of the breaker. Specific requirements for the LCS has been introduced in order to make it fast, reliable, and robust commutation switch of LCS. It is shown that conventional snubber circuits prevent fast operation of the LCS. Therefore, three alternatives are introduced in order to overcome this problem. On the other hand, ten different internal topologies for LCS, including different number of conducting paths, are evaluated regarding the generated power loss, component stress, and reliability factors. Finally, an LCS full-scale prototype has been built and tested in a high-voltage test setup along with the other parts of the hybrid HVDC breaker. The test was conducted to illustrate the maximum component stresses over the LCS during current interrupting event in the hybrid HVDC breaker. The functionality test of the hybrid HVDC breaker does not only confirm the reliable mechanical design, but also verifies the detailed simulation model of the system. The presented LCS design brings modularity and easy maintenance, as well as fast, low loss, and reliable operation of the hybrid HVDC breaker.

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