Small-Signal Stability Analysis of Three-Phase AC Systems in the Presence of Constant Power Loads Based on Measured *d-q* Frame Impedances

Bo Wen, *Member, IEEE*, Dushan Boroyevich, *Fellow, IEEE*, Rolando Burgos, *Member, IEEE*, Paolo Mattavelli, *Fellow, IEEE*, and Zhiyu Shen, *Member, IEEE*

***Abstract*—Small-signal stability is of great concern for electrical power systems with a large number of regulated power converters. In the case of dc systems, stability can be predicted by examining the locus described by the ratio of the source and load impedances in the complex plane per the Nyquist stability criterion. For balanced three-phase ac systems the same impedance-based method applies, for which this paper uses impedances in the synchronous rotating reference (*d-q*) frame. Small-signal stability can be determined by applying the generalized Nyquist stability criterion (GNC). This approach relies on the actual measurement of these impedances, which up to now has severely hindered its applicability. Addressing this shortcoming, this paper investigates the small-signal stability of a three-phase ac system using measured *d-q* frame impedances. The results obtained show how the stability at the ac interface can be easily and readily predicted using the measured impedances and the GNC, thus illustrating the practicality of the approach, and validating the use of ac impedances as a valuable dynamic analysis tool for ac system integration, in perfect dualism with the dc case.**

***Index Terms*—Impedance, inverters, Nyquist stability, power system stability, rectifiers, stability.**

I. Introduction

POWER electronics converters with regulated output voltage feature a negative incremental input impedance [1], which translates into a constant power load behavior. A high number of constant power loads in an electrical system, can in consequence, induce oscillations and overvoltages, potentially leading to a system shutdown. Strong power grids can tolerate a large number of loads with negative input impedance, but smaller electrical systems, such as aircrafts, ships and microgrids, cannot. This is easily explained as small-signal stability depends on the source to load impedance ratio at any given interface, as has been demonstrated for both dc and ac systems [2], [3]. As a result, the analysis of small-signal stability is critical for the design of three-phase power conversion systems in this type of applications [4], [5].

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B. Wen, D. Boroyevich, R. Burgos, and Z. Shen are with the Bradley Department of Electrical and Computer Engineering, Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA 24061 USA (e-mail: wenbo@vt.edu; dushan@vt.edu; rolando@vt.edu; shenzy@vt.edu).

P. Mattavelli is with the University of Padova, 35122 Padova, Italy (e-mail: paolo.mattavelli@unipd.it).

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The stability of power systems nonetheless is often analyzed using eigenvalues, which are extracted from the system matrix "**A**" of the canonical state space model representation of the system in question [5]. This approach requires the use of full dynamic models for all the elements in the system, including physical and control parameters. As such, system integrators need to manage an enormous amount of information to derive these models; from converter topologies, to circuit parameters, to control strategies, information that must also be updated every time any of the components changes in the system. Naturally, the system model needs to be derived again too. Using this approach, the sharing of proprietary information from different system component vendors is not feasible, ultimately impeding the proper modeling of the system.

Loop gain is also a useful stability analysis tool for analog circuit with feedback control system [6]–[9]. When the phase margin of the loop gain is positive, then the feedback system is stable. Moreover, increasing the phase margin (could be more than 60°) causes the system transient response to be better behaved, with less overshoot and ringing. Loop gain can be measured.

However, both eigenvalue- and loop-gain-based stability analysis need information of components' inner physical structure and parameters, which, usually, are not available for system integrator. When components in the system are acquired as "black boxes" for use in bigger electrical system to deliver power from source to load, it may be found that the system oscillates or becomes unstable because the particular source or load impedances were not foreseen by the components' designers; or, the components may have inadequate input or output filters, so the system integrator has to provide external filters which in turn may cause the system to oscillate. Under such condition, it is difficult to use eigenvalue- and loop-gain-based analysis.

As a more practical alternative to the earlier method, impedance-based stability analysis, as previously mentioned, has been successfully used in dc systems for a long time [2], where the stability at each interface is determined using measured impedances. The main advantage of this approach is that the measured impedances intrinsically model all circuit components, including physical components and control systems. Stability criteria can be formulated then by establishing forbidden regions in the complex plane where the locus of possible source and load impedance ratios cannot reside thus ensuring a stable operation [10]–[13]. This allows for new loads to be added to the system easily without knowing their internal parameters

and without requiring the remodeling of the whole system to assess its impact on the system stability. This approach for instance was used in the design of the electrical power system for the International Space Station [14].

In the case of three-phase ac systems, the impedance-based stability can be formulated using the synchronous *d-q* frame source and load impedances, where the return-ratio matrix defined by the product of the source impedance and load admittance is used to study the stability at three-phase interfaces. For this, conventional multivariable linear control theory can be used to limit the source and load impedance magnitudes [3]. More recently, the use of the generalized Nyquist stability criterion (GNC) was proposed to predict stability at ac interfaces in the *d-q* frame [15]–[17]. This method was used to study the stability of a hybrid ac/dc system in [16], and the resonances between input filter and three-phase converters in [18]. It has also been applied to study the stability of grid-connected and islanded microgrid systems [19]. Different from *d-q* frame method where three-phase ac system becomes two coupled dc systems, so that traditional linearization can be applied, an interesting approach extract impedances in the stationary *abc*-frame using harmonic linearization [20].

Regardless of the method employed, impedance-base stability analysis in *d-q* frame using GNC has been mainly reported using computer simulation using either average or switching models. None of the references discussed earlier has verified its results using actual *d-q* frame measured impedances because of the difficulty associated with this procedure. Consequently, a significant effort has been devoted to solving this problem; by using current or voltage injection in order to characterize the frequency response of the system [21]–[24], or by investigating the transient response to shorten the measurement process [25]–[26]. Reference [21] is interesting in the sense that it discussed the stability of a three-phase motor drive system; however, did it at the interface between the inverter and a resistive load, plotting several frequency points of the generalized Nyquist diagram for this stable case. At this point, a study of three-phase ac system stability using GNC with measured *d-q* impedances is critical. This study not only demonstrates the feasibility of using GNC in practical ac system, but also opens the door of validating the simulation models for stability analysis using *d-q* impedances.

This paper presents, for the first time, the small-signal stability analysis of a balanced three-phase ac system with constant power loads based on the GNC and measured impedances in *d-q* frame. To this end, three experiments are shown for stable, critical stable, and unstable conditions, demonstrating the stability prediction accuracy of the approach. Furthermore, results in the time and frequency domains are put side by side to show the effectiveness of the stability analysis based on the measured impedances. This also validates the assumptions previously made to study the stability of ac systems using the GNC and simulation-based analysis. Specifically, using the *d-q* impedance measurement algorithm and equipment developed in [23], this paper studies the small-signal stability of an ac system comprised of a voltage-source inverter (VSI) feeding a boost rectifier or voltage-source converter (VSC), in what is regarded

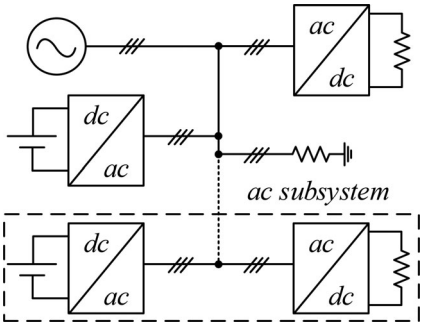

Fig. 1. Experimental ac system used for stability analysis.

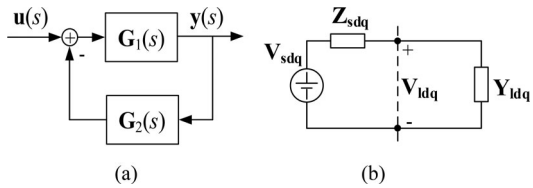

Fig. 2. (a) Generic multivariable closed-loop configuration, and (b) three-phase system in the *d-q* frame.

a very generic system configuration. In effect, it could represent many applications, for example, an uninterruptable power supply feeding an active load in a building, or an ac subsystem within a microgrid as shown in Fig. 1. Accordingly, the analysis presented is kept as generic as possible to be representative of any such ac system interface. Stable and unstable conditions then are created by adjusting the voltage control bandwidth of the VSI, where by measuring the source (VSI) output impedance and the load (VSC) input impedance the GNC is applied characterizing the stability conditions at the ac interface.

The paper is organized as follows: in Section II, the GNC and its application in three-phase ac power system are described; in Section III, the setup and parameters of the ac system used for experiments are discussed; Section IV discusses how stable and unstable cases are created in the experimental system; before the experimental results are shown, in Section V, the *d-q* frame impedance measurement techniques are discussed; finally, Section VI shows the experimental results, including time-domain waveforms, measured *d-q* frame impedances, and GNC characteristic loci used to validate all stability conditions; Section VII gives a brief discussion about the experiments; and Section VIII gives the conclusion.

II. GNC Applied to AC Systems

What follows briefly describes the GNC, but the reader is referred to [17] for a detailed explanation. In terms of notation, bold fonts are used in the paper to represent vector and matrix quantities. Specifically, a generic multivariable feedback configuration is shown in Fig. 2, where $\mathbf{G}_1(s)$ and $\mathbf{G}_2(s)$ are two linear multivariable subsystems. Suppose that $\mathbf{G}_1(s)$ has m inputs and that $\mathbf{G}_2(s)$ has m outputs, then the output $\mathbf{y}(s)$ of the system can be expressed as shown in (1) as a function of $\mathbf{G}_1(s)$, $\mathbf{G}_2(s)$, the

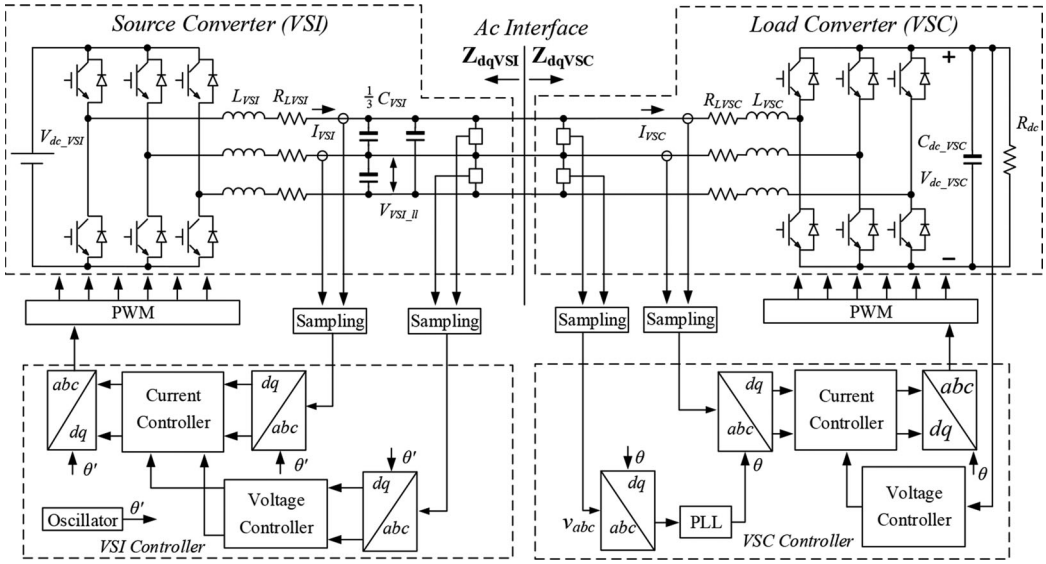

Fig. 3. Experimental system setup and control scheme.

input vector $\mathbf{u}(s)$, and an m-by-m identity matrix $\mathbf{I}$

$$\mathbf{y}(s) = [\mathbf{I} + \mathbf{G}_1(s)\mathbf{G}_2(s)]^{-1}\mathbf{G_1}(s)\mathbf{u}(s). \tag{1}$$

Let $\mathbf{L}(s)$ be the return-ratio matrix of the system defined as

$$\mathbf{L}(s) = \mathbf{G_1}(s)\mathbf{G_2}(s). \tag{2}$$

Let $\{l_1(s), l_2(s), \ldots, l_m(s)\}$ be the set of frequency-dependent eigenvalues of $\mathbf{L}(s)$, which trace in the complex plane the characteristic loci of matrix $\mathbf{L}(s)$ as the variable s traverses the standard Nyquist contour in the clockwise direction. Then, the GNC can be formulated as:

"Let the multivariable feedback system shown in Fig. 2(a) have no open-loop unobservable or uncontrollable modes whose corresponding characteristic frequencies lie in the right-half plane. Then, the system will be closed-loop stable if and only if the net sum of anticlockwise encirclements of the critical point $(-1 + j0)$ by the set of characteristic loci of $\mathbf{L}(s)$ is equal to the total number of right-half plane poles of $\mathbf{G}_1(s)$ and $\mathbf{G}_2(s)$."

Now, since a three-phase ac system is time-varying in nature, its voltages and currents cross zero periodically in steady state; hence, no steady-state operating point exists to conduct small-signal stability analysis. For this purpose, a synchronous reference frame transformation is applied where the ac system becomes a multiple-input and multiple-output (MIMO) dc system with a quiescent operating point. Fig. 2(b) depicts such generic ac system configuration in the synchronous d-q frame, where $\mathbf{V_{sdq}}$ represents the source voltage, $\mathbf{V_{ldq}}$ the ac load voltage, and $\mathbf{Z_{sdq}}$ and $\mathbf{Y_{ldq}}$ the ac source and load impedance and admittance, respectively. Notice that in the d-q frame the voltage and current in the system are two-dimensional vectors, and the source and load impedances (admittances) are correspondingly 2×2 matrices [3]. In this case, the load or ac bus voltage $\mathbf{V_{ldq}}$ can be expressed as [27]

$$\mathbf{V_{ldq}}(s) = [\mathbf{I} + \mathbf{Z_{sdq}}(s)\mathbf{Y_{ldq}}(s)]^{-1}\mathbf{V_{sdq}}(s). \tag{3}$$

By simple inspection, the earlier expression is seen to be equivalent to the closed-loop transfer function of the multivariable system (2); hence, the bus voltage stability at the ac interface in Fig. 2(b) can be studied by applying the GNC to the return-ratio matrix defined as follows [27]:

$$\mathbf{L_{dq}}(s) = \mathbf{Z_{sdq}}(s)\mathbf{Y_{ldq}}(s). \tag{4}$$

III. System Setup and Parameters

Fig. 3 shows the circuit schematic and control system block diagram of the experimental setup where the VSI, VSC, and ac interface of interest are clearly identified. At this interface, the VSI closes its outer control loop regulating the ac bus voltage $V_{\mathrm{VSI\_ll}}$, from where the VSC draws its current I_{VSC}. As such, the VSI output impedance $\mathbf{Z_{dqVSI}}$ and the VSC input impedance $\mathbf{Z_{dqVSC}}$ seen at this interface are solely of each converter's parameters and do not depend on each other's components and control systems. Also, when performing the measurements this interface is a common coupling point fully accessible from the exterior of the VSI and VSC cabinets.

The parameters of this system are listed in Table I.

As seen, the control systems of both converters are implemented in the d-q frame. For the VSI, the inductor currents are measured in the inner current control-loop, and the capacitor voltages are measured in the outer voltage-control loop. For the VSC, the input terminal voltages are measured by the phase-locked loop (PLL) in order to estimate the phase of the ac bus voltage and synchronize the converter operation. The PLL scheme implemented is based on the positive-sequence d-q frame transformation [28]. The boost inductor currents are measured in the inner current control-loop, and the output capacitor voltage is measured in the outer voltage-control loop. All the regulators employed use a Proportional and Integral (PI) structure, and no dynamic decoupling schemes were implemented between d-q axis variables. Both control systems are run on a single digital signal processor (DSP) control board, at a

TABLE I
EXPERIMENTAL SYSTEM PARAMETERS

Symbol	Description	Value
V_{dc_VSI}	VSI input dc voltage	270 V
V_{VSI_ll}	VSI output line–line rms voltage	99.6 V
f	VSI output voltage frequency	400 Hz
L_{VSI}	Inductance of VSI output inductor	970 μH
R_{LVSI}	Resistance of VSI output inductor self-resistor	120 mΩ
C_{VSI}	Capacitance of VSI output capacitor	31.8 μF
L_{VSC}	Inductance of VSC boost inductor	470 μH
R_{LVSC}	Resistance of VSC boost inductor self-resistor	90 mΩ
V_{dc_VSC}	VSC output dc voltage	270 V
C_{dc_VSC}	Capacitance of VSC output capacitor	100 μF
R_{dc}	Resistance of VSC load resistor	96 Ω
R_l	Resistances of resistor load for VSI output impedance test	13 Ω
R_b	Resistances of resistor for VSC input impedance test	0.5 Ω

sampling rate of 20 kHz. All analog signals are previously conditioned via a second-order Sallen–Key low-pass Butterworth filter with a 200 kHz cutoff frequency. Continuous space vector modulation (SVM) was used as pulsewidth modulation (PWM) scheme for both converters [29].

IV. DESCRIPTION OF EXPERIMENTAL TESTS CONDUCTED

In order to illustrate how the output impedance of VSI is increased by decreasing the control bandwidth of the VSI output voltage, and why an unstable condition could be created at the ac interface of the system under consideration, *d-q* frame average models of both VSI and VSC are employed in what follows. These models are shown in Fig. 4, where their derivation is discussed in detail in [30]. In this figure, $\mathbf{G_{del}}$ represents the transfer function due to the digital control and PWM delays; $\mathbf{K}$ represents the transfer function of the signal conditioning filter, and $\mathbf{T}_{\Delta\theta}$ is a rotation matrix as shown in (5). To obtain the *d-q* frame impedances of the VSI and VSC, small-signal linearization can be applied as discussed extensively in [30]–[33]. Using these average models, output impedance of VSI and input impedance of VSC are extracted by simulation to illustrate their features

$$\mathbf{T}_{\Delta\theta} = \begin{bmatrix} \cos(\Delta\theta) & \sin(\Delta\theta) \\ -\sin(\Delta\theta) & \cos(\Delta\theta) \end{bmatrix}. \tag{5}$$

A. *d-q* Frame Output and Input Impedances

Using the average models of VSI and VSC, this section discusses the features of VSI output impedances and VSC input impedances in principle. Fig. 5 shows the open-loop *d-q* frame output impedance of the VSI superimposed over the impedance of the output *LC* filter in the *abc*-frame. As observed, due to the modulation effect of the *d-q* frame transformation, the VSI impedance in the *d-q* frame has two resonant frequencies, which correspond to the transformed *abc*-frame impedance of the *LC* filter. These two resonant frequencies are consequently separated by two-times the line frequency around the *LC* filter resonant frequency [34]. Fig. 5 depicts this phenomenon where

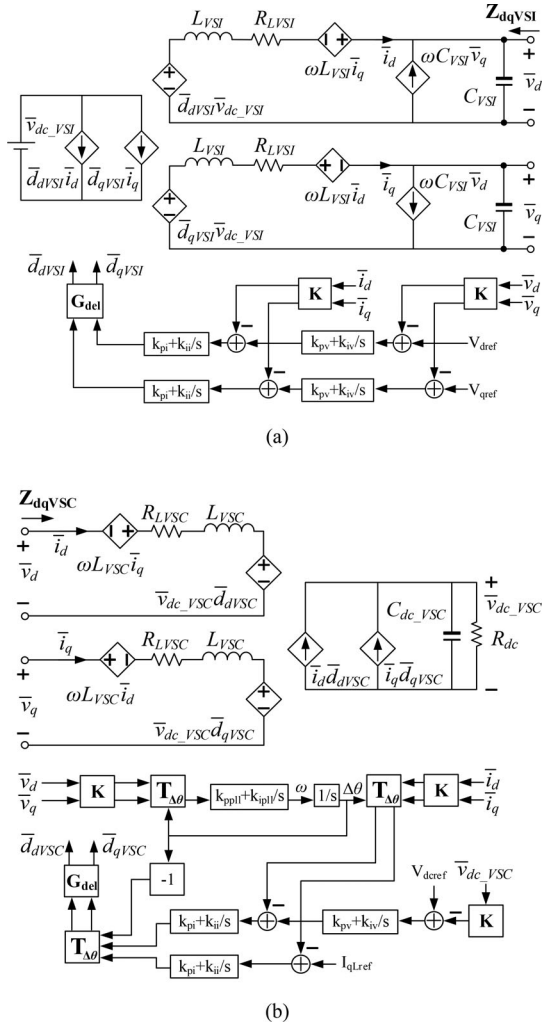

Fig. 4. Average models: (a) VSI and (b) VSC.

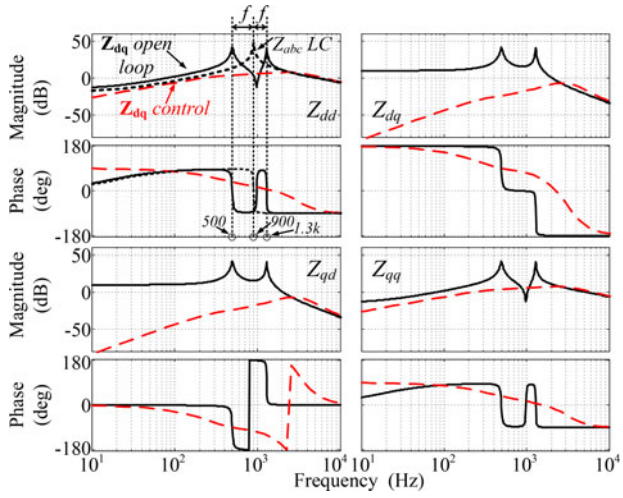

Fig. 5. VSI output impedance in *d-q* frame; black dot line: impedance of *LC* filter in *abc* frame; black solid line: open-loop impedance in *d-q* frame; red dashed line: closed-loop impedance in *d-q* frame.

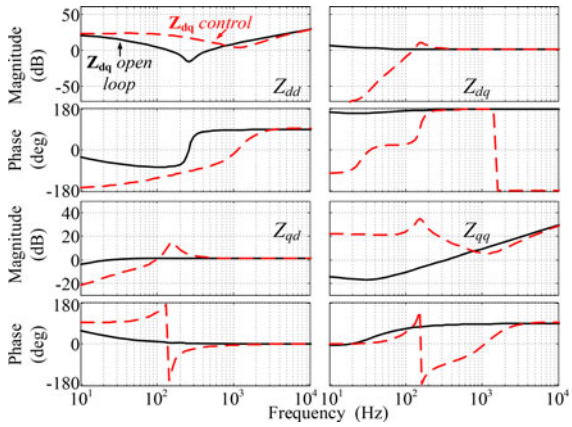

Fig. 6. VSC input impedance in *d-q* frame; black solid line: open-loop impedance; red dashed line: closed-loop impedance.

the *LC* resonant frequency at 900 Hz is clearly seen, as well as the two corresponding resonant peaks at 500 Hz and 1.3 kHz respectively for the VSI impedance in the *d-q* frame given the 400 Hz line frequency employed. This figure also shows the VSI output impedance in the *d-q* frame under closed-loop control. The most prominent feature in this case is that these *LC* resonances are effectively smoothed out by the converter current loop, and that the magnitude of the VSI output impedance, in the low frequency range, is controlled by its output voltage controller; hence, the higher the voltage loop bandwidth is, the lower the output impedance is.

Fig. 6 shows the open-loop and closed-loop *d-q* frame input impedance of the VSC. As it can be observed, the open-loop impedance is a combination of the ac side inductor impedance (at high frequency) and the dc side impedance of capacitor and resistor (at low frequency) weighted by *d* channel and *q* channel duty ratios [32]. After the closed-loop control (unity power factor control in this paper) is applied, the negative resistor impedance effect can be observed in the *d–d* channel impedance Z_{dd}, which is the main feature of the VSC input impedance, a direct result of its constant power load dynamics. In this case, the higher the control bandwidth of the VSC voltage loop is, the wider the frequency range of the negative resistor is.

B. Constant Power Loads and Instability

A constant power load behaves as a negative incremental resistor in the low frequency range, corresponding to the origin of instability discussed in [1] and [2] for regulated dc–dc converter systems. When output impedance of the source is high, the negative incremental resistor behavior of the converter input impedance can lead the system to instability. As shown in Fig. 6, this behavior is observed in the Z_{dd} element of the VSC input impedance that also acts a constant power load [33], as a result of which instability can be induced in the ac system due to the negative resistance of Z_{dd}. Further, Fig. 6 also illustrates how the current controllers in the *d–d* and *q–q* channels of the VSC attenuate the impedance elements Z_{dq} and Z_{qd}. In consequence, instability is induced mainly due to the impedance interaction in the *d–d* channel [27], [33]. Recent work has also shown that since the PLL shapes the input impedance of the VSC, especially the *q–q* channel element, instability can also be induced in ac systems by impedance interactions across this channel [31], [32], [35]. In this paper, however, instability conditions are created solely through the *d–d* channel, and in order to ensure this, the PLL bandwidth is set to 1 Hz, which is very low with respect to the 400 Hz line frequency used.

TABLE II
FEEDBACK CONTROLLER PARAMETERS FOR VSI AND VSC

	VSI		VSC	
	Voltage loop	Current loop	Voltage loop	Current loop
Case 1	0.0495 + 130/s	0.0465 + 121/s	0.0462 + 4.58/s	0.0116 + 46.5/s
Case 2	0.0297 + 78.5/s			
Case 3	0.0158 + 41.9/s			

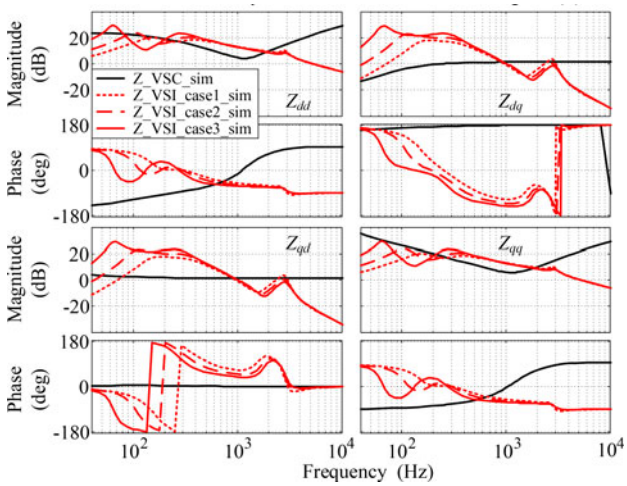

Fig. 7. Impedances of VSI and VSC for three cases from average model simulation.

C. Description of Experiments

The most intuitive way of making the system unstable is to increase the VSI output impedance, which can be accomplished by decreasing the bandwidth of its output voltage-control loop. In this study accordingly, the VSC control parameters were kept constant, and only the VSI voltage controller is adjusted to create stable and unstable conditions. Specifically, feedback controllers of VSI and VSC are list in Table II. Using the average models of VSI and VSC together with their controllers, three cases are considered as shown in Fig. 7, which are bode plots of VSI output impedances and VSC input impedance. As list in Table II, from case 1 to case 3, parameters of PI controller in VSI voltage control loop are decreased. As a result, output impedance of VSI increases from case 1 to case 3. Input impedance of VCS is kept unchanged from case 1 to case3. Using the simulated *d-q* impedances, characteristic loci ($\lambda_{1\_case1\_sim}$, $\lambda_{2\_case1\_sim}$) of return ratio (Z_VSI_case1_sim∗(Z_VSC_sim)$^{-1}$) which

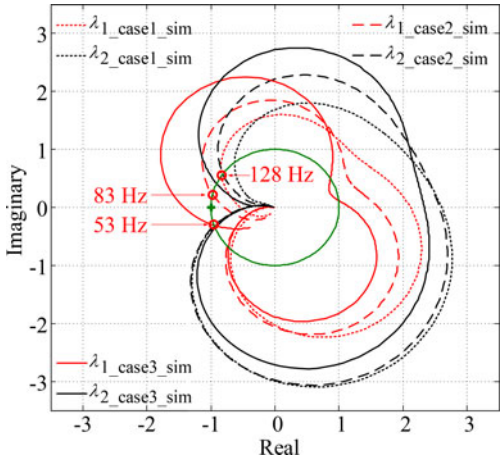

Fig. 8. Characteristic loci of three cases using simulated impedance from average model.

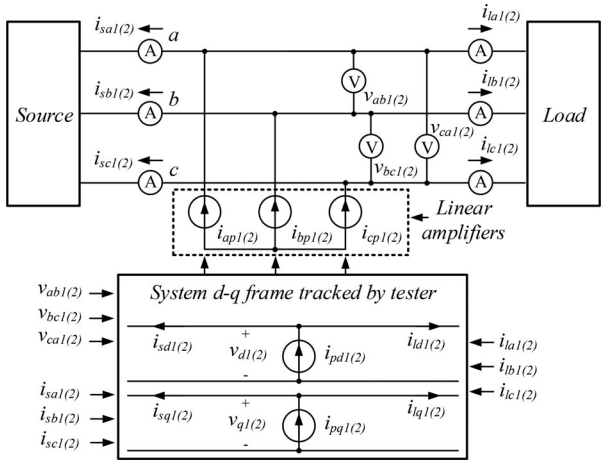

Fig. 10. *d-q* frame impedance measurement.

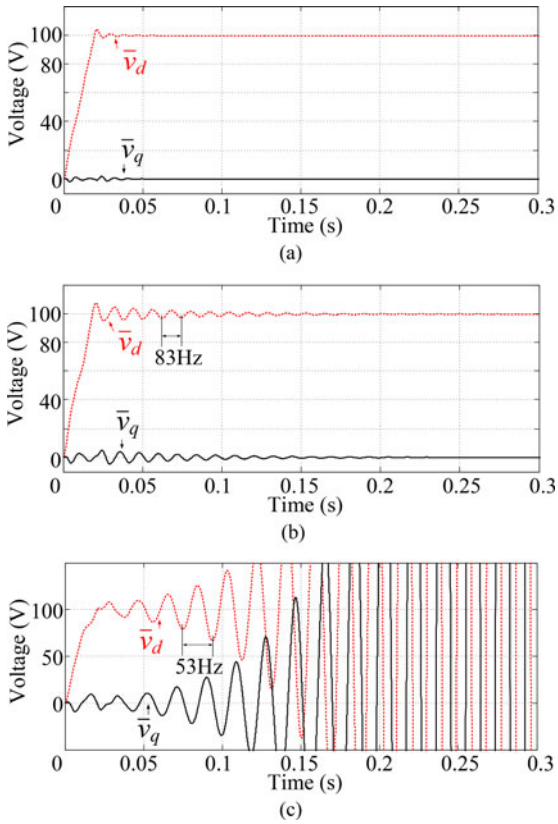

Fig. 9. Time-domain simulation of interface voltage in *d-q* frame: (a) case 1, (b) case 2, and (c) case 3.

are shown in Fig. 8 indicate the system is stable. Time-domain response of interface voltage when VSI is loaded by VSC in *d-q* frame, which is shown in Fig. 9(a), indicates the prediction of GNC is correct. In case 2, the loci indicate the system is still stable, but $\lambda_{1\_case2\_sim}$ is very close to the critical point, it intersects with the unit cycle at 83 Hz. This means there is a damped oscillation with 83 Hz in the system, and this is shown in the time-domain simulation results in Fig. 9(b). Case 3 is an unstable case. $\lambda_{1\_case3\_sim}$ encircles the critical point, it intersects with the unit cycle at 53 Hz. this means the time-domain response has an intensified oscillation with 53 Hz. This is verified by simulation results in Fig. 9(c).

V. *d-q* Frame Impedance Measurement

A. Algorithm

The measurement of impedances in the *d-q* frame needs special algorithms and equipment. This paper uses the impedance tester developed in [23] to measure the source and load impedances in the *d-q* frame. As shown in Fig. 10, the tester first tracks the system angle in order to align with the system *d-q* frame, then a sinusoidal perturbation signal with certain frequency is generated on the *d*-axis (i_{pd1}) while keeping the *q*-axis perturbation null ($i_{pq1}=0$), and then converted into the *abc*-frame by a real-time microcontroller. Three linear amplifiers, controlled by the same real-time microcontroller, act as current injection devices and inject the current perturbations into the system at the ac interface. The system responses, namely, the interface voltage and the currents of both source and load sides are measured and converted back into the *d-q* frame by the microcontroller. A second perturbation sequence is carried out then but perturbing the *q*-axis instead (i_{pq2}), with the *d*-axis components being zero ($i_{pd2}=0$), which completes a set of two system response signals in the *d-q* frame. These are

$$\begin{bmatrix} v_{d1} \\ v_{q1} \end{bmatrix}, \begin{bmatrix} i_{ld1} \\ i_{lq1} \end{bmatrix}, \begin{bmatrix} i_{sd1} \\ i_{sq1} \end{bmatrix}; \quad \begin{bmatrix} v_{d2} \\ v_{q2} \end{bmatrix}, \begin{bmatrix} i_{ld2} \\ i_{lq2} \end{bmatrix}, \begin{bmatrix} i_{sd2} \\ i_{sq2} \end{bmatrix} \tag{6}$$

$$\mathbf{Z_{ldq}} = \begin{bmatrix} Z_{ldd} & Z_{ldq} \\ Z_{lqd} & Z_{lqq} \end{bmatrix} \tag{7}$$

$$\mathbf{Z_{sdq}} = \begin{bmatrix} Z_{sdd} & Z_{sdq} \\ Z_{sqd} & Z_{sqq} \end{bmatrix}. \tag{8}$$

Let the subscripts 1 and 2 denote the variables measured during the two independent perturbations, and let (7) and (8)

be the definition of the source and load impedance in the *d-q* frame. Then, when measuring the load impedance $\mathbf{Z_{ldq}}$, the two perturbations yield

$$\begin{bmatrix} v_{d1} \\ v_{q1} \end{bmatrix} = \begin{bmatrix} Z_{ldd} & Z_{ldq} \\ Z_{lqd} & Z_{lqq} \end{bmatrix} \cdot \begin{bmatrix} i_{ld1} \\ i_{lq1} \end{bmatrix} \quad (9)$$

$$\begin{bmatrix} v_{d2} \\ v_{q2} \end{bmatrix} = \begin{bmatrix} Z_{ldd} & Z_{ldq} \\ Z_{lqd} & Z_{lqq} \end{bmatrix} \cdot \begin{bmatrix} i_{ld2} \\ i_{lq2} \end{bmatrix}. \quad (10)$$

Notice that since the system is the same, the impedance must remain unchanged. Then, (9) and (10) containing v_{d1} and v_{d2} can be regrouped as in (11), and the equations containing v_{q1} and v_{q2} can be regrouped as in (12)

$$\begin{bmatrix} v_{d1} \\ v_{d2} \end{bmatrix} = \begin{bmatrix} i_{ld1} & i_{lq1} \\ i_{ld2} & i_{lq2} \end{bmatrix} \cdot \begin{bmatrix} Z_{ldd} \\ Z_{ldq} \end{bmatrix} \quad (11)$$

$$\begin{bmatrix} v_{q1} \\ v_{q2} \end{bmatrix} = \begin{bmatrix} i_{ld1} & i_{lq1} \\ i_{ld2} & i_{lq2} \end{bmatrix} \cdot \begin{bmatrix} Z_{lqd} \\ Z_{lqq} \end{bmatrix}. \quad (12)$$

Equations (11) and (12), in turn, can similarly be regrouped as

$$\begin{bmatrix} v_{d1} & v_{d2} \\ v_{q1} & v_{q2} \end{bmatrix} = \begin{bmatrix} Z_{ldd} & Z_{ldq} \\ Z_{lqd} & Z_{lqq} \end{bmatrix} \cdot \begin{bmatrix} i_{ld1} & i_{ld2} \\ i_{lq1} & i_{lq2} \end{bmatrix}. \quad (13)$$

Then, the load impedance can be calculated as (14). A similar process is followed to derive the source impedance $\mathbf{Z_{sdq}}$ in (15)

$$\begin{bmatrix} Z_{ldd} & Z_{ldq} \\ Z_{lqd} & Z_{lqq} \end{bmatrix} = \begin{bmatrix} v_{d1} & v_{d2} \\ v_{q1} & v_{q2} \end{bmatrix} \cdot \begin{bmatrix} i_{ld1} & i_{ld2} \\ i_{lq1} & i_{lq2} \end{bmatrix}^{-1} \quad (14)$$

$$\begin{bmatrix} Z_{sdd} & Z_{sdq} \\ Z_{sqd} & Z_{sqq} \end{bmatrix} = \begin{bmatrix} v_{d1} & v_{d2} \\ v_{q1} & v_{q2} \end{bmatrix} \cdot \begin{bmatrix} i_{sd1} & i_{sd2} \\ i_{sq1} & i_{sq2} \end{bmatrix}^{-1}. \quad (15)$$

B. Measurement Setup

When the system shown in Fig. 3 is stable, both source and load impedances can be measured at once by connecting the tester to the ac interface of original system shown in Fig. 3. When the system is unstable, the system must be split at the ac interface in order to measure their impedances. To measure the output impedance of the VSI, the VSC is replaced by a three-phase resistor (R_l) of equal power as shown in Fig. 11(a). The *d-q* impedance tester is then inserted in between the VSI and the three-phase resistors. The setup for the VSC input impedance measurement is shown in Fig. 11(b), where in this case the VSI is replaced by a three-phase voltage source. A 0.5-Ω three-phase resistor (R_b) is additionally connected between the impedance tester and this voltage source in order to increase its total output impedance, which improves the measurement results. This is so since the voltage response (measurement) at the interface is larger when the impedance of the system is increased. The voltage source amplitude is then adjusted to make the VSC input voltage the same as when the source is the VSI. Actually, for system integration, impedances of source and load equipment are usually tested by suppliers separately using resistive load (for source converter) an ideal voltage source (for load converter) to check the system stability before they are connected by system integrator.

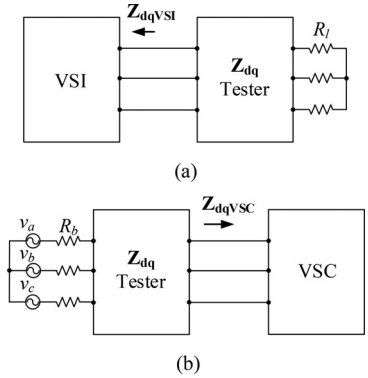

Fig. 11. Measurement setups: (a) VSI output impedance and (b) VSC input impedance.

In this paper, both the VSI output impedance and the VSC input impedance in the *d-q* frame were measured from 40 Hz to 10 kHz with 100 frequency points [23]. Because of frequency of instability in the electrical system under study, the measurement frequency range is chosen as such. The system line frequency is 400 Hz. Frequency of instability in the system under study is between 40 Hz to 10 kHz. For other applications, for example, 60 Hz system, instability could happen below 1 Hz, corresponding impedance testers should have the ability to measure impedance lower than 1 Hz. Upper limit of impedance measurement is chosen as half switching frequency of converters in the system, where the small-signal model extract from the system is still a good linear approximation of the system. In this paper the switching frequencies of VSI and VSC are 20 kHz, 10 kHz is set to be the upper limit of impedance measurement. For different application, switching frequency of power converter is different. For 60 Hz system where power rating could be megawatt and several kilo hertz could be the switching frequencies of most power converters. Then, impedance measurement up to 1 kHz is sufficient. For transportation electrical system, high switching frequency (over 20 kHz) is preferred to reduce the size of magnetic components, impedance measurement can be higher than 10 kHz.

VI. Experimental Results

Using the test-bed hardware prototype shown in Fig. 12, experimental results of three cases discussed before are shown in this section. Fig. 13 shows the measurement results of case 1, the stable case. Specifically, Fig. 13(a) shows the time-domain waveforms showing the rectifier starting up until it reaches steady state. Fig. 13(b) is the zoomed in view of the steady state waveforms. Fig. 13(c) shows the Bode plot of the impedance matrices, where it is clear that the *d–d* channel impedance (Z_{dd}) of the VSC is negative at lower frequencies. Using the measured impedances, the return-ratio matrix ($\mathbf{Z_{sdq}Y_{ldq}}$) is calculated and its characteristic loci is obtained as shown in Fig. 13(d). As evinced, none of the loci encircles the critical point ($-1 + j0$) indicating that the system is stable.

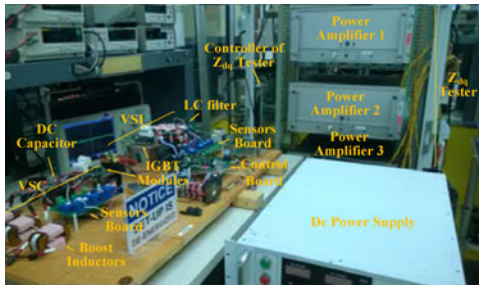

Fig. 12. Test-bed hardware prototype for experimental system.

The second test corresponds to case 2, the critical stable condition. Specifically, when the PI parameters of VSI voltage control loop are decreased, the system becomes less stable as it can be observed from the time-domain waveforms shown in Fig. 14(a). In effect, when the PWM control of the VSC starts, a damped oscillation with a frequency of 80 Hz can be found in the system. This was not observable in case 1. Nonetheless, the system is still stable according to the characteristic loci plot shown in Fig. 14(d), but the distance between the critical point $(-1 + j0)$ and the loci is less than that seen in case 1. Further, one of the characteristic loci $\lambda_{1\_case2\_exp}$ intersects the unit circle at 81.7 Hz approximately, which corresponds to the damped oscillation observed in time-domain waveforms.

Lastly, in case 3, the unstable condition, the PI parameters of VSI voltage control loop are further decreased. As shown in Fig. 15(a) the system becomes unstable as soon as the PWM control of the VSC starts. The characteristic loci plot in Fig. 15(d) agrees with this conclusion. In effect, when the PWM control of the VSC starts an unstable oscillation with frequency of 50 Hz appears in the system, which can be verified by the loci shown in Fig. 15(d), as the loci of $\lambda_{1\_case2\_exp}$ intersects the unit circle around 49.8 Hz.

As seen, the experimental results obtained from both time-domain and frequency domain show that the stability analysis based on measured impedances has good accuracy, which can be observed both in the impedance Bode plots and in the characteristic loci of the return-ratio matrix eigenvalues.

VII. Discussion

In Section IV, impedances extracted from average models can predict system stability accurately in simulation. This is shown by Figs. 7 and 8 in frequency domain and verified by Fig. 9 in time domain both in *d-q* frame. These results represent the original theory of stability analysis using GNC for balanced three-phase ac system. However, it has been observed that in practice, a lot of uncertainties exit which can influence the robustness of the analysis. GNC-based small-signal stability analysis for three-phase ac system requires: first, the three-phase ac system is balanced, second, *d-q* impedances of the practical system are measured accurately. Three is no ideal balanced three-phase ac system in practice. On the other hand, *d-q* impedance tester relays on PLL to track the system *d-q* frame and measure impedances. The accuracy of phase tracking influences the measurement accuracy of impedances and further the stability analysis.

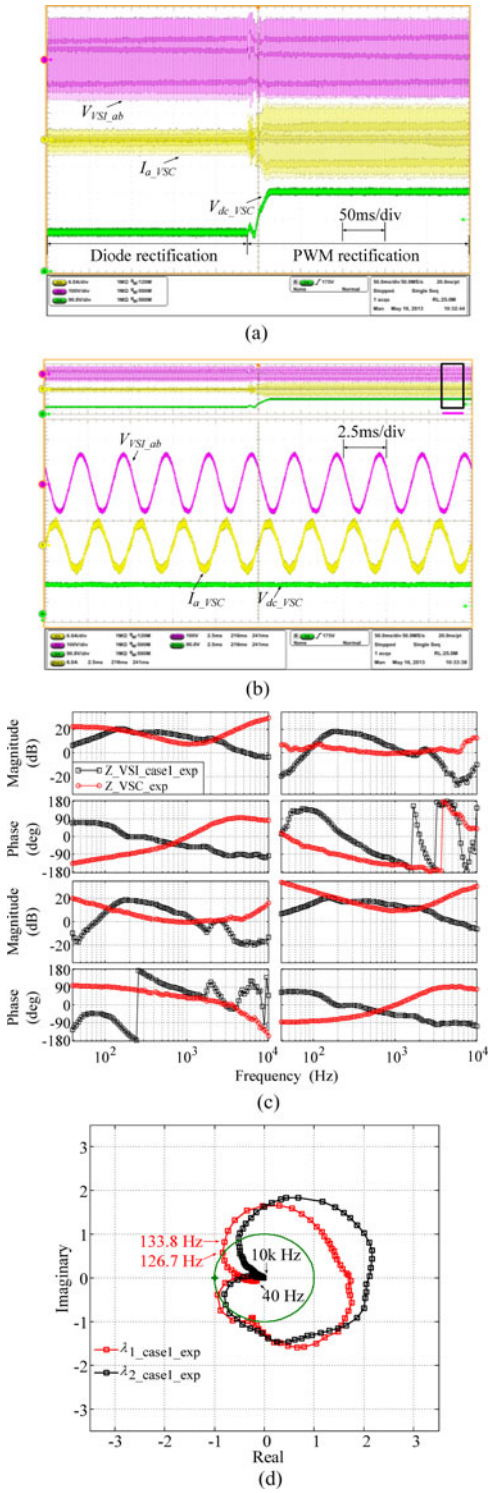

Fig. 13. Measurement results of case 1: (a) time-domain results; (b) zoomed in time-domain results; (c) *d-q* impedance; (d) characteristic loci plot. Interface *a* to *b* voltage ($V_{\mathrm{VSI\_}ab}$) (purple) (100 V/div), VSC phase *a* current (I_{a_VSC}) (yellow) (6 A/div), VSC output voltage ($V_{\mathrm{dc\_VSC}}$) (green) (90 V/div).

Unbalance of the experimental system in this paper is kept less than 1%. PLL bandwidth of *d-q* impedance tester utilized in this paper is 1 Hz to assure a good phase tracking accuracy. Under

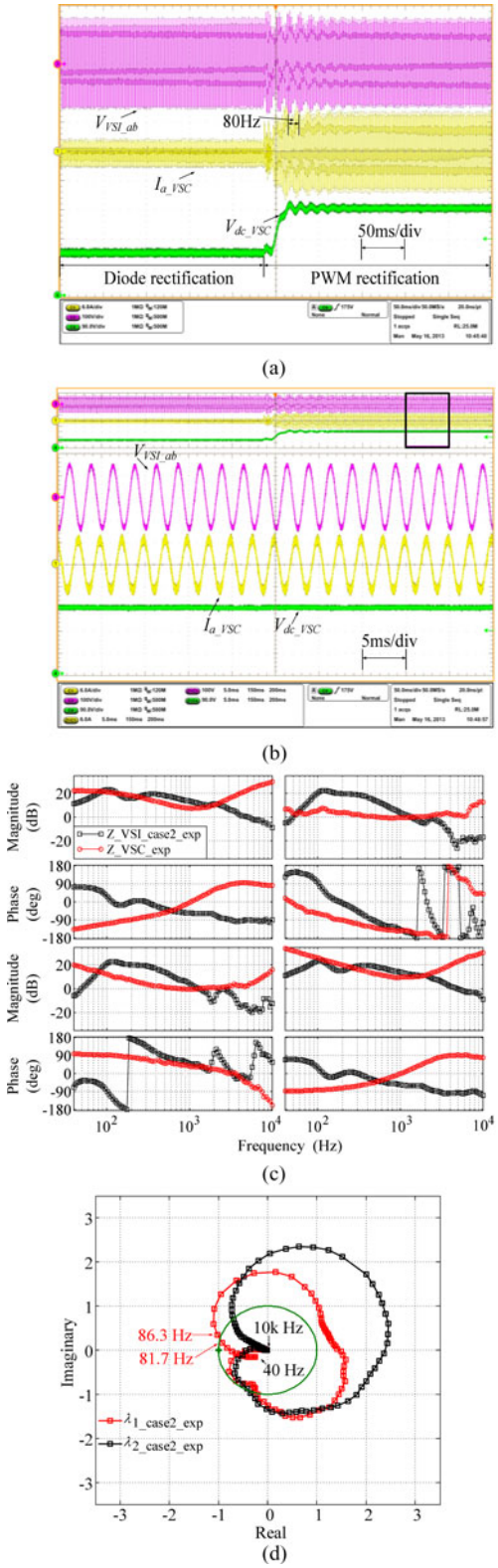

Fig. 14. Measurement results of case 2: (a) time-domain results; (b) zoomed-in time-domain results; (c) *d-q* impedance; (d) characteristic loci plot. Interface *a* to *b* voltage ($V_{\mathrm{VSI\_}ab}$) (purple) (100 V/div), VSC phase *a* current (I_{a_VSC}) (yellow) [6 A/div], VSC output voltage ($V_{\mathrm{dc\_VSC}}$) (green) [90 V/div].

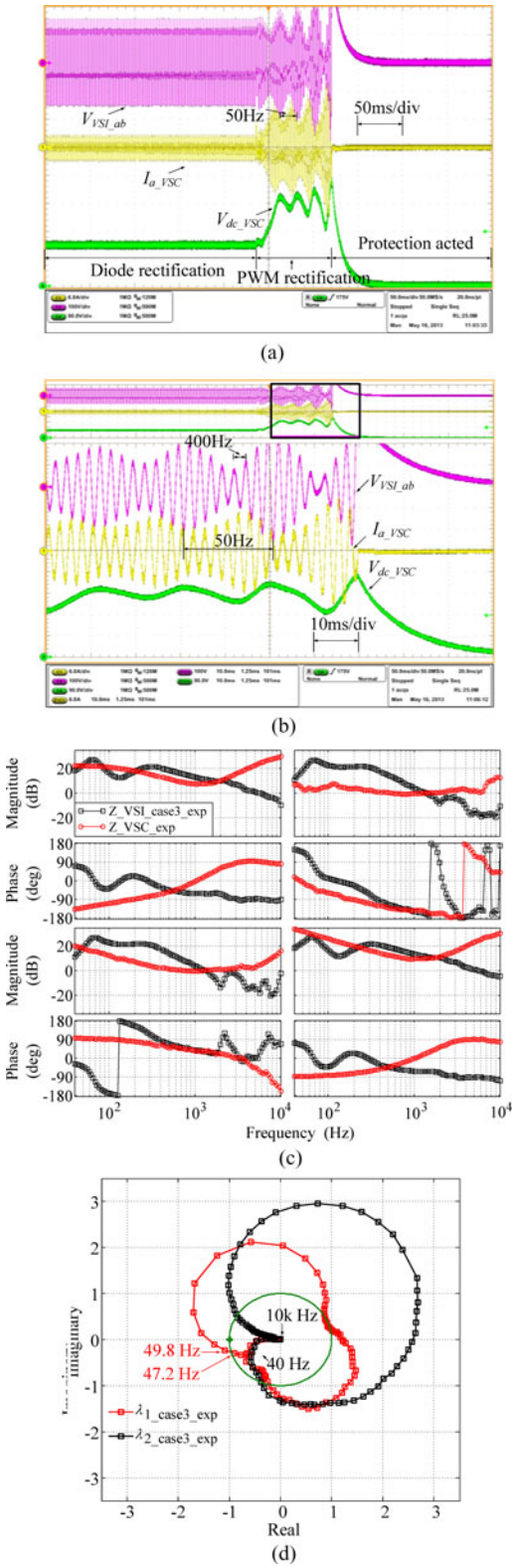

Fig. 15. Measurement results of case 3: (a) time-domain results; (b) zoomed in time-domain results; (c) *d-q* impedance; (d) characteristic loci plot. Interface a to b voltage ($V_{\mathrm{VSI\_}ab}$) (purple) (100 V/div), VSC phase *a* current (I_{a_VSC}) (yellow) (6 A/div), and VSC output voltage ($V_{\mathrm{dc\_VSC}}$) (green) (90 V/div).

such condition, stability prediction using GNC in experiments shows very good accuracy for the system under study. Still the paper does not study the robustness of the stability analysis using GNC, it is an important topic to be explored in the future.

When comparing the simulation results with experimental results, it can be found that, although they give same conclusion on the stability condition of the system under study, the oscillation frequencies of the system are different in the two studies. When comparing impedances of the system in high frequency, there are more differences between simulation and experimental results. In order to achieve such agreement between simulation and experimental results, a lot of model verification and validation work have been done. Model validation needs measurement of from real hardware. This paper presents for the first time, the small-signal stability analysis of three-phase ac system in the presence of constant power loads based on measured *d-q* frame impedances. This paper not only demonstrates the feasibility of using GNC in practice but also opens the door of model validation for stability analysis using GNC in three-phase ac system.

The experimental results also demonstrate that three-phase PWM rectifiers with output voltage control are constant power loads, when the source impedance is high, they can make the system unstable. From the experimental study, simple design guidance can be provided regarding ac system with controlled PWM rectifiers. First, in order to make the system stable, source impedance should be kept small. This can be achieved by increasing the voltage control bandwidth of the source as shown in this paper. Also, reducing the output voltage control bandwidth of the rectifier could also stabilize the system. Weak output voltage control reduces the frequency range of constant power load behavior of three-phase PWM rectifier, which consequently stabilizes the system.

Stability analysis using GNC relies on plotting characteristic loci of the system. Characteristic loci are calculated from impedances of source and load. Stability cannot be judged intuitively from impedances interaction as what has been done in dc system. Although some initial work has been reported to simplify stability analysis using GNC for three-phase system [27] under certain condition, more efforts are needed before simple design guidance can be provided based on impedances.

VIII. Conclusion

The impedance-based stability analysis has now been used for over 20 years in dc systems, having become an essential component of their design and integration. In effect, by using this method, system integrators can easily specify valid ranges for the impedance of components in order to ensure the system stability when using equipment from different suppliers. For ac systems, however, this method is still not common practice. Accordingly, this paper has strived to demonstrate the experimental accuracy of stability prediction in both frequency domain and time domain that can be attained in ac systems when using this approach. This has the potential to enable the use of impedance specification as a design tool for future ac systems. To this end, an experimental setup comprised of a VSI acting as ac source, and a three-phase boost rectifier acting as constant power load, was built. Three experiments were then conducted and analyzed, showing stable, critical stable, and unstable conditions by adjusting the control bandwidth of the source converter—modifying its output impedance. The corresponding ac impedances in the *d-q* frame of both source and load subsystems were then measured, and the GNC was applied, showing how both stable and unstable conditions could be effectively predicted and verified using this approach. Time-domain and frequency domain waveforms and plots were used to illustrate this.

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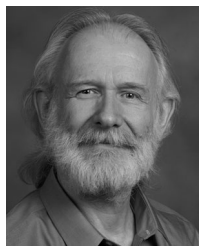
Bo Wen (S'11–M'15) received the B.S. degree from Xi'an Jiaotong University, Xian, China, in 2006, the M.S. and Ph.D. degrees from Virginia Tech, Blacksburg, USA, in 2011 and 2014 all in electrical engineering.

He is currently with Virginia Tech. His current research interests include multiphase power conversion, power electronics systems modeling, and stability analysis.



Dushan Boroyevich (S'81–M'86–SM'03–F'06) received the Dipl.Ing. degree from the University of Belgrade, Belgrade, Serbia, in 1976, and the M.S. degree from the University of Novi Sad, Novi Sad, Serbia, in 1982, in what then used to be Yugoslavia, and the Ph.D. degree from Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, USA, in 1986.

From 1986 to 1990, he was an Assistant Professor and the Director of the Power and Industrial Electronics Research Program in the Institute for Power and Electronic Engineering, University of Novi Sad. He then joined the Bradley Department of Electrical and Computer Engineering, Virginia Tech, as an Associate Professor, where he is currently the American Electric Power Professor in the Department and Co-director of the Center for Power Electronics Systems (CPES). His current research interests include multiphase power conversion, electronic power distribution systems, power electronics systems modeling and control, and multidisciplinary design optimization.

Prof. Boroyevich is a recipient of the IEEE William E. Newell Power Electronics Technical Field Award. He was the 2011–2012 President of the IEEE Power Electronics Society.

Rolando Burgos (S'96–M'03) received the B.S. degree in electronics engineering, the Electronics Engineering Professional degree, and the M.S. and Ph.D. degrees in electrical engineering from the University of Concepción, Concepción, Chile, in 1995, 1997, 1999, and 2002 respectively.

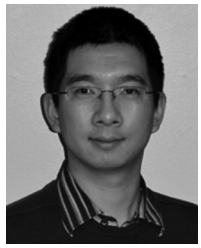
In 2002, he joined, as a Postdoctoral Fellow, the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA, becoming a Research Scientist in 2003 and a Research Assistant Professor in 2005. In 2009, he joined ABB Corporate Research, Raleigh, NC, USA, as a Scientist, becoming a Principal Scientist in 2010. In 2010, he was appointed Adjunct Associate Professor in the Electrical and Computer Engineering Department, North Carolina State University, working at the Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center. In 2012, he returned to Virginia Tech, where he is currently an Associate Professor in the Bradley Department of Electrical and Computer Engineering and CPES faculty. His current research interests include multiphase multilevel power conversion, grid power electronics systems, stability of ac and dc power systems, high power density power electronics, modeling, and control theory and applications.

Dr. Burgos is Member of the IEEE Power Electronics Society where he is currently an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE POWER ELECTRONICS LETTERS, and the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is also the Vice-Chair of the Power and Control Core Technologies Committee of the Power Electronics Society. He is also a Member of the IEEE Industry Applications Society and the IEEE Industrial Electronics Society.

Paolo Mattavelli (S'95–A'96–M'00–SM'10–F'14) received the Ph.D. degree (with Hons.) in electrical engineering from the University of Padova, Padova, Italy, 1995.

From 1995 to 2001, he was a Researcher at the University of Padova. From 2001 to 2005, he was an Associate Professor at the University of Udine, where he led the Power Electronics Laboratory. In 2005, he joined the University of Padova in Vicenza with the same duties. From 2010 to 2012, he was a Professor and a Member of the Center for Power Electronics Systems (CPES), Virginia Tech. He is currently (2014) a professor with the University of Padova. His current research interests include analysis, modeling and analog and digital control of power converters, grid-connected converters for renewable energy systems and microgrids, and high-temperature and high-power density power electronics. In these research fields, he has been leading several industrial and government projects.

Dr. Mattavelli was as an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2003 to 2012. From 2005 to 2010, he was the Industrial Power Converter Committee (IPCC) Technical Review Chair for the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS. For terms 2003–2006 and 2006–2009, he was a Member-at-Large of the IEEE Power Electronics Society's Administrative Committee. In 2005, 2006, and 2011, he received the Prize Paper Award in the IEEE Transactions on Power Electronics, and in 2007, the 2nd Prize Paper Award at the IEEE Industry Application Annual Meeting.



Zhiyu Shen (S'11–M'13) received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2004 and 2007, respectively, and the Ph.D. degree in electrical engineering from Virginia Tech, Blacksburg, USA, in 2013.

His is currently a Research Scientist in the Center for Power Electronics System (CPES), Virginia Tech. His current research interests include three-phase ac system impedance measurement, three-phase ac system small signal stability, high-frequency high-density converter design, and control system architecture in high-power converters.