Reliability Evaluation of Conventional and Interleaved DC–DC Boost Converters

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***Abstract*—Obviously for the correct operation of conventional boost converters, all components should work correctly. Interleaved boost converters having several stages, can be used to increase the reliability. So in this paper, a reliability comparison is done between the conventional boost converter and the interleaved structure. Two different operation modes are defined for the interleaved boost converter: half-power and full-power operation modes. The reliability calculation is based on the Markov model of the converters. The power loss effect of converter components on their failure rates, and therefore, on the reliability of converter has been assessed. For the first time different failure rates have been considered for different operation modes. Also a laboratory prototype of a two-stage interleaved boost dc–dc converter has been built up and the failure rate of components in different operation modes are calculated practically. Results show that in addition to other benefits, interleaved structure has higher reliability and as the power increases, there will be a decrease in the reliability.**

***Index Terms*—Interleaved dc–dc converters, power electronics, reliability.**

NOMENCLATURE

P_0^C	Occupational probability of state 0 for conventional boost converter.
P_1^c	Occupational probability of state 1 for conventional boost converter.
P_1^I	Occupational probability of state 1 for interleaved boost converter.
P_2^I	Occupational probability of state 2 for interleaved boost converter.
P_3^I	Occupational probability of state 3 for interleaved boost converter.
λ_L	The failure rate of inductor (failure/h).
λ_D	The failure rate of diode (failure/h).
λ_Q	The failure rate of power MOSFET (failure/h).
λ_{LH}	The failure rate of inductor in half-power operation mode (failure/h).
λ_{DH}	The failure rate of diode in half-power operation mode (failure/h).
λ_{QH}	The failure rate of power MOSFET in half-power operation mode (failure/h).
T_j	Junction temperature (°C).
λ_{LF}	The failure rate of inductor in full-power operation mode (failure/hours).
λ_{DF}	The failure rate of diode in full-power operation mode (failure/hours).
λ_{DF}	The failure rate of power MOSFET in full-power operation mode (failure/hours).
P_R	The probability that the fault management mechanism can manage the fault in case of fault occurrence.
$T_{\rm HS}$	Hot-spot temperature (°C).
T_C	The case temperature (°C).
T_a	Ambient temperature (°C).
θ_{JC}	Junction-to-case thermal resistance (°C/W).
P_D	The device's worse case power dissipation (W).
θ_{CA}	The thermal resistance between the case and ambient (°C/W).
ΔT	Average temperature rise above ambient (°C).
A	Radiating surface area of the case ($\rm in^2$).
v_T	On-state drain–source voltage of the switch (V).
$R_{\rm DS(on)}$	Drain–source on-state resistance of the switch (Ω).
v_F	Forward voltage of the diode.
r_D	On-state resistance of the diode.
$P_{D,\rm Switch}$	Average power dissipation on the switch in a switching period (W).
$P_{D,\rm Diode}$	Average power dissipation on the diode in a switching period (W).
$P_{D,\rm Inductor}$	Average power dissipation on the inductor (W).
I_L	Average current flowing into inductor (A).
$i_S(t)$	Instantaneous switch current (A).
$i_D(t)$	instantaneous diode current (A).
$i_L(t)$	Instantaneous inductor current (A).
λ_b	The basic failure rate.
π_T	The temperature factor.
π_A	The application factor.
π_Q	The quality factor.
π_E	The environmental factor.
π_S	The electrical stress factor.
π_C	The contact construction factor.

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I. INTRODUCTION

THE last decades have generated extremely strong forces for the advancement of reliable products beyond the current state of the art. The obvious technical requirements of military forces and space programs have resulted in a need for vastly improved reliability in machinery components. Power electronic converters are broadly used in these applications and are considered a critical reliability concern. With the features continually being improved for semiconductor power components, almost all the power electronic converters are based on semiconduc-

tor switches. But in case of failure, the semiconductor power devices are the weakest components in power converters.

There has been a little research on the reliability of power electronics. The authors in [1] and [2] have conducted surveys on the reliability of power electronic systems. The reliability prediction and modeling of high-power switches (IGBTs and MOSFETs) has been studied in some works [3]–[8]. In [9], a review on the improvement of reliability of capacitors for dc link in power electronic converters is presented. The reliability calculation of multilevel converters is studied in [10]. Also [11] presented reliability comparison of power electronic converters for grid-connected 1.5-kW wind energy converter systems.

In order to increase the power processing capability and to improve the reliability of the power electronic system, interleaved converters are one of the recent research issues in power electronics engineering. Many articles have studied different aspects of interleaved boost converters. For instance, development of a high-efficiency dual-input interleaved dc–dc converter for reversible power sources to convert low-voltage reversible power sources to a high-voltage dc bus individually or simultaneously by the phase-shift control is studied in [12]. A novel multidevice interleaved boost converter that interfaces the fuel cell with the powertrain of hybrid electric vehicles is proposed in [13]. A fault-diagnostic method is introduced in [14] for a three-phase interleaved dc–dc converters using only the dc-link current derivative sign features. To achieve high step-up gain, an interleaved winding-coupled boost converter is proposed in [15]. A two-phase interleaved boost converter is used as critical conduction mode power factor corrector in [16], which uses a variation-tolerant phase shifter to ensure accurate 180° phase shift between the two interleaved converters. Application of interleaved dc–dc boost converters for the photovoltaic generation system is studied in [17] and a maximum power point tracking controller is proposed in [18]. Yet, reliability modeling, calculations, or comparisons have not been researched in these previous publications.

This paper calculates the reliability of interleaved boost dc–dc converter and presents a comparison with the reliability of the conventional boost converter. Two different operation scenarios (half-power and full-power operation) are considered for the interleaved converter. The failure rate of converter components are calculated for different operation scenarios. Also the power loss effect on the failure rate of components and on the reliability of converters is discussed. Finally, a two-stage prototype of interleaved boost dc–dc converter is built up and the failure rates of components are calculated for the practical results.

II. Markov Reliability Model Development

One very important technique between the several analytical techniques for evaluating the reliability of systems that has received considerable attention and use during the past few years is known as the Markov approach. The Markov approach will be applicable if the behavior of the system is characterized by a lack of memory.

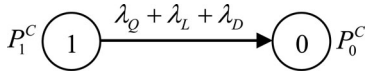


Fig. 1. Conventional boost converter.

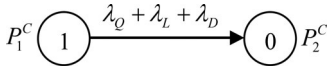


Fig. 2. Markov chain of the conventional boost converter.

Markov chains are defined as restricted class of stochastic processes $\{X_{\rm n}\}$ with finite or denumerable state-space *S* if for any positive integers *k, n, k* ≤ *n,* and for any choice of states i_0, ..., i_{n+1} in *S*, we have

$$\begin{aligned} &\mathrm{P}(X_{n+1} = i_{n+1} | X_n = i_n, ..., X_{k+1} = i_{k+1}, X_k = i_k) \\ &\quad = \mathrm{P}(X_n = i_n). \end{aligned} \tag{1}$$

The Markov reliability models of the conventional and interleaved dc–dc boost converters are presented in this section.

A. Conventional Boost Converter

A traditional boost converter simply consists of an inductor, a switch, and a diode. Fig. 1 shows the circuit diagram of a conventional boost converter and Fig. 2 shows its Markov chain diagram. Two states can be identified: the state in which all the components are healthy (state 1) and the state in which converter fails (state 0). The Markov chain transition from state 1 to 0 is $\lambda_Q + \lambda_L + \lambda_D$. According to Fig. 2, the occupational probabilities are given by

$$\frac{d}{dt}\begin{bmatrix} P_1^C \\ P_0^C \end{bmatrix} = \begin{bmatrix} -(\lambda_Q + \lambda_L + \lambda_D) & 0 \\ \lambda_Q + \lambda_L + \lambda_D & 0 \end{bmatrix} \begin{bmatrix} P_1^C \\ P_0^C \end{bmatrix}. \tag{2}$$

Assuming that the first state is where the chain begins, the initial condition of the aforementioned equation is

$$P(0) = [1 \quad 0]. \tag{3}$$

Considering the initial condition, one can find the reliability function of the interleaved configuration

$$R^c(t) = e^{-(\lambda_Q + \lambda_L + \lambda_D)t}. \tag{4}$$

B. Interleaved Boost Converter

A simplified block diagram of an *n*-stage interleaved boost converter is shown in Fig. 3. Each stage consists of an inductor L_i, a diode D_i, and a switch Q_i, where *i* is the stage number $(i = 1, 2, \ldots, n)$. In this study, a two-stage interleaved boost converter has been considered to calculate its relative reliability. Fig. 4 shows the Markov chain diagram for an interleaved configuration with two stages. Since both stages operate at the same voltage and current levels, they can be identical. Three states can be identified: 1) the state in which both stages are healthy (state 11); 2) the state in which the one of the state's failed, was detected, and was isolated, but the other stage is still

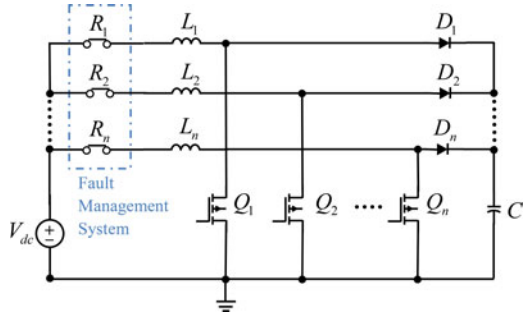


Fig. 3. *n*-stage interleaved boost converter.

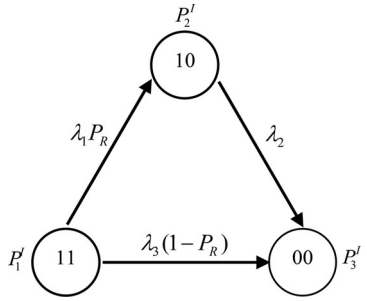


Fig. 4. Markov chain of two-stage interleaved boost converter.

healthy (state 10); and 3) the final state in which the whole configuration failed (state 00). These states and their occupational probabilities P_1^I, P_2^I, and P_3^I are shown in Fig. 4. The rate at which the Markov chain transitions from state 11 to state 10 (one stage fails and the other stage works) is $\lambda_1 P_R$. The rate at which the Markov chain transitions from state 11 to state 10 (one stage fails and the other stage works) is λ_2. The rate at which the Markov chain transitions from state 11 to state 00 is $\lambda_3(1-P_R)$.

According to Fig. 4, the evolution of the occupational probabilities is governed by

$$\frac{d}{dt}\begin{bmatrix} P_1^I \\ P_2^I \\ P_3^I \end{bmatrix} = AP(t) = \begin{bmatrix} -\lambda_1 P_R - \lambda_3(1-P_R) & 0 & 0 \\ \lambda_1 P_R & -\lambda_2 & 0 \\ \lambda_3(1-P_R) & \lambda_2 & 0 \end{bmatrix} \begin{bmatrix} P_1^I \\ P_2^I \\ P_3^I \end{bmatrix}. \tag{5}$$

where A is the transition matrix.

Assuming that the first state is where the chain begins, the initial condition of the aforementioned equation is

$$P(0) = [1 \quad 0 \quad 0]. \tag{6}$$

TABLE I
FAILURE RATE MODELS

MOSFET	$\lambda_{\mathrm{MOSFET}} = \lambda_b \pi_T \pi_A \pi_Q \pi_E$
Diode	$\lambda_{\mathrm{Diode}} = \lambda_b \pi_T \pi_S \pi_C \pi_Q \pi_E$
Inductor	$\lambda_{\mathrm{Inductor}} = \lambda_b \pi_T \pi_Q \pi_E$

Considering the initial condition, one can find the reliability function of the interleaved configuration

$$R(t) = 1 - P_3^I = -\frac{(\lambda_2 - \lambda_3(1-P_R))e^{-(\lambda_1 P_R + \lambda_3(1-P_R))t} - \lambda_1 P_R e^{-\lambda_2 t}}{\lambda_1 P_R + \lambda_3(1-P_R) - \lambda_2}. \tag{7}$$

Two scenarios are studied to access the Markov reliability model of the interleaved boost converter. In the first scenario, it is assumed that after the failure of one of the stages, the other stage continues with the half-power operation, i.e., the failure rate of its components does not change. In the second scenario, it is assumed that after the failure of one of the stages, the other one operates at full power.

1) First Scenario (Half-Power Operation): In the first scenario, when a fault occurs and one of the stages fails, the other stage continues to operate with half power. This means that $\lambda_1 = \lambda_3 = 2\lambda_2$. Also we have $\lambda_1 = 2(\lambda_{QH} + \lambda_{DH} + \lambda_{LH})$ in this scenario.

2) Second Scenario (Full-Power Operation): In this scenario, when a fault occurs and one stage fails, the other one operates with full power. So the failure rate of the stage before and after the fault will differ. In this scenario, λ_1, λ_2, and λ_3 are defined as $\lambda_1 = 2(\lambda_{QH} + \lambda_{DH} + \lambda_{LH})$, $\lambda_2 = \lambda_{QF} + \lambda_{DF} + \lambda_{LF}$, and $\lambda_3 = 2(\lambda_{QH} + \lambda_{DH} + \lambda_{LH})$, respectively. It is clear that λ_2 is different in the two scenarios described previously. Precise calculation of λs is necessary for reliability calculation of converters. As a result, in the next sections, a detailed analysis of the failure rate of components and their affecting factors is done.

III. PARAMETERS AFFECTING THE FAILURE RATE

According to MIL-HDBK-217F [19], the failure rate for a microelectronic part is

$$\lambda_{\mathrm{part}} = \lambda_b \prod_{i=1}^{n} \pi_i \tag{8}$$

where n is the number of π factors that affect the part's failure rate.

The basic failure rate (λ_b) is usually expressed by a model relating the influence of electrical and temperature stresses on the part. The failure rate models for different parts of the boost converter (power MOSFET, diode, and inductor) are represented in Table I. As temperature rises, the failure rate increases; in other words, the probability to fail rises. Moreover, the temperature factor π_T is a function of the device junction temperature T_j

TABLE II
TEMPERATURE FACTOR OF THE PARTS

MOSFET	$\pi_T = \exp\left[-1925\left(\frac{1}{T_j+273}-\frac{1}{298}\right)\right]$
Diode	$\pi_T = \exp\left[-3091\left(\frac{1}{T_j+273}-\frac{1}{298}\right)\right]$
Inductor	$\pi_T = \exp\left[\frac{-0.11}{8.617\times10^{-5}}\left(\frac{1}{T_{\rm HS}+273}-\frac{1}{298}\right)\right]$

(for MOSFET and diode) or the hot-spot temperature $T_{\rm HS}$ (for inductor). The temperature factor π_T for different parts of the boost converter (power MOSFET, diode, and inductor) is listed in Table II.

The failure rate also depends on the application of the device in the circuit. The quality and the type of materials used in the fabrication of the device affects its failure rate. For more details about quality factor, one can refer to MIL-S-19500 [20]. Environment of operation is also effective in the failure rate of a device. For instance, a device operating on the ground will have different π_E than a device operating in space. In this paper, the environment for all parts is assumed to be ground benign (G_B), so $\pi_E = 1$ is considered in the reliability calculations. The electrical stress factor for a diode is affected by its voltage stress ratio V_S, which is the ratio of reverse voltage applied to rated reverse voltage. Also for a diode, if it is metallurgically bonded, the contact construction factor will be $\pi_C = 1$; otherwise $\pi_C = 2$.

Except the temperature factor, the other factors are constant in all of the calculated converter circuits (conventional boost, half-power, and full-power interleaved boost converters) and considered the same. Therefore, in the next section a detailed analysis of temperature factor is presented.

IV. TEMPERATURE EFFECT

In this section, the objective is to study temperature effect on the junction temperature T_j, and thereby, on the part failure rate with more details.

Junction temperature for semiconductor devices should be computed based on worst case power (or maximum power dissipation) and the device junction to case thermal resistance. The case temperature should be determined from a detailed thermal analysis of the equipment. The following equation is the relationship to calculate device junction temperature

$$T_j = T_C + \theta_{JC} P_D. \tag{9}$$

Furthermore, the case temperature T_C is expressed as

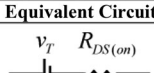
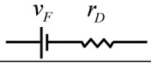
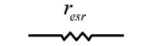
$$T_C = T_a + \theta_{CA} P_D. \tag{10}$$

When a heat sink is used, the junction-to-case thermal resistance and the case-to-ambient thermal resistance will be replaced with the thermal resistance of the heat sink.

Also for the inductor, the hot-spot temperature is a function of its power dissipation and radiating surface area of the case. The relations are

$$T_{\rm HS} = T_a + 1.1\,\Delta T \tag{11}$$

TABLE III
EQUIVALENT CIRCUIT MODEL AND RELATIVE POWER LOSS RELATIONS OF BOOST CONVERTER COMPONENTS

	Equivalent Circuit	Power Loss
MOSFET		$P_D = i_S^2(t)R_{DS(on)} + i_S(t)v_T$
Diode		$P_D = i_D^2(t)r_D + i_D(t)v_F$
Inductor		$P_D = r_{esr} i_L^2(t)$

$$\Delta T = 125\,P_D/A. \tag{12}$$

Since the power loss is the only parameter that affects the temperature factor in the test case systems, next section is devoted to power loss analysis and its effect on temperature factor and the failure rate of boost converter components.

V. POWER LOSS EFFECT

The equivalent circuit diagram of boost converter components and their relative relations with power loss are shown in Table III. The output voltage of the converter is regulated. Therefore, as the power flowing from the device increases, its corresponding current and power dissipation will rise. According to (9)–(12), it can be concluded that higher power dissipation (P_D) yields to higher T_j, T_C, and T_a temperatures, which directly increases the value of corresponding π_T. All in all, an increment in power will result in an increase in the failure rate of parts.

According to the aforementioned explanations, we have $\lambda_{QH} < \lambda_{QF}$, $\lambda_{DH} < \lambda_{DF}$, and $\lambda_{LH} < \lambda_{LF}$ for the interleaved boost converter.

Neglecting the converter's switching loss, for the boost converter, we have following equations in a switching period:

$$\begin{aligned} P_{D,\rm Switch} &= \frac{1}{T_S}\int_0^{T_S} \left(v_T + R_{\rm on} i_S(t)\right) i_S(t) dt \\ &= D\left(v_T + R_{\rm on} i_S(t)\right) i_S(t) \end{aligned} \tag{13}$$

$$\begin{aligned} P_{D,\rm Diode} &= \frac{1}{T_S}\int_0^{T_S} \left(v_F + r_d i_D(t)\right) i_D(t) dt \\ &= (1-D)\left(v_F + r_d i_D(t)\right) i_D(t). \end{aligned} \tag{14}$$

Assuming that $i_L(t) \approx I_L$, we have

$$0 < t < DT_S \begin{cases} i_S(t) = I_L \\ i_D(t) = 0 \end{cases} \tag{15}$$

and

$$DT_S < t < T_S \begin{cases} i_S(t) = 0 \\ i_D(t) = I_L. \end{cases} \tag{16}$$

Fig. 5 shows the failure rate of MOSFET, diode, and inductor versus the power dissipation on them. According to this figure, it is obvious that the switch is the weakest one in case of fault occurrence.

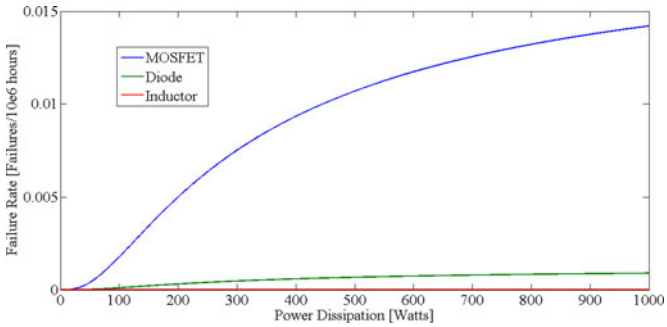


Fig. 5. Comparison of failure rates of boost converter components.

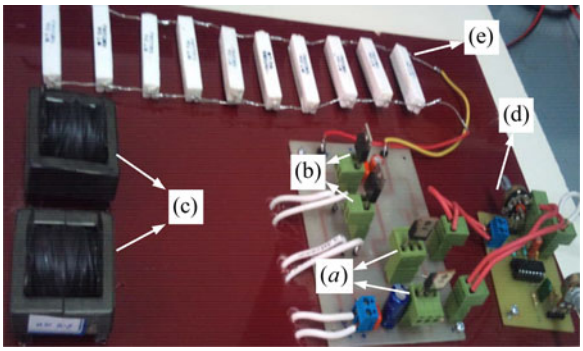


Fig. 6. Laboratory prototype of the two-stage interleaved dc–dc boost converter. (a) MOSFETs. (b) Diodes. (c) Inductors. (d) Control Circuit. (e) Load.

VI. Comparing Reliabilities

The reliability of systems is a good measure to compare their expected lifetime. As discussed in the previous sections, the failure rate of power electronic devices depends on the mission time and their power dissipation.

Before the comparative analysis of the reliabilities, a two-stage interleaved dc–dc boost converter is built to determine its operation modes. Every aspect of the two stages is identical. The circuit parameters and the manufacturer number of converter components are given in Appendix. Fig. 6 shows the experimental setup of the two-stage interleaved dc–dc boost converter.

Fig. 7 shows the converter operating in normal condition. So both stages are operating correctly. The input voltage of 27 V is boosted to the output of 40 V as shown in Fig. 7(a). The current of the inductor is shown in Fig. 7(b). Fig. 7(c) shows the drain–source voltage of the switches and it can be seen that the switches of the two stages are in 180° phase shift. The duty cycle is $D = 0.41$ and current flowing from each stage is 0.8 A.

Fig. 8 shows the half-power operation mode of the converter. One of the stages has failed and the other one is still working. In order to decrease the output power to its half value, the output voltage has been decreased to its $1/\sqrt{2}$ by means of the duty cycle. The input voltage of 27 V is boosted to 30 V as shown in Fig. 8(a). The inductor's current and the drain–source voltage of the switch are shown in Fig. 8(b) and (c), respectively. The duty cycle in this operation mode is $D = 0.17$. The current flowing from the working stage is 0.9 A.

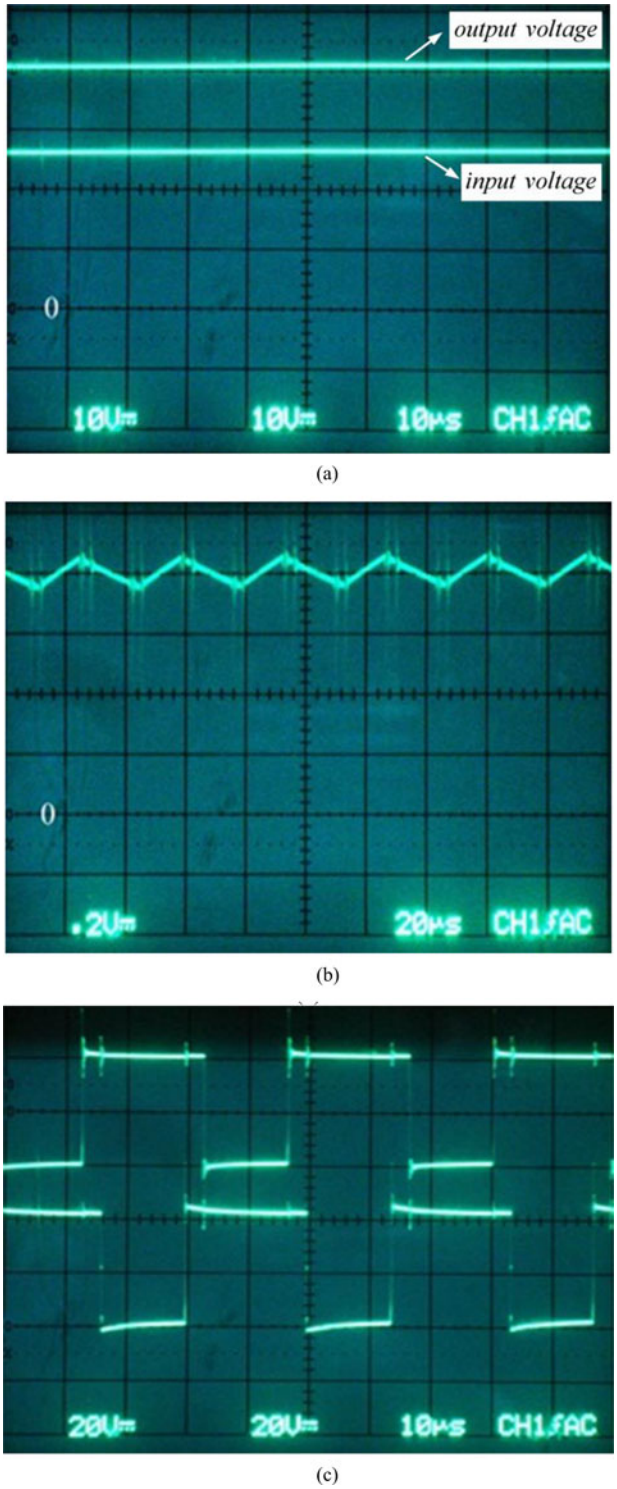


Fig. 7. Normal operation mode of the interleaved dc–dc boost converter: (a) input and output voltages, (b) first stage's input current ripple, and (c) drain–source voltage of the switches.

Using the relations given in Table III and (13)–(16), power dissipations on the individual components in this scenario are as follows.

Switch power dissipation

$$P_{D,\mathrm{Switch}} = 0.17(0.5 + 0.4 \times 0.9) \times 0.9 = 0.13 \text{ W}.$$

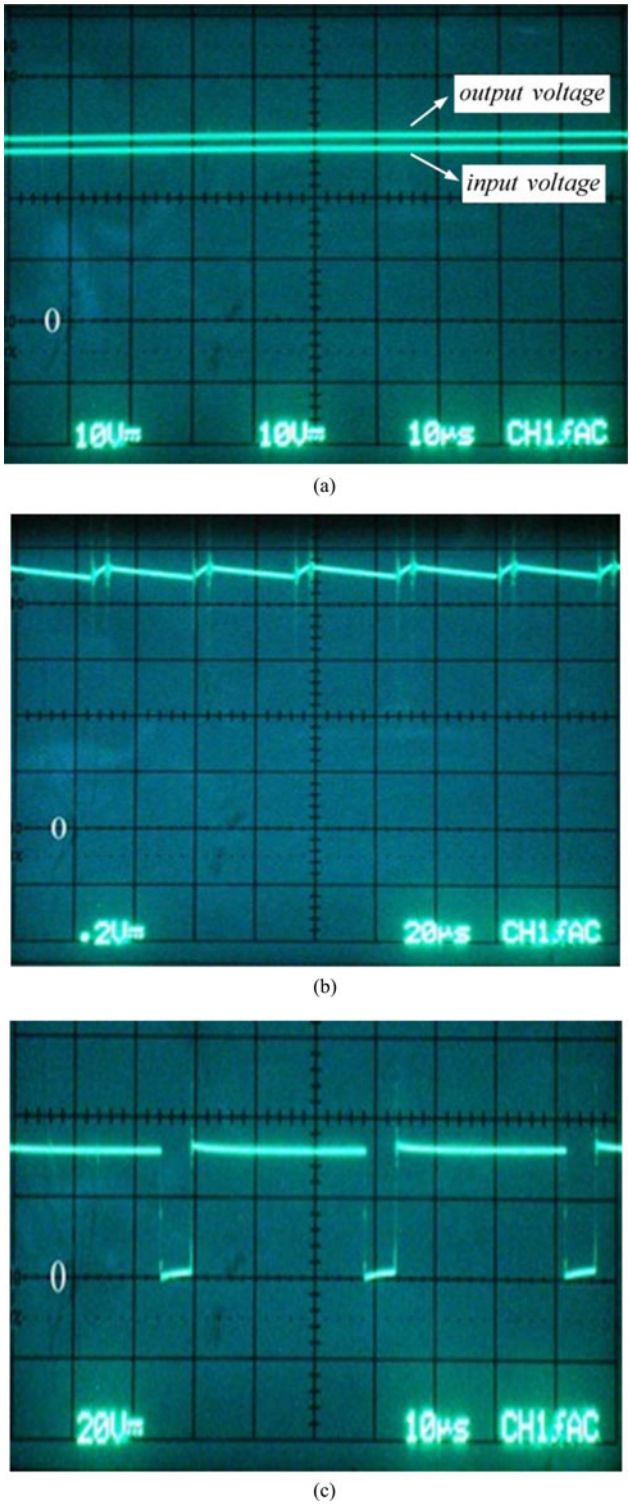


Fig. 8. First scenario: half-power operation mode of the interleaved dc–dc boost converter: (a) input and output voltages, (b) first stage's input current ripple, and (c) drain–source voltage of the switches.

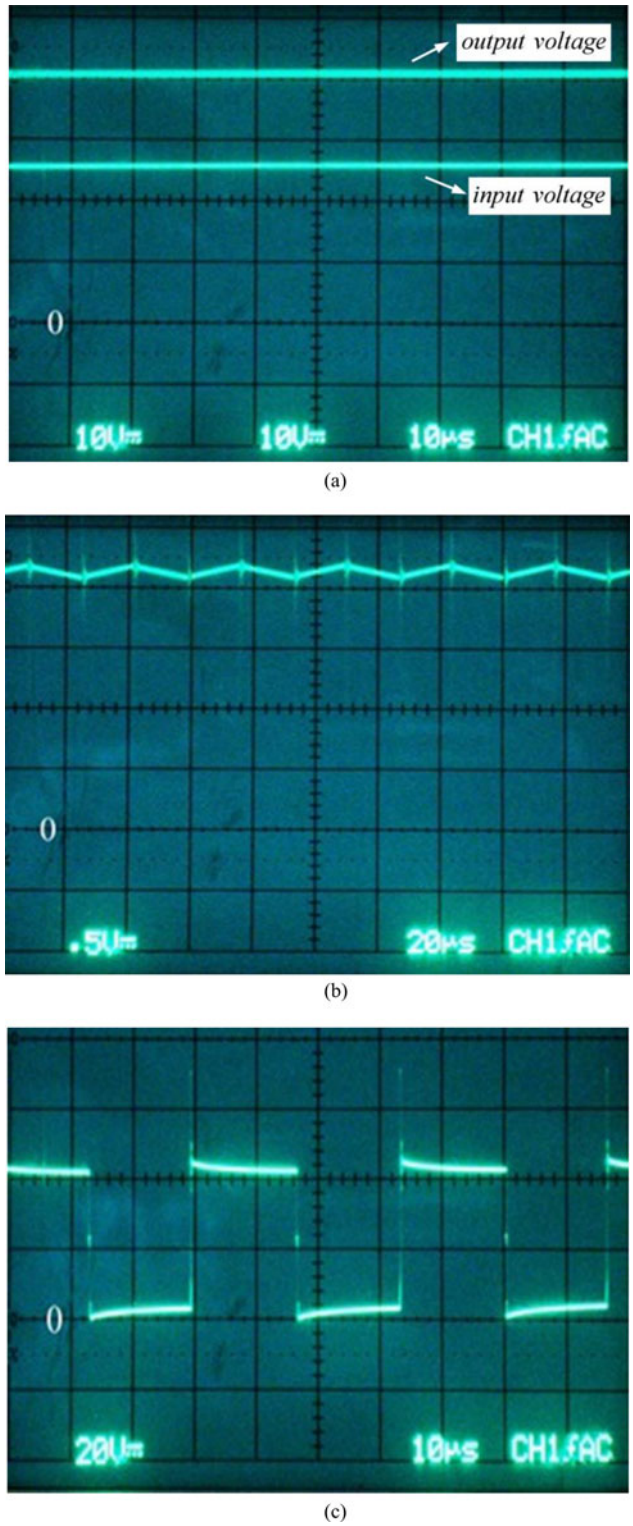


Fig. 9. Second scenario: half-power operation mode of the interleaved dc–dc boost converter: (a) input and output voltages, (b) first stage's input current ripple, and (c) drain–source voltage of the switches.

Diode power dissipation

$$P_{D,\mathrm{Diode}} = (1 - 0.17)(0.5 + 0.2 \times 0.9) \times 0.9 = 0.51 \text{ W}.$$

Inductor's power loss

$$P_{D,\mathrm{Inductor}} = 0.8 \times 0.9^2 = 0.65 \text{ W}.$$

In this scenario, the failure rates of the aforementioned components are $\lambda_{\mathrm{MOSFET}} = 7.8846 \times 10^{-7}$, $\lambda_{\mathrm{Diode}} = 1.2025 \times 10^{-7}$, and $\lambda_{\mathrm{Inductor}} = 4.1972 \times 10^{-10}$, respectively.

The operation of the interleaved boost converter in the full-power scenario is shown in Fig. 9. As shown in Fig. 9(a), the

TABLE IV
CONSIDERED PARAMETER VALUES USED FOR RELIABILITY CALCULATIONS

	λ_b	Junction to case thermal resistance [°C/W]	$T_a\,[^\circ C]$	P_D [W] Full-power Operation	P_D [W] Half-power Operation	π_Q Quality Factor	π_E Environmental Factor
MOSFET	0.06	10	25	3.1	0.2	1	1
Diode	0.0038	10	25	1.45	0.5	1	1
Inductor	0.00003	–	25	3.5	0.6	1	1

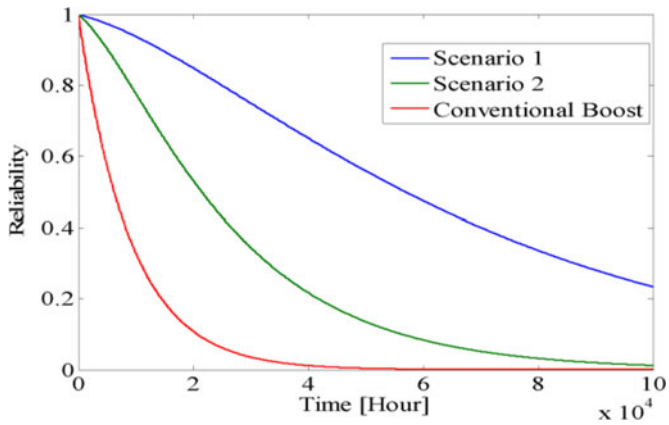


Fig. 10. Comparison of reliabilities of conventional and interleaved boost converters.

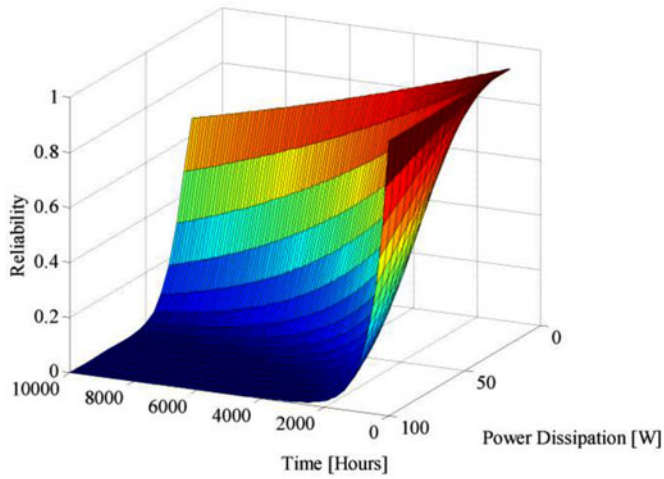


Fig. 11. Conventional boost converter.

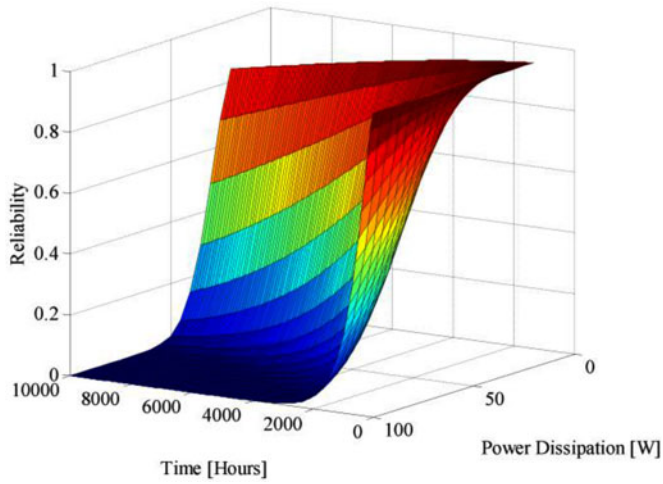


Fig. 12. Interleaved boost converter.

input voltage of 27 V is boosted to 40 V with a duty ratio of $D = 0.48$. Fig. 9(b) shows that value of the current flowing through the operating stage is 2.1 A. The drain–source voltage of the switch is also shown in Fig. 9(c).

According to Table III and (13)–(16), power dissipations on the individual components in this scenario are as follow.

Switch power dissipation

$$P_{D,\mathrm{Switch}} = 0.48 \times (2 + 0.5 \times 2.1) \times 2.1 = 3.1\ \mathrm{W}.$$

Diode power dissipation

$$P_{D,\mathrm{Diode}} = (1 - 0.48) \times (0.7 + 0.3 \times 2.1) \times 2.1 = 1.45\ \mathrm{W}.$$

Inductor's power loss

$$P_{D,\mathrm{Inductor}} = 0.8 \times 2.1^2 = 3.5\ \mathrm{W}.$$

In this scenario, the failure rates of the aforementioned components are $\lambda_{\mathrm{MOSFET}} = 3.5025 \times 10^{-5}$, $\lambda_{\mathrm{Diode}} = 5.7607 \times 10^{-7}$, and $\lambda_{\mathrm{Inductor}} = 4.5092 \times 10^{-10}$, respectively.

The values of the parameters considered in the reliability calculations are presented in Table IV. Fig. 10 shows the reliabilities of the conventional and interleaved boost converters. For the interleaved converter, the reliability of both scenarios described in Section II is calculated. As the interleaved converter has two stages, we can consider it as a conventional boost converter with a redundant stage in parallel.

Figs. 11 and 12 show the effect of mission time and power dissipation on the reliability of the converters, for the conventional and interleaved structures, respectively. The power dissipation of each component is considered to vary between 20 and 100 W. It is understood that in low power and small mission times, the reliability is very high. As the mission time and power dissipation on each component increases, the reliability drops. Comparing Figs. 11 and 12, it is clear that for a specific mission time, the reliability drop in the conventional boost converter is higher than the reliability drop of the interleaved boost converter.

VII. CONCLUSION

The reliability of the conventional and interleaved dc–dc boost converters have been presented. For the interleaved structure, half-power and full-power operating scenarios have been considered. The effect of power loss has been assessed on the

temperature, which is a stress factor in the reliability analysis. Then, the failure rate of converter components has been calculated based on their power loss in different scenarios. The results show that with an increase in power, the reliability of components, and thereby, the reliability of the whole converter decreases. Also the interleaved boost converter operating in both scenarios is more reliable in comparison to the conventional boost converter.

APPENDIX

The circuit parameters of the converter's components used in each stage are as follows: $R_{(\mathrm{on}),\mathrm{MOSFET}} = 0.55\ \Omega$, $\theta_{JC,\mathrm{MOSFET}} = 1\ ^\circ\mathrm{C/W}$, $\theta_{JA,\mathrm{MOSFET}} = 62\ ^\circ\mathrm{C/W}$, IRF740 MOSFETs, $\theta_{JC,\mathrm{Diode}} = 1.5\ ^\circ\mathrm{C/W}$, $\theta_{JA,\mathrm{Diode}} = 73\ ^\circ\mathrm{C/W}$, MUR1560 diodes, and $L = 3.5$ mH with $r_{\mathrm{esr}} = 0.8\ \Omega$. Also a 39-$\Omega$ resistor (ten 390-Ω resistors are paralleled) is used for the load. The switching frequency (f_s) is about 30 kHz. The currents are measured with a resistance of 1 Ω.

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