Letters

A Secondary-Side Phase-Shift-Controlled *LLC* Resonant Converter With Reduced Conduction Loss at Normal Operation for Hold-Up Time Compensation Application

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***Abstract*—A novel secondary-side phase-shift-controlled (SS-PSC) *LLC* resonant converter is proposed for applications requiring hold-up time operation, such as distributed power systems and server power supplies. High efficiency at the normal input voltage is achieved because the proposed SS-PSC *LLC* converter always operates at the series-resonant frequency of the resonant tank. The magnetizing inductor of the proposed converter does not need to be reduced to provide desired voltage boost ratio for the hold-up time operation, which results in reduced conduction losses and improved efficiency. Sufficient voltage boost ratio for the hold-up time operation is provided by using SS-PSC strategy. In comparison with the conventional variable-frequency-controlled (VFC) *LLC* resonant converter, the main advantages are that the circulating current caused by the magnetizing inductor is effectively suppressed and the efficiency of normal operation is significantly improved. The operation principles, output characteristics, and design considerations of the proposed converter are presented in detail. Experimental results are given to verify the effectiveness and the advantages of the proposed solutions.**

***Index Terms*—DC–DC converter, hold-up time compensation, *LLC* resonant converter, phase-shift control.**

I. Introduction

HOLD-UP time is a special requirement for the distributed power systems and server power supplies, which require continuous output voltage regulation for certain time after input ac line dropout [1]. During the hold-up time, i.e., during the ac line dropout, the energy of the front-end dc/dc converter is provided by the bulky link capacitors. To minimize the size of the hold-up time capacitors and to reduce the cost and improve the power density, a requirement for the front-end dc–dc converter is that it should be able to provide regulated output voltage in a wide input voltage range [2].

There have been many topologies proposed for the front-end dc–dc converter. Among them, the *LLC* resonant converter is the most attractive topology due to its excellent soft-switching performance and voltage step-up capability [3]–[6]. Fig. 1 shows the design relationship with hold-up time requirement for a front-end *LLC* resonant converter. Generally, the normal operation point is designed at the series-resonant frequency to maximize the efficiency and realize unity voltage gain [3], [4]. However, as for the hold-up time requirement, the parameters of the *LLC* converter have to be designed according to the minimal input voltage, resulting in bulky magnetizing components and low efficiency of the normal operation point due to large circulating current of the magnetizing inductance. Many design methods have been presented to optimize the efficiency and extend the operating range of the *LLC* resonant converter [6]–[8]. Unfortunately, to satisfy the voltage step-up ratio during the hold-up time, the magnetizing inductance of the *LLC* resonant converter has to be decreased leading to increased circulating current within the entire operation range, which will affect the efficiency of the normal operation. In other words, the performance of the *LLC* resonant converter at the normal operation point will be degraded ineluctably when considering the hold-up time requirements.

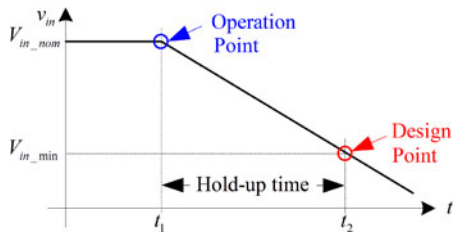

Fig. 1. Hold-up time operation for dc–dc converter.

If the resonant converter always operates at the series-resonant frequency, operating as a dc–dc transformer [9], the efficiency can be maximized, but the voltage regulation ability is lost. To achieve voltage regulation for a dc–dc transformer, active-boost rectifier with secondary-side phase-shift control (SS-PSC) is proposed in [10] by Wu *et al.* This drops a hint that the output voltage of a resonant converter may also be regulated through the secondary-side rectifier. To maximize the efficiency of normal operation point and provide sufficient voltage gain for the hold-up time requirement, an improved *LLC* resonant converter with SS-PSC is proposed in this letter. The proposed converter always operates at the series-resonant frequency. Voltage step-up during hold-up time is realized with phase-shift control rather than variable frequency. As a result,

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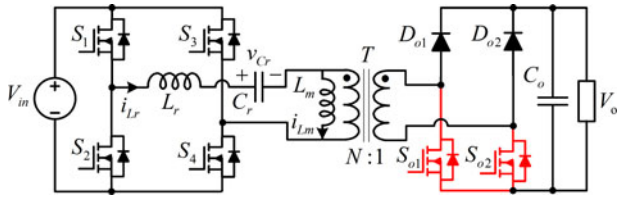

Fig. 2. Proposed SS-PSC *LLC* resonant converter.

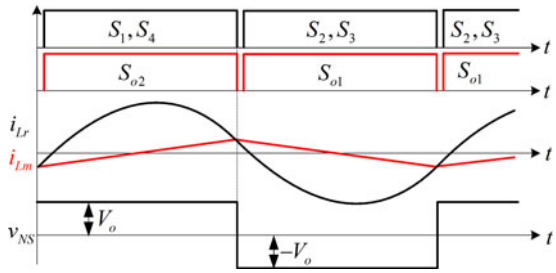

Fig. 3. Key waveforms of the proposed converter for normal operation with $\varphi = 0$.

when designing the magnetizing inductor, only the achievement of soft-switching is considered, which can help to reduce the circulating current and maximize the efficiency at the normal operation.

II. Proposed Topology and Control Strategy

The proposed SS-PSC *LLC* resonant converter is shown in Fig. 2. The difference of the proposed converter in comparison with a traditional *LLC* resonant converter is that a hybrid full-bridge rectifier composed of two diodes and two synchronous rectification switches is employed. The proposed converter operates at the constant series-resonant frequency f_r determined by the resonant tank

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}. \tag{1}$$

In Fig. 2, the combination of S_{o1} and S_{o2} functions as a bidirectional switch, which can short the transformer winding, and make the voltages of input and resonant capacitor charge the resonant inductor L_r directly. When the bidirectional switch is OFF, L_r discharges and voltage step-up can be realized, which is similar to a boost converter and the same as the active-boost rectifier in [10]. So, the voltage step-up of the proposed converter is realized by regulating S_{o1} and S_{o2}.

A. Normal Operation

In the normal state, the operation of the proposed converter is the same as the *LLC* resonant converter. The key waveforms of the normal operation are illustrated in Fig. 3, where the phase-shift angle φ, the phase-difference between the turn-off signals of $S_{o1}(S_{o2})$ and $S_2\&S_3$ ($S_1\&S_4$) is zero. S_{o1} and S_{o2} are used as synchronous rectification switches.

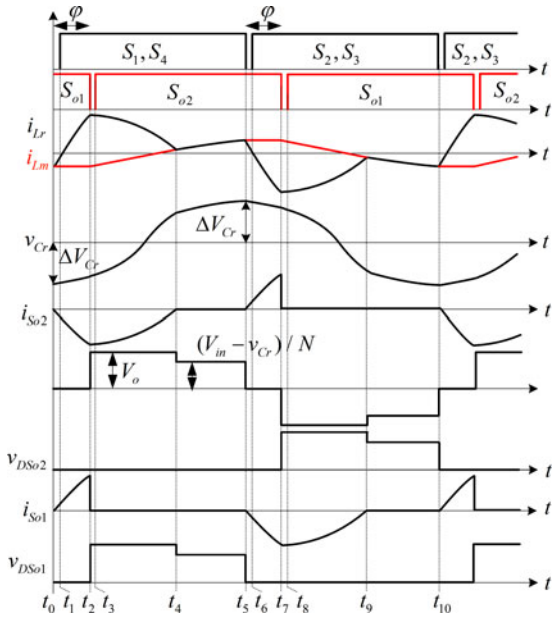

Fig. 4. Waveforms of the hold-time operation.

Since the switching frequency is fixed at the series-resonant frequency f_r, the normalized voltage gain G is

$$\mathrm{G}_{f_S = f_r} = \frac{NV_o}{V_{\mathrm{in}}} = 1 \tag{2}$$

where N is the primary-to-secondary turns ratio of the transformer, and V_{in} and V_o are the input and output voltages. Similar to the traditional *LLC* resonant converter, soft-switching of all of the primary-side switches S_1–S_4, the secondary-side synchronous rectification switches S_{o1} and S_{o2}, and diodes D_{o1} and D_{o2}, can be achieved for the normal operation. It may also be noted that both the controlled switches on the secondary-side are referenced to output ground, which results in an easier gate drive.

B. Hold-Up Time Operation

The key waveforms of the proposed SS-PSC resonant converter during the hold-up time operation are shown in Fig. 4, where the phase-shift angle φ is employed to boost the output voltage during the hold-up time. There are totally ten switching stages in one switching cycle. Due to the symmetry of the operation, only half of the switching cycle *Stage 1–Stage 5* are analyzed here. The equivalent circuit of each switching stage is shown in Fig. 5. It should be noted that, for simplicity, the resonance between the magnetizing inductance L_m and the resonant capacitor is neglected in the following analysis, because L_m is sufficiently large and the current i_{Lm} is sufficiently small to be neglected.

Stage 1 $[t_0, t_1]$ [see Fig. 5(a)]: Before t_0, S_2, S_3, and S_{o1} are ON, both D_{o1} and D_{o2} are OFF. At t_0, S_2 and S_3 are turned OFF. Because of the negative value of magnetizing inductor current i_{Lm}, the body-diodes of S_1 and S_4 begin to conduct, resulting in a positive voltage across the primary side of the transformer. As S_{o1} remains ON, the secondary-winding of the transformer is shorted by S_{o1} and the body diode of S_{o2}, resulting in zero

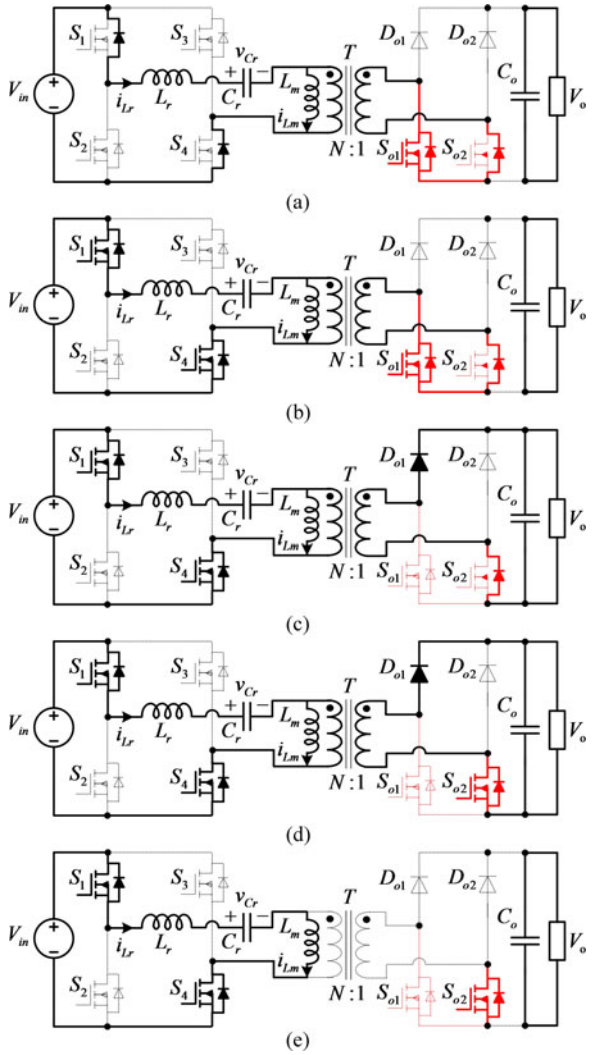

Fig. 5. Equivalent circuit of (a) *Stage 1* $[t_0, t_1]$, (b) *Stage 2* $[t_1, t_2]$, (c) *Stage 3* $[t_2, t_3]$, (d) *Stage 4* $[t_3, t_4]$, and (e) *Stage 5* $[t_4, t_5]$.

voltage across the magnetizing inductor. So, L_r and C_r begin to resonate. At the beginning of the resonance, the voltage across C_r, $v_{\rm Cr}$ is at its minimum value $-\Delta V_{Cr}$, which can be calculated according to the charge balance of the resonant capacitor and expressed as

$$\Delta V_{Cr} = \frac{P_o}{4 f_S V_{\rm in} C_r} = \frac{V_o^2}{R_o} \frac{1}{4 f_S V_{\rm in} C_r} \tag{3}$$

where f_s is the switching frequency, and P_o and R_o are the output power and load resistance, respectively.

Stage 2 $[t_1, t_2]$ [see Fig. 5(b)]: At t_1, $\rm S_1$ and $\rm S_4$ are turned ON with ZVS. This stage ends until $\rm S_{o1}$ is turned OFF at t_2.

During *Stage 1* and *Stage 2*, the resonant inductor current i_{Lr} is expressed as

$$i_{Lr}(t) = \frac{V_{\rm in} + \Delta V_{Cr}}{Z_r} \sin \omega_r (t - t_0) \tag{4}$$

where $Z_r = \sqrt{L_r / C_r}$, and $\omega_r = 2\pi f_r$.

Stage 3 $[t_2, t_3]$ [see Fig. 5(c)]: At t_2, the current in L_r is charged to an initial condition from the previous stage, which is expressed as

$$i_{Lr}(t_2) = \frac{V_{\rm in} + \Delta V_{Cr}}{Z_r} \sin \frac{\omega_r \varphi}{2\pi f_S} = \frac{V_{\rm in} + \Delta V_{Cr}}{Z_r} \sin \varphi \tag{5}$$

and $\rm S_{o1}$ is turned OFF. The diode D_{o1} and the body diode of $\rm S_{o2}$ begin to conduct.

Stage 4 $[t_3, t_4]$ [Fig. 5(d)]: At t_3, $\rm S_{o2}$ is turned ON with ZVS.

The operation principles of *Stage 3* and *Stage 4* are similar to the traditional *LLC* resonant converter. In these two Stages, L_r and C_r resonate, as the power is transferred to the load, and the magnetizing inductor current $i_{\rm Lm}$ increases linearly due to the positive voltage applied on the L_m. The resonant current i_{Lr} is expressed as

$$i_{\rm Lr}(t) = \frac{N V_o - V_{\rm in} + \Delta V_{Cr}}{Z_r} \sin[\theta_1 + \omega_r (t - t_2)] \tag{6}$$

where θ_1 is the initial angle and can be calculated according to (5) and (6), and can be expressed as

$$\theta_1 = \arcsin\left(\frac{V_{\rm in} + \Delta V_{Cr}}{N V_o - V_{\rm in} + \Delta V_{Cr}} \sin \varphi \right). \tag{7}$$

Stage 5 $[t_4, t_5]$ [see Fig. 5(e)]: At t_4, the current flowing through the secondary-winding of the transformer reaches zero, and the diode D_{o1} is OFF naturally and without reverse recovery. The converter enters an idle mode where no power is being transferred from the source to the load. The operation of this stage is also similar to the traditional *LLC* resonant converter. However, because the magnetizing inductance is sufficiently large, although L_m and L_r resonate with C_r, the resulted voltage ripple on C_r is neglected and the resonant current i_{Lr} in this stage is treated to be zero in the following analysis.

A similar operation works in the rest stages of a switching period, with the roles of $\rm S_1$ and $\rm S_2$, $\rm S_3$ and $\rm S_4$, D_{o1} and D_{o2}, and $\rm S_{o1}$ and $\rm S_{o2}$ exchange.

III. Characteristics and Design Considerations

A. Voltage Conversion Ratio

According to the aforementioned analysis, the average current of the resonant inductor L_r, which is equivalent to the average input current $I_{\rm in}$, can be obtained as

$$I_{\rm in} = 2 f_S \int_{t_0}^{t_4} i_{Lr}(t) = 2 f_S \times \left(\frac{V_{\rm in} + \Delta V_{Cr}}{Z_r \omega_r} \int_0^{\varphi} \sin\theta d\theta + \frac{N V_o - V_{\rm in} + \Delta V_{Cr}}{Z_r \omega_r} \int_{\theta 1}^{\pi} \sin\theta d\theta \right). \tag{8}$$

Ignoring the power losses, input current can also be calculated as

$$I_{\rm in} = P_{\rm in} / V_{\rm in} = P_o / V_{\rm in} = V_o^2 / (V_{\rm in} R_o). \tag{9}$$

Substitute (7) and (9) into (8), the relationship between the normalized voltage conversion ratio *G* and the phase shift angle φ can be derived

$$G_{f_S = f_r}(\varphi, Q) = \frac{\sqrt{\pi Q} + \sqrt{-2(\cos\varphi)^2 + \pi Q + 2}}{\sqrt{\pi Q}(1 + \cos\varphi)} \tag{10}$$

where Q is the normalized quality factor and can be defined as

$$Q = \frac{Z_r}{N^2 R_o}. \tag{11}$$

From (10), when $\varphi = 0$ and $cos\varphi = 1$, we have $G_{fS=fr} = 1$, which is the same as (2). Meanwhile, when φ is in the range of 0–π, cosφ is inversely proportional to φ. So, $G_{fS=fr}$ is proportional to φ, which means the voltage gain is greater than 1 when φ>0.

B. Design Consideration

The design of the proposed converter is very similar to the *LLC*-based dc–dc transformer [9], which always operates at the series-resonant frequency and has no voltage regulation ability. For the applications in this paper, the transformer turns ratio N is selected according to the normal input voltage $V_{\text{in\_norm}}$,

$$N = \frac{V_{\text{in\_norm}}}{V_o}. \tag{12}$$

The resonant tank, L_r and C_r, should be designed according to the resonant frequency. Meanwhile, the required voltage boost ratio and maximum phase-shift angle under minimum input voltage and full-load should be taken into consideration, when selecting L_r and C_r, because the voltage ratio is affected by the quality factor Q, as indicated by (10).

The magnetizing inductance of the proposed SS-PSC *LLC* resonant converter should be selected to be as large as possible to reduce the circuiting current-related conduction loss. The only consideration for the magnetizing inductance is the realization of ZVS of the primary-side switches at the normal input voltage. The ZVS condition of the primary-side MOSFET can be given by

$$I_{Lm\_pk} T_{\text{DT}} \geq 2 C_{\text{oss}} V_{\text{in\_norm}} \tag{13}$$

where C_{oss} is the drain-source capacitance of the primary-side switches, T_{DT} is the dead-time of the primary-side switching bridge, and I_{Lm_pk} is the peak value of magnetizing current

$$I_{Lm\_pk} = \frac{V_{\text{in\_norm}}}{4 L_m f_S}. \tag{14}$$

According to (13) and (14), we have

$$L_m \leq \frac{T_{\text{DT}}}{8 C_{\text{oss}} f_S}. \tag{15}$$

It can be seen that a tradeoff should be made between the magnetizing inductance and dead-time.

IV. Experimental Verification

A 500-W experimental prototype is built to verify the effectiveness of the proposed solution. Following the design considerations discussed in [3] and design methods presented in [11], a traditional VFC-*LLC* resonant converter is designed first. To satisfy the voltage gain at full load, the ratio $k = L_m / L_r$ is designed to be 6 for the VFC-*LLC* converter. The switching frequency of the VFC-*LLC* is in the range of 90–200 kHz, and resonant frequency is 200 kHz. To make a fair comparison, after designing the VFC-*LLC*, the parameters of the proposed SS-PSC *LLC* converter are obtained by only redesigning the magnetizing inductance, according to (15). The parameters of both the VFC *LLC* and SS-PSC *LLC* converters are listed in Table I. It can be seen that, in addition to the magnetizing inductance and switching frequency, the parameters and devices of the two converters are all the same. To make a fair performance comparison, the two converters are tested on the same prototype. Thus, the PCB board, the switches and diodes on the primary and secondary sides, the resonant inductor and resonant capacitor, the windings and turns ratio of the transformer, and the experimental test equipments of the two converters are all the same. The only difference is that the magnetizing inductance of the VRC *LLC* converter is smaller than that of the proposed SS-PSC converter.

TABLE I
Parameters of Experimental Test

	VFC *LLC*	SS-PSC *LLC*
Input voltage (V_{in})	200V (Minimum) –400 V (Normal)	
Output voltage	48 V/500 W	
Resonant inductor (L_r)	40 μH	
Resonant capacitor (C_r)	15 nF	
Turns ratio of transformer (N)	25:3	
Magnetizing inductor (L_m)	250 μH	420 μH
Switching frequency (f_S)	90 –200 kHz (f_r)	200 kHz (f_r)
Hold-up capacitor	220 μF	
Primary switches (S_1–S_4)	5R190CE	
Secondary switches (S_{o1}, S_{o2})	052NE7N3G	
Rectifying diodes (D_{o1}, D_{o2})	STPS30SM80C	

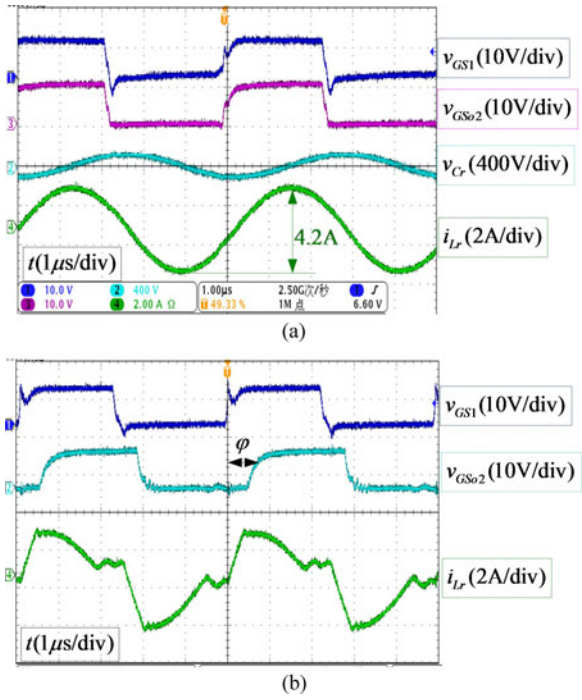

Fig. 6. Steady-state waveforms of the proposed converter under full-load, (a) $V_{\text{in}} = 400$ V, (b) $V_{\text{in}} = 200$ V.

The steady-state switching waveforms of the proposed SS-PSC *LLC* converter with full-load output are shown in Fig. 6. Fig. 6(a) is the waveforms in normal operation with $V_{\text{in}} = 400$

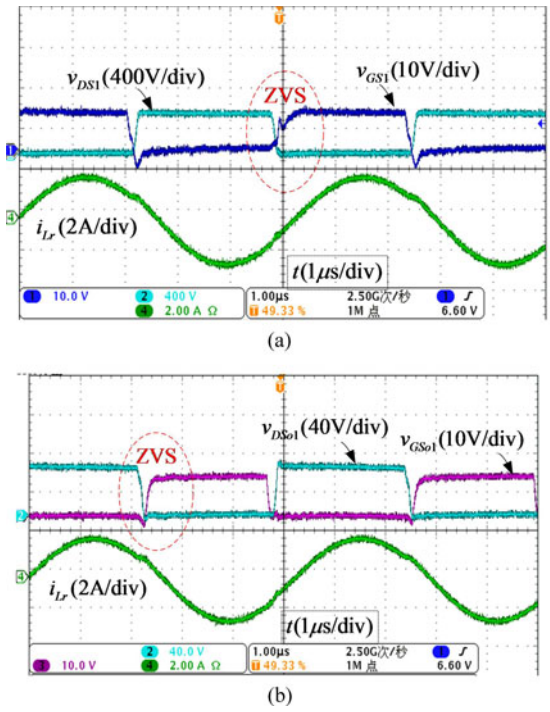

Fig. 7. Soft-switching waveforms at normal operation, (a) primary-side switch S_1, (b) secondary-side switch S_{o1}.

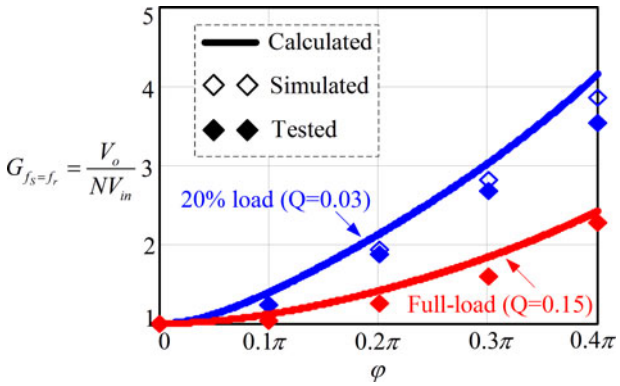

Fig. 8. Voltage gain curves of the SS-PSC *LLC* resonant converter.

V, where the driving voltage of S_{o2} is in phase with S_1, because the phase-shift angle is zero when the converter is in the normal operation. Fig. 6(b) is the waveforms in hold-up time operation with $V_{\rm in} = 250$ V, where a phase delay between the driving voltages of S_{o2} and S_1 can be seen. The experimental waveforms are consistent with the theoretic analysis pretty well.

The soft-switching waveforms of the primary and secondary-side switches are shown in Fig. 7. These waveforms are tested under normal operation with $V_{\rm in} = 400$ V. It can be seen that ZVS has been achieved for both the primary and secondary-side switches.

The calculated voltage gain of the SS-PSC *LLC* converter, as given by (10), is verified with both simulation and experiment tests. The calculated, simulated, and tested voltage gains are shown in Fig. 8, where the tested results are consistent with the calculated results pretty well. The calculated gain is higher than

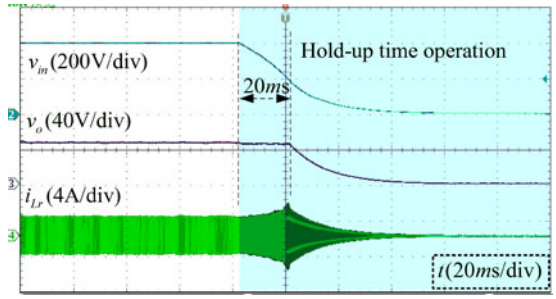

Fig. 9. Waveforms of hold-up time operation.

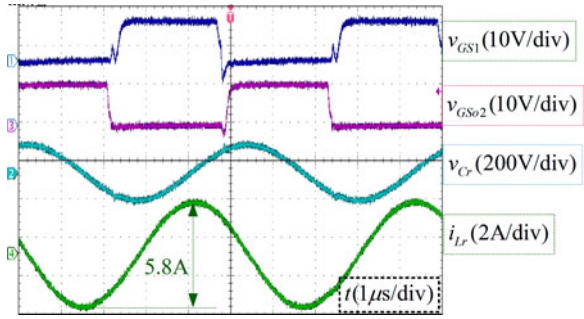

Fig. 10. Steady-state waveforms of traditional *LLC* resonant converter with $V_{\rm in} = 400$ V.

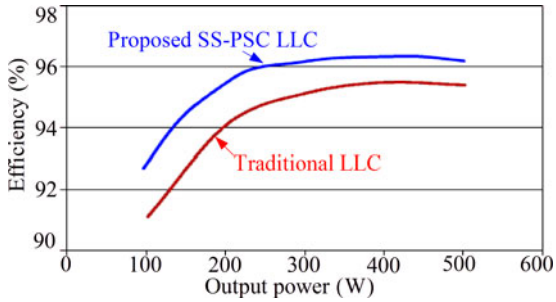

Fig. 11. Efficiency comparison of the proposed SS-PSC resonant converter and traditional *LLC* resonant converter.

the tested results because the magnetizing inductance is ignored in the theoretical analysis.

The hold-up time operation waveforms are tested and shown in Fig. 9, where it is shown that the hold-up time requirements are satisfied by using the proposed converter and control strategy.

The steady-state waveforms of the traditional *LLC* converter at normal operation with $V_{\rm in} = 400$ V and full load is shown in Fig. 10, where the peak-to-peak resonant current is up to 5.8 A, however, the peak-to-peak resonant current of the proposed converter with the same conditions is only 4.2 A, as shown in Fig. 6(a). Obviously, the conduction losses of the primary side can be reduced significantly by using the proposed SS-PSC *LLC* converter, because the square value of i_{Lr} in Fig. 6(a) is only half of that in Fig. 10. As a result, the efficiency at normal operation can be improved.

The efficiency curves of the proposed converter and traditional converter in the normal state with $V_{\rm in} = 400$ V are shown in Fig. 11. It can be seen that the efficiency is improved by nearly

1% by using the proposed converter, because the conduction losses of primary side are reduced significantly by increasing the value of magnetizing inductance. It should be noted that we only care the efficiency with normal input voltage, while the efficiency in the hold-up time operation is not important for this application, because the time of hold-up operation is very short.

V. Conclusion

The proposed SS-PSC *LLC* resonant converter is well suited for the applications requiring hold-up time operation such as front-end converters for servers and computers. The conversion efficiency at the normal input voltage can be maximized with the proposed converter, because the circulating current-related conduction losses can be minimized, while soft-switching performance can also be realized for all of the switches and diodes. Sufficient voltage step-up ratio required by the minimum input voltage can be provided by using the SS-PSC strategy. The resonant tank and transformer of the proposed converter can be optimized, because the converter always operates at the series-resonant frequency of the resonant tank. This paper provides a new solution for the voltage regulation of *LLC* resonant converter. Experimental results indicate that high efficiency at normal input voltage and voltage regulation during hold-up time has been achieved with the proposed solution.

References

[1] Y.-S. Lai, Z.-J. Su, and W.-S. Chen, "New hybrid control technique to improve light load efficiency while meeting the hold-up time requirement for two-stage server power," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4763–4775, Sep. 2013.

[2] X. Wang, F. Tian, and I. Batarseh, "High efficiency parallel post regulator for wide range input DC-DC converter," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 852–858, Mar. 2008.

[3] B. Yang, F. C. Lee, A. J. Zhang, and G. Huang, "LLC resonant converter for front end DC/DC conversion," in *Proc. IEEE 17th Annu. Appl. Power Electron. Conf. Expo.*, Mar. 2002, pp. 1108–1112.

[4] D. Fu, B. Lu and F. C. Lee, "1 MHz high efficiency LLC resonant converters with synchronous rectifier," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2007, pp. 2404–2410.

[5] I.-H. Cho, Y.-D. Kim, and G.-W. Moon, "A half-bridge LLC resonant converter adopting boost PWM control scheme for hold-up state operation," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 841–850, Feb. 2014.

[6] Z. Hu, Y. Qiu, Y.-F. Liu, and P. C. Sen, "A control strategy and design method for interleaved LLC converters operating at variable switching frequency," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4426–4437, Aug. 2014.

[7] H. Hu, X. Fang, F. Chen, Z. J. Shen, and I. Batarseh, "A modified high-efficiency LLC converter with two transformers for wide input-voltage range applications," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1946–1960, Apr. 2013.

[8] R. Beiranvand, B. Rashidian, M. R. Zolghadri, and S. M. H. Alavi, "A design procedure for optimizing the LLC resonant converter as a wide output range voltage source," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3749–3763, Aug. 2012.

[9] W. Feng, P. Mattavelli, and F. C. Lee, "Pulsewidth locked loop (PWLL) for automatic resonant frequency tracking in LLC DC-DC transformer (LLC-DCX)," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1862–1869, Apr. 2013.

[10] H. Wu, Y. Lu, T. Mu, and Y. Xing, "A family of soft-switching DC-DC converters based on a phase-shift-controlled active boost rectifier," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 657–667, Feb. 2015.

[11] I.-O. Lee and G.-W. Moon, "The k-Q analysis for an LLC series resonant converter," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 13–16, Jan. 2014.