A Reduced Switching Loss PWM Strategy to Eliminate Common-Mode Voltage in Multilevel Inverters

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***Abstract*—This paper introduces a novel pulse width modulation (PWM) technique to eliminate common-mode voltage in odd-multilevel inverters using the three zero common-mode vectors principles. Similarly, as in conventional PWM for multilevel inverters, this PWM can be properly depicted in an active two-level voltage inverter. With the help of two standardized PWM patterns, the characteristics of the PWM process can be fully explored in that active inverter as a switching time diagram and switching state sequence. Due to an unequal number of commutations of three phases in each sampling period, the switching loss is optimized by a proposed current-based mapping algorithm. The switching loss reduction can be up to 25% compared to the same PWM technique with nonoptimized algorithms. The PWM method has been then generalized as an equipotential PWM control, which is valid to both odd- and even-multilevel inverters. The theoretical analysis is verified by simulation and experimental results.**

***Index Terms*—Common-mode voltage (CMV), multilevel inverter, pulse width modulation (PWM), switching loss.**

I. Introduction

In recent years, great progress has been made in the development of multilevel inverters in electric drives and other applications. Two basic circuits are commonly used in practice: diode clamped multilevel inverters and cascaded multilevel inverters, as shown in Fig. 1. The three most common PWM schemes are the space vector pulse width modulation (PWM), carrier-based PWM, and selective harmonic elimination PWM techniques [1]–[6].

Common-mode voltages (CMVs) are associated with excessive bearing currents, which may cause premature motor bearing failure and electromagnetic interference [17]–[32]. There have been a number of approaches to cope with the CMV issue, including the use of extra hardware with passive and/or active devices [26]–[32]. However, the extra hardware causes a significant increase in the system's volume or much more complex control methods.

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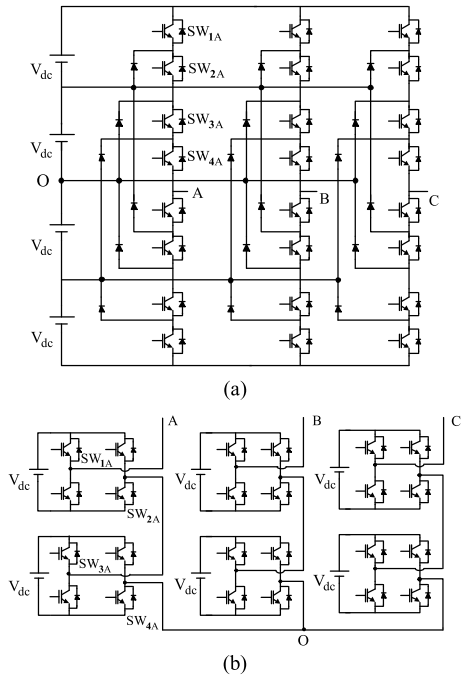

Fig. 1. Multilevel inverter circuits. (a) Five-level diode clamped inverter. (b) Five-level cascaded inverter.

The multilevel inverters have a high number of switching states that can either reduce or eliminate the CMV. Based on this advantage, many studies of CMV mitigation have been conducted using multilevel inverters [7]–[19].

In partial PWM methods to eliminate CMV, the output voltage can be obtained normally by a conventional discontinuous PWM technique (DPWM) [7], [8]. In order to attain reduced CMV at a high modulation index, a new DPWM pattern from three nonnearest vectors was proposed [9]. In another work, a tradeoff in the THD factor and switching loss to reduce the number of common-mode current pulses (dv/dt) could be managed with a change in sequence of the nonnearest vectors [10].

In another approach to avoid the common-mode influence, researchers have tried to fully eliminate the CMV. The idea of complete CMV elimination that restricts the inverter switching states to those states of zero CMV (ZCMV) was first proposed by Ratnayake and Murai [11] for a three-level NPC inverter. This idea was further developed in other studies [12]–[16]. In [13], the modulation of selected ZCMV states is applied to the three-level NPC using both carrier-based and space vector modulation schemes. Similar to [11], the method utilizes the three vectors of

ZCMV in the three-level NPC inverter to synthesize the reference output voltages. However, the rule of distribution of these vectors in each switching sequence is not mentioned. In the work [15], modulation strategies for partial CMV elimination and complete CMV elimination in cascaded multilevel inverters are proposed. The proposed control process, with regard to complete common-mode elimination, is relatively complex for multilevel inverters with high number of levels. Furthermore, the symmetrical double-sided pattern (which consists of up to 12 commutations) causes a considerable switching loss. In [16], the authors have used space vector PWM approach of ZCMV switching state selection and proposed a method of eliminating CMV spikes for a five-level NPC inverter. However, similar to [13], investigation of the selection of switching patterns from the three vectors is outside the scope of this study.

This paper presents a simple carrier-based method to cope with this problem. Its main contributions are clarified in the following points:

1) A general PWM method of eliminating CMV for an odd-multilevel inverter is proposed. The proposed PWM method is based on the principle of the three zero common-mode vectors. All switching sequences and corresponding switching time diagrams are derived from two generalized PWM patterns. The two patterns represent the equipotential switching state sequence of a two-level inverter. The proposed carrier-based PWM algorithm to produce the PWM pattern is simple and can be applied to an arbitrary number of levels. The proposed PWM method to eliminate CMV is then generalized as an equipotential PWM control method that will be valid to both odd- and even-multilevel inverter.
2) A reduced switching loss PWM method is proposed. The resultant double-sided switching PWM patterns have a minimum number of commutations. The number of commutations per sampling period is eight, which globally reduces the switching loss. By utilizing information about feedback currents and the degree of freedom in the switching state arrangements, the switching state sequence is locally optimized within the standardized PWM patterns, which can help to reduce switching loss by up to 25% compared to nonoptimized algorithms, and by up to 43% compared to [15]. The experimental results obtained with a five-level cascaded inverter are used to verify the performance of the proposed PWM strategy.

II. Proposed PWM Method to Eliminate CMV

A. Voltage Modeling of the Multilevel Inverter and Offset Condition for Eliminating CMV

Due to the difference in structure of the diode clamped inverter (NPC) and cascaded inverter (as illustrated in Fig. 1 for a five-level inverter), established rules of switching combinations for a same reference output voltage are completely different. In this paper, the analytical process for the two topologies can be unified by a simple voltage modeling. Under the condition of balanced dc-link voltages, with the selected neutral point "*O*" and designated switches of the *A*-phase represented as $\mathrm{SW}_{1A}, \mathrm{SW}_{2A}, \mathrm{SW}_{3A}, \mathrm{SW}_{4A}$ for the two topologies in Fig. 1, the pole voltage V_{AO} is generally determined as

$$V_{\mathrm{AO}} = (s_{1A} + s_{2A} + s_{3A} + s_{4A})V_{\mathrm{dc}} - 2V_{\mathrm{dc}} \tag{1}$$

where $s_{1A}, s_{2A}, s_{3A}, s_{4A}$ represent the switching states of $\mathrm{SW}_{1A}, \mathrm{SW}_{2A}, \mathrm{SW}_{3A}, \mathrm{SW}_{4A}$, respectively; s_{1A} is 1 if SW_{1A} is ON; otherwise, its value is 0.

$s_{1A}, s_{2A}, s_{3A}, s_{4A}$ can be selected randomly in the five-level cascaded inverter, but are further restricted in the five-level NPC inverter due to the limit of its switching combinations. The constraint is simply expressed as

$$s_{1A} \le s_{2A} \le s_{3A} \le s_{4A}. \tag{2}$$

For an *n*-level inverter of the two topologies, (1) and (2) can be generalized as

$$\begin{aligned} V_{XO} =\ & \left(s_{1X} + s_{2X} + \cdots + s_{(n-2)X} + s_{(n-1)X}\right) \\ & V_{\mathrm{dc}} - \frac{n-1}{2}V_{\mathrm{dc}} \\ =\ & \left(\sum_{j=1}^{n-1} s_{jX}\right) V_{\mathrm{dc}} - \frac{n-1}{2}V_{\mathrm{dc}}, \quad X = A, B, C \end{aligned} \tag{3}$$

and $s_{1X} \le s_{2X} \le \cdots \le s_{n-1X}$ (for the NPC inverter topology)

The component $\left(\sum_{j=1}^{n-1} s_{jX}\right) V_{\mathrm{dc}}, \quad X = A, B, C$, in (3) is called the switching voltages. We define $V_{Xn} = \sum_{j=1}^{n-1} s_{jX}$ as the normalized switching voltage which, for further analysis, can be used to represent V_{XO}. The relationship between V_{Xn} and V_{XO} is described as

$$V_{Xn} = \frac{V_{XO}}{V_{\mathrm{dc}}} + \frac{n-1}{2}. \tag{4}$$

The normalized switching voltage V_{Xn} can be decomposed into two components: L_X and s_X

$$V_{Xn} = L_X + s_X. \tag{5}$$

During a sampling period, L_X is a constant integer value that represents the base component of V_{Xn}, and s_X is the active component of V_{Xn}, which value can be 0 or 1. Taking (4) and (5) into account, the equivalent circuit of the instantaneous voltage of V_{XO} is derived as in Fig. 2(a). (L_A, L_B, L_C) is called the normalized state of the three-phase base voltages, and (s_A, s_B, s_C) is called the normalized state of the three-phase active voltages in Fig. 2(a).

If ξ_X is defined as the average active component of s_X in a sampling period, then the average value of V_{Xn} (defined as v_{Xn}) can be derived as follows:

$$\begin{aligned} v_{Xn} =\ & L_X + \xi_X, \quad (0 \le \xi_X \le 1, \\ \xi_X =\ & 1, \quad \text{if } v_{Xn} = n-1) \end{aligned} \tag{6}$$

and the equivalent circuit of the average voltage of V_{XO} can now be described as in Fig. 2(b).

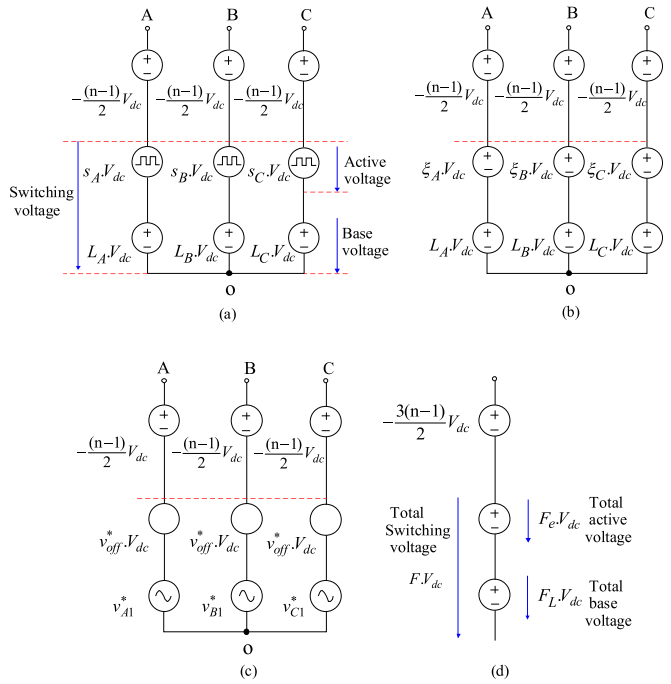

Fig. 2. (a) Equivalent circuit of instantaneous three-leg voltages of n-level voltage source inverter. (b) Average modeling of three-leg voltages. (c) Average voltage modeling from reference fundamental voltage and offset voltage components. (d) Total switching voltage and its components ($F_e = \xi_A + \xi_B + \xi_C, F_L = L_A + L_B + L_C$).

We define $v^*_{X1}(X = A, B, C)$ as the reference load voltages, and v_{Xn} in (5) can also be expressed as

$$v_{Xn} = \frac{v^*_{X1}}{V_{\rm dc}} + v^*_{\rm off}. \tag{7}$$

The offset voltage $v^*_{\rm off}$ of the circuit in Fig. 2(c) for any PWM method can be designed to have any value in the limits as

$$v_{\rm off\_min} = -\frac{\rm MIN}{V_{\rm dc}} \le v^*_{\rm off} \le v_{\rm off\_max} = (n-1) - \frac{\rm MAX}{V_{\rm dc}} \tag{8}$$

where MAX and MIN are the highest and the smallest of the three reference load voltages $(v^*_{A1}, v^*_{B1}, v^*_{C1})$, and n is the number of levels.

Fig. 2(c) describes the equivalent circuit of the average voltage of V_{XO} following (4) and (7).

The CMV defined for the n-level inverter in Fig. 1 is described as in [8], [10], [11], [13], [15], [16], [31]:

$$V_{\rm CM} = \frac{V_{AO} + V_{BO} + V_{CO}}{3}. \tag{9}$$

The instantaneous value of $V_{\rm CM}$ following Fig. 2(a) is derived as

$$V_{\rm CM} = \frac{(V_{An} + V_{Bn} + V_{Cn} - 3(n-1)/2).V_{\rm dc}}{3}. \tag{10}$$

The combinations of (V_{AO}, V_{BO}, V_{CO}) that do not contribute any CMV represent the ZCMV vectors in the vector diagram of the n-level inverter, which result in a zero value of $V_{\rm CM}$.

We define f_n as

$$f_n = V_{An} + V_{Bn} + V_{Cn}. \tag{11}$$

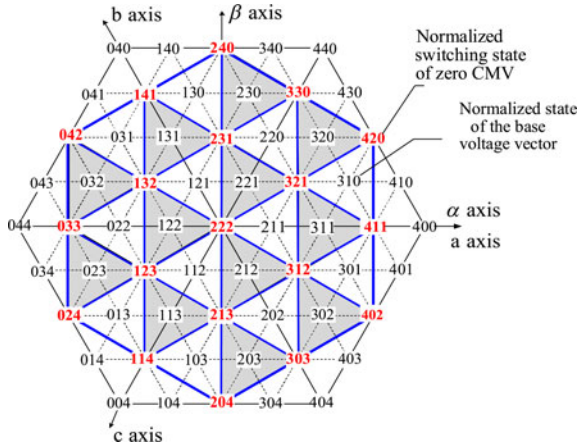

Fig. 3. Space vector diagram of five-level inverter with ZCMV states (bold letters).

It can be seen from (10) that under the condition of eliminating CMV PWM control

$$f_n = f_{\rm ZCMV} = 3(n-1)/2. \tag{12}$$

For example, considering the cascaded five-level inverter in Fig. 3, there are 19 switching combinations that produce ZCMV among 125 possible combinations. All ZCMV vectors satisfy (12) with $f_n = 6$. With a normalized switching state of ZCMV described as $(V_{An}, V_{Bn}, V_{Cn}) = (4, 1, 1)$, for example, the pole leg voltages are derived using (4) as $V_{AO} = 2V_{\rm dc}, V_{BO} = -V_{\rm dc}, V_{CO} = -V_{\rm dc}$.

In the case of the equivalent circuits described in terms of average voltages in a sampling period as shown in Fig. 2(b) and (c), with a note that $v^*_{A1} + v^*_{B1} + v^*_{C1} = 0$, the condition of zero average CMV results in

$$v^*_{\rm off} = v_{\rm off,ZCMV} = (n-1)/2. \tag{13}$$

The sum of the average values of $V_{Xn}(X = A, B, C)$ defined as $F_n = v_{An} + v_{Bn} + v_{Cn}$ is obtained with the following value:

$$F = F_{\rm ZCMV} = F_L + F_e = 3(n-1)/2 \tag{14}$$

where F_L and F_e are determined, respectively, as

$$F_L = L_A + L_B + L_C \tag{15}$$

$$F_e = \xi_A + \xi_B + \xi_C;\ 0 \le F_e \le 3 \quad (0 \le \xi_X \le 1; \xi_X = 1, \quad \text{if } v_{Xn} = n-1). \tag{16}$$

The functions F, F_L, F_e determine the total switching voltage, total base voltage, and total active voltage, respectively, as described in Fig. 2(d).

B. Medium Triangle Active Voltage Vector Diagram of the Two-Level Active Voltage Inverter for Eliminating CMV PWM Control

In the space vector diagram of a multilevel inverter, a discrete vector can be decomposed into two components as follows:

$$\vec{V_S} = \vec{L} + \vec{s} \tag{17}$$

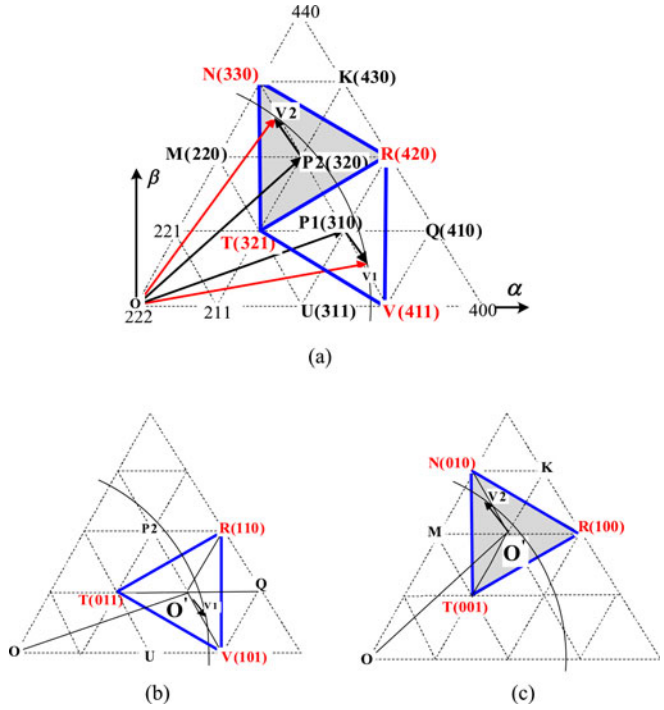

Fig. 4. (a) Five-level inverter: Voltage space vector synthesis illustration in two adjacent triangles TNV ($\vec{L} = \overrightarrow{OP1}, \vec{s^*} = \overrightarrow{P_1V_1}$) and TRN ($\vec{L} = \overrightarrow{OP2}$, $\vec{s^*} = \overrightarrow{P_2V_2}$). (b) Medium triangle vector diagram with normalized state of base voltage vector (3,1,0) and normalized states of active voltage vector (1,1,0), (1,0,1), (0,1,1) ($O' = P_1$). (c) Medium triangle vector diagram with normalized state of base voltage vector (3,2,0) and normalized states of active voltage vector (1,0,0), (0,1,0),(0,0,1) ($O' = P_2$).

where $\vec{L}$ is the pointing vector formed by the three phase base voltages, and $\vec{s}$ is the active vector formed by the three phase active voltages in Fig. 2(a). Following (17), any discrete vector in the space vector diagram of an n-level inverter can be represented by $(\vec{L}, \vec{s})$. The three nearest vectors of ZCMV in the space vector diagram have the same base voltage vector $\vec{L}$, the tip of which is located at the center of the equilateral medium triangle formed by the tips of the three vectors.

Considering a partial illustration of a five-level inverter space vector diagram with ZCMV as shown in Fig. 4(a), the common base voltage vector of the three zero common-mode vectors is $\overrightarrow{OP1}$, which corresponds to the normalized state $(L_A, L_B, L_C) = (3, 1, 0)$ in case the active triangle is TRV. Similarly, the common base voltage vector is $\overrightarrow{OP2}$, which corresponds to the normalized state $(3, 2, 0)$ when the active triangle is TRN. Assume that at an instant, an active triangle is determined by the three zero common-mode vectors characterized by $(\vec{L}, \vec{s} = \vec{s}_1)$, $(\vec{L}, \vec{s} = \vec{s}_2)$ and $(\vec{L}, \vec{s} = \vec{s}_3)$. If the time duties of three vectors in a sampling period T_S are T_1, T_2, T_3 respectively, then the synthesis of the reference output voltage space vector $\vec{v}^*$ is expressed as

$$\vec{v}^* = \vec{L} + \left(\frac{T_1}{T_S}\vec{s}_1 + \frac{T_2}{T_S}\vec{s}_2 + \frac{T_3}{T_S}\vec{s}_3\right) = \vec{L} + \vec{s}^*. \qquad (18)$$

The component $\vec{s}^*$ in (18) is synthesized by three active voltage vectors similar to the space vector synthesis of a two-level inverter. Therefore, with the base voltage vector determined, the synthesis of the output reference space vector of an n-level inverter with ZCMV using the principle of the three zero common-mode vectors can be simplified to that of a two-level inverter. Fig. 4(a) shows the reference voltage space vector decomposition using (18) inside two adjacent equilateral medium triangles of the space vector diagram in Fig. 3. In case the active triangle is TNV, three discrete vectors ($\vec{s}_1 = \overrightarrow{O'T}$, $\vec{s}_2 = \overrightarrow{O'R}$, and $\vec{s}_3 = \overrightarrow{O'V}$) with normalized active switching states (0,1,1), (1,1,0), and (1,0,1), respectively, are used to synthesize $\vec{s}^*$, as shown in Fig. 4(b). Similarly, three discrete vectors $\overrightarrow{O'T}$, $\overrightarrow{O'N}$, and $\overrightarrow{O'R}$ with respective normalized active switching states (0,0,1), (0,1,0), and (1,0,0) are used to implement $\vec{s}^*$ when the active triangle is TNR, as shown in Fig. 4(c).

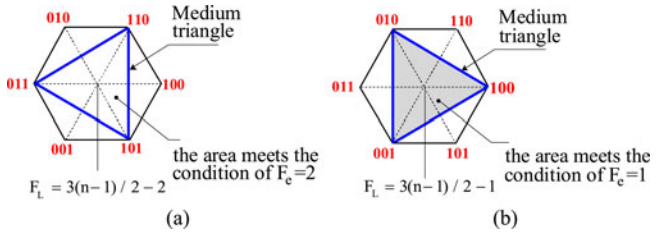

Fig. 5. Medium triangle active voltage vector diagrams. (a) Active switching states for $F_e = 2$. (b) Active switching states for $F_e = 1$.

A simple carrier-based ZCMV PWM control method is established under the consideration of (5) and (12) for instantaneous voltage modeling in Fig. 2(a), and (6), (7), and (13)–(16) for average voltage modeling in Fig. 2(b)–(d). The function F_L in (15) is determined by the base voltage vector, the tip of which is located at the center of the active triangle, and the function F_e is related to the active voltage vectors of the medium triangle vector diagram illustrated in Fig. 4(b) and (c) for two specific cases of the base voltage vector. A general analysis has shown that for an n-level inverter, the ZCMV condition confines the possible values of F_L and F_e to those expressed as

$$\begin{aligned} F_L &= 3(n-1)/2 - 2, \quad F_e = 2 \quad \text{(a)} \\ F_L &= 3(n-1)/2 - 1, \quad F_e = 1 \quad \text{(b)} \\ F_L &= 3(n-1)/2, \quad F_e = 0. \quad \text{(c)} \end{aligned} \qquad (19)$$

The proposed CMV elimination PWM in multilevel inverters can be obtained by solving (19). With the exception of case (19c) related to several pivot vectors, the two remaining available values of F_L and F_e are further limited to (19a) and (19b).

In case $F_L = 3(n-1)/2 - 2$ and $F_e = 2$ (19a), the condition of $F_e = 2$ will be realized with three active switching states of (1,1,0), (0,1,1), and (1,0,1) in the active voltage hexagonal diagram shown in Fig. 5(a).

Similar to the previous case, when $F_L = 3(n-1)/2 - 1$ and $F_e = 1$ (19b), the condition of $F_e = 1$ will be realized with three active switching states of (1,0,0), (0,1,0), and (0,0,1) in the active voltage hexagonal diagram shown in Fig. 5(b).

For the space vector diagram with ZCMV of a five-level inverter as shown in Fig. 3, 24 equilateral medium triangles defined by set of the three zero common-mode vectors can be

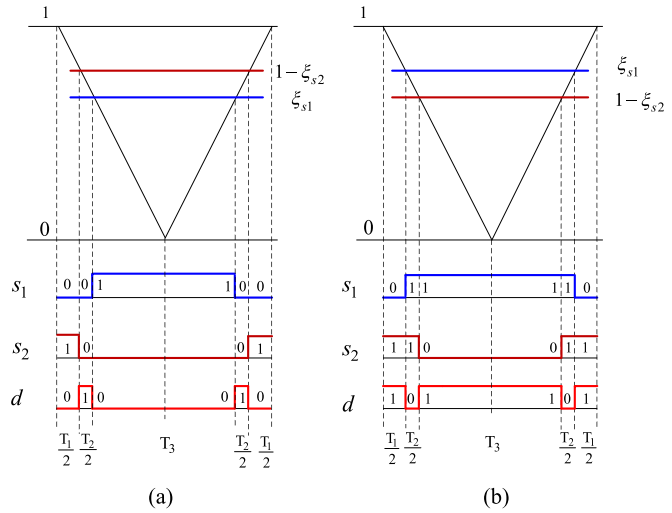

Fig. 6. Two standardized virtual PWM patterns from the three zero common-mode vectors.

found: 12 triangles corresponding to the base vectors meet the condition $F_L = F_{L1} = 4$ and confine the light area; the others satisfy $F_L = F_{L1} = 5$ and cover the shaded area.

The value of the base voltage and the active voltage can be deduced from (20) and (21)

$$L_X = \begin{cases} \text{Int}(v_{Xn}), & \text{if } v_{Xn} < n-1 \\ n-2, & \text{if } v_{Xn} = n-1 \end{cases},$$
$$0 \le L_X \le n-2; X = A, B, C \qquad (20)$$
$$\xi_X = v_{Xn} - L_X, \quad X = A, B, C. \qquad (21)$$

The values v_{Xn} under the conditions of ZCMV are defined by (7) and (13), and $\text{Int}(v_{Xn})$ denotes a function that returns a nearest lower integer value of v_{Xn}.

C. Equipotential PWM Patterns and Control Algorithm

Based on the medium triangle active vector diagrams generalized for an n-level inverter as shown in Fig. 5, the PWM switching state sequence of the active voltage vectors in the ZCMV PWM control can be grouped into two so-called equipotential PWM patterns related to the common-mode function values F_e.

When $F_e = 1$, the active switching state sequence forms PWM pattern 1 as described in Fig. 6(a). Two of the three ABC phases are mapped to s_1 and s_2 such that the s_1-level varies as 0–1–0 in a sampling period, and the s_2-level varies as 1–0–1 in a sampling period. All of them have a single pulse waveform. The remaining phase is mapped to the d-phase such that the d-level varies as 0–1–0–1–0 and has a double pulse waveform in a sampling time period.

When $F_e = 2$, the active switching state sequence corresponds to PWM pattern 2 as shown in Fig. 6(b). Two of the ABC phases are mapped to s_1 and s_2 such that the s_1-level varies as 0–1–0 in a sampling period and the s_2-level varies as 1–0–1 in a sampling time period. All of them have a single pulse waveform. The remaining phase is mapped to the d-phase such that the d-level varies as 1–0–1–0–1 and has a double pulse waveform in a sampling time period.

TABLE I
Possible Mapping Functions and Modulating Signals Determination

A→d	A→d	A→s_1	A→s_2	A→s_1	A→s_2
B→s_1	B→s_2	B→d	B→d	B→s_2	B→s_1
C→S_2	C→s_1	C→s_2	C→s_1	C→d	C→d
$\xi_{s1} = \xi_B$	$\xi_{s1} = \xi_C$	$\xi_{s1} = \xi_A$	$\xi_{s1} = \xi_C$	$\xi_{s1} = \xi_A$	$\xi_{s1} = \xi_B$
$\xi_{s2} = \xi_C$	$\xi_{s2} = \xi_B$	$\xi_{s2} = \xi_C$	$\xi_{s2} = \xi_A$	$\xi_{s2} = \xi_B$	$\xi_{s2} = \xi_A$

For three-phase outputs with the use of the two patterns in Fig. 6, Table I lists six possible mapping functions. Different mapping functions result in different three-phase active switching sequences. For example, when using the mapping function $(A \to d, B \to s_1, C \to s_2)$ for Pattern I, the three phases A, B, and C are mapped to the d, s_1, s_2-sequence, respectively. Hence, the three-phase active switching sequence represented as (s_A, s_B, s_C) is (0,0,1) →(1,0,0) →(0,1,0) →(1,0,0) →(0,0,1). In another example, if the mapping function is selected as $A \to s_1, B \to s_2, C \to d$, then the three-phase active switching sequence is (0,1,0) →(0,0,1) →(1,0,0) →(0,0,1) →(0,1,0).

Since a commutation of the d-sequence in Fig. 6 happens simultaneously with one from both sequences s_1 and s_2, it is sufficient to use two modulating voltages ξ_{s1}, ξ_{s2} to deduce the switching time diagram of the proposed PWM method. The modulating voltages ξ_{s1}, ξ_{s2} are determined based on the mapping function as described in Table I. The switching time diagram can be derived accordingly by comparing $\xi_{s1}, 1-\xi_{s2}$ with a unit carrier as in Fig. 5.

D. Generalized Equipotential PWM Control of Minimum Common Mode for Multilevel Inverters

The functions in (12)–(14) of the described ZCMV PWM method are valid for odd-level inverters. However, if number of levels is even, these functions result in noninteger values, which make the proposed eliminated CMV PWM method no longer applicable. The method principle and its mathematical equations can be simply modified so that they can be applied for an arbitrary n-level inverter. The previous principle can be then generalized as an equipotential PWM control of minimum CMV. For this purpose, we need to redefine the reference potential point and values of the reference CMV.

With the selected reference potential "O" as in Fig. 8, a unified expression of the instantaneous CMV, which is applicable to both odd- and even-level inverters, is described as

$$V_{\text{CM}} = \left(\frac{s_A + s_B + s_C}{3} + \frac{F_L}{3} - \frac{n-1}{2} \right) V_{\text{dc}}. \qquad (22)$$

1) For Odd-Level Inverters

The reference potential point is a connecting point at the midpoint of the dc-link voltage. The values of the CMV V_{CM} produced by all of switching voltage vectors can be obtained as: $((n-1)/2)V_{\text{dc}}$, $((n-1)/2-1/3))V_{\text{dc}}, \ldots, V_{\text{dc}}/3, 0, -V_{\text{dc}}/3, -2V_{\text{dc}}/3, \ldots,$

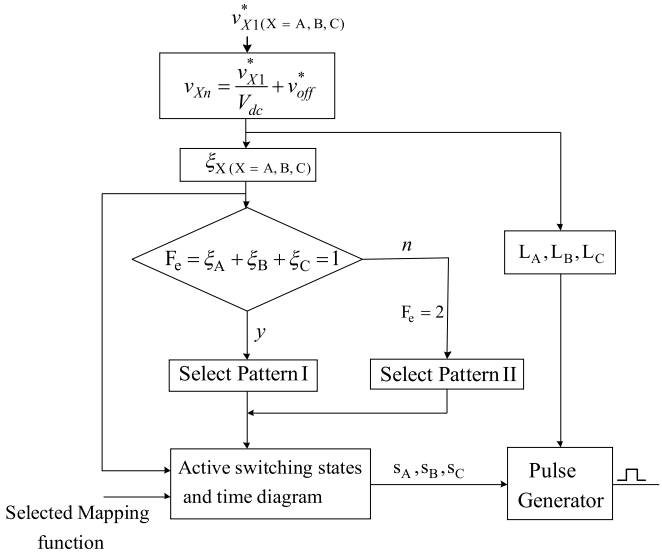

Fig. 7. Block diagram of the proposed PWM method to eliminate CMV (or to attain equipotential CMV).

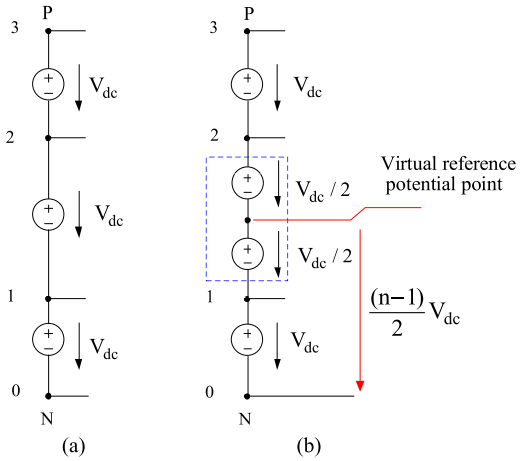

Fig. 8. (a) DC-link voltage of a four-level NPC inverter. (b) Definition of virtual reference potential point "O."

$(-(n-1)/2)V_{\rm dc}$. The ZCMV vectors form the largest vector diagram, which can produce maximum voltage amplitude of $((n-1)/2)V_{\rm dc}$ in the ZCMV PWM control. The vectors of nonzero equipotential, unfortunately, form smaller vector diagrams, which cause the amplitude of the fundamental voltage be lower than $((n-1)/2)V_{\rm dc}$. Therefore, if the equipotential PWM control for attaining the maximum fundamental voltage under condition of minimum CMV is considered, the ZCMV vectors would be preferred. For the sake of increasing modulation depth, the ZCMV PWM control could be extended with the use of the equipotential vectors of different values [17].

2) For Even-Multilevel Inverter

The reference potential as a virtual point that it divides the (n/2)th dc source into two equal half sources as shown in Fig. 8. Referring to this virtual reference potential, the values of the CMV produced by all of switching voltage vectors can be attained as: $((n-1)/2)V_{\rm dc}$, $((n-1)/2-1/3))V_{\rm dc},\ldots,$ $+V_{\rm dc}/6$, $-V_{\rm dc}/6$, $-V_{\rm dc}/2,\ldots,$ $(-(n-1)/2)V_{\rm dc}$. Since the ZCMV vector does not exist, two potential levels $+V_{\rm dc}/6$ and $-V_{\rm dc}/6$ that are closest to zero can be considered in the generalized equipotential PWM control method. There are the same number of equipotential vectors of $V_{\rm CM}=+V_{\rm dc}/6$ and $V_{\rm CM}=-V_{\rm dc}/6$. Their corresponding vector diagrams produce maximum amplitudes of the fundamental voltage. As a result, the generalized equipotential PWM control of minimum CMV for even-level inverters will be proposed based on the condition of $V_{\rm CM}=+V_{\rm dc}/6$ or $V_{\rm CM}=-V_{\rm dc}/6$.

The PWM algorithms proposed for odd- and even-multilevel inverters will be unified by defining the reference common-mode values as

$$V_{\rm CM}=\begin{cases}0, & \text{for odd}-\text{level inverter}\\ \pm V_{\rm dc}/6, & \text{for even}-\text{level inverter.}\end{cases}\tag{23}$$

With the use of the real reference potential (if *n* is an odd number) or the virtual reference one (if *n* is an even number), the voltage modeling of both even- and odd-multilevel inverters circuits can be described the same way. The equivalent multilevel inverter circuit diagrams in Fig. 2 and the PWM algorithm to generate PWM patterns in Fig. 7 remain valid for an arbitrary number *n*-level inverter when the offset function $v^*_{\rm off}$ in (13) is generalized in the form as $v^*_{\rm off}=\frac{n-1}{2}+\frac{V_{\rm CM}}{V_{\rm dc}}$. Then, the equipotential PWM control of minimum common mode will be realized by setting the reference CMV $V_{\rm CM}$ to minimum with the use of (23).

The formulation (14) is thus generalized as

$$F_L+F_e=\begin{cases}3(n-1)/2, & \text{for odd level inverter} \quad \text{(a)}\\ (3(n-1)\pm 1)/2, & \text{for even level inverter.} \quad \text{(b)}\end{cases}\tag{24}$$

The algorithms of the equipotential PWM control of minimum CMV can be implemented based on the common-mode functions (F_L, F_e). Solving (24a) to obtain $(F_L,\ F_e)$ values of odd-multilevel inverters has been described in (19). For even-multilevel inverters, the values of $(F_L,\ F_e)$ of the two cases in (24b) can be expressed as follows:

$$\begin{cases}F_e=1, & F_L=3n/2-2\\ F_e=2, & F_L=3n/2-3\end{cases},\quad V_{\rm CM}=+V_{\rm dc}/6\tag{25}$$

$$\begin{cases}F_e=1, & F_L=3n/2-3\\ F_e=2, & F_L=3n/2-4\end{cases},\quad V_{\rm CM}=-V_{\rm dc}/6.\tag{26}$$

The operating voltage range of the equipotential PWM control of minimum CMV can be deduced from the CMV limits (4), (8) and Fig. 2.

For odd-multilevel inverters, a symmetrical operating voltage range is deduced as

$$-\frac{n-1}{2}\le\frac{\rm MIN}{V_{\rm dc}}<\frac{\rm MAX}{V_{\rm dc}}\le\frac{n-1}{2}.\tag{27}$$

For an even-multilevel inverter with PWM control of the equipotential levels of $+V_{\rm dc}/6$ and $-V_{\rm dc}/6$, the corresponding

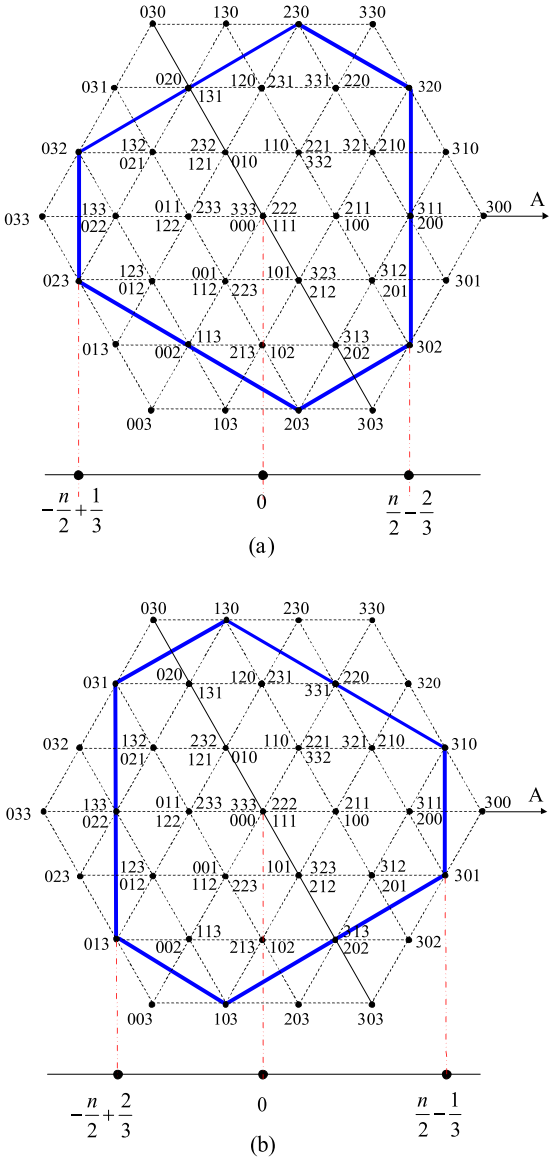

Fig. 9. Vector diagrams of four-level inverter. (a) Limits of the equipotential vector diagram of the CMV of $+V_{\rm dc}/6$. (b) Limits of the equipotential vector diagram of the CMV of $-V_{\rm dc}/6$.

limits of working areas are determined, respectively, as

$$-\frac{n}{2}+\frac{1}{3}\le\frac{\rm MIN}{V_{\rm dc}}<\frac{\rm MAX}{V_{\rm dc}}\le\frac{n}{2}-\frac{2}{3} \tag{28}$$

$$-\frac{n}{2}+\frac{2}{3}\le\frac{\rm MIN}{V_{\rm dc}}<\frac{\rm MAX}{V_{\rm dc}}\le\frac{n}{2}-\frac{1}{3}. \tag{29}$$

It can be concluded from (27) that the PWM control method to eliminate CMV of the odd-multilevel inverters attains a full voltage range in the symmetrical vector diagram. Equations (28) and (29) show that the voltage vector diagram of even-level inverters in the equipotential PWM control is unsymmetrical, as illustrated in Fig. 9(a) and (b), of a four-level inverter, corresponding to the CMVs of $V_{\rm CM}=\pm V_{\rm dc}/6$. Under the unsymmetrical hexagon diagram, the dc-link voltage capability cannot be fully utilized. A hybrid PWM control combining both equipotential vector diagrams of $V_{\rm CM}=\pm V_{\rm dc}/6$ can help extend the output voltage range, thus improving the dc voltage performance.

The PWM method has been proposed under the condition of dc voltage balancing, which can be satisfied in the multilevel inverter topologies with the active front end rectifiers. For the NPC inverter topology with the passive front-end rectifier, the dc voltage balancing is often problematical. The dc voltage balancing can be improved by controlling the dc neutral point currents. For the equipotential PWM control with the neutral point currents taken into account, several PWM modes may be considered as (we suppose odd-level inverter): 1) PWM mode from three nearest ZCMV vectors; 2) PWM mode from three nonnearest ZCMV vectors; 3) PWM mode from three nearest equipotential vectors; and 4) PWM mode from three nonnearest equipotential vectors. The PWM mode from three nonnearest vectors may require higher number of switching as compared to other PWM modes. Afterward, a PWM mode to satisfy some optimal condition for dc voltage balancing will be selected.

Recently, the predictive control has been intensively developed for power converters [34]. The method selects among the ZCMV vectors those to meet the cost function, which includes minimizing the dc voltage imbalance factor.

III. Switching Losses Optimization

The switching losses increase linearly with the magnitude of the commutating phase current under the condition of the same dc-link voltages. The average value of the local (per carrier cycle) switching loss over the fundamental (for instance, for phase A) can be calculated as [33]

$$P_{\rm swave}=\frac{1}{2\pi}\frac{V_{\rm dc}(t_{\rm on}+t_{\rm off})}{2T_s}\int_0^{2\pi}f_{iA}(\theta)d\theta \tag{30}$$

where $t_{\rm on}$ and $t_{\rm off}$ represent the turn-on and turn-off times of the switching devices, respectively, and $f_{iA}(\theta)$ is the switching current function, the instantaneous value of which is defined as a product of the number of commutations on the *A*-phase in a switching period and the absolute value of its corresponding current $|i_A(\theta)|$

$$f_{iA}(\theta)=k.\,|i_A(\theta)|\,. \tag{31}$$

The switching loss function (SLF) is defined as

$$\text{SLF}=\frac{P_{\rm swave}}{P_0} \tag{32}$$

where P_0 is the maximum value of the switching loss attainable for the defined load currents.

When using the proposed PWM method with two standardized PWM patterns in Fig. 6, the distribution of commutations in a switching period is unequal on each phase. The *d*-sequence has double the number of commutations compared to the other s_1, s_2-sequences. The factor k is thus determined as follows:

$$k=\begin{cases}2, & \text{if } A\to d\\ 1, & \text{else.}\end{cases} \tag{33}$$

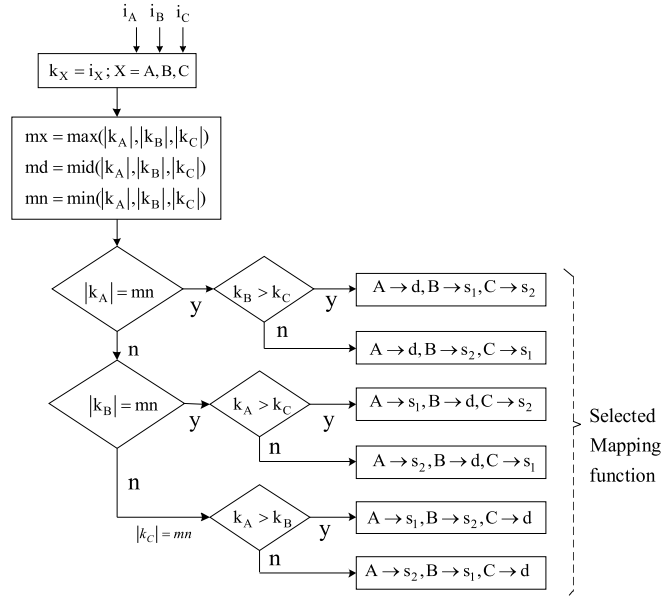

Fig. 10. Block diagram of the proposed current-based mapping PWM algorithm to optimize the switching loss.

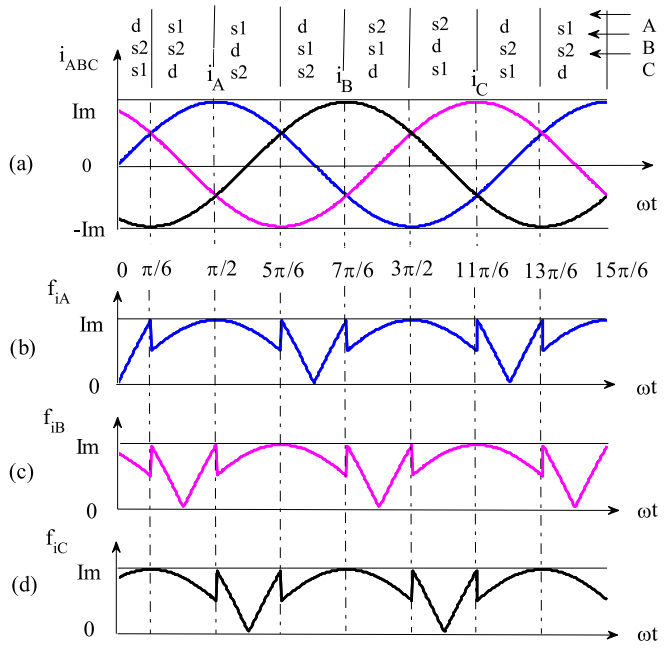

Fig. 11. (a) Current-based mapping PWM method and switching current functions: (b) $f_{iA}(\theta)$. (c) $f_{iB}(\theta)$. (d) $f_{iC}(\theta)$.

By substituting (33) into (31), we conclude that $f_{iA}(\theta)$ equals double the absolute value of the corresponding phase current in the interval that the *A*-phase is mapped into the *d*-sequence ($A \rightarrow d$), and equals the absolute value of the current in other cases.

The mapping function, as described in Table I, can be altered between six possible cases so that an arbitrary output phase can be mapped into the *d*-sequence. If all the selected mapping functions satisfy the constraint that only the output phase of the minimum absolute current is mapped to the *d*-sequence, then the switching current function described in (31) will always be obtained with the minimized value. The switching loss function in (32) can thereby be optimized. Based on this idea, a current-based mapping PWM algorithm that optimizes the switching loss is proposed in Fig. 10.

In the proposed mapping PWM algorithm with optimized switching loss shown in Fig. 10, the feedback currents i_A, i_B, i_C are utilized as inputs of the flow diagram: $k_X = i_X (X = A, B, C)$. mx, md, mn are determined as the maximum, medium, and minimum of the absolute values of i_A, i_B, i_C, respectively. The mapping function is chosen so that the phase with minimum absolute current is mapped to the *d*-sequence. The selected mapping function is then utilized to complete the proposed PWM scheme of ZCMV in Fig. 7.

Fig. 11(a) illustrates the operation of the proposed current-based mapping method in Fig. 10 following the feedback waveforms of the output currents. By using (31) and (33), the *A*-phase switching current function waveform $f_{iA}(\theta)$ is derived as shown in Fig. 11(b). Since the *A*-phase is set to the *d*-sequence during the interval that its current attains a minimum absolute value, the waveform of $f_{iA}(\theta)$ always confines a minimized Ampere-second area regardless of the phase displacement. Hence, the waveform $f_{iA}(\theta)$ corresponds to a minimum value P_{swOpt} of the switching loss P_{swave} defined by (30)

$$P_{\mathrm{swOpt}} = \frac{1}{4\pi} \frac{V_{\mathrm{dc}} I_m (t_{\mathrm{on}} + t_{\mathrm{off}})}{T_s} A_{\mathrm{Opt}}$$
$$A_{\mathrm{Opt}} = 8 - 2\sqrt{3} = 4.5359. \quad (34)$$

Similarly, the optimized waveforms of the *B* and *C* phase switching current functions are shown in Fig. 11(c) and (d), respectively.

To evaluate the improvement of the switching loss when using the proposed current-based mapping PWM, it is necessary to determine the range of the switching loss function. This can be done by an analysis of a so-called voltage-based mapping algorithm under different phase displacements. The voltage-based mapping algorithm can be simply implemented by replacing $i_X (X = A, B, C)$ with the reference load voltages $v^*_{X1} (X = A, B, C)$ as inputs of the flow diagram in Fig. 10. mx, md, mn are then, respectively, the maximum, medium, and minimum of the absolute values of $v^*_{X1} (X = A, B, C)$. The voltage-based mapping algorithm which operation following the waveforms of the reference output voltages is illustrated in Fig. 12(a). Since the rule of switches distribution of the voltage-based mapping PWM is based on information of the reference voltage (offline), the waveform of $f_{iA}(\theta)$ is changed differently depending on the phase displacement φ. For example, three cases of phase displacement: $\varphi = 0, \varphi = \pi/6, \varphi = \pi/2$ shown in Fig. 12(b)–(d), respectively, will result in three different waveforms of $f_{iA}(\theta)$ as shown in Fig. 13(a)–(c).

In the case of $\varphi = 0$, the *A*-phase output current, as illustrated in Fig. 12(b), is in phase with its corresponding reference load voltage v^*_{A1}. As shown in Fig. 13(a), the waveform of the

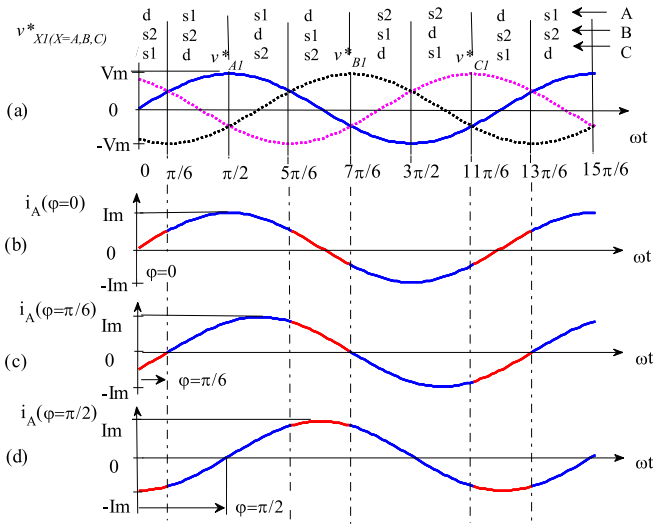

Fig. 12. (a) Voltage-based mapping PWM method with different phase displacements: (b) $\varphi = 0$. (c) $\varphi = \pi/6$. (d) $\varphi = \pi/2$.

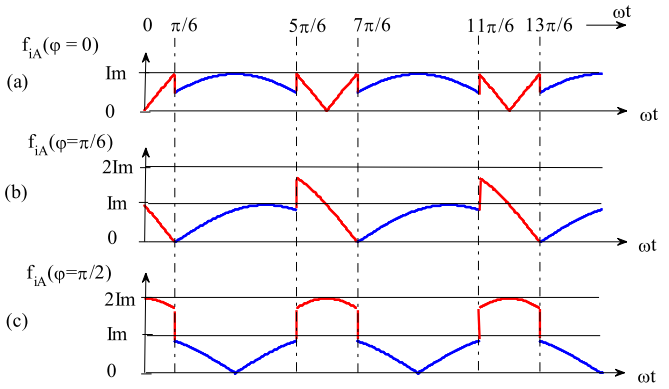

Fig. 13. Waveforms of switching current function using the voltage-based PWM method: (a) $\varphi = 0$. (b) $\varphi = \pi/6$. (c) $\varphi = \pi/2$.

A-phase switching current function is identical to one obtained by using the current-based mapping algorithm in Fig. 11(b). The switching loss P_{swave} thus corresponds to the minimum value P_{swOpt} expressed in (34).

A general evaluation using (30), (31), and (33) shows that the switching loss P_{swave} increases from its optimum value P_{swOpt} to its maximum value P_0 attainable for the defined load current if the phase displacement φ increases from 0 to $\pi/2$. As shown in Fig. 12(d), at $\varphi = \pi/2$, the *A*-phase is set to the *d*-sequence of double commutations during the interval when its current reaches its maximum absolute value. P_0 can be computed as

$$P_0 = \frac{1}{4\pi}\frac{V_{\text{dc}} I_m (t_{\text{on}} + t_{\text{off}})}{T_s} A_{\text{Max}}, \qquad A_{\text{Max}} = 6. \tag{35}$$

As a result, the SLF characteristics of the voltage-based mapping algorithm along with the current-based mapping algorithm (optimizing algorithm) analyzed in the region $0 \le \varphi \le \pi$ are shown in Fig. 14.

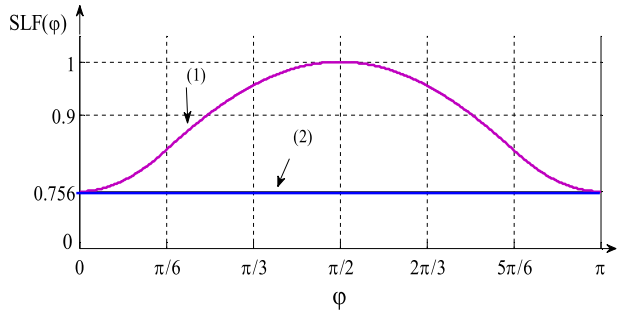

Fig. 14. Characteristic of switching loss function $\text{SLF}(\varphi)$ of the voltage-based mapping PWM method (1) and optimizing method (2).

By applying the optimizing algorithm at the power factor (PF) of 0.85, in comparison with the voltage-based mapping PWM algorithm, the switching loss function decreases by about 10%. For PF<0.55, the reduction can be more than 20%. Fig. 14 shows that the switching loss function can be reduced by 25% at the phase displacement of 90°. Since the number of commutations in a switching period of the proposed PWM method is reduced to two thirds as compared to [15], the switching loss function can then be reduced by 43% compared to the mentioned method.

The average switching loss over the fundamental given in (30) is based on an assumption that a phase-current is constant during a sampling period. In fact, the instantaneous current at the turn-on and turn-off transitions in one sampling period can be different if the sampling period is large enough. In order to obtain a more accurate value of the total switching loss from the simulation data, the switching losses at the turn-on and turn-off processes of each IGBT can be estimated separately. If we define v_{CE} the measured voltage across the IGBT and i_C the current through the switch, the average switching loss P_{loss} in the switch (over the output fundamental) can be calculated as [35]

$$P_{\text{loss}} = \frac{1}{2} f_o \cdot \left[\sum_{j=1}^{N1} v_{\text{CE}} i_{j\text{ON}} . t_{\text{on}} + \sum_{j=1}^{N2} v_{\text{CE}} i_{j\text{OFF}} . t_{\text{off}} \right] \tag{36}$$

where $i_{j\text{ON}}$ is the value of i_C at the end of an jth turn-on transition, $i_{j\text{OFF}}$ is the value of i_C at the beginning of an jth turn-off transition and $N1$ and $N2$ are, respectively, the number of turn-on and turn-off transitions in one output cycle.

If we suppose that a five level cascaded inverter is made up of IGBTs of $t_{\text{on}} = 0.46\,\mu$s and $t_{off} = 0.76\,\mu$s , characteristics of the total switching loss P_{SWloss} versus the modulation index of the proposed method with voltage-based mapping algorithm, current based mapping algorithm and [15] are given in Fig. 15.

The comparisons are given for two switching frequencies of 2.1 and 4.2 kHz. The P_{SWloss} comparison is shown in Fig. 15(a) for the load parameters of $R = 1\,\Omega$, $L = 1\,\text{mH}$, which corresponds to the phase displacement $\varphi = 17.5°$. It can be derived from Fig. 15(a) that, at switching frequency of 2.1 kHz, the switching loss reduction of the proposed ZCMV PWM with current-based mapping as compared to [15] is about 39.1% and 41.1% at modulation indices of 0.2 and 0.8, respectively. When the switching frequency is set as 4.2 kHz, these

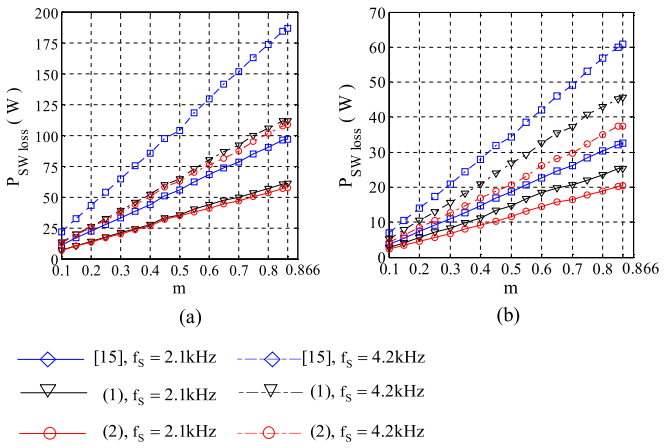

Fig. 15. Comparison of estimated switching losses of the proposed ZCMV PWM method [voltage-based mapping (1) and current-based mapping (2)] and [15] of a five-level cascaded inverter ($V_{\rm dc} = 100\,{\rm V}, f_o = 50\,{\rm Hz}$). (a) $R = 1\,\Omega, L = 1\,{\rm mH}$. (b) $R = 0.5\,\Omega, L = 10\,{\rm mH}$.

percentages of reduction are about 41.4% and 41.6%. Similarly, the switching loss comparison is given in Fig. 15(b) for the case of $R = 0.5\,\Omega,\ L = 10\,{\rm mH}$ ($\varphi = 81°$).

The proposed ZCMV with voltage-based mapping algorithm, as expected, yields higher switching loss as compared to the proposed ZCMV with current-based mapping algorithm in the two cases of the phase displacement (see Fig. 15). The percentage of switching loss reduction of the proposed PWM method with current-based mapping algorithm compared to the one with voltage-based mapping algorithm is increased corresponding to the increased value of φ in Fig. 15(b). For example, at switching frequency of 2.1 kHz and modulation index of 0.8, the percentage of reduction in the case of $\varphi = 17.5°$ is 6.6%, whereas it is 19.7% in the case of $\varphi = 81°$.

Fig. 16(a) and (b) illustrates the total harmonic distortion (THD) characteristic of the output line voltage of five-level and seven-level cascaded inverters following the variation of the modulation index m and the phase displacements φ of the proposed ZCMV PWM method with switching loss optimization. In the simulation model of the cascaded seven-level inverter, each phase consists of three H-bridges, each of which is supplied with the dc-link voltage of $V_{\rm dc} = 66.66$ V. The THDs are analyzed up to the 49th harmonic of the fundamental output frequency.

Illustrations of line voltage THD versus the modulation index corresponding to phase displacements of 0°, 18.5°, 55°, 80°, 90° are given in Fig. 17(a) for a five-level inverter and Fig. 17(b) for a seven-level inverter. At modulation index of 0.2, the output line voltage THDs of the five-level inverter for the phase displacements of 18.5° and 80° are 96.3% and 78.05%, respectively, whereas they are 62.4% and 60.07%, respectively, for the seven-level inverter.

For comparison, the THD performances of the five-level and seven-level inverter with conventional sinusoidal PWM method are also illustrated in Fig. 17(a) and (b). The conventional method, as expected, yields better results of output line voltage THD in the entire region of the modulation index.

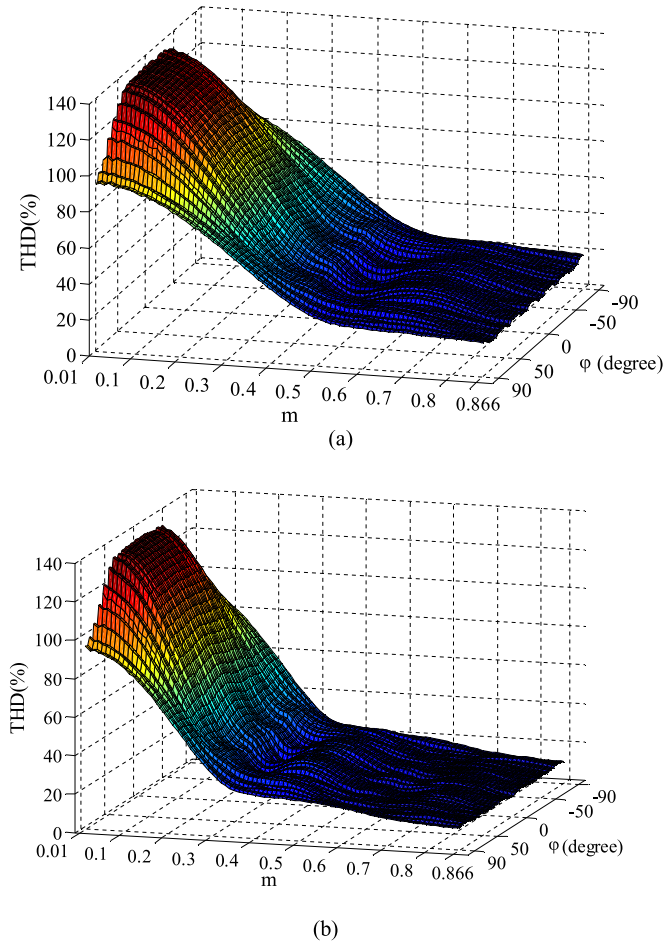

Fig. 16. THD of output line voltage of the proposed ZCMV PWM method with switching loss optimization. (a) Five level ($V_{dc} = 100\ V, f_S = 2100\ Hz, f_o = 50\ Hz$). (b) Seven level ($V_{dc} = 66.66\ V, f_S = 2100\ Hz, f_o = 50\ Hz$).

IV. Experimental Verification

In order to validate the proposed PWM strategy, experimental results were obtained by applying the proposed schemes to a five-level cascaded inverter. Each H-Bridge is made up of IGBTs using FGL-60N100-BNTD. The dc voltage on each H-Bridge is held constant at 100 V. The rating of each dc-link capacitor used for the experimental setup is 6800 μF. The load is an *RL* load, which can be set at a different value in each experiment to create different phase displacements. The fundamental frequency f_o is selected as 50 Hz. The frequency of the triangle carrier waveform f_s is 2.1 kHz. In an online algorithm for switching loss optimization, two additional Hall sensors LA55-P are used to measure two output currents. Since the three-phase load is balanced, the third current can be deduced from the two measured currents. For comparison, the conventional sinusoidal PWM method is also realized.

Figs. 18 and 19 represent the obtained waveforms of the output line voltage when using the conventional sinusoidal PWM method and the proposed ZCMV PWM method with switching loss optimization at a modulation index of 0.4 and 0.866, respectively. There are different line-to-line voltage

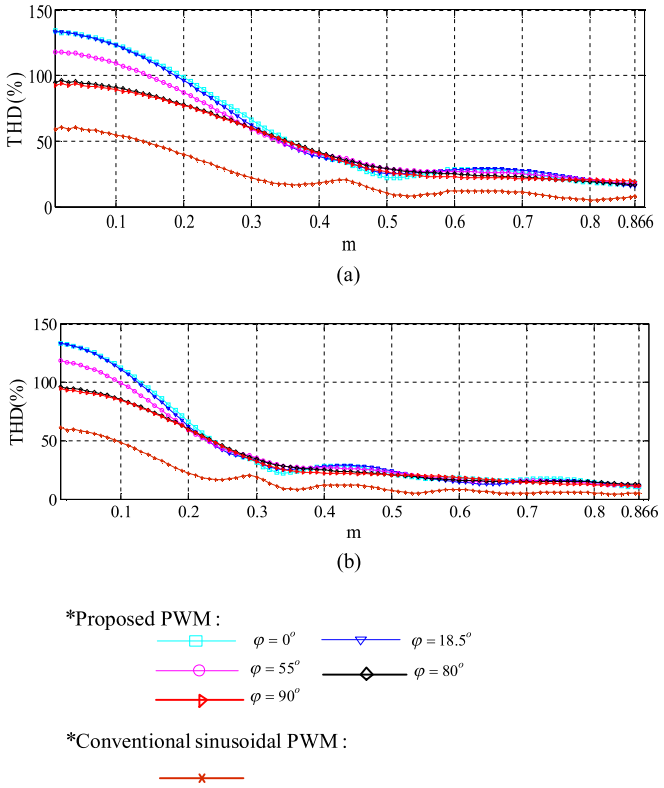

Fig. 17. Line voltage THD characteristics of the proposed ZCMV PWM method with switching loss optimization at different phase displacements and the sinusoidal PWM method. (a) Five level ($V_{dc} = 100\,V, f_S = 2.1\,kHz,\ f_o = 50\,Hz$). (b) Seven level ($V_{dc} = 66.66\,V, f_S = 2.1\,kHz,\ f_o = 50\,Hz$).

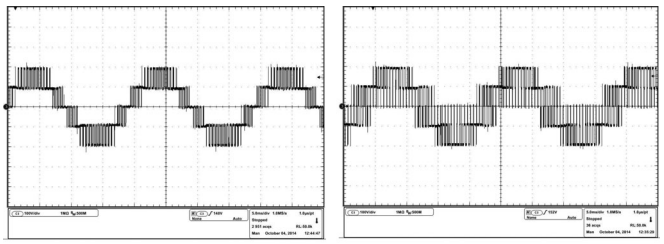

Fig. 18. Waveforms of output line voltage V_{AB} at modulation index $m = 0.4$ ($f_o = 50\,\text{Hz}$, $R = 80\,\Omega$, $L = 85\,\text{mH}$): *X*-axis: 5 ms/div; *Y*-axis: 100 V/div. (a) Conventional sinusoidal PWM method (THD = 19.14%). (b) Proposed ZCMV PWM method with switching loss optimization (THD = 39.55%).

levels when the inverter operates with and without a CMV elimination scheme. The output line voltage THD of the proposed PWM method (calculated up to the 49th harmonic of f_o) is 39.55% and 16.62% at a modulation indices of 0.4 and 0.866, respectively, whereas it is 19.14% and 8.07%, respectively, with the conventional sinusoidal PWM method. For different modulation indices in the range [0.1–0.866], Fig. 20 shows the experimental line voltage THD comparison between the proposed PWM method corresponding to three-phase displacements $\varphi = 18.5°$ ($R = 80\,\Omega,\ L = 85\,\text{mH}$), 55° ($R = 40\,\Omega,\ L = 160\,\text{mH}$), 80°($R = 10\,\Omega,\ L = 180\,\text{mH}$), and

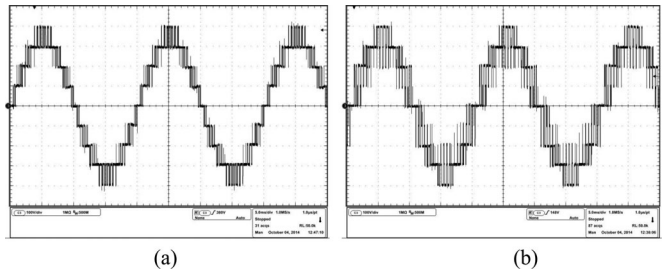

Fig. 19. Waveforms of output line voltage V_{AB} at modulation index $m = 0.866$ ($f_o = 50\,\text{Hz}$, $R = 80\,\Omega$, $L = 85\,\text{mH}$): *X*-axis: 5 ms/div; *Y*-axis: 100 V/div. (a) Conventional sinusoidal PWM method (THD = 8.07%). (b) Proposed ZCMV PWM method with switching loss optimization (THD = 16.62%).

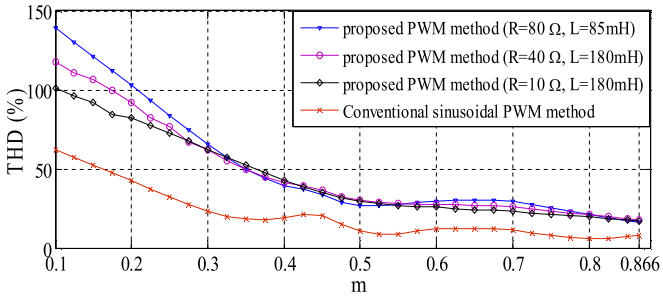

Fig. 20. Experimental line voltage THD comparison between the proposed ZCMV PWM method with switching loss optimization ($\varphi = 18.5°$,$\varphi = 55°$, and $\varphi = 80°$) and the sinusoidal PWM method for different modulation indices. (a) Conventional sinusoidal PWM method (THD = 2.98%). (b) Proposed ZCMV PWM method with switching loss optimization (THD = 6.27%).

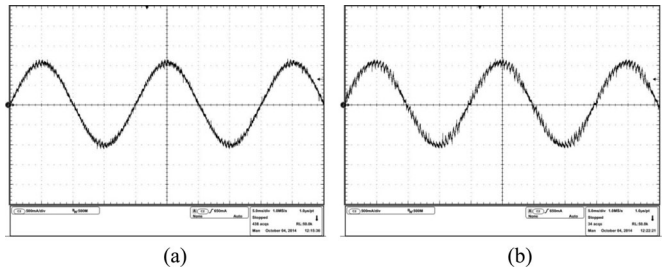

Fig. 21. Waveforms of output line current at modulation index $m = 0.4$ ($f_o = 50\,\text{Hz}$, $R = 80\,\Omega$, $L = 85$ mH.): *X*-axis: 5 ms/div; Y-axis: 0.5 A/div. (a) Conventional sinusoidal PWM method (THD = 2.98%). (b) Proposed ZCMV PWM method with switching loss optimization (THD = 6.27%).

the conventional sinusoidal PWM method. The output current waveforms at modulation indexes 0.4 and 0.866 using the two PWM methods are also depicted in Figs. 21 and 22, respectively. The output current THD (calculated up to the 49th harmonic of f_o) when using the proposed PWM method is 6.27% and 2.53% for a modulation index of 0.4 and 0.866, whereas it is 2.98% and 1.38% with the conventional sinusoidal PWM method.

Figs. 23 and 25 compare the CMV waveform between the proposed PWM method and the conventional PWM method for modulation indices of 0.4 and 0.866. The CMV represented with a large magnitude in Figs. 23(a) and 25(a) has been eliminated in Figs. 23(b) and 25(b). The existence of switching spikes in the CMV waveforms in Fig. 23(b) and 25(b) is due to the

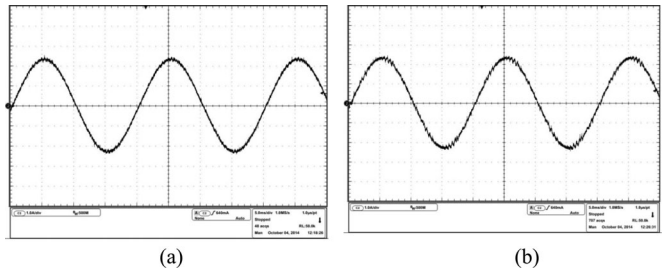

Fig. 22. Waveforms of output line current at modulation index $m = 0.866$ ($f_o = 50\,\mathrm{Hz}$, $R = 80\,\Omega$, $L = 85\,\mathrm{mH}$): *X*-axis: 5 ms/div; *Y*-axis: 1 A/div. (a) Conventional sinusoidal PWM method (THD = 1.38%). (b) Proposed ZCMV PWM method with switching loss optimization (THD = 2.53%).

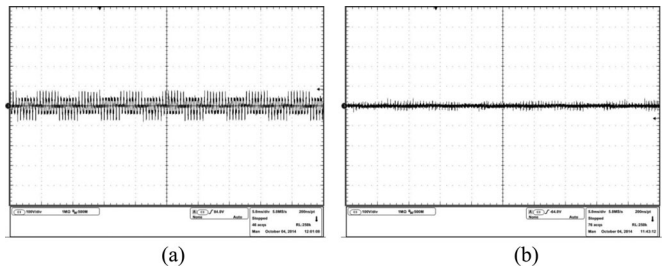

Fig. 23. Waveforms of the CMV at modulation index $m = 0.4$($f_o = 50\,\mathrm{Hz}$, $R = 80\,\Omega$, $L = 85\,\mathrm{mH}$): *X*-axis: 5 ms/div; *Y*-axis: 100 V/div. (a) Conventional sinusoidal PWM method. (b) Proposed ZCMV PWM method with switching loss optimization.

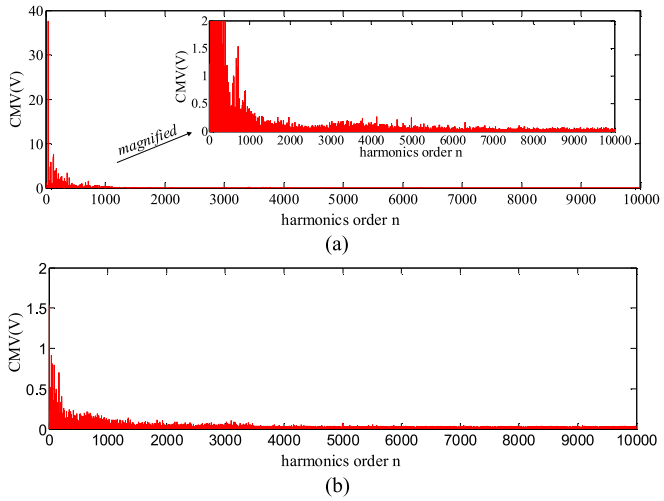

Fig. 24. Harmonic spectrums of the CMV at modulation index $m = 0.4$ ($f_o = 50\,\mathrm{Hz}$, $R = 80\,\Omega$, $L = 85\,\mathrm{mH}$). (a) Conventional sinusoidal PWM method. (b) Proposed ZCMV PWM method with switching loss optimization.

dead-time intervals during switching transitions. Figs. 24(a) and 26(a) show the spectrum of the CMV with the conventional sinusoidal PWM method, while Figs. 24(b) and 26(b) show the spectrum of the CMV with the proposed ZCMV PWM method with switching loss optimization. All harmonic spectrums are analyzed up to the 10 000th harmonic of the output fundamental frequency f_o. Comparisons of Figs. 24(a), (b) and Figs. 26(a), (b) clearly show the effectiveness of the proposed PWM strategy

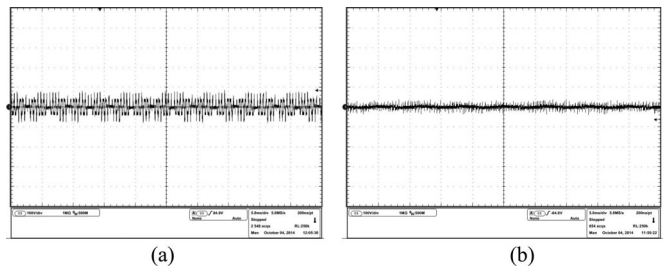

Fig. 25. Waveforms of the CMV at modulation index $m = 0.866$($f_o = 50\,\mathrm{Hz}$, $R = 80\,\Omega$, $L = 85\,\mathrm{mH}$): *X*-axis: 5 ms/div; *Y*-axis: 100 V/div. (a) Conventional sinusoidal PWM method. (b) Proposed ZCMV PWM method with switching loss optimization.

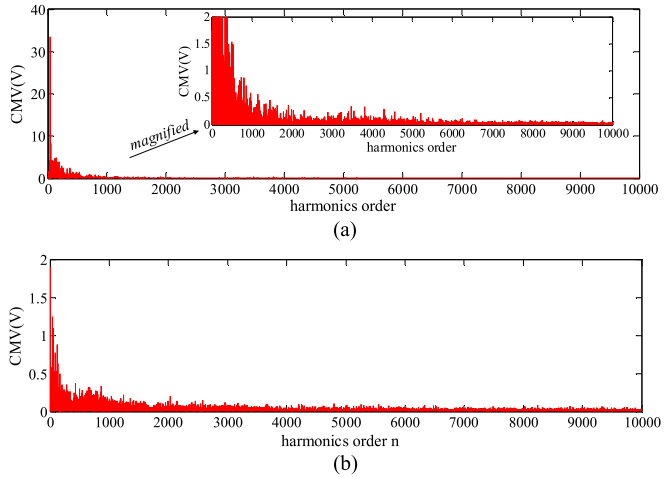

Fig. 26. Harmonic spectrums of the CMV at modulation index $m = 0.4$ ($f_o = 50\,\mathrm{Hz}$, $R = 80\,\Omega$, $L = 85\,\mathrm{mH}$). (a) Conventional sinusoidal PWM method. (b) Proposed ZCMV PWM method with switching loss optimization.

to eliminate the CMV. There are harmonics with high magnitudes in the harmonic spectrum of the CMV as depicted in Figs. 24(a) and 26(a). The largest peak values of harmonic magnitude (which are located at the carrier frequency) are about 37.5 and 33.5 V at modulation indices of 0.4 and 0.866, as shown in Figs. 24(a) and 26(a), respectively. In the harmonic spectrum of the CMV with the proposed PWM method in Figs. 24(b) and 26(b), magnitudes of the carrier harmonic and other harmonics are limited to small levels that are below 2-V peak value. The harmonic spectra of the conventional PWM in Figs. 24(a) and 26(a) are also magnified in the same scale of volt/harmonic-order of the harmonic spectra in Figs. 24(b) and 26(b). The comparisons also demonstrate significant improvement of CMV harmonic spectra in high frequency when using the proposed ZCMV PWM method. Considering the nonideal conditions of the experiment, the obtained results of CMV harmonic spectra using the proposed PWM method are acceptable compared to the ideal result of all zero levels in theoretical analysis.

Experimental results including waveforms of three-phase currents $i_X\,(X = A, B, C)$ and *A*-phase output voltage V_A (which is measured from the output terminal *A* to the load neutral) are shown in Fig. 27 for the voltage-based mapping algorithm and in Fig. 28 for the switching loss optimizing mapping algorithm.

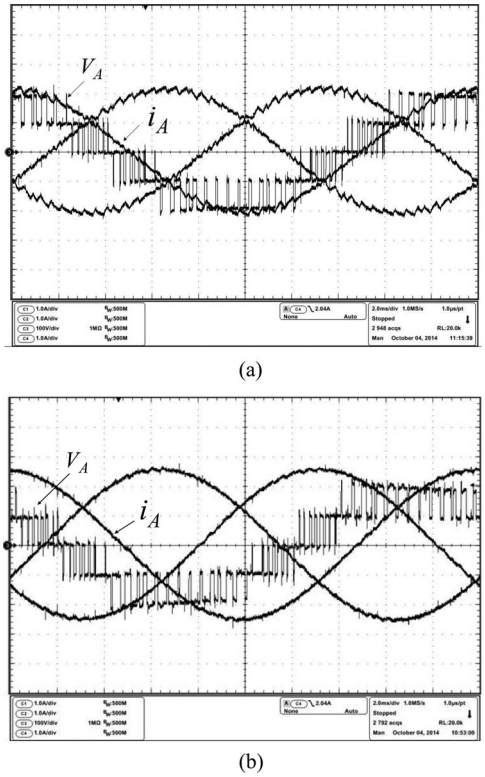

Fig. 27. Experimental results when using the proposed ZCMV PWM method with the voltage-based mapping technique. $m = 0.8, f_o = 50\,\mathrm{Hz}$, waveforms include three phase currents (*Y*-axis: 1 A/div) and *A*-phase voltage V_A (*Y*-axis: 100 V/div). *X*-axis: 5 ms/div. (a) $\varphi = 18.5^\circ$ ($R = 80\,\Omega,\ L = 85\,\mathrm{mH}$). (b) $\varphi = 55^\circ$ ($R = 40\,\Omega$,$L = 180\,\mathrm{mH}$).

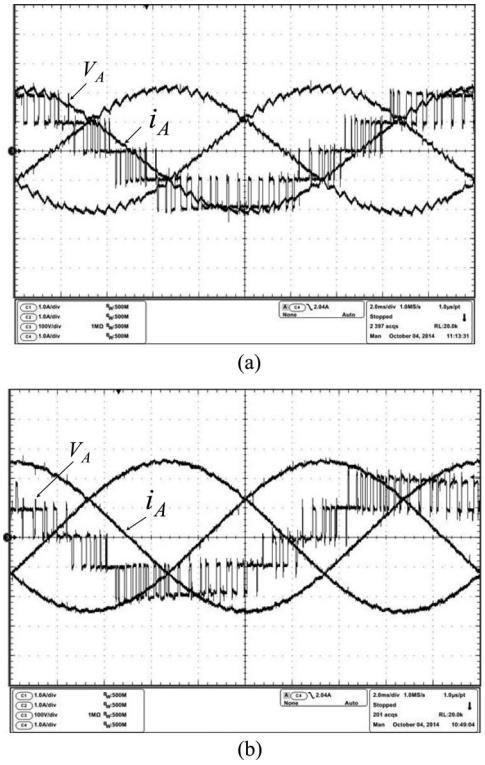

Fig. 28. Experimental results when using the proposed ZCMV PWM method with switching loss optimization. $m = 0.8,\ f_o = 50\,\mathrm{Hz}$, waveforms include three phase currents (*Y*-axis: 1 A/div) and *A*-phase voltage V_A (*Y*-axis: 100 V/div). *X*-axis: 5 ms/div. (a) $\varphi = 18.5^\circ$ ($R = 80\,\Omega$,$L = 85\,\mathrm{mH}$). (b)$\varphi = 55^\circ$ ($R = 40\,\Omega$,$L = 180\,\mathrm{mH}$).

The *RL* load with $R = 80\,\Omega,\ L = 85\,\mathrm{mH}$ corresponds to the phase displacement $\varphi = 18.5°$, which is used for the experiment of the voltage-based mapping algorithm in Fig. 27(a). In Fig. 27(b), the load is changed to $R = 40\,\Omega,\ L = 180\,\mathrm{mH}$, which corresponds to $\varphi = 55°$. As shown in Fig. 27(a) and (b), double commutation on the *A*-phase occurs at two different intervals of its fundamental period when the displacement is changed from $\varphi = 18.5°$ to 55°. By using the same experimental configuration in Fig. 27 and applying the current-based mapping algorithm (switching loss optimizing algorithm), the experimental results are obtained as shown in Fig. 28. In both cases of the phase displacement, the double commutations on the *A*-phase are confined to intervals of the minimum absolute value of its current, as shown in Fig. 28(a) and (b). This confirms the effectiveness in switching loss optimization of the current-based mapping algorithm that is analyzed theoretically in this paper.

V. Conclusion

This paper proposes a novel PWM strategy to eliminate CMV for multilevel inverters using the principle of the three zero common-mode vectors. The modulation of an *n*-level inverter with CMV elimination is simplified to that of an active two-level inverter with three available switching states. Based on a general analysis of an *n*-level inverter, two standardized virtual PWM patterns are proposed to cover the whole space vector diagram. The resultant PWM patterns made up of switching states of the three zero common-mode vectors have a minimum number of commutations among those in which each switching state is symmetrically distributed. Using the optimizing PWM algorithm, the local reduction of switching loss can be up to 25% compared to nonoptimized algorithms and 43% compared to the previous work [15]. At the beginning, the PWM method was proposed to eliminate the CMV. Then, it has been generalized as an equipotential PWM control method, which is valid to both odd- and even-multilevel inverter. Experimental results verify the effectiveness of the proposed PWM method in CMV elimination and switching loss optimization.

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