A Novel Control Scheme of DCM Boost PFC Converter

Kai Yao, Wenbin Hu, Qiang Li, and Jianguo Lyu

***Abstract*—The discontinuous current mode boost power factor (PF) correction converter features a zero-current turn-on for the switch, no reverse recovery in diode, and constant frequency operations. However, when the duty cycle is constant in a line cycle, the input current contains rich third harmonic which has a phase difference of π with respect to the fundamental component. The harmonic results in not only a lower PF but also larger peak and RMS current values of the main power components, which lead to a higher conduction and switching turn-off loss. In this paper, a variable duty cycle control scheme is proposed to make the input current contain only third harmonic which is in phase with fundamental component, while remaining the same PF at a certain input voltage as that of constant duty cycle control. A method of fitting the duty cycle is further proposed for simplifying the circuit implementation. The efficiency is improved as the critical inductance increases and the peak and RMS current values consequently decrease. The proposed method also achieves an output voltage ripple or the output storage capacitance reduction. The experimental results from a prototype of 120 W are given to verify the effectiveness of the proposed method.**

***Index Terms*—Boost power factor correction (PFC), discontinuous current mode (DCM), efficiency, third harmonic.**

I. Introduction

POWER factor correction (PFC) converters have been widely used in ac–dc power conversion applications to achieve a high power factor (PF) and a low harmonic distortion. The PFC methods can be classified into active and passive types. Generally, compared with passive PFC converters, active ones can achieve a higher PF and a smaller size. There are different topologies and controls to implement active PFC techniques [1]–[11], among which, the boost converter is a representative topology. Depending on the inductor current to be continuous or not, the boost PFC converter can be designed to operate in three modes: continuous current mode (CCM), critical current mode (CRM), and discontinuous current mode (DCM).

When the boost PFC converter operates in CCM, the inductor current ripple is very small, leading to low root-mean-square (RMS) currents on the inductor and switch, and low electromagnetic interference (EMI) as well. However, the switch always operates at hard switching, and the diode suffers a reverse recovery. Hence, the CCM boost PFC converter is mainly used in high- and medium-power applications [14]–[16].

The CRM boost PFC converter has such advantages as zero-current turn-on of the switch, no reverse recovery in diode, and a high PF. However, the switching frequency is variable, resulting in difficulty in the design of the inductor and EMI filter. The CRM boost PFC converter is mainly used in medium- and low-power applications [17]–[20].

Similar to the CRM approach, the DCM boost PFC converter features zero-current turning on for the switch and no reverse recovery in diode, and it operates at a constant switching frequency, which is beneficial for designing the inductor and EMI filter [21]–[23]. Besides, as it only needs an output voltage loop control, the control circuit is simple and the cost is low. The main drawback is that the PF is not high enough, especially at a high input voltage. However, the harmonics of the input current still meet the standards of IEC and EN 61000-3-2 Class D. The DCM boost PFC converter is widely used in medium- and low-power applications.

A simplified design approach and the conduction boundary for the DCM boost PFC converter were analyzed in [24] and [25]. Theoretically, an unity PF of the DCM boost PFC converter may be achieved by a variable duty cycle control (VDC) scheme [26]–[28], which can be precisely implemented by a digital and one-cycle control [29]–[31], or approximately realized by a feedforward control [32]–[36]. Zhang and Joseph [37] derived an A-switching map to determine the exact numerical boundary between DCM and CCM under different circuit parameters circumstances. An interleaved DCM boost PFC converter was discussed in [38] and [39].

As in DCM, the power transfer does not cover the whole switching cycle, so the peak and RMS values of the inductor as well as the switch and diode current are large. Correspondingly, the current stress of the power components and the conduction and switching turn-off loss are increased; thus, the efficiency of the converter is lowered. The objective of this paper is to improve the efficiency of the DCM boost PFC converter. Section II analyzes the PF and input current harmonics of the DCM boost PFC converter. Section III analyzes the effect of the third harmonic on the input current. Section IV analyzes the derivation of the novel control scheme. In Section V, the comparison

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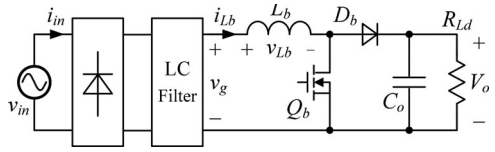

Fig. 1. Main circuit of boost PFC converter.

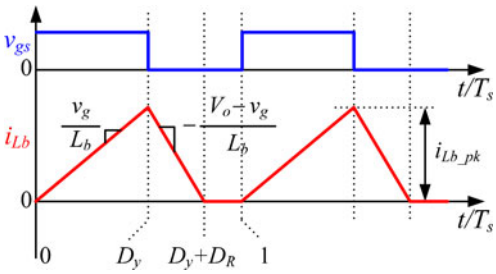

Fig. 2. Inductor current waveform in a switching cycle.

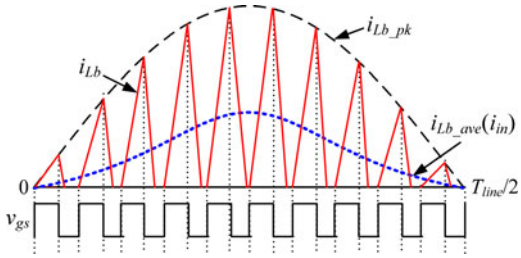

Fig. 3. Peak and average current waveforms of the inductor in a half-line cycle.

between the proposed control and the traditional constant duty cycle control is made in terms of the inductor design together with its current, input current harmonics, and output voltage ripple. A 120-W prototype has been built and tested, and the experimental results are presented in Section VI.

II. PF and Input Current Harmonics of DCM Boost PFC Converter

Fig. 1 shows the main circuit of the boost PFC converter. Fig. 2 shows the inductor current waveform in a switching cycle when the converter operates in DCM. Fig. 3 shows the peak and average current waveforms of the inductor in a half-line cycle.

The input voltage is defined as follows:

$$v_{\rm in} = V_m \sin \omega t \tag{1}$$

where V_m is the amplitude of the input voltage, and ω is the angular frequency of the input voltage.

For a constant duty cycle in a line cycle, assuming that the efficiency of the converter is 100% (a presumption which also applies to the following analysis), the peak current $i_{Lb\_\rm pk}$, the input current $i_{\rm in}$, i.e., the average inductor current $i_{Lb\_\rm ave}$ during $[0, \pi]$, the duty cycle D_y, and the PF are, respectively, expressed as

$$i_{Lb\_\rm pk} = \frac{V_m \sin \omega t \cdot D_y}{L_b f_s} \tag{2}$$

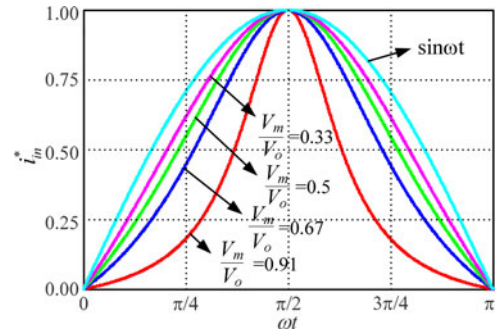

Fig. 4. Normalized input current waveform in a half-line cycle.

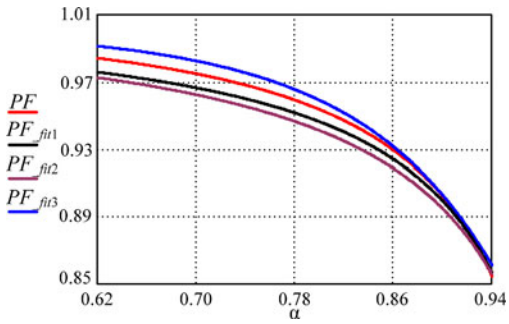

Fig. 5. PF curves.

$$i_{\rm in} = i_{Lb\_\rm ave} = \frac{V_m D_y^2}{2L_b f_s} \frac{\sin \omega t}{1 - V_m \left|\sin \omega t\right| / V_o} \tag{3}$$

$$D_y = \frac{1}{V_m} \sqrt{\frac{2\pi L_b f_s P_o}{\int_0^\pi \frac{\sin^2 \omega t}{1 - V_m \left|\sin \omega t\right| / V_o} d\,\omega t}} \tag{4}$$

$$\begin{aligned} \mathrm{PF} &= \frac{P_{\rm in}}{V_{\rm in\_rms} I_{\rm in\_rms}} = \frac{\frac{1}{\pi}\int_0^\pi v_{\rm in} i_{\rm in} d\,\omega t}{\frac{V_m}{\sqrt{2}} \sqrt{\frac{1}{\pi}\int_0^\pi i_{\rm in}^2 d\,\omega t}} \\ &= \frac{\sqrt{\frac{2}{\pi}} \int_0^\pi \frac{\sin^2 \omega t}{1 - V_m \left|\sin \omega t\right| / V_o} d\,\omega t}{\sqrt{\int_0^\pi \left(\frac{\sin \omega t}{1 - V_m \left|\sin \omega t\right| / V_o}\right)^2 d\,\omega t}} \end{aligned} \tag{5}$$

where V_o is the output voltage, P_o is the output power, and f_s is the switching frequency.

For the benefit of simplicity in the analysis, the average input current is normalized with the base of $\frac{V_m D_y^2}{2L_b f_s} \frac{1}{1 - V_m / V_o}$, and $i_{\rm in}^* = (1 - \frac{V_m}{V_o}) \frac{\sin \omega t}{1 - V_m \left|\sin \omega t\right| / V_o}$, which is plotted in Fig. 4. As can be seen, the shape of the average input current is only dependent on V_m / V_o, and a smaller V_m / V_o will lead to a shape closer to sinusoidal. Defining $\alpha = V_m / V_o$, $V_o = 400$ V and V_m ranges from $175\sqrt{2}$ to $265\sqrt{2}$ V, then α ranges from 0.62 to 0.94. From (5), the input PF can be plotted as the red line shown in Fig. 5, where PF decreases when the input voltage increases, and PF is 0.859 at the highest input voltage of 265 VAC.

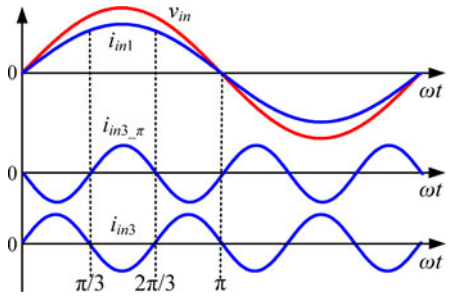

Fig. 6. Waveforms of the fundamental and third harmonics.

By Fourier analysis, the harmonics of the input current can be obtained as

$$i_{\text{in}} = \sum_{n=1}^{\infty} b_n \sin n\omega t \,(n = 1, 3, 5 \ldots) \tag{6}$$

$$b_n = \frac{2}{\pi}\int_0^{\pi} i_{\text{in}} \cdot \sin n\omega t d\,\omega t. \tag{7}$$

Substituting (3) into (6), the harmonics of the input current can be figured out.

The resultant amplitudes of the third, fifth, and seventh harmonics normalized by the fundamental component are, respectively, plotted as the curves 6, 2, and 5 shown in Fig. 13. It should be noted that the negative amplitude means that the corresponding harmonic has an initial phase difference of π with respect to the fundamental component. As can be seen, the input current mainly contains such third harmonic. The higher the input voltage, the larger the third harmonic.

III. Effect of the Third Harmonic Current on Input Current

When PFC is achieved, the fundamental input current i_{in1} is in phase with the input voltage v_{in}, i.e.,

$$i_{\text{in1}} = I_1 \sin\omega t \tag{8}$$

where I_1 is the amplitude of the fundamental component.

For an input current that contains the third harmonic with an initial phase difference of 0 with respect to the fundamental component, the third harmonic current can be expressed as

$$i_{\text{in3}} = I_3 \sin 3\omega t \tag{9}$$

where I_3 is the amplitude of the third harmonic current.

The third harmonic that has an initial phase difference of π with respect to the fundamental component can be expressed as

$$i_{\text{in3\_}\pi} = I_3 \sin(3\omega t - \pi). \tag{10}$$

Fig. 6 shows the waveforms of i_{in1}, i_{in3} and $i_{\text{in3\_}\pi}$ in a line cycle. As can be seen, in a half-line cycle and on the basis of i_{in1}, in the intervals of [0–π/3] and [2π/3–π], $i_{\text{in3\_}\pi}$ decreases the amplitude of the input current, while in the interval of [π/3–2π/3], i.e., around the peak value of i_{in1}, $i_{\text{in3\_}\pi}$ increases the amplitude of the input current. As the input current is the average value of the inductor current in a switching cycle, the peak and RMS values of the inductor current become larger. On the contrary, in the intervals of [0–π/3] and [2π/3–π], i_{in3} increases the amplitude of the input current, while in the interval of [π/3–2π/3], i.e., around the peak value of i_{in1}, i_{in3} decreases the amplitude of the input current, so the peak and RMS values of the inductor current become smaller.

In summary, if the input current contains the same amount of $i_{\text{in3\_}\pi}$ and i_{in3} in addition to i_{in1}, the PF will be the same; however, the peak and RMS current values of the inductor with i_{in3} will be greatly reduced compared to that with $i_{\text{in3\_}\pi}$. This result also applies to the current of the switch and diode. The novel control scheme of the DCM boost PFC converter is hence educed, which will be analyzed in detail in the following sections.

IV. Derivation of the VDC Control Scheme

A. Ideal Duty Cycle

An input current that contains the third harmonic with an initial phase difference of 0 can be expressed as

$$i_{\text{in}} = I_1 \sin\omega t + I_3 \sin 3\omega t = I_1 \left(\sin\omega t + I_3^* \sin 3\omega t\right) \tag{11}$$

where I_3^* is the normalized amplitude of the third harmonic by the base of the fundamental component, $I_3^* = I_3/I_1$.

According to the relationship between the PF and the total harmonics distortion (THD), PF can be expressed as

$$\begin{aligned}\text{PF} &= 1\Big/\sqrt{1+(\text{THD})^2} = 1\Big/\sqrt{1+(I_3/I_1)^2} \\ &= 1\Big/\sqrt{1+I_3^{*2}}.\end{aligned} \tag{12}$$

Due to the complexity of (5), it is hard to derive expression of the relationship between I_3^* and V_m/V_o from (5) and (12). So, it is necessary to seek a function that fits (5), which is

$$\text{PF}_{\text{\_fit1}} = (1 - 0.968\alpha)\,/\,(1 - 0.952\alpha)\,. \tag{13}$$

$\text{PF}_{\text{\_fit1}}$ is plotted in Fig. 5 and the curve of $\text{PF}_{\text{\_fit1}}$ fits well with that of PF expressed in (5).

From (12) and (13), I_3^* is calculated as

$$I_3^* = \sqrt{(1-0.952\alpha)^2/(1-0.968\alpha)^2 - 1}. \tag{14}$$

The average input power and the output power are

$$\begin{aligned}P_{\text{in}} = P_o &= \frac{1}{\pi}\int_0^{\pi} v_{\text{in}} i_{\text{in}} d\,\omega t \\ &= \frac{1}{\pi}\int_0^{\pi} V_m \sin\omega t \cdot I_1 \left(\sin\omega t + I_3^* \sin 3\omega t\right) d\,\omega t \\ &= \frac{V_m I_1}{2}.\end{aligned} \tag{15}$$

From (11) and (15), the input current with the injected third harmonic is derived as

$$i_{\text{in}} = 2P_o \left(\sin\omega t + I_3^* \sin 3\omega t\right)/V_m\,. \tag{16}$$

From (3) and (16), the corresponding duty cycle to achieve such a third harmonic in the input current is

$$D_y = D_0\sqrt{\left(1 - \alpha\left|\sin\omega t\right|\right)\left(1 + 3I_3^* - 4I_3^* \sin^2\omega t\right)} \tag{17}$$

where $D_0 = 2\sqrt{L_b f_s P_o}/V_m$.

B. Fitting Duty Cycle

Substituting (14) into (17), the duty cycle is too complicated to be implemented due to its requirement of several multipliers, dividers, and square root extractors.

For the benefit of convenience and simplicity, define $y = |\sin \omega t|$, then (17) can be rewritten as

$$D_y = D_0\sqrt{(1-\alpha y)\left(1+3I_3^*-4I_3^* y^2\right)}. \tag{18}$$

Based on Taylor's series, a function can be expanded around a point in the domain. So, (18) can be expressed as

$$D_y = D_0\left[\frac{\sqrt{(1-\alpha y_0)\left(1+3I_3^*-4I_3^* y_0^2\right)}+}{\dfrac{12I_3^*\alpha y_0^2-8I_3^* y_0-\alpha\left(1+3I_3^*\right)}{2\sqrt{(1-\alpha y_0)\left(1+3I_3^*-4I_3^* y_0^2\right)}}(y-y_0)+\cdots}\right] \tag{19}$$

where y_0 is the expanding point.

Reserving only the constant and the first derivative item, (19) is approximated as

$$D'_{y\_\text{fit}} = D_{0\_\text{fit}}\left[1-\frac{\alpha\left(1+3I_3^*\right)+8I_3^* y_0-12I_3^*\alpha y_0^2}{2\left(1+3I_3^*\right)-\alpha\left(1+3I_3^*\right)y_0-4I_3^*\alpha y_0^3}y\right] \tag{20}$$

where $D_{0\_\text{fit}} = D_0\frac{2\left(1+3I_3^*\right)-\alpha\left(1+3I_3^*\right)y_0-4I_3^*\alpha y_0^3}{2\sqrt{(1-\alpha y_0)\left(1+3I_3^*-4I_3^* y_0^2\right)}}$.

Substituting (20) into (3) leads to

$$i_{\text{in}} = \frac{V_m D_{0\_\text{fit}}^2}{2L_b f_s}\frac{\sin\omega t}{1-\alpha|\sin\omega t|}\cdot\left[1-\frac{\alpha\left(1+3I_3^*\right)+8I_3^* y_0-12I_3^*\alpha y_0^2}{2\left(1+3I_3^*\right)-\alpha\left(1+3I_3^*\right)y_0-4I_3^*\alpha y_0^3}|\sin\omega t|\right]^2. \tag{21}$$

The average input power is

$$P_{\text{in}} = \frac{1}{\pi}\int_0^\pi v_{\text{in}} i_{\text{in}} d\omega t = \frac{V_m^2 D_{0\_\text{fit}}^2}{2\pi L_b f_s}\times\int_0^\pi\frac{\left(\sin^2\omega t\right)\left[1-\frac{\alpha\left(1+3I_3^*\right)+8I_3^* y_0-12I_3^*\alpha y_0^2}{2\left(1+3I_3^*\right)-\alpha\left(1+3I_3^*\right)y_0-4I_3^*\alpha y_0^3}|\sin\omega t|\right]^2}{1-\alpha|\sin\omega t|}d\omega t. \tag{22}$$

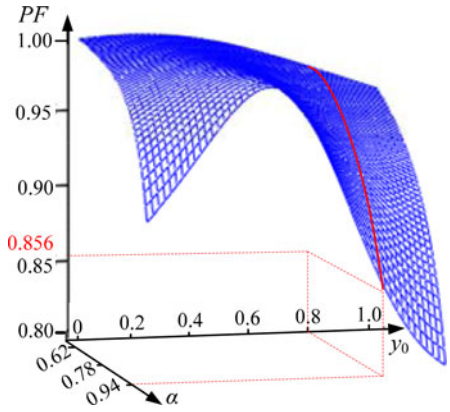

Fig. 7. Surface of the input PF as the function of α and y_0.

From (21) and (22), PF is calculated as

$$\text{PF} = \frac{P_{\text{in}}}{V_{\text{in\_rms}} I_{\text{in\_rms}}} = \frac{P_{\text{in}}}{\frac{V_m}{\sqrt{2}}\sqrt{\frac{1}{\pi}\int_0^\pi i_{\text{in}}^2 d\omega t}} = \frac{\sqrt{\frac{2}{\pi}}\int_0^\pi\frac{\sin^2\omega t\left(1-\frac{\alpha\left(1+3I_3^*\right)+8I_3^* y_0-12I_3^*\alpha y_0^2}{2\left(1+3I_3^*\right)-\alpha\left(1+3I_3^*\right)y_0-4I_3^*\alpha y_0^3}|\sin\omega t|\right)^2}{1-\alpha|\sin\omega t|}d\omega t}{\sqrt{\int_0^\pi\frac{\sin^2\omega t\left(1-\frac{\alpha\left(1+3I_3^*\right)+8I_3^* y_0-12I_3^*\alpha y_0^2}{2\left(1+3I_3^*\right)-\alpha\left(1+3I_3^*\right)y_0-4I_3^*\alpha y_0^3}|\sin\omega t|\right)^4}{(1-\alpha|\sin\omega t|)^2}d\omega t}}. \tag{23}$$

The PF expressed in (23) depends on the parameters α and y_0. The value of y_0 should be figured out so as to ensure that the PF of (23) fits well with the curve of PF in Fig. 5.

Substituting (14) into (23), PF can be plotted, as shown in Fig. 7. When $y_0 = 0.8$, the variation rule of PF with the change of α is nearly the same as that of CDC. Substituting $y_0 = 0.8$ and (14) into (23), $PF_{\_\text{fit}2}$ can be plotted in Fig. 5.

Substituting $y_0 = 0.8$ and (14) into (20) leads to (24), as shown at the bottom of the page.

It is necessary to simplify the duty cycle expressed in (24) due to its complexity.

Define $f(\alpha)$ as follow (25), as shown at the bottom of the next page, and plot it in Fig. 8

As shown in Fig. 8, the shape of $f(\alpha)$ is similar to a straight line, so a straight line function as follow is used to fit (25)

$$f_{\text{fit}}(\alpha) = m\alpha + n. \tag{26}$$

To ensure that both PF near the highest input voltages are the same as possible before and after substituting the fitting function of (26) into (24), (26) equals (25) and m is set to be the

$$D'_{y\_\text{fit}} = D_{0\_\text{fit}}\left[1-\frac{\alpha\left(1+3\sqrt{\left(\frac{1-0.952\alpha}{1-0.968\alpha}\right)^2-1}\right)+6.4\sqrt{\left(\frac{1-0.952\alpha}{1-0.968\alpha}\right)^2-1}-7.68\alpha\sqrt{\left(\frac{1-0.952\alpha}{1-0.968\alpha}\right)^2-1}}{2\left(1+3\sqrt{\left(\frac{1-0.952\alpha}{1-0.968\alpha}\right)^2-1}\right)-0.8\alpha\left(1+3\sqrt{\left(\frac{1-0.952\alpha}{1-0.968\alpha}\right)^2-1}\right)-2.048\alpha\sqrt{\left(\frac{1-0.952\alpha}{1-0.968\alpha}\right)^2-1}}|\sin\omega t|\right]. \tag{24}$$

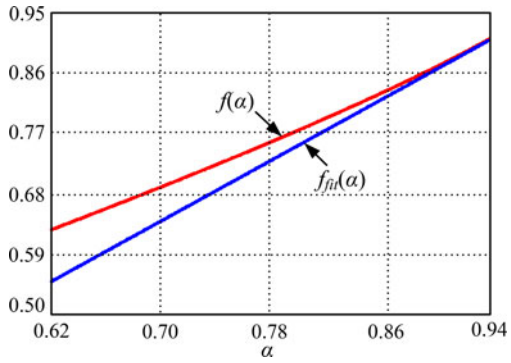

Fig. 8. Comparison of $f(\alpha)$ and $f_{\rm fit}(\alpha)$.

slope of $f(\alpha)$ at $\alpha = 0.94$, then $m = 1.13$ and $n = -0.149$. So, $f_{\rm fit}(\alpha) = 1.13\alpha - 0.149$, as shown in Fig. 8.

Substituting $f_{\rm fit}(\alpha)$ into (24), the duty cycle is expressed as

$$D_{y\_\rm fit} = D_1 \left[1 - (1.13\alpha - 0.149)\left|\sin\omega t\right|\right]. \tag{27}$$

After the design parameters of the converter are determined, D_1 in (27), $D_{0\_\rm fit}$ in (20), and D_0 in (17) are nearly the same at the same input voltage.

Derived from (1), (3), and (27), PF is

$$\begin{aligned}\mathrm{PF}_{\_\rm fit3} &= \frac{P_{\rm in}}{V_{\rm in\_rms} I_{\rm in\_rms}} = \frac{\frac{1}{\pi}\int_0^{\pi} v_{\rm in} i_{\rm in}\, d\,\omega t}{\frac{V_m}{\sqrt{2}}\sqrt{\frac{1}{\pi}\int_0^{\pi} i_{\rm in}^2\, d\,\omega t}} \\ &= \frac{\sqrt{\frac{2}{\pi}}\int_0^{\pi} \frac{\sin^2\omega t[1-(1.13\alpha-0.149)|\sin\omega t|]^2}{1-\alpha|\sin\omega t|} d\,\omega t}{\sqrt{\int_0^{\pi} \frac{\sin^2\omega t[1-(1.13\alpha-0.149)|\sin\omega t|]^4}{(1-\alpha|\sin\omega t|)^2} d\,\omega t}}. \end{aligned} \tag{28}$$

According to (28), the curve of $PF_{\_\rm fit3}$ is plotted in Fig. 5, where the value of $PF_{\_\rm fit3}$ is higher than $PF_{\_\rm fit2}$ at a low input voltage. The reason is as follows: as shown in Fig. 8, the value of $f_{fit}(\alpha)$ is lower than $f(\alpha)$ at a low input voltage which means that the variation range of the duty cycle during a half-line cycle obtained by (27) is narrower than that by (24). However, at a low input voltage, PF is high and close to 1 for CDC, so the variation range of the duty cycle can not be too wide during a half-line cycle; otherwise, PF will become lower.

According to Fig. 5, within the whole range of the input voltage, the curve of $PF_{\_\rm fit3}$ fits well with that of PF, i.e., PF of VDC is almost the same as that of CDC at any input voltage.

C. Implementation of the Control Circuit

The control circuit can be implemented as shown in Fig. 9. The rectified input voltage v_g is sensed through a voltage divider composed of R_1 and R_2, and $v_A = k_{vg} V_m \left|\sin\omega t\right|$, where k_{vg} is the voltage sensor gain. R_3, D_1, C_1, and R_4 form a circuit to obtain the peak value of the rectified input voltage, i.e., $v_B = k_{vg} V_m$. The output voltage signal, sensed through a voltage divider composed of R_5 and R_6, can be expressed as $v_C = k_{vg} V_o$, where the voltage sensor gain is k_{vg}. So, the output of the multiplier 1 is $v_D = v_A v_C / v_B = k_{vg} V_o \left|\sin\omega t\right|$.

When $R_{13}/(R_{13} + R_{15}) = 0.5 k_{vg}$ and $R_{14} = 1.3 R_{12}$, then $v_E = k_{vg}(1.15 V_o - 1.3 V_m \left|\sin\omega t\right|)$. When $R_7 = R_8$, $R_{10} = 6.6 R_9$ and $R_{11} = 1.13 R_9$, then $v_F = k_{vg}[V_o - (1.13 V_m - 0.149 V_o)\left|\sin\omega t\right|]$. The output voltage is regulated through the error amplifier; the sensed output voltage through a voltage divider composed of R_{16} and R_{17} compares with the reference voltage V_{og}. Here, V_{og} is set as 5.1 V, and the output voltage sense gain is set at 1/78.43, i.e., $R_{16} = 77.43 R_{17}$. v_F, v_C, and v_{EA}, i.e., the error signal from the compensation network formed by R_{18} and C_2, are sent to the multiplier 2, and the output $v_P = v_{EA} \cdot v_F / v_C = v_{EA}[1 - (1.13 V_m / V_o - 0.149)\left|\sin\omega t\right|]$. v_P is sent to the pulse width modulation IC and compared with the saw-tooth carrier, then the duty cycle varies as expressed in (27), where the coefficient D_1 is determined by v_{EA} and the amplitude of the saw-tooth. The component values are listed in Table I, where the no-nominal resistances are replaced by series or parallel resistors in practice.

V. Performance Comparison

A. Design of the Inductor

Substituting (27) into (3), the input current of VDC is expressed as

$$i_{\rm in} = \frac{V_m D_1^2 \left[1 - (1.13\alpha - 0.149)\left|\sin\omega t\right|\right]^2}{2 L_b f_s} \frac{\sin\omega t}{1 - \alpha\left|\sin\omega t\right|}. \tag{29}$$

From (1) and (29), the output power is expressed as

$$\begin{aligned} P_o = P_{\rm in} &= \frac{1}{\pi}\int_0^{\pi} v_{\rm in} i_{\rm in}\, d\,\omega t \\ &= \frac{V_m^2 D_1^2}{2\pi L_b f_s}\int_0^{\pi} \frac{\sin^2\omega t\left[1 - (1.13\alpha - 0.149)\left|\sin\omega t\right|\right]^2}{1 - \alpha\left|\sin\omega t\right|} d\,\omega t. \end{aligned} \tag{30}$$

Eq. (30) can be rewritten as

$$D_1 = \frac{1}{V_m}\sqrt{\frac{2\pi L_b f_s P_o}{\int_0^{\pi} \frac{\sin^2\omega t[1-(1.13\alpha-0.149)|\sin\omega t|]^2}{1-\alpha|\sin\omega t|} d\,(\omega t)}}. \tag{31}$$

Substituting (31) into (27) leads to

$$D_{y\_\rm fit} = \frac{\frac{1}{V_m}\sqrt{2\pi L_b f_s P_o}\left[1 - (1.13\alpha - 0.149)\left|\sin\omega t\right|\right]}{\sqrt{\int_0^{\pi} \frac{\sin^2\omega t[1-(1.13\alpha-0.149)|\sin\omega t|]^2}{1-\alpha|\sin\omega t|} d\,\omega t}}. \tag{32}$$

$$f(\alpha) = \frac{\alpha\left(1 + 3\sqrt{\left(\frac{1-0.952\alpha}{1-0.968\alpha}\right)^2 - 1}\right) + 6.4\sqrt{\left(\frac{1-0.952\alpha}{1-0.968\alpha}\right)^2 - 1} - 7.68\alpha\sqrt{\left(\frac{1-0.952\alpha}{1-0.968\alpha}\right)^2 - 1}}{2\left(1 + 3\sqrt{\left(\frac{1-0.952\alpha}{1-0.968\alpha}\right)^2 - 1}\right) - 0.8\alpha\left(1 + 3\sqrt{\left(\frac{1-0.952\alpha}{1-0.968\alpha}\right)^2 - 1}\right) - 2.048\alpha\sqrt{\left(\frac{1-0.952\alpha}{1-0.968\alpha}\right)^2 - 1}}. \tag{25}$$

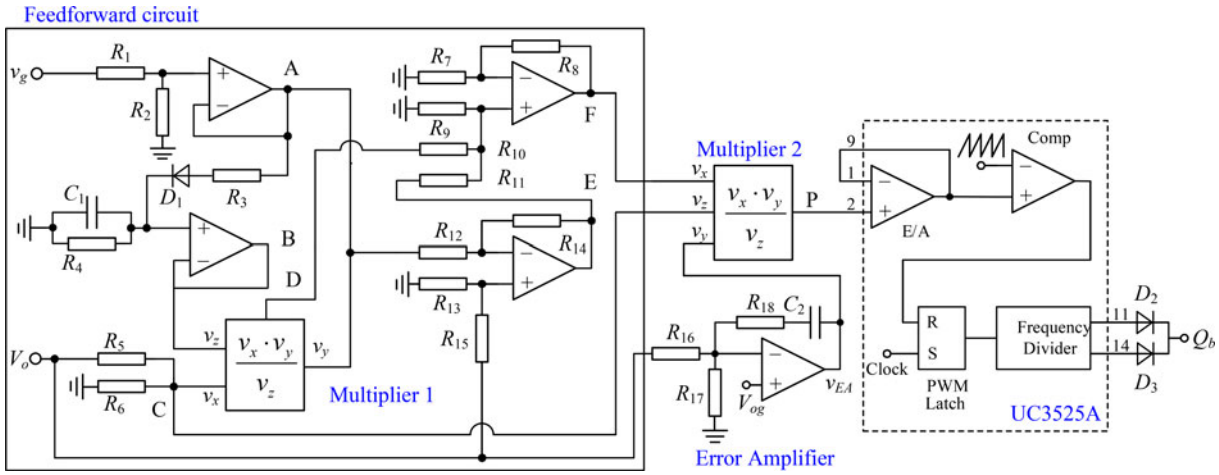

Fig. 9. Implementation circuit of VDC for the DCM boost PFC converter.

TABLE I
COMPONENTS VALUE OF THE CONTROL CIRCUIT

R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8	R_9	R_{10}	R_{11}	R_{12}
1.98 MΩ	20 kΩ	1 kΩ	750 kΩ	1.98 MΩ	20 kΩ	10 kΩ	10 kΩ	10 kΩ	66 kΩ	11 kΩ	10 kΩ
R_{13}	R_{14}	R_{15}	R_{16}	R_{17}	R_{18}						
10 kΩ	13 kΩ	1.99 MΩ	1.8 MΩ	24 kΩ	1 kΩ						

From Fig. 2, the condition for the converter to operate in DCM is

$$D_y + D_R = D_y + \frac{V_m\,|\sin\omega t|}{V_o - V_m\,|\sin\omega t|}D_y = \frac{V_o}{V_o - V_m\,|\sin\omega t|}D_y \le 1. \quad (33)$$

Substituting (4) into (33), the critical boost inductance with CDC is obtained as

$$L_{b1} \le (1-\alpha)^2 \frac{V_m^2}{2P_o f_s}\frac{1}{\pi}\int_0^{\pi}\frac{\sin^2\omega t}{1-\alpha\,|\sin\omega t|}d\,\omega t. \quad (34)$$

Substituting (32) into (33), the critical boost inductance with VDC is derived as

$$L_{b2} \le \frac{\frac{V_m^2}{2\pi P_o f_s}\int_0^{\pi}\frac{\sin^2\omega t[1-(1.13\alpha-0.149)|\sin\omega t|]^2}{1-\alpha|\sin\omega t|}d\,\omega t}{\left[\frac{1-(1.13\alpha-0.149)|\sin\omega t|}{1-\alpha|\sin\omega t|}\right]^2}. \quad (35)$$

According to (34), (35), and the specifications of the converter to be given in Section VI, the critical boost inductance over the input voltage range for CDC and VDC is depicted in Fig. 10, where the critical inductance $L_{b1} = 92\ \mu$H and $L_{b2} = 365\ \mu$H.

The RMS value of the inductor current in a line cycle is

$$I_{Lb\_\mathrm{rms}} = \frac{V_m T_s}{L_b}\sqrt{\frac{1}{\pi}\int_0^{\pi}\frac{V_o D_y^3(\sin\omega t)^2}{3\,(V_o - V_m\,|\sin\omega t|)}d\,\omega t}. \quad (36)$$

Substituting (4) with $L_{b1} = 92\ \mu$H and (32) with $L_{b2} = 365\ \mu$H into (36), I_{Lb1_rms} and I_{Lb2_rms} can be obtained, and plotted in Fig. 11. As seen, I_{Lb2_rms} is lower than I_{Lb1_rms},

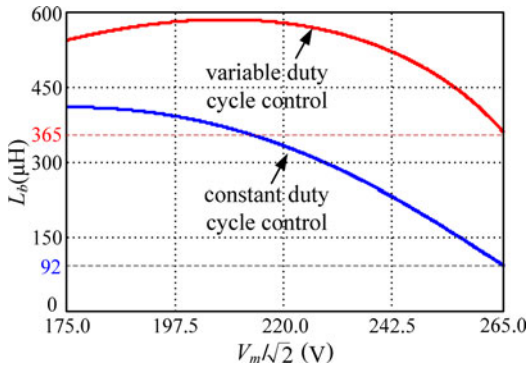

Fig. 10. Critical inductors over the input voltage range.

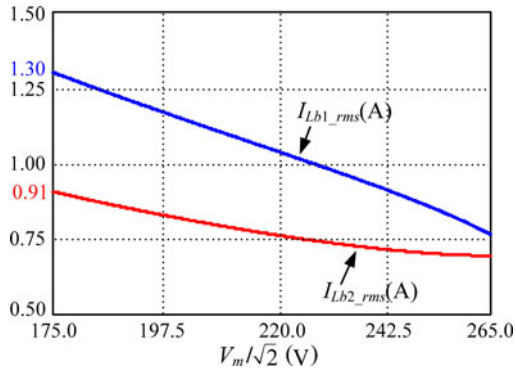

Fig. 11. RMS value of the inductor current for both CDC and VDC control schemes.

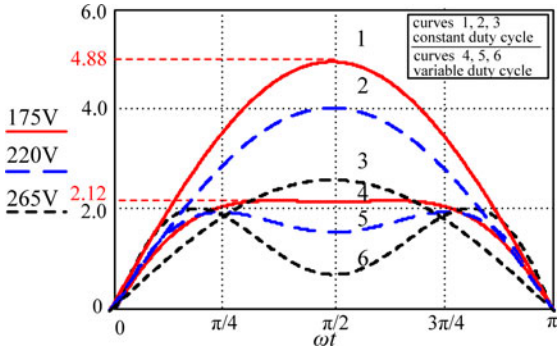

Fig. 12. Peak values of the inductor current for both CDC and VDC control schemes.

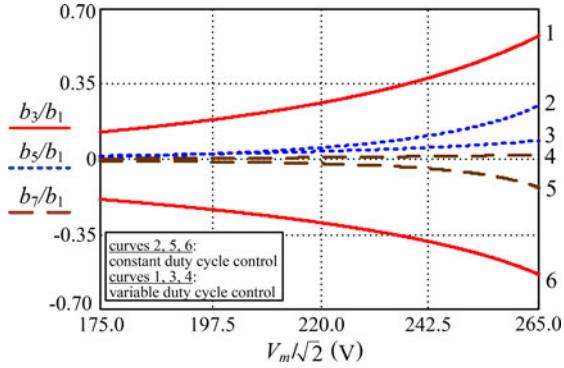

Fig. 13. Normalized amplitudes of the third, fifth, and seventh harmonics.

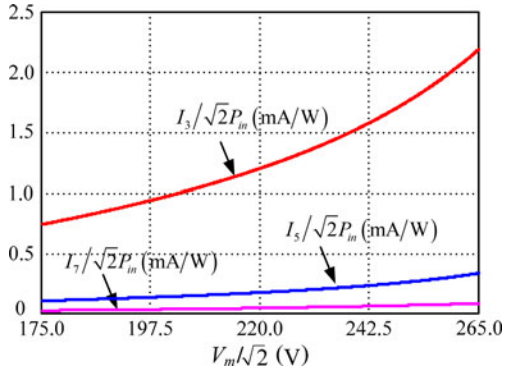

Fig. 14. Per watt contents of the third, fifth, and seventh harmonics.

particularly at a low input voltage. The reduction of the RMS current is due to the increment of the inductance and the resulting reduction of the current ripple. Thus, the conduction loss of the power components can be reduced, leading to a higher efficiency.

Substituting (4) with $L_{b1} = 92\ \mu$H and (32) with $L_{b2} = 365\ \mu$H into (2), the peak values of the inductor current for both CDC and VDC control schemes can be obtained and plotted in Fig. 12. As seen, a relatively smaller peak value for VDC leads to a great reduction of the current stress for power components.

The turns number N_b, the section area of the winding S, the filling factor K_u, and air-gap δ of the inductor are, respectively, as

$$N_b = \frac{L_b I_{Lb\_\mathrm{pk}\_\max}}{\Delta B A_e} \tag{37}$$

$$S = \frac{I_{Lb\_\mathrm{rms}\_\max}}{J} \tag{38}$$

$$K_\mu = \frac{N_b S}{A_w} \tag{39}$$

$$\delta = \frac{\mu_0 N_b^2 A_e}{L_b} \tag{40}$$

where $I_{Lb\_\mathrm{pk}\_\max}$ and $I_{Lb\_\mathrm{rms}\_\max}$ are the maximum peak and RMS value of the inductor current, respectively. ΔB is the flux density, A_e and A_w are, respectively, the effective area and window area of the magnetic core, J is current density, and μ_0 is the permeability.

Substituting (37)–(38) into (39), K_u can be rewritten as

$$K_\mu = \frac{L_b I_{Lb\_\mathrm{pk}\_\max} I_{Lb\_\mathrm{rms}\_\max}}{\Delta B A_w A_e J}. \tag{41}$$

Substituting (37) into (40), δ is

$$\delta = \frac{\mu_0 L_b I_{Lb\_\mathrm{pk}\_\max}^2}{\Delta B^2 A_e}. \tag{42}$$

Substituting $L_{b1} = 92\ \mu H$, $I_{Lb\_\mathrm{pk}\_\max} = 5.23\ A$, $I_{Lb\_\mathrm{rms}\_\max} = 1.3\ A$, $L_{b2} = 365\ \mu H$, $I_{Lb\_\mathrm{pk}\_\max} = 2.12\ A$, and $I_{Lb\_\mathrm{rms}\_\max} = 0.91\ A$ into (41) and (42), K_u and δ for both CDC and VDC control schemes can be calculated, respectively. The results show that K_u and δ for VDC are nearly the same as that for CDC, which means that the inductors can remain basically the same despite the fact that substantial increment in the inductance, the peak, and RMS values of the inductor current is reduced to a great extent.

B. PF and the Input Current Harmonics

Substituting (31) into (29), the input current with VDC is expressed as

$$i_{\mathrm{in}} = \frac{\pi P_o \sin\omega t \left[1 - (1.13\alpha - 0.149)\left|\sin\omega t\right|\right]^2}{V_m \left(1 - \alpha\left|\sin\omega t\right|\right) \int_0^\pi \frac{\sin^2\omega t[1-(1.13\alpha-0.149)|\sin\omega t|]^2}{1-\alpha|\sin\omega t|} d\,\omega t}. \tag{43}$$

Substituting (43) into (7), the amplitudes of the fundamental component and the third, fifth, and seventh harmonics can be calculated. Figs. 13 and 14 show the ratio of the harmonic amplitudes to the fundamental component and the ratio of the RMS values of the input harmonic currents to the input power, respectively.

In Fig. 13, for VDC the amplitude of the third harmonic is basically the same as that of CDC while the initial phase is different and the amplitudes of the fifth and seventh harmonics are reduced.

According to IEC 61000-3-2 Class D, per watt contents of the third, fifth, and seventh harmonics should be less than 3.4, 1.9, and 1.0 mA/W respectively. As seen from Fig. 14, the harmonics for VDC meet the standard requirements.

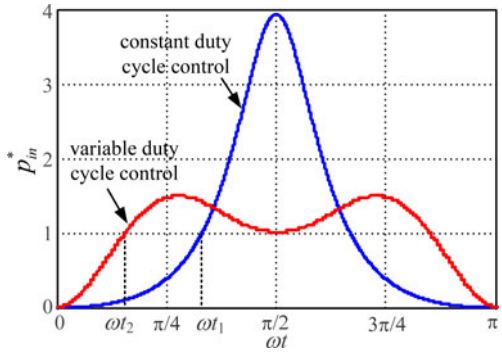

Fig. 15. Normalized instantaneous input power in a half-line cycle for both CDC and VDC control schemes.

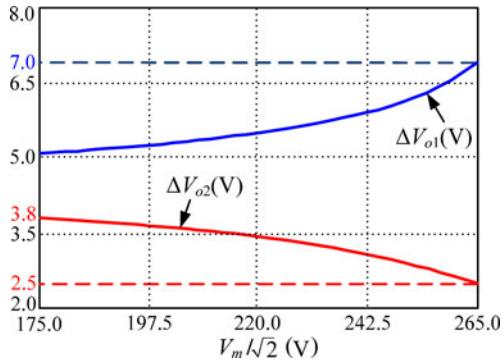

Fig. 16. Output voltage ripple for CDC and VDC.

C. Reduction of the Output Voltage Ripple

For a CDC operation of the DCM boost PFC converter, from (1), (3), and (4), the normalized instantaneous input power is derived as

$$p^*_{\text{in}\_1} = \frac{v_{\text{in}} i_{\text{in}}}{P_o} = \frac{\frac{\sin^2 \omega t}{1-\alpha|\sin \omega t|}}{\frac{1}{\pi}\int_0^{\pi} \frac{\sin^2 \omega t}{1-\alpha|\sin \omega t|} d\,\omega t}. \tag{44}$$

From (1) and (43), the normalized instantaneous input power is derived as

$$p^*_{\text{in}\_2} = \frac{v_{\text{in}} i_{\text{in}}}{P_o} = \frac{\frac{(\sin \omega t)^2}{1-\alpha|\sin \omega t|}\left[1-(1.13\alpha-0.149)\,|\sin \omega t|\right]^2}{\frac{1}{\pi}\int_0^{\pi} \frac{(\sin \omega t)^2[1-(1.13\alpha-0.149)|\sin \omega t|]^2}{1-\alpha \sin \omega t} d\,\omega t}. \tag{45}$$

According to the range of α from 0.62 to 0.94 in Section IV, take $\alpha = 0.94$, for example, then from (44) and (45), the normalized instantaneous input power in a half-line cycle for both CDC and VDC control schemes are plotted in Fig. 15.

From Fig. 15, when $p^*_{\text{in}} > 1$, the storage capacitor C_o is charged, and when $p^*_{\text{in}} < 1$, C_o is discharged. The normalized energy discharging C_o, which equals the charged energy, in a half-line cycle for both CDC and VDC are

$$\Delta E^*_1 = 2\int_0^{t_1} \left[1 - p^*_{\text{in}\_1}\right] dt/\left(T_{\text{line}}/2\right) \tag{46}$$

$$\Delta E^*_2 = 2\int_0^{t_2} \left[1 - p^*_{\text{in}\_2}\right] dt/\left(T_{\text{line}}/2\right) \tag{47}$$

respectively, where t_1 and t_2 are the time instants when p^*_{in} crosses 1 for CDC and VDC, respectively.

ΔE^*_1 and ΔE^*_2 can be also expressed as follows:

$$\Delta E^*_1 \approx \frac{\frac{1}{2}C_o\left(V_o + \frac{\Delta V_{o1}}{2}\right)^2 - \frac{1}{2}C_o\left(V_o - \frac{\Delta V_{o1}}{2}\right)^2}{P_o T_{\text{line}}/2} = \frac{2C_o V_o \Delta V_{o1}}{P_o T_{\text{line}}} \tag{48}$$

$$\Delta E^*_2 \approx \frac{\frac{1}{2}C_o\left(V_o + \frac{\Delta V_{o2}}{2}\right)^2 - \frac{1}{2}C_o\left(V_o - \frac{\Delta V_{o2}}{2}\right)^2}{P_o T_{\text{line}}/2} = \frac{2C_o V_o \Delta V_{o2}}{P_o T_{\text{line}}} \tag{49}$$

TABLE II
SPECIFICATIONS OF THE PROTOTYPE

Input voltage	Output voltage	Output power	Switching frequency
$v_{\text{in}} = 175 \sim 265$ VAC/50 Hz	$V_o = 400$ VDC	$P_o = 120$ W	$f_s = 100$ kHz

where ΔV_{o1} and ΔV_{o2} are the output voltage ripple for both CDC and VDC, respectively.

From (46) to (49), ΔV_{o1} and ΔV_{o2} are derived as

$$\Delta V_{o1} = 2P_o \int_0^{t_1} \left[1 - p^*_{in\_1}\right] dt/C_o V_o \tag{50}$$

$$\Delta V_{o2} = 2P_o \int_0^{t_2} \left[1 - p^*_{in\_2}\right] dt/C_o V_o. \tag{51}$$

According to (44), (45), (50), (51), and the specifications of the converter to be given in Section VI, the curves of the output voltage ripple can be plotted in Fig. 16. As seen, over the whole range of the input voltage, the output voltage ripple increases from 5.0 to 7.0 V for CDC while it decreases from 3.8 to 2.5 V for VDC with the maximum ripple for VDC being 54.3% of that for CDC, which means that if the maximum output voltage ripple remains the same, the storage capacitor will be reduced to 54.3%.

VI. Experimental Verification

To verify the proposed control scheme, a prototype has been built and tested in the lab. The specifications of the prototype are shown in Tables II and III.

Figs. 17 and 18 show the full-load experimental waveforms of the input voltage, input current, boost inductor current, and output voltage for CDC and VDC at 175, 220, and 265 VAC input, respectively. It can be seen that, in the input current, there are some distortions arising from the DCM operation and it mainly contains the third harmonic which has a phase difference of π and 0 with respect to the fundamental component, for CDC and VDC, respectively, especially at a high input voltage.

Figs. 19–21 show the full-load experimental curves of the measured efficiency, PF, and output voltage ripple.

From Fig. 19, compared with CDC, VDC has an increased efficiency which is more obviously improved at a low input voltage. The reason is that in Figs. 12, 17, and 18, at a low input

TABLE III
POWER DEVICES AND COMPONENTS OF THE PROTOTYPE

Input rectifier bridge *RB* GBU406 (600 V, 4 A)	Power switch Q_b FCI11N60 (600 V, 11 A)	Boost diode D_b STTH8L06D (600 V, 8 A)	Control IC UC3525A
Boost inductor 80 μH (CDC), 350 μH (VDC)	Input filter inductor $L_{\rm in} = 230\ \mu$H	Input filter capacitor $C_{\rm in} = 0.22\ \mu$F	Output filter capacitor $C_o = 220\ \mu$F

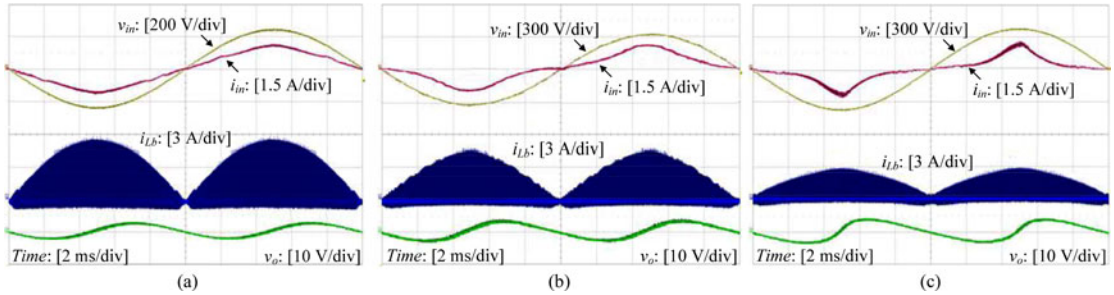

Fig. 17. Experimental waveforms of input voltage, input current, inductor current, and output voltage for CDC at 100% load. (a) 175 V, (b) 220 V, and (c) 265 V.

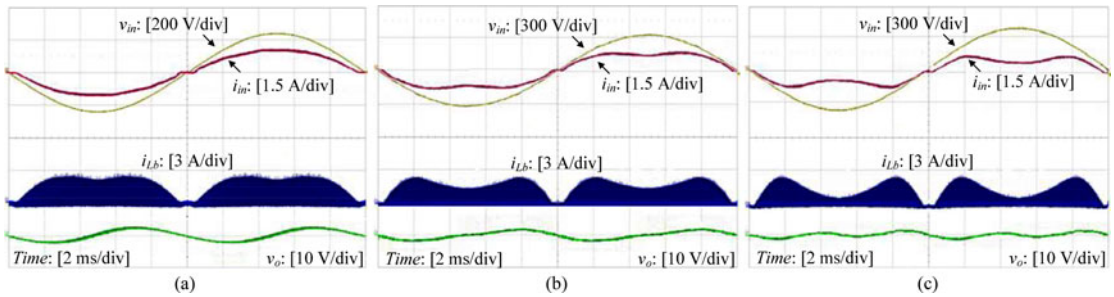

Fig. 18. Experimental waveforms of input voltage, input current, inductor current, and output voltage for VDC at 100% load. (a) 175 V, (b) 220 V, and (c) 265 V.

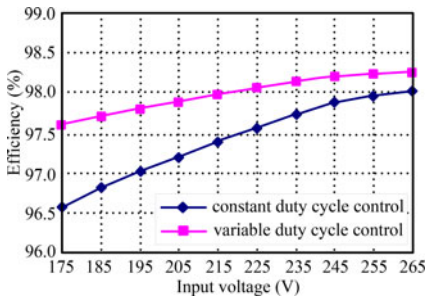

Fig. 19. Measured efficiency.

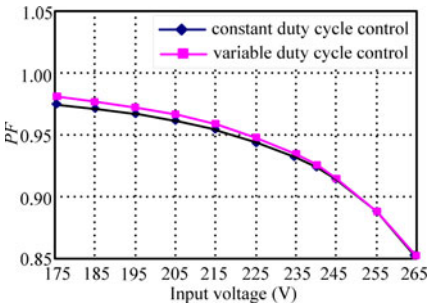

Fig. 20. Measured PF.

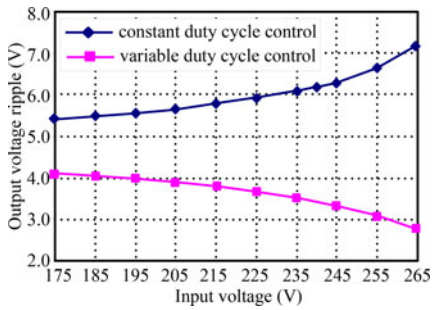

Fig. 21. Measured output voltage ripple.

voltage, the peak value of the switch current, i.e., the peak value of the inductor current, is greatly reduced at any line angle in a half-line cycle of [0, π], while, at a high input voltage, the value decreases at around $\pi/2$ and increases at around 0 and π, so the switching turn-off loss is reduced, especially at a low input voltage; meanwhile, the conduction loss of the power components is reduced as well, which has been analyzed in Section V-A.

From Fig. 20, the PF variation rule for VDC is basically the same as that of CDC. As analyzed in Sections IV and V, compared with CDC, the VDC control makes the phase difference

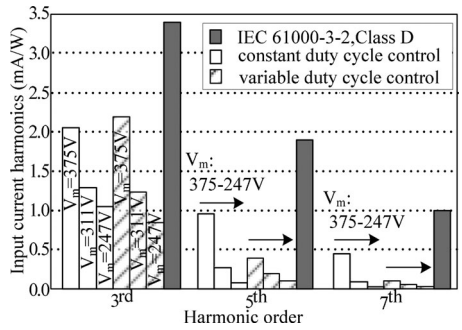

Fig. 22. Measured input current harmonics at 100% load.

between the third and first input current harmonics change from π to 0, with a nearly identical PF at a certain input voltage, as the curves of PF and $PF_{\_\mathrm{fit3}}$ show in Fig. 5.

From Figs. 17, 18, and 21, with the input voltage increasing, the output voltage ripple increases for CDC while it decreases for VDC and is greatly reduced compared with that of CDC, especially at a high input voltage, which agrees well with the analysis of Section V-C.

Figs. 22 shows the measured third, fifth, and seventh harmonics of the input current at 100% loads, of which for VDC, compared with that of CDC, the third harmonic is nearly the same, while the fifth and seventh harmonics decrease. The harmonics for both CDC and VDC control schemes meet the IEC 61000-3-2 Class D standard. The measurement is consistent with the theoretical analysis as shown in Figs. 13 and 14.

VII. Conclusion

A VDC control scheme is proposed in this paper so as to make the input current contain only the third harmonic that is in phase with the fundamental component. A method of fitting the duty cycle is further proposed. Compared with that of the constant duty cycle control:

1) the critical inductance is increased, which leads to a current ripple decrement and a higher efficiency;
2) PF remains the same at a certain input voltage;
3) the input current harmonics meet the IEC61000-3-2 Class D standard;
4) the output voltage ripple or the output storage capacitance can be greatly reduced.

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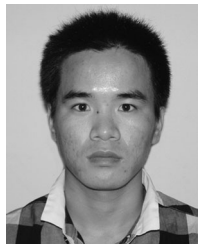

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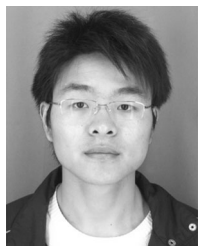

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