A Method to Improve the Dynamic Performance of Moving Average Filter-Based PLL

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***Abstract*—Phase-locked loop (PLL) technique is widely used for synchronization applications. A variety of moving average filter (MAF)-based PLLs have been presented in recently published literatures. MAF-based PLL can completely eliminate the effect of unbalanced voltage, characteristic harmonics, and dc offset. Unfortunately, the open-loop bandwidth is drastically reduced after incorporating MAF into the PLL structure. The problem is analyzed in detail in this paper, and it is proved to be caused by the large MAF window width which is determined by the lowest order harmonic. Then, an improved method named differential MAF-PLL (DMAF-PLL) is proposed. This method can rapidly eliminate the lowest order harmonic to narrow the MAF window width. DMAF-PLL is realized by incorporating a special proportional component into the MAF-based PLL. The special proportional component can online change its value according to the frequency of input signal, and it will not introduce phase lag, so as not to deteriorate the stability of PLL. DMAF-PLL increases the open-loop bandwidth and greatly improves the dynamic performance of MAF-based PLL, and it is easy to be implemented with low computational burden. DMAF-PLL can be used in both three-phase and single-phase voltage systems. Simulation and experimental results are included to validate the effectiveness and robustness of the proposed method.**

***Index Terms*—Bandwidth, dynamic response, grid synchronization, moving average filter, phase-locked loop (PLL).**

I. Introduction

SINCE distributed generation systems, flexible ac transmission systems, active power filter, and VSC-HVDC systems are all connected to the grid through power converters, one of the most important aspects of their control strategy is to synchronize the converters with the utility grid at the point of common coupling (PCC). For this reason, the fundamental positive sequence voltage information (e.g., phase angle and frequency) at the PCC must be obtained quickly and accurately [1]–[6].

PLL is the main technique used to obtain the voltage information. In the past few years, various kinds of PLLs have been proposed. The most widely used one is the synchronous rotating frame PLL (SRF-PLL). SRF-PLL is extremely simple and can be used in single-phase [7]–[9] and three-phase [10]–[12] systems. Under ideal grid conditions without any harmonic, unbalance, or dc offset, SRF-PLL can achieve a fast and precise detection of the phase angle and frequency of the grid voltage. In case the grid voltage is only distorted with high-order harmonics, the SRF-PLL can still work properly by narrowing the loop bandwidth to attenuate the effect of high-order harmonics at the cost of reducing the PLL response speed. However, the performance of SRF-PLL becomes unacceptable when the utility voltage is unbalanced [13], [14]. In order to solve this problem, lots of improved versions of SRF-PLL have been presented in literatures. In [15], double second-order generalized integrator-based PLL (DSOGI-PLL) was presented.

This method is realized by using a DSOGI structure operating in the $\alpha\beta$-frame to obtain the fundamental positive sequence component from the unbalanced voltage. An alternative method, adaptive notch fi (ANF)-based PLL (ANF-PLL) was presented in [16], which is similar to DSOGI-PLL except it adopts ANF rather than DSOGI to acquire the fundamental positive sequence component from the unbalanced voltage. An enhanced PLL (EPLL) was presented for the same purpose by Ghartemani *et al.* [17], [18]. EPLL can estimate the phase angle and amplitude of input signals at the same time and could reconstruct the targeted signals easily. EPLL possesses a perfect filtering capability but a relatively lower response speed compared to some other synchronization methods. In [19], a decoupled double synchronous reference-frame PLL (DDSRF-PLL) was presented. DDSRF-PLL uses double synchronous frame transformations and a decoupling network to detect the positive and negative sequence components. In [20], a multiple complex coefficient fi-based PLL (MCCF-PLL) was presented by Guo *et al.* Unlike traditional real-coefficient fi, the complex-coefficient fi can distinguish the positive and negative sequences for the same frequency. In [21] and [22], delayed signal cancellation (DSC) technique was introduced into the PLL and DSC-PLL was presented. In DSC-PLL, the input signals are delayed one quarter of the fundamental period to produce a 90° phase shift, and the delayed signals are added into the input ones to acquire the fundamental positive sequence component from the unbalanced voltage. ANF and lead compensators were used as loop filters in PLLs to eliminate the effect of the unbalanced voltage in [23] and [24], respectively.

Though the aforementioned PLLs can eliminate the effect of unbalanced voltage, most of them act as traditional low-pass filter or notch filter. In highly distorted case, the PLLs have to narrow the bandwidth to attenuate the harmonics, which seriously reduces their dynamic response speed. In order to eliminate the effect of the unbalanced voltage and low-order harmonics without reducing too much of the dynamic response speed, multiple reference frame-based PLL (MRF-PLL) was presented in [25]. The MRF-PLL utilizes two synchronous reference frames rotating at the same angular speed with opposite directions and

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a decoupling network to eliminate the effect of the unbalanced voltage. Under highly distorted grid conditions, the MRF decoupling network can be extended to include the low-order harmonics, which significantly improves its filtering capacity. In [26], multiple-SOGI-FLL (MSOGI-FLL) was presented for the same purpose. MSOGI is similar to SOGI except it adopts multiple SOGI structures tuned at the proper frequencies to eliminate the effect of low-order harmonics. Another approach is generalized DSC PLL (GDSC-PLL) [27]. GDSC structure can be regarded as an improved version of DSC structure because it contains several DSC structures in cascaded manner in the $\alpha\beta$-frame to eliminate different low-order harmonics. Although MRF-PLL, MSOGI-FLL, and GDSC-PLL have been presented and show great filtering capacity, they cannot be easily implemented in the digital controller due to their complexity. In addition, these PLLs still cannot acquire fast dynamic response since the open-loop bandwidth of PLLs must be sufficiently smaller than $2\omega_n$ (ω_n is the fundamental angular frequency) to ensure the system stability [28], [29].

Since MAF is a kind of linear phase finite impulse response filter which can act as an ideal low-pass filter under certain conditions, MAF-based PLL can completely eliminate the effect of unbalanced voltage, characteristic harmonics, and dc offset. Several kinds of MAF-based PLLs have been proposed in recent literatures. In [30] and [31], MAF was incorporated into SRF-PLL, and a new PLL called MA-PLL was presented. MA-PLL greatly enhances the filtering capability of traditional SRF-PLL at the cost of reducing its dynamic response speed. In [32], MAFs were introduced into MRF-PLL to replace the first-order low pass filters, which improved its filtering capability. MAF-PLL was presented in [33] and [34]. The basic structure of MAF-PLL is the same as MA-PLL except its MAF is frequency adaptive (the MAF uses PLL to estimate the online frequency of grid and change its window width accordingly). In [35], a variable sampling period fi PLL (VSPF-PLL) was presented, which is also a kind of MAF-based PLLs. Several other MAF-based PLLs can be found in [36]–[40]. In addition to great filtering capacity, MAF-based PLL has other advantages, such as simple digital realization and low computational burden [42]. Though MAF-based PLL has so many advantages, the open-loop bandwidth is drastically reduced after incorporating MAF into the PLL structure because of the influence of MAF window width, thus seriously degrading the dynamic performance of PLL.

The problem that the dynamic performance of PLL is greatly influenced by the MAF is analyzed in detail in this paper, and it is proved to be caused by the large MAF window width which is determined by the lowest order harmonic. Then, a method which can fast eliminate the lowest order harmonic to narrow the MAF window width is proposed. The method is named as DMAF-PLL in this paper, and it is realized by incorporating a special proportional component (defined as "PF" in this paper) into the conventional MAF-based PLL, and the value of PF can change with the frequency of input signal. The PF will not introduce phase lag, so as not to deteriorate the stability of MAF-based PLL. DMAF-PLL increases the open-loop bandwidth and greatly improves the dynamic performance of MAF-based PLL, and it is easy to be implemented with low computational burden. Simulation and experimental results are presented to validate the effectiveness and robustness of proposed method. This paper is organized as follows. Section II presents a detailed analysis of MAF-PLL (the proposed method can be applied to all the MAF-based PLLs, such as MAF-PLL, MA-PLL, and VSPF-PLL and this paper uses MAF-PLL [33], [34] to illustrate) and presents the influence of MAF window width. Section III introduces DMAF-PLL in detail. The simulation of MAF-PLL and DMAF-PLL is carried out to make a comparison in Section IV. In Section V, MAF-PLL and DMAF-PLL are implemented in hardware platform, and the experimental results are presented. Finally, Section VI concludes this paper.

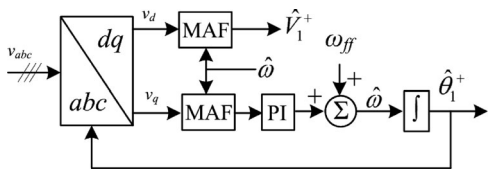

Fig. 1. Block diagram of three-phase MAF-PLL.

II. Overview of MAF-PLL

This section gives a detailed description of three-phase MAF-PLL in the continuous domain and then derives its small-signal model to obtain the amplitude-frequency and phase-frequency response characteristics. In addition, the influence of MAF window width is also analyzed and explained. Fig. 1 shows the block diagram of three-phase MAF-PLL.

A. Description of Moving Average Filter

MAF is a kind of linear phase finite impulse response filter [42]. With the input signal $x(t)$ and the output signal $y(t)$, MAF can be expressed in continuous-time domain as

$$y(t) = \frac{1}{T_w}\int_{t-T_w}^{t} x(\tau)d\tau \tag{1}$$

where T_w represents the window width. From (1), the MAF transfer function can be described in Laplace domain by

$$\mathrm{MAF}(s) = \frac{y(s)}{x(s)} = \frac{1-e^{-T_w s}}{T_w s}. \tag{2}$$

It can be seen from (2) that the MAF needs a time equal to its window width to reach steady-state condition [42]. Hence, a wider window width will result in a slower MAF transient response, and it will also result in a smaller MAF-PLL open-loop bandwidth which will be explained in later section.

Substituting $s = j\omega$ into (2) and the magnitude and phase expressions of MAF can be obtained as

$$\mathrm{MAF}(j\omega) = \left|\frac{\sin(\omega T_w/2)}{\omega T_w/2}\right| \angle -\omega T_w/2 \tag{3}$$

It can be observed from (3) that MAF can pass the dc component and completely block the ac components with frequencies

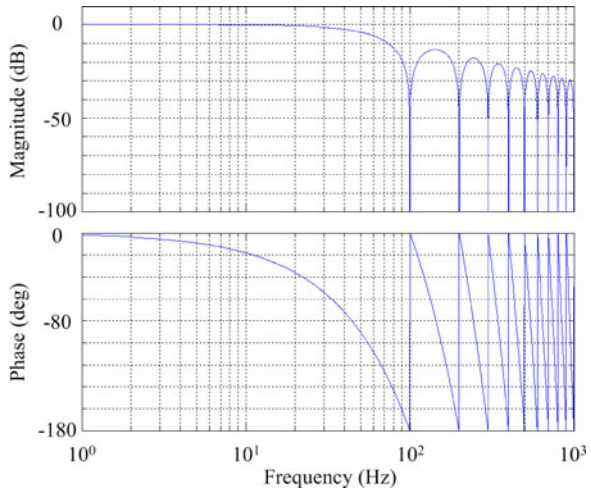

Fig. 2. Bode plot of MAF for $T_w = 0.01$ s.

of integer multiples of $1/T_w$ in hertz. This characteristic can be visualized through its Bode plot shown in Fig. 2.

As shown in Fig. 2, MAF can block the ac components at a frequency of integer multiples of 100 Hz when $T_w = 0.01$ s. It means that a MAF can block all the characteristic harmonics if T_w is properly chosen. Unfortunately, MAF has a 180° phase lag at frequencies it can completely block and it first appears at the frequency of $1/T_w$ Hz. Hence, the cutoff frequency of the MAF-PLL must be sufficiently smaller than $1/T_w$ Hz to achieve a robust performance. That is, the open-loop bandwidth is determined by T_w, and the smaller the T_w, the faster the dynamic response.

B. Small-Signal Modeling of MAF-PLL

In order to easily derive the small-signal model of MAF-PLL, it is assumed T_w is a constant, and the three-phase input voltages contain fundamental positive, negative sequence components, dc offset, and the dominant nontriplen odd harmonics (e.g., -5th, $+7$th, -11th, $+13$th, etc.) [29]. Thus, the input voltage can be expressed as

$$v_i = V_1^+ \cos\left(\theta_1^+ - k_i\frac{2\pi}{3}\right) + V_1^- \cos\left(\theta_1^- - k_i\frac{2\pi}{3}\right) + \sum_{h=-5,7\cdots} V_h \cos\left(\theta_h - k_i\frac{2\pi}{3}\right) + V_{di} \quad (4)$$

where $i = a, b, c$, and the corresponding $k_i = 0, 1, 2$. V_1^+ and θ_1^+ are the magnitude and phase angle of fundamental positive sequence component, respectively. V_1^- and θ_1^- are the magnitude and phase angle of fundamental negative sequence component, respectively. V_h and θ_h are the magnitude and phase angle of hth harmonic, respectively. V_{di} is the dc offset added into the input voltage. Applying the Clark (*abc*-to-$\alpha\beta$) and the Park

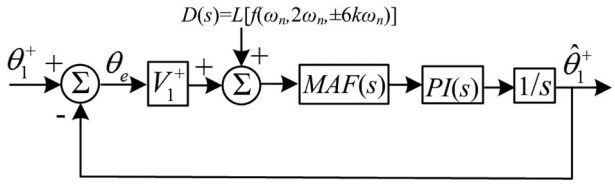

Fig. 3. Small-signal model of three-phase MAF-PLL.

($\alpha\beta$-to-*dq*) transformation one after another, yields

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = T_{\alpha\beta}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = T_{dq}\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} \cos\hat{\theta}_1^+ & \sin\hat{\theta}_1^+ \\ -\sin\hat{\theta}_1^+ & \cos\hat{\theta}_1^+ \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \quad (5)$$

then

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = V_1^+\begin{bmatrix} \cos(\theta_1^+ - \hat{\theta}_1^+) \\ \sin(\theta_1^+ - \hat{\theta}_1^+) \end{bmatrix} + V_1^-\begin{bmatrix} \cos(\theta_1^- - \hat{\theta}_1^+) \\ \sin(\theta_1^- - \hat{\theta}_1^+) \end{bmatrix} + A\begin{bmatrix} \sin(\hat{\theta}_1^+ + \varphi_d) \\ -\cos(\hat{\theta}_1^+ + \varphi_d) \end{bmatrix} + \sum_{h=-5,7\cdots} V_h\begin{bmatrix} \cos(\theta_h - \hat{\theta}_1^+) \\ \sin(\theta_h - \hat{\theta}_1^+) \end{bmatrix} \quad (6)$$

where $A = \sqrt{v_{d\alpha}^2 + v_{d\beta}^2}$, $v_{da} = (2v_{da} - v_{db} - v_{dc})/3$, $v_{d\beta} = \sqrt{3}(v_{db} - v_{dc})/3$ and$\varphi_d = \tan^{-1}(v_{d\alpha}/v_{d\beta})$.

Under a quasi-locked condition ($\omega_n = \hat{\omega}$,$\theta_1^+ \approx \hat{\theta}_1^+$), v_q can be expressed as

$$v_q \approx V_1^+(\theta_1^+ - \hat{\theta}_1^+) + f(\omega_n, -2\omega_n, \pm 6k\omega_n) \quad (7)$$

where ω_n is the fundamental angular frequency and $k = 1, 2, 3\ldots$. As it can be seen from (7), after the Clark and Park transformations, the fundamental positive component turns into the dc component, the fundamental negative sequence component turns into the negative sequence second harmonic, the dc offset turns into the ripple of fundamental frequency, and the hth harmonic turns into $(h-1)$th harmonic in *dq* frame. Fig. 3 shows the small-signal model of three-phase MAF-PLL obtained from (7) and Fig. 1.

C. Selection of the MAF Window Width

Selection of T_w is the most important issue to be considered in designing a MAF because T_w can determine the dynamic response speed and filtering capability of MAF-PLL. Fortunately, the principle of choosing T_w is very simple because it is determined by the lowest order harmonic to be eliminated (actually T_w is variable for frequency adaptive MAF, but here it is assumed to be a constant for clear illustration). For example, T_w is often set to 0.01 s in a 50-Hz grid system to eliminate the negative sequence second harmonic caused by fundamental negative sequence voltage when ignoring the dc offset, while it is recommended that T_w is set to 0.02 s when considering the

dc offset as the dc offset can result in the ripple of fundamental frequency.

D. PI Parameters Design

In this section, the symmetrical optimum method, which is a standard design procedure used in [42] and [43], is applied to design the PI parameters. In order to use the method, MAF has to be replaced by its first-order Padé approximation, that is, the delay term in (2) is approximated by

$$e^{-T_w s} \approx \frac{1 - T_w s/2}{1 + T_w s/2}. \tag{8}$$

Substituting (8) into (2), yields

$$\mathrm{MAF}(s) \approx \frac{1}{1 + T_w s/2}. \tag{9}$$

As it can be seen from Fig. 3, the open-loop transfer function of MAF-PLL can be described by

$$G_{ol}(s) = \frac{\hat{\theta}_1^+}{\theta_e}\bigg|_{D(s)=0} = V_1^+ \mathrm{MAF}(s)\mathrm{PI}(s)\frac{1}{s}. \tag{10}$$

The transfer function of PI(s) is

$$\mathrm{PI}(s) = k_p + k_i/s \tag{11}$$

where k_p and k_i are the proportional and integral gains, respectively. Substituting (9) and (11) into (10), yields

$$G_{ol}(s) \approx V_1^+ \frac{(2/T_w)(k_p s + k_i)}{s^2[s + (2/T_w)]}. \tag{12}$$

According to the symmetrical optimum method, the PLLs can achieve optimum performance when

$$2/T_w = b\omega_c \tag{13a}$$

$$k_p = \omega_c/V_1^+ \tag{13b}$$

$$k_i = \omega_c^2/bV_1^+ \tag{13c}$$

where ω_c is the cutoff frequency and b is a constant determined by both transient response speed and stability margin. According to [42] and [43], b is set to 2.4 to acquire a fast transient response and a sufficient phase margin. With this selection and considering $T_w = 0.01$ s when ignoring the dc offset, the control parameters can be calculated as

$$\begin{aligned} \omega_c &= 83.33 \approx 2\pi \times 13.3 \\ k_p &= 83.33 \\ k_i &= 2893.52. \end{aligned} \tag{14}$$

When considering the dc offset, $T_w = 0.02$ s is recommended, and the control parameters can be calculated as

$$\begin{aligned} \omega_c &= 41.67 \approx 2\pi \times 6.63 \\ k_p &= 41.67 \\ k_i &= 723.38. \end{aligned} \tag{15}$$

All the parameters calculated above are in a 50-Hz grid system and $V_1^+ = 1$ p.u.

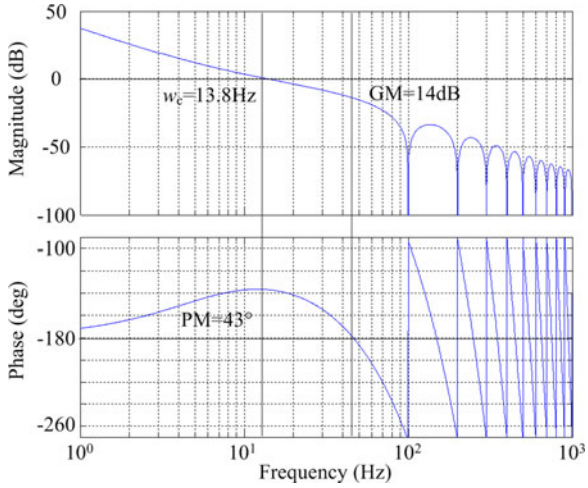

Fig. 4. Open-loop bode plot of MAF-PLL when using the parameters of (14) and $T_w = 0.01$ s.

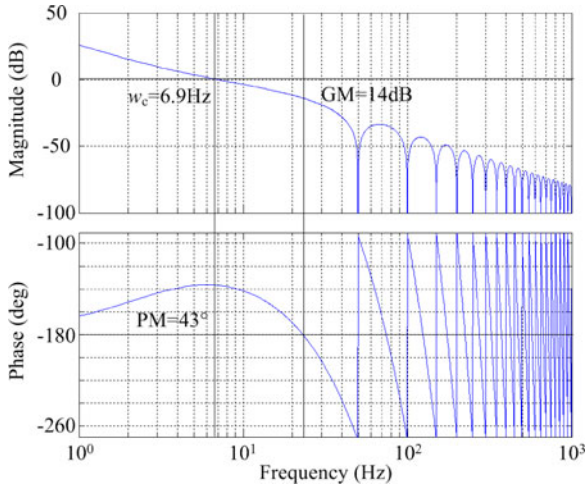

Fig. 5. Open-loop bode plot of MAF-PLL when using the parameters of (15) and $T_w = 0.02$ s.

Figs. 4 and 5 show the Bode plots of MAF-PLL. The cutoff frequency of PLL is about 13.8 Hz when ignoring the dc offset, and it is about 6.9 Hz when considering the dc offset. The stability margins are basically identical in both cases. Fast transient response cannot be obtained because of the low cutoff frequency determined by the lowest order harmonic.

III. Proposed DMAF-PLL Method

DMAF-PLL is proposed and analyzed in this section. The impact of amplitude variations, frequency variations, and differentiation on DMAF-PLL is analyzed. Its low computational burden and fast dynamic response are also presented.

A. DMAF-PLL Introduction

The block diagram of DMAF-PLL is shown in Fig. 6. The "PF" in Fig. 6 represents the decoupling transfer function, and it is proved to be a variable proportional component later.

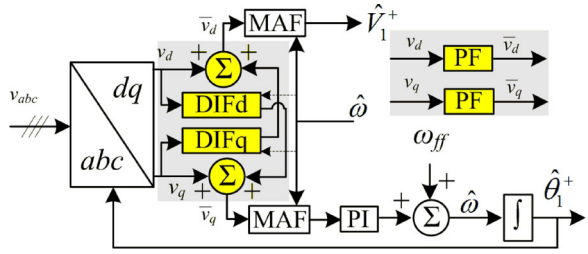

Fig. 6. Block diagram of DMAF-PLL.

In Fig. 6, when ignoring the dc components DIFq (or DIFd) realizes the function of taking the derivative of input signal and then divides $2\omega_n$ (or $-2\omega_n$). The transfer functions of DIFd(s) and DIFq(s) can be written as

$$\mathrm{DIFd}(s) = -s/(2\omega_n) \tag{16a}$$

$$\mathrm{DIFq}(s) = s/(2\omega_n). \tag{16b}$$

According to Fig. 6, the decoupling transfer function PF(s) can be written as

$$\begin{aligned}\mathrm{PF}(s) &= \bar{v}_q/v_q = (v_q + v_d\mathrm{DIFd})/v_q = 1 + v_d\mathrm{DIFd}/v_q \\ &= \bar{v}_d/v_d = (v_d + v_q\mathrm{DIFq})/v_d = 1 + v_q\mathrm{DIFq}/v_d. \end{aligned} \tag{17}$$

Since v_q has a 90° phase lag compared with v_d, it can be obtained that $v_d/v_q = \mathrm{j}$. Therefore, (17) can be written as

$$\mathrm{PF}(s) = 1 + j \times (-j\omega)/(2\omega_n) = 1 + \omega/(2\omega_n) \tag{18}$$

where ω is the angular frequency of input signal and ω_n is the fundamental angular frequency. It can be observed that the PF is actually a proportional component, the value of which changes with the frequency of input signal. The PF can eliminate the negative sequence second harmonic because its value is zero when the angular frequency of input signal is $-2\omega_n$.

Under a quasi-locked condition ($\omega_n = \hat{\omega}$,$\theta_1^+ \approx \hat{\theta}_1^+$), (6) can be approximated by

$$\begin{aligned}\begin{bmatrix} v_d \\ v_q \end{bmatrix} &\approx V_1^+ \begin{bmatrix} 1 \\ 0 \end{bmatrix} + A \begin{bmatrix} \sin(\omega_n t + \varphi_0) \\ -\cos(\omega_n t + \varphi_0) \end{bmatrix} \\ &+ V_1^- \begin{bmatrix} \cos(-2\omega_n t + \varphi_1) \\ \sin(-2\omega_n t + \varphi_1) \end{bmatrix} + \sum_{h=-5,7\ldots} V_h \begin{bmatrix} \cos[(h-1)\omega_n t + \varphi_h] \\ \sin[(h-1)\omega_n t + \varphi_h] \end{bmatrix} \end{aligned} \tag{19}$$

where $\varphi_0 = \varphi_1^+ + \varphi_d$, $\varphi_1 = \varphi_1^- - \varphi_1^+$, $\varphi_h = \varphi_h^\pm - \varphi_1^+$, and φ_1^+, φ_1^- and $\varphi_h^\pm$ are the initial phase angles of fundamental positive component, fundamental negative sequence component, and hth harmonic, respectively. The derivatives of v_d and v_q can be described by

$$\begin{aligned}\begin{bmatrix} v_d' \\ v_d' \end{bmatrix} &= A\omega_n \begin{bmatrix} \cos(\omega_n t + \varphi_0) \\ \sin(\omega_n t + \varphi_0) \end{bmatrix} - 2V_1^-\omega_n \begin{bmatrix} -\sin(-2\omega_n t + \varphi_1) \\ \cos(-2\omega_n t + \varphi_1) \end{bmatrix} \\ &+ \sum_{h=-5,7\ldots} (h-1)V_h\omega_n \begin{bmatrix} -\sin[(h-1)\omega_n \mathrm{t} + \varphi_h] \\ \cos[(h-1)\omega_n \mathrm{t} + \varphi_h] \end{bmatrix}. \end{aligned} \tag{20}$$

When ignoring the dc components, the signals passing through the PF can be expressed as

$$\begin{aligned}\begin{bmatrix} \bar{v}_d \\ \bar{v}_q \end{bmatrix} &= \begin{bmatrix} v_d + v_q\mathrm{DIFq}(t) \\ v_q + v_d\mathrm{DIFd}(t) \end{bmatrix} = \begin{bmatrix} v_d + \dfrac{v_q'}{2\omega_n} \\ v_q - \dfrac{v_d'}{2\omega_n} \end{bmatrix} \\ &= V_1^+ \begin{bmatrix} 1 \\ 0 \end{bmatrix} + \sum_{h=-5,7\ldots} \frac{(h+1)}{2} V_h \begin{bmatrix} \cos[(h-1)\omega_n t + \varphi_h] \\ \sin[(h-1)\omega_n t + \varphi_h] \end{bmatrix}. \end{aligned} \tag{21}$$

Now, the signals passing through the PF do not contain negative sequence second harmonic anymore, and the lowest order harmonic needed to be eliminated by the MAF is the sixth harmonic. Then, T_w can be reduced to 0.0033 s from 0.01 s in a 50-Hz system, which can greatly improve the dynamic response speed of MAF-based PLL.

When considering the dc components, DIFq (or DIFd) realizes the function of taking the derivative of input signal and then divides $-\omega_n$ (or ω_n). The transfer functions of DIFd(s) and DIFq(s) can be written as

$$\mathrm{DIFd}(s) = s/\omega_n \tag{22a}$$

$$\mathrm{DIFq}(s) = -s/\omega_n. \tag{22b}$$

Similar to (18), PF(s) can be written as

$$\mathrm{PF}(s) = 1 - \omega/\omega_n. \tag{23}$$

In case the dc components have to be considered, the PF in the proposed approach can fast eliminate the effect of dc components because PF is zero when the angular frequency of input signal is ω_n. When considering the dc components, the signals passing through the PF can be expressed as

$$\begin{aligned}\begin{bmatrix} \bar{v}_d \\ \bar{v}_q \end{bmatrix} &= \begin{bmatrix} v_d - \dfrac{v_q'}{\omega_n} \\ v_q + \dfrac{v_d'}{\omega_n} \end{bmatrix} = V_1^+ \begin{bmatrix} 1 \\ 0 \end{bmatrix} + 3V_1^- \begin{bmatrix} \cos(-2\omega_n t + \varphi_1) \\ \sin(-2\omega_n t + \varphi_1) \end{bmatrix} \\ &+ \sum_{h=-5,7\ldots} (2-h)V_h \begin{bmatrix} \cos[(h-1)\omega_n t + \varphi_h] \\ \sin[(h-1)\omega_n t + \varphi_h] \end{bmatrix}. \end{aligned} \tag{24}$$

In this case, although DMAF-PLL will not be affected by the dc components and T_w can be reduced to 0.01 s from 0.02 s in a 50-Hz system, it cannot keep the same dynamic performance as in the case of ignoring the dc components because the window width of MAF has to be set to 0.01 s to eliminate the negative sequence second harmonic.

B. DC Elimination Structure

In order to obtain a fast dynamic performance, the frequency-adaptive MAF is recommended as a special prefiltering structure in the stationary reference frame to filter out the dc components (constant and/or slowly varying dc components), and thus the PF in DMAF-PLL can be reserved for the second-order harmonic component. The block diagram of the DMAF-PLL used in case with dc components is shown in Fig. 7.

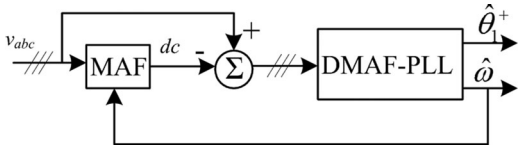

Fig. 7. Block diagram of the DMAF-PLL used in case with dc components.

In order to acquire and eliminate the dc components, the window width of MAF in the stationary reference frame is often set to $1/f_n$ (f_n is the fundamental frequency). As for the constant dc components, they can be accurately acquired by the MAF in the stationary reference frame and thus be removed completely. As for the slowly varying dc components, they cannot be accurately acquired by the MAF, but the effect of them can be reduced significantly. For instance, the dc component is increasing from t_0 with a speed of 1.0 p.u./s, and its equation can be written as

$$V_{\rm dc}(t) = t - t_0 (t \geq t_0). \tag{25}$$

The acquired dc component by the MAF is

$$V_{\rm dco}(t) = \frac{1}{T_w}\int_{t-T_w}^{t} V_{\rm dc}(\tau)d\tau = t - t_0 - T_w/2 \tag{26}$$

where T_w is often set to $1/f_n$. It can be observed from (25), (26), and Fig. 7 that the rest of dc component is $T_w/2$, and it is a constant. Assuming $f_n = 50$ Hz, the amplitude of the remaining dc component is 0.01 p.u., and it would have very little influence on DMAF-PLL.

In addition to use MAF to eliminate the dc components, another method which can fast eliminate dc components in the stationary reference frame is presented in [48]. This method can eliminate both the constant and the slowly varying dc components within 1 ms, and it can be used in three-phase and single-phase voltage systems. Since the method adopts differentiation, its performance is not very satisfactory in highly distorted grid environment.

When using the proposed DMAF-PLL in a 50-Hz grid system, the window width of MAF(s) used to eliminate the dc components (if they are exist) is set to 0.02 s, and the window width of MAF(s) used in the PLL loop is set to 0.0033 s because the negative sequence second harmonic has already been eliminated by the PF. According to (13), the new control parameters can be calculated as

$$\begin{aligned} \omega_c &= 250 \approx 2\pi \times 40 \\ k_p &= 250 \\ k_i &= 26041.68. \end{aligned} \tag{27}$$

The open-loop transfer function of DMAF-PLL can be expressed as

$$G_{ol}(s) = \frac{\hat{\theta}_1^+}{\theta_e}\bigg|_{D(s)=0} = V_1^+ {\rm PF}(s){\rm MAF}(s){\rm PI}(s)\frac{1}{s}. \tag{28}$$

The open-loop Bode plot of DMAF-PLL can be obtained from (27) and (28). In order to show that the PF can eliminate the negative sequence second harmonic, the abscissa axis of the Bode plot shown in Fig. 8 uses negative frequency.

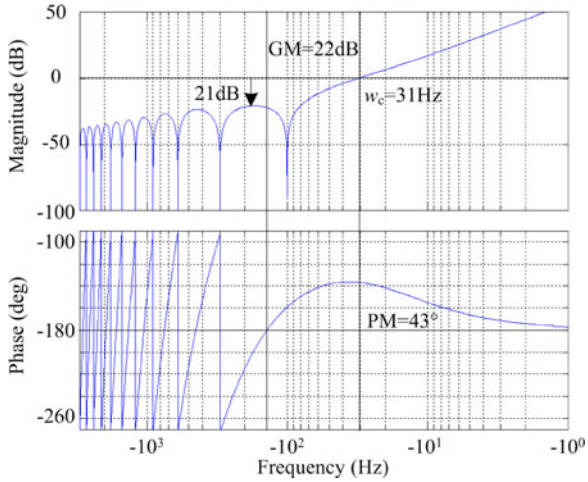

Fig. 8. Open-loop bode plot of DMAF-PLL when using the parameters of (27) and $T_w = 0.0033$ s.

As it can be seen from the Bode plot of DMAF-PLL, the cutoff frequency is 31 Hz, and the phase and magnitude margin are 43° and 22 dB, respectively. Compared with MAF-PLL, DMAF-PLL has a similar stability margin but a larger open-loop bandwidth, and thus a faster dynamic response.

C. Comparison Between DMAF-PLL and Some Multichannel Mode PLL Techniques

Since DMAF-PLL has excellent filtering capacity and can be used in highly distorted grid environment, some multichannel mode PLLs (MSOGI-FLL, MRF-PLL, MCCF-PLL . . .) which can also be used in highly distorted grid environment are adopted to make a comparison. DMAF-PLL has two great advantages, lower computational burden, and faster dynamic response, compared with these multichannel mode PLLs. Since multichannel mode PLLs have similar structures and small-signal models [29], MSOGI-FLL is adopted in this section to make a comparison with DMAF-PLL. Fig. 9 shows the structure of MSOGI-FLL presented in [26].

Assuming that there are n different characteristic harmonics need to be eliminated, $n+1$ DSOGI-QSNs and one PNSC are needed to accurately obtain the phase angle and frequency of fundamental positive sequence voltage. Since one DSOGI-QSC contains four integrators, six multipliers, and four subtractors, there are $4n+4$ integrators, $6n+6$ multipliers, and $4n+4$ subtractors in the MSOGI structure, which significantly increases the complexity and computational burden of the implementation.

Since the MAF is usually implemented in the discrete-time domain, a discrete-time definition is required. Assuming that the window width of MAF contains N samples (N is an integer which determines the MAF order) of its input signal, i.e., $T_w = NTs$ where Ts is the sampling time, the discrete-time description of MAF can be obtained as

$$\bar{x}(k) = \frac{1}{N}\sum_{i=0}^{N-1} x(k-i) \tag{29}$$

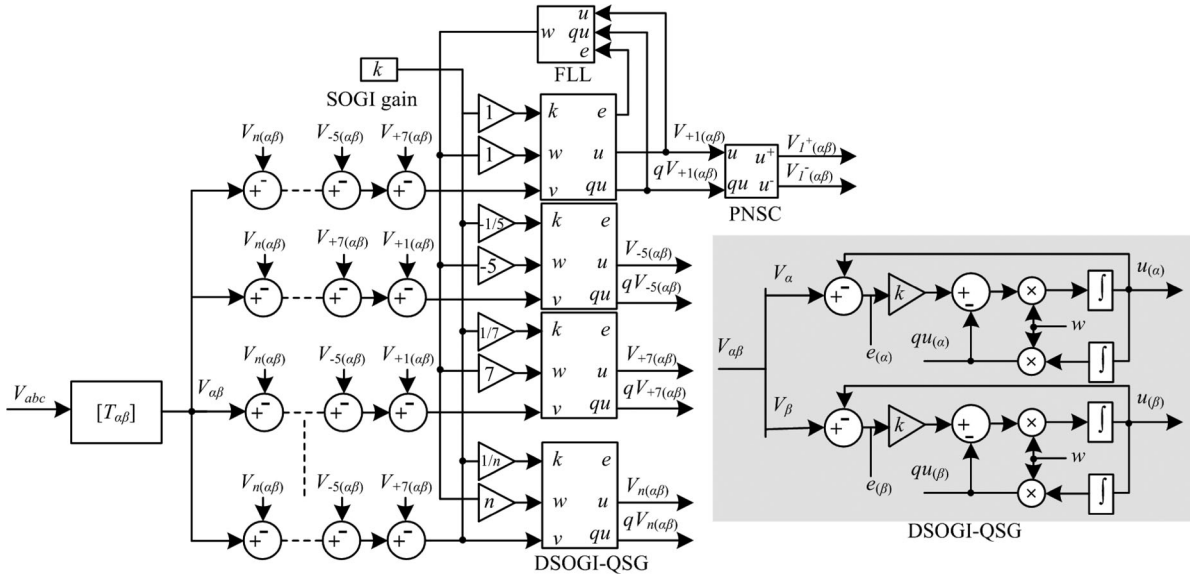

Fig. 9. Block diagram of the MSOGI-FLL in [26].

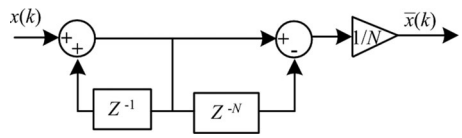

Fig. 10. Discrete-time realization of MAF.

where *x(k)* is the current sample. Fig. 10 shows the Z-domain realization of (29).

As shown in Fig. 10, the MAF is computationally efficient. For a fixed window width, it requires only one multiplier, one adder, and one subtractor. The DMAF-PLL needs only a MAF and a PF to accurately obtain the phase angle and frequency of fundamental positive sequence voltage, and PF is consisted of only one differentiator, one multiplier, and one adder. That is to say, the proposed approach requires only two multiplier, two adders, one subtractor, and one differentiator to eliminate all the characteristic harmonics.

In addition to a lower computational burden, DMAF-PLL has a faster dynamic response. The characteristics of MSOGI-FLL, MRF-PLL, and MCCF-PLL have been fully studied in [28] and [29], which shows that the open-loop bandwidth of these multichannel mode PLLs must be sufficiently smaller than $2\omega_n$ (ω_n is the fundamental angular frequency) to ensure the system stability [28], [29]. According to [29], the open-loop bandwidth of these multichannel mode PLLs should be set to 22 Hz to get an optimal performance, which is smaller than that of DMAF-PLL (31 Hz). It can be concluded that even if the MSOGI-FLL with a complex structure and high computational burden can eliminate all characteristic harmonics, its dynamic response is still slower than that of DMAF-PLL. A detailed comparison between the structure of MSOGI and DMAF has been listed in Table I.

TABLE I
COMPARISON BETWEEN MSOGI AND DMAF

Aspects	MSOGI	DMAF
Implementation details		
Integrations/differentiations	$4n+4$	1
Multiplications	$6n+6$	2
Additions/subtractions	$4n+4$	3
Harmonics elimination	*n* characteristic harmonics	all characteristic harmonics
Dc offset elimination	no	yes
Dynamic response speed	slow	fast

Note: "*n*" is the number of different characteristic harmonics needed to be eliminated.

D. Impact of Frequency Variations on DMAF-PLL

The DMAF-PLL contains MAF and PF structures, and a major problem associated with the MAF and PF is their frequency-dependent characteristics. Assuming the MAF has a fixed window width equals to $1/f_n$ (f_n is the nominal grid frequency), the MAF can completely eliminate all characteristic harmonics whose frequencies are integer multiples of f_n. If the grid frequency deviates from f_n, the frequencies of characteristic harmonics will also deviate from integer multiples of f_n, and then the MAF can only attenuate but not completely eliminate them [40], [42], which can be easily observed from Fig. 2. The MAF used in the proposed approach is frequency-adaptive because it uses PLL to estimate the online frequency of the grid and change the window width accordingly [42]. Being similar to the frequency-adaptive MAF, the PF proposed in this paper is also frequency adaptive because it also uses the estimated grid frequency to change its dividend. Since both MAF and PF adopted in DMAF-PLL are frequency adaptive, the DMAF-PLL can always accurately obtain the phase angle and frequency of grid even when the grid frequency deviates from its nominal value.

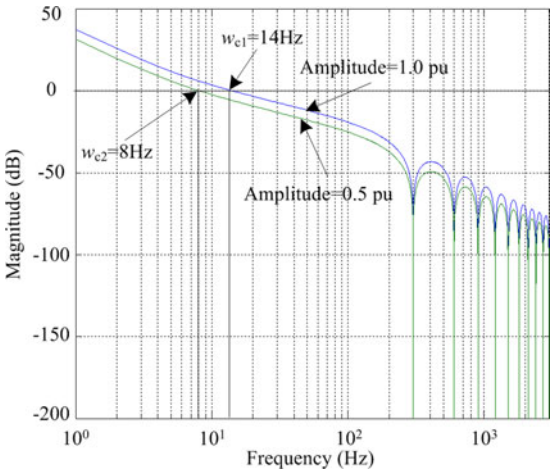

Fig. 11. Open-loop bode plot of MAF-PLL with different amplitudes of the positive sequence grid voltage.

E. Impact of Amplitude Variations on DMAF-PLL

It can be observed from Fig. 3 and (10) that the variations in the amplitude of positive sequence grid voltage impact on the open-loop gain of PLL, and thus on the dynamics of the closed-loop PLL. MAF-PLL and DMAF-PLL both have this problem. Fig. 11 shows the open-loop Bode plot of MAF-PLL with different amplitudes of the positive sequence grid voltage.

It can be observed from Fig. 11 that the open-loop bandwidth is reduced to 8 Hz from 14 Hz when the amplitude drops to 0.5 p.u. from 1.0 p.u., which means that the dynamic adjusting time of PLL increases accordingly. The problem can be solved by normalizing the amplitude, and it is realized by dividing the open-loop gain by a variable equals to $\hat{V}_1^+$ (refer to Figs. 1 and 6).

F. Impact of Differentiation

Although PF can fast eliminate the lowest order harmonic to narrow the window width of MAF, two problems are brought in. First, the PF can amplify the harmonics because it adopts differentiation, for example, the amplitude of hth harmonic is amplified to its $(1 + h/2)$ times. The problem is indispensible and also presented in [45] in which S. Alepuz *et al*. proposed a method of using differentiation for fast separating the symmetrical components in a clean grid voltage. However, this problem can be solved in the proposed approach because the MAF acts as an ideal low-pass filter which can completely eliminate all the amplified characteristic harmonics. The direct use of differentiation can also amplify the interharmonics and noncharacteristic harmonics but they can be attenuated more by the later MAF and PLL structures, which can be proved by (28) and easily observed from the open-loop Bode plot of DMAF-PLL shown in Fig. 8. From Fig. 8, the interharmonics and noncharacteristic harmonics are attenuated by at least 21 dB by the whole DMAF-PLL structure and the higher the frequencies of them, the more they could be attenuated. In addition, antialiasing fi which is a kind of analog low-pass fi is usually used before analog to digital conversion to limit the noise bandwidth in practical implementations [42], [44]. This low-pass filter can also attenuate all the harmonics including the interharmonics and noncharacteristic harmonics.

TABLE II
SIMULATION CONDITIONS FOR DIFFERENT CASES

Case	Simulation conditions
1	Voltage initial phase is 20° and phase jumps of 40° at 0.15 s.
2	Frequency jumps of 5 Hz at 0.05 s.
3	Amplitude jumps of -20% at 0.05 s.
4	Phase A drops to 0 at 0.05 s and restores at 0.15 s; Phase A and B drop to 0.5 p.u. at 0.25 s and restore at 0.35 s.
5	Phase A drops to 0.5 p.u., phase jumps of 20°, and 10% -5th, 5% $+7$th, 5% -11th, 2% $+13$th harmonics are injected at 0.05 s.
6	Phase B drops to 0.5 p.u., phase jumps of 20°, 0.1 p.u. constant dc component and 1 p.u./s slowly varying dc component are added into phase A at 0.05 s and all the faults restore at 0.25 s.

The other problem is the phase angle and frequency fluctuations caused by taking derivative of v_d when amplitude step change appears. It can be easily realized that v_d' equals to zero when the amplitude does not change but its value is very large when amplitude step change appears. The large value could influence the phase error and cause the phase angle and frequency fluctuations. Since the absolute value of v_d' is commonly very large when amplitude step change appears, it can be easily recognized and eliminated. For example, assuming a 2% amplitude step change appears, and the sampling rate is 20 kHz (sampling period is 0.05 ms), then the absolute value of v_d' can be calculated as

$$|v_d'| = \frac{\left|\Delta V_1^+\right|}{\Delta T} = \frac{1}{5 \times 10^{-5}} \times 2\% = 400 \tag{30}$$

where ΔV_1^+ is the difference value of the amplitude acquired before and after the step change occurs and ΔT is the sampling period. In order to eliminate the undesired effect of differentiation, the output of PF should keep to its last value if the absolute value of v_d' is very large, otherwise to its current value.

IV. SIMULATION RESULTS

In order to evaluate the performance of DMAF-PLL, the time-domain simulations of MAF-PLL and DMAF-PLL are both carried out to make a comparison in the MATLAB/Simulink environment using 20-kHz discrete fixed-step solver. The initial input voltage is set to its nominal values, i.e., amplitude is 1 p.u., phase is 0, and frequency is 50 Hz. The initial conditions of PLL are set as follows: amplitude is 0, phase is 0, and frequency is 50 Hz. In this paper, the grid code IEC 610000-3-6 [46] and some other grid codes mentioned in [47] which are usually adopted in the test of PLL techniques are considered. Since the new method is an improvement of the MAF(s)-based PLL, test conditions used in MAF(s)-based PLL [34] [42] are also considered. The detailed simulation conditions and parameters can be seen in Tables II and III, respectively.

In order to conveniently calculate the settling time and compare the performance of MAF-PLL and DMAF-PLL, it is

TABLE III
SIMULATION PARAMETERS OF MAF-PLL AND DMAF-PLL

Method	Parameters	Note
MAF-PLL	$k_p = 83.33, k_i = 2893.52, T_w = 0.01$ s	$T_w = 0.02$ s for MAF used to eliminate dc components
DMAF-PLL	$k_p = 250, k_i = 26041.68, T_w = 0.0033$ s	$T_w = 0.02$ s for MAF used to eliminate dc components

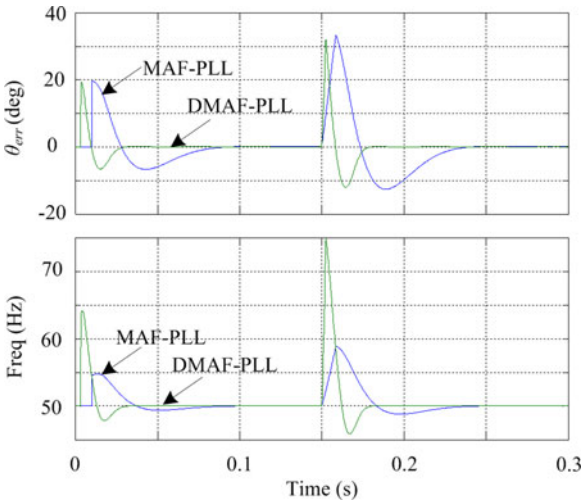

Fig. 12. Startup and phase jump performance of MAF-PLL and DMAF-PLL.

considered that the transient response finishes and the PLL turns into its steady state when the following conditions are met, i.e., the amplitude fluctuation is less than 0.02 p.u.; the phase fluctuation is less than 1°; the frequency fluctuation is less than 20 mHz. In all the simulation results, $\theta_{\rm err}$ stands for the error between the real and estimated phase angles, Freq means the frequency and Amp represents the amplitude.

Case 1: Startup and phase jump.

Since the PLL needs some time to reach the steady state after its first startup, a startup time is defined to evaluate the startup speed of MAF-PLL and DMAF-PLL. It can be observed from Fig. 12 that the phase startup time of MAF-PLL is 76.9 ms which is much longer than DMAF-PLL of 25.4 ms, and the frequency startup time of MAF-PLL is 95.9 ms which is much longer than DMAF-PLL of 31.8 ms. That is to say the startup time (phase and frequency startup time) of DMAF-PLL is decreased by about 66% compared with MAF-PLL. From Fig. 12, it can also be observed that when phase jump occurs, the phase settling time of MAF-PLL and DMAF-PLL is 78.7 and 25.5 ms, respectively, and the frequency settling time is 94.8 and 35.9 ms, respectively. It can be concluded that when phase jump occurs, the settling time (phase and frequency settling time) of DMAF-PLL is decreased by about 66% compared with MAF-PLL.

Case 2: Frequency jump.

From Fig. 13, the phase settling time of MAF-PLL and DMAF-PLL is 67.8 and 19.3 ms, respectively, and the frequency settling time is 111.6 and 35.9 ms, respectively. It can be observed that when frequency jump occurs, the phase and

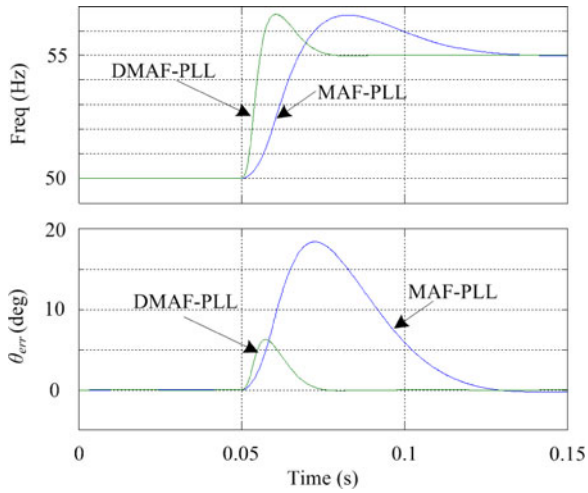

Fig. 13. Performance of MAF-PLL and DMAF-PLL when frequency jump occurs.

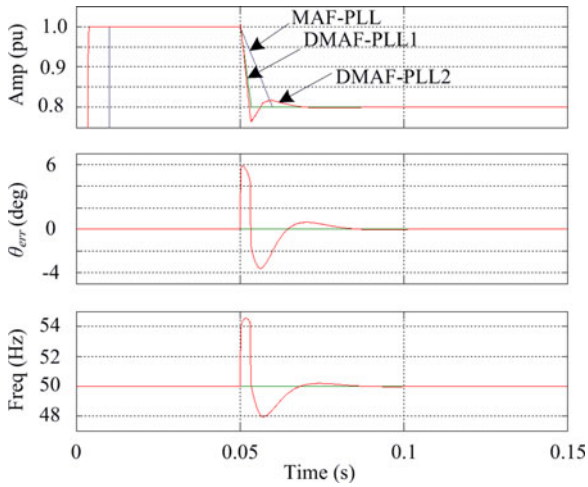

Fig. 14. Performance of MAF-PLL and DMAF-PLL when amplitude jump occurs.

frequency settling time of DMAF-PLL are both decreased by about 70% compared to MAF-PLL, and this is a great improvement in dynamic response.

Case 3: Amplitude jump.

In Fig. 14, DMAF-PLL1 and DMAF-PLL2 stand for the performance of DMAF-PLL with and without elimination of the undesired effect of differentiation, respectively.

From Fig. 14, MAF-PLL and DMAF-PLL with differentiation effect elimination do not appear in phase and frequency fluctuations when the amplitude jump occurs, but DMAF-PLL without differentiation effect elimination does. It can also be observed from Fig. 14 that DMAF-PLL with differentiation effect elimination has the shortest amplitude settling time (3.3 ms) which is shorter than MAF-PLL of 10 ms. It can be concluded that DMAF-PLL has a better performance than MAF-PLL as it has shorter amplitude settling time and an equivalent phase and frequency performance when the amplitude jump occurs.

Case 4: Unbalanced voltage caused by asymmetric faults.

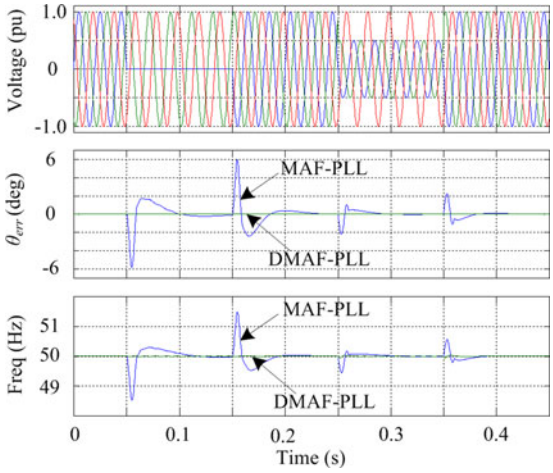

Fig. 15. Performance of MAF-PLL (blue) and DMAF-PLL (green) when asymmetric faults occur.

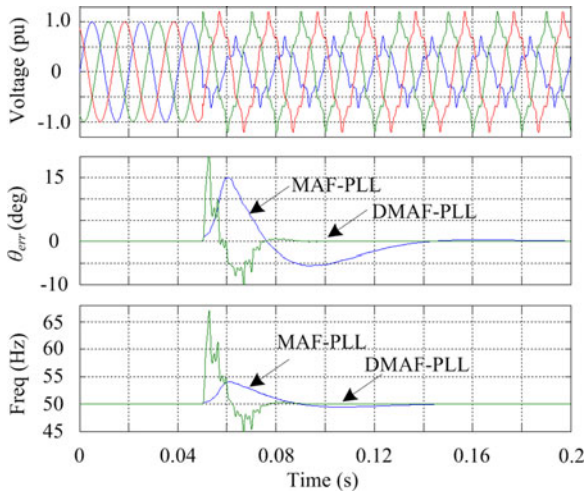

Fig. 16. Performance of MAF-PLL (blue) and DMAF-PLL (green) under highly distorted grid environment.

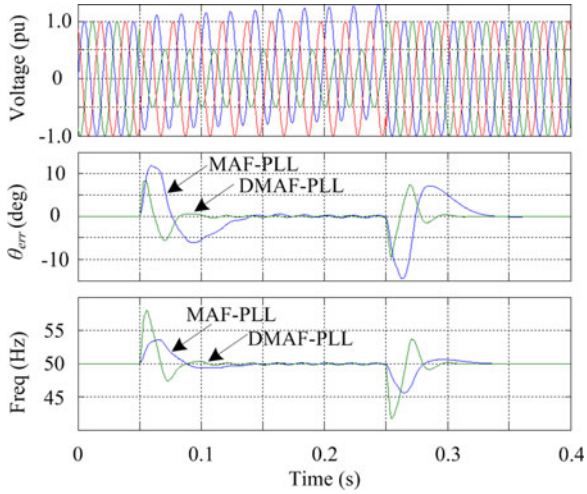

Fig. 17. Performance of MAF-PLL (blue) and DMAF-PLL (green) when asymmetric fault occurs in grid environment with dc components.

TABLE IV
SETTLING TIME OF MAF-PLL AND DMAF-PLL

Case	Phase settling time (ms) MAF-PLL/DMAF-PLL	Frequency settling time (ms) MAF-PLL/DMAF-PLL	Note
1	76.9/25.4	95.9/31.8	Startup
	78.7/25.5	94.8/35.9	Phase jump
2	67.8/19.3	111.6/35.9	Frequency jump
3	0/0	0/0	Amplitude jump
4	① 30.8/0 ② 27.3/0	① 111.2/0 ② 74.7/0	Asymmetric faults
	③ 8.6/0 ④ 9.3/0	③ 49.6/8.8 ④ 34.7/7	
5	80.5/23.6	102.5/36.8	Distorted environment
6	① 80/29.5 ② 72/37	① 90/60 ② 72/43	Dc offset

Note: ① represents single-phase fault occurs; ② represents single-phase fault restores; ③ represents phase to phase fault occurs; ④ represents phase to phase fault restores.

Fig. 15 shows that large phase and frequency fluctuations appear in MAF-PLL but not in DMAF-PLL when single-phase and phase-to-phase faults occur because the PF in DMAF-PLL can fast eliminate the negative sequence second harmonic caused by the asymmetric faults. It can be concluded that DMAF-PLL can fast eliminate the effect caused by asymmetric faults, which greatly improves the dynamic performance of MAF-PLL.

Case 5: Highly distorted grid environment.

Fig. 16 shows the performance of MAF-LL and DMAF-PLL under highly distorted grid environment. It can be observed that both of them can accurately estimate the phase angle and frequency of fundamental positive sequence component, but DMAF-PLL has a much shorter settling time when phase jump (grid faults usually cause phase jump) occurs in this distorted gird environment.

Case 6: Grid environment with dc components.

Fig. 17 shows the performance of MAF-PLL and DMAF-PLL when asymmetric fault occurs in grid environment with dc components. The dc components consist of constant and slowly varying dc components. It can be observed that both MAF-PLL and DMAF-PLL can accurately estimate the phase angle and frequency of fundamental positive sequence component, which means that the prefiltering structures (MAF in the stationary reference frame) can eliminate the effect of the dc components. From Fig. 17, DMAF-PLL has a much shorter settling time when phase jump (grid faults usually cause phase jump) occurs in this gird environment with dc components. The detailed settling time of different cases can be seen in Table IV.

V. EXPERIMENTAL VALIDATIONS

In order to validate the simulation results, the conventional and improved algorithms have been implemented using a dSPACE DS1103 control board, and the sampling frequency is fixed to 20 kHz. The input voltage is provided by a programmable three-phase ac-power source. All the experimental waveforms are captured by the LeCroy oscilloscope connected

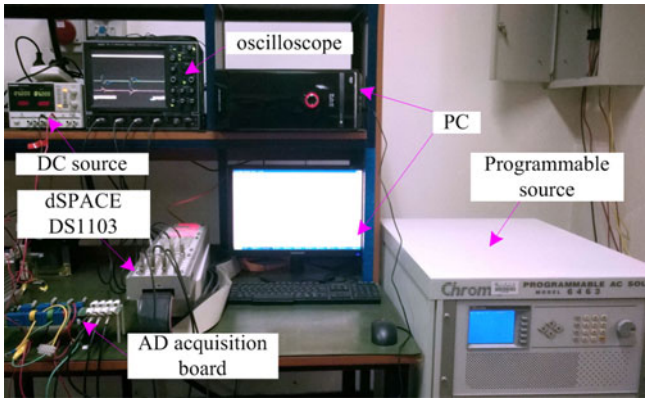

Fig. 18. Experimental setup.

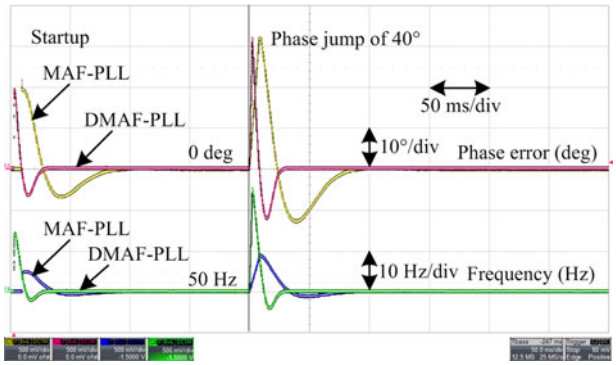

Fig. 19. Startup and phase jump performance of MAF-PLL and DMAF-PLL.

to the D/A channels of the dSPACE1103. Fig. 18 is the picture of the experimental setup.

In order to provide a better visualization, the frequency and three-phase amplitude jump have been increased to 10 Hz and 0.5 p.u., respectively. Other experimental conditions and parameters are the same as those used in the simulation in Section IV. In all the experimental results, the phase errors acquired from MAF-PLL (yellow) and DMAF-PLL (red) and the frequencies acquired from MAF-PLL (blue) and DMAF-PLL (green) are captured to make a comparison.

It can be observed from Fig. 19 that DMAF-PLL has a shorter startup time and a shorter phase and frequency settling time compared with MAF-PLL when phase jump occurs. Fig. 20 shows the experimental results of MAF-PLL and DMAF-PLL when frequency and amplitude (three phase) jumps occur. From Fig. 20, both algorithms do not appear in phase and frequency fluctuations when the amplitude of three-phase voltage jump occurs and restores but DMAF-PLL has a shorter phase and frequency settling time compared with MAF-PLL when frequency jump occurs. It can be observed from Fig. 21 that MAF-PLL appears in large phase and frequency fluctuations when asymmetric faults occur while DMAF has an excellent performance with negligible phase and frequency fluctuations because DMAF-PLL can fast eliminate the negative sequence second harmonic caused by asymmetric faults. From Fig. 22, in highly distorted grid environment, both MAF-PLL and DMAF-PLL

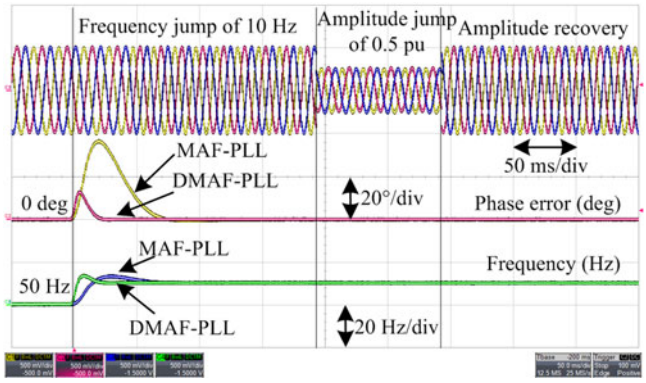

Fig. 20. Frequency and amplitude jump performance of MAF-PLL and DMAF-PLL.

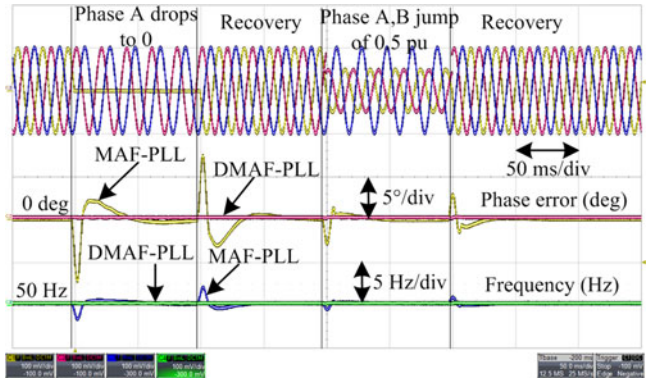

Fig. 21. Performance of MAF-PLL and DMAF-PLL when asymmetric faults occur.

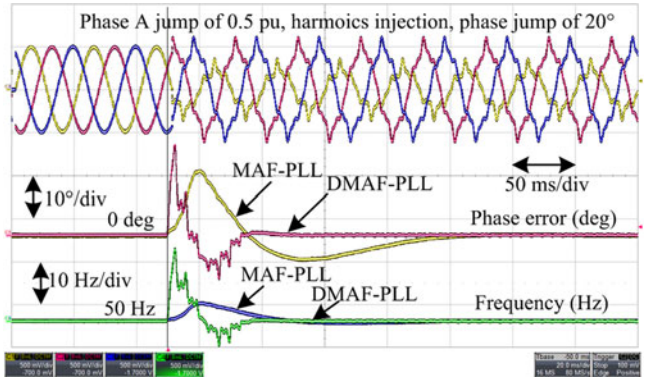

Fig. 22. Performance of MAF-PLL and DMAF-PLL under highly distorted grid conditions.

can accurately lock the phase angle and frequency of ac voltages but DMAF-PLL has a faster dynamic response because of its larger loop bandwidth compared with MAF-PLL. Fig. 23 shows that the prefiltering structure (MAF in the stationary reference frame) can eliminate the effect of dc components, and both MAF-PLL and DMAF-PLL can accurately estimate the phase angle and frequency of fundamental positive sequence component but DMAF-PLL has a faster dynamic response. All the

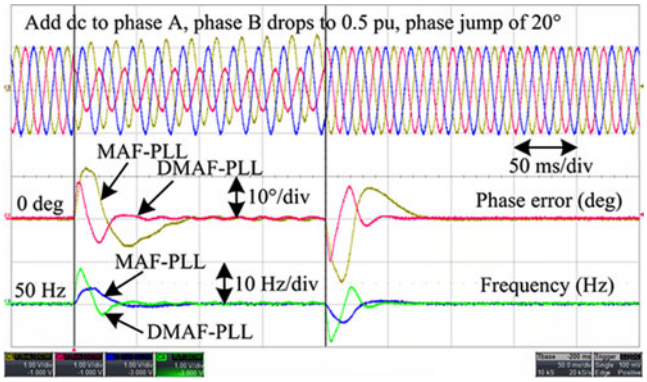

Fig. 23. Performance of MAF-PLL and DMAF-PLL when asymmetric fault occurs in grid environment with dc components.

experimental and simulation results are basically identical, and both of them validate the effectiveness of the proposed method.

VI. Conclusion

In this paper, a synchronization technique named DMAF-PLL has been proposed and evaluated through theoretical analysis, simulation, and experimental tests. DMAF-PLL can be regard as an improved version of the MAF(s)-based PLL because of its greatly improved dynamic performance. The method is realized by incorporating a variable proportional component (named PF in this paper) into the MAF(s)-based PLL. The value of PF changes according to the frequency of input signal, and it can fast eliminate the negative sequence second harmonic caused by the unbalanced voltage to increase the MAF bandwidth. Theoretical analysis and the open-loop Bode plot of DMAF-PLL show that the proposed method greatly improves the transient response speed of MAF(s)-based PLL, and it can keep a sufficient stability margin. Then, the impact of frequency variations, amplitude variations, and differentiation on DMAF-PLL has been analyzed in detail. Its advantages over some established PLL techniques used in highly distorted grid environment have also been addressed. Finally, simulation and experimental verifications of MAF-PLL and DMAF-PLL are both carried out to make a comparison under different operational conditions, whose results verify the effectiveness and robustness of the improved method.

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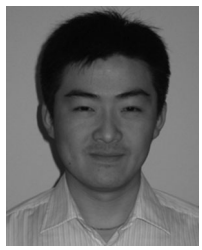

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