On Reducing Power Losses in Stack Multicell Converters with Optimal Voltage Balancing Method

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***Abstract*—This paper proposes a voltage balancing method for stacked multicell converters (SMCs) based on phase-disposition pulse-width modulation (PD-PWM). In order to reduce the switching transitions of the power devices, only optimal transitions between consecutive voltage levels are used. Selection of the optimal transition sequence is performed by evaluating a cost function. Significant reductions in the switching transitions and power losses of the power devices are achieved as compared to the optimal-state voltage balancing method where nonoptimal transitions are allowed. Simulation and experimental results from a seven-level 3×2 SMC verifies that the proposed PD-PWM voltage balancing method is robust under linear/nonlinear loads and transients.**

***Index Terms*—Capacitor voltage balancing, multilevel converter, pulse-width modulation (PWM), stacked multicell converter.**

I. Introduction

MULTILEVEL converters are widely used in high-power applications [1]–[6]. In the recent years, new hybrid multilevel topologies have appeared [7]. Hybrid multilevel converters require to store less energy than the popular multilevel topologies, i.e., the cascaded H-bridge converter [8], the modular multilevel converter [9], the neutral-point-clamped converter [10], and the flying capacitor (FC) converter [11]. Hybrid multilevel converters allow higher voltage/power ratings, lower total harmonic distortion (THD), and lower power losses, when compared with the conventional two-level converter [12]–[14] and also with some of the popular multilevel topologies.

Fig. 1 shows the hybrid multilevel topology called stacked multicell converter (SMC). The SMC is capable of generating a higher number of voltage levels besides requiring less energy stored in the capacitors when compared to the conventional FC converter. Like in the other multilevel topologies, this hybrid multilevel converter also requires capacitor voltage balancing. In

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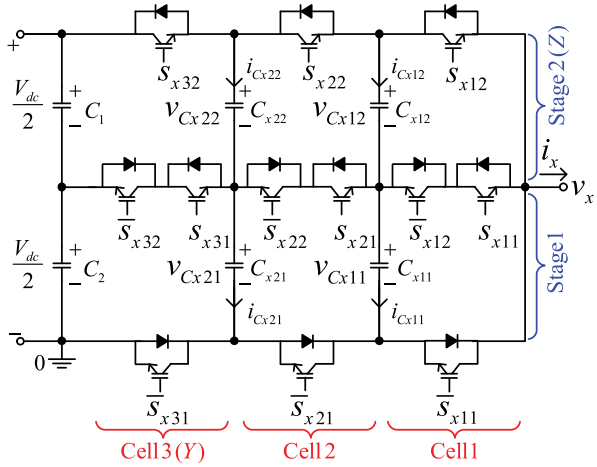


Fig. 1. Circuit diagram of a 3×2 SMC.

[15]–[22], phase-shifted pulse-width modulation (PS-PWM) was applied to the SMC, which provides natural voltage balancing. However, natural voltage balancing depends on the load conditions and the converter dynamics slow down with different types of loads, especially nonlinear ones. In [16]–[19], a booster was used to achieve faster voltage balancing dynamics. This balance booster consists of a passive RLC filter, and thus, introduces some power losses, reduces converter's reliability, and increases its size.

There are a few active voltage balancing methods found in the technical literature [23]–[25]. In [23], a direct torque control method was proposed. Another method was proposed in [24], which uses a sliding mode observer. This method performs very well and does not require any voltage sensors. However, its implementation is complicated and requires a lot of computations. An active voltage balancing method was proposed in [23] for hybrid converters such as the active neutral-point-clamped converter and the SMC. The method requires evaluation of a cost function for the selection of the redundant states using space vector modulation in a four-level SMC. The authors suggested increasing the number of voltage levels to extend the operating range of the converter, which is apparently not an optimal solution. An active voltage balancing method based on PS-PWM was proposed in [26]. The method performs very well in achieving capacitor voltage balance, however, PS-PWM produces line-to-line voltages with lower quality when compared to those generated using phase-disposition PWM (PD-PWM).

This paper presents a capacitor voltage balancing method for SMCs based on PD-PWM that uses only optimal switching transitions and is called the optimal transition voltage balancing

(OTVB) method. The method is performed by evaluating a cost function that selects the optimal switching transition between consecutive voltage levels from a pool of available transitions. The method proposed here is an improvement of the optimal-state voltage balancing (OSVB) method [27], where the number of switchings was not optimized. The improved method was briefly introduced in [28], and it has been extended further in this paper by including a more detailed analysis and experimental results taken from a three-phase seven-level 3×2 SMC laboratory prototype. Furthermore, this paper presents switching transitions, power losses in the semiconductors, the efficiency, and compares them with those obtained from applying OSVB [27].

The rest of this paper is organized as follows. Section II describes the operating principle of an SMC and the OSVB method. Section III introduces the OTVB method for reducing the switching transitions of the power devices. Section IV analyzes switching transitions, capacitor voltage ripples, power losses in the semiconductors, and the computation burden, comparing all of them with those produced with OSVB. Section V presents simulation and experimental results obtained from a low-power three-phase seven-level 3×2 SMC prototype. Finally, the conclusions of this paper are summarized in Section VI.

II. SMC AND THE OSVB METHOD

Fig. 1 shows a circuit diagram of a phase-leg of a seven-level SMC. It consists of three cells $(Y = 3)$ of an FC converter, which are integrated to form two stages/stacks $(Z = 2)$. This is why it is also called a 3×2 $(Y \times Z)$ SMC topology. The converter comprises of four FCs, the upper FCs C_{x12} and C_{x22} in Stage 2, and the lower FCs C_{x11}, C_{x21} in Stage 1, where the subscript x is used for phase identification $x = \{a, b, c\}$. The dc bus consists of two capacitors C_1 and C_2, each of them is regulated to operate at a half of the dc bus voltage $(V_{\rm dc}/2)$. During normal operation, the mean voltage of the FCs C_{x11} and C_{x12} has to be maintained at $V_{\rm dc}/6$, whereas for C_{x21} and C_{x22}, it has to be maintained at $V_{\rm dc}/3$. The output voltage v_{x0} consists of seven $(3 \times 2 + 1)$ voltage levels, i.e., 0, $V_{\rm dc}/6$, $V_{\rm dc}/3$, $V_{\rm dc}/2$, $2V_{\rm dc}/3$, $5V_{\rm dc}/6$, $V_{\rm dc}$. The switch control function is defined as $s_{x\,yz}$, where y denotes the switch number corresponding to a particular cell in the phase-leg x of the SMC converter $y = \{1, ..., Y\}$ $(Y = 3)$, and z defines the Stage $z = \{1, ..., Z\}$ $(Z = 2)$. The switch control functions can take two values $s_{x\,yz} = \{0, 1\}$, meaning "0" and "1" that the switch is OFF and ON, respectively. The switch pairs in each phase leg ($s_{x\,yz}$ and $\overline{s}_{x\,yz}$) operate in a complementary manner.

The OSVB method is based on minimizing a cost function, which is defined as the absolute value of deviation of energy stored in all the FCs from the rated conditions. It is given as follows [25], [29], [30]:

$$J_{xz\,s} = \frac{1}{2} \sum_{j=1}^{Y-1} C_{xjz} (v_{Cxjz} - V^*_{Cxjz})^2, \tag{1}$$

where x identifies the phase $(x = \{a, b, c\})$, and s is the switching state $(s = \{0, .., 63\})$ of Stage z. For example, $J_{a2\,57}$ is the cost function calculated for phase a $(x = a)$, at Stage 2 $(z = 2)$ and Switching State 57 $(s = 57)$, i.e., $s_{a31} = 1$, $s_{a21} = 1$, $s_{a11} = 1$, $s_{a32} = 0$, $s_{a22} = 0$, and $s_{a12} = 1$. j is the index used for the identification of each FC $j = \{1, 2\}$, being C_{xjz} a particular FC and V^*_{Cxjz} its reference voltage.

The cost function 1 is positively defined and becomes zero if all the FC voltages are at the reference values. Such function should be minimized by using a differentiation, as follows:

$$\begin{aligned} \frac{d}{dt} J_{xz\,s} &= \frac{d}{dt} \frac{1}{2} \sum_{j=1}^{Y-1} C_{xjz} (v_{Cxjz} - V^*_{Cxjz})^2 \\ &= \sum_{j=1}^{Y-1} (\Delta v_{Cxjz} i_{Cxjz}) \leq 0, \end{aligned} \tag{2}$$

where Δv_{Cxjz} is the voltage deviation of an FC $(\Delta v_{Cxjz} = v_{Cxjz} - V^*_{Cxjz})$, and i_{Cxjz} is the current in each FC, which depends on the selected redundant switching state and load current, as shown in Table I. When the modulator defines two particular voltage levels for the following switching period at Stage z, the cost function is evaluated for all redundant switching states available for those levels. Based on the calculated values for a particular output voltage level, the switching state that provides the minimum value to the cost function is the one selected

$$\min \left[\sum_{j=1}^{Y-1} (\Delta v_{Cxjz} i_{Cxjz}) \right], \tag{3}$$

and are used for the gating signals.

It should be noted that the optimal switching states between two consecutive voltage levels are selected independently one from another. Therefore, the OSVB method does not avoid the nonoptimal transitions, i.e., those transitions that produce more switchings, thus resulting in higher switching frequencies for the power devices. The OTVB proposed in this paper overcomes this problem because it avoids the use of nonoptimal transitions.

III. PROPOSED OTVB METHOD

The switching transitions between consecutive voltage levels of all the possible combinations of switching states from $000000\{0\}$ to $111111\{63\}$ are shown in Fig. 3. The transitions between two switching states shown by solid lines are called optimum transitions, as those transitions involve changing only one bit. Therefore, they produce the minimum number of switching events. On the other hand, the transitions represented by dashed lines are nonoptimal, as more than one bit changes in the transition between consecutive levels. For example, a minimum transition is produced when switching between the States $111001\{57\}$ and $111101\{61\}$ (see Fig. 3), while the transition between the States $111001\{57\}$ and $111110\{62\}$ is a nonoptimal one. Hence, if the nonoptimal transitions are chosen, switching frequencies of the power devices increase.

Furthermore, additional switching transitions can be produced using traditional triangular carriers. When using these carriers, once a switching period has ended, the following one will usually start providing the same voltage level as that in

TABLE I
SEVEN-LEVEL 3 × 2 SMC: VOLTAGE LEVELS, SWITCHING STATES, FC CURRENTS, AND EFFECTS ON THE FC VOLTAGES

		Switching States							FC Currents				FC Voltages				
	Output Voltage Level (v_{x0})	s_{x31}	s_{x21}	s_{x11}	s_{x32}	s_{x22}	s_{x12}	State	i_{Cx21}	i_{Cx11}	i_{Cx22}	i_{Cx12}	v_{Cx21}	v_{Cx11}	v_{Cx22}	v_{Cx12}	
6	V_{dc}	1	1	1	1	1	1	{63}	0	0	0	0	NC	NC	NC	NC	
5	$5\frac{V_{dc}}{6}$	1	1	1	1	1	0	{62}	0	0	0	i_x	NC	NC	NC	↑	
		1	1	1	1	0	1	{61}	0	0	i_x	-i_x	NC	NC	↑	↓	
		1	1	1	0	1	1	{59}	0	0	-i_x	0	NC	NC	↓	NC	$v_{xref} > 0$
4	$2\frac{V_{dc}}{3}$	1	1	1	1	0	0	{60}	0	0	i_x	0	NC	NC	↑	NC	
		1	1	1	0	1	0	{58}	0	0	-i_x	i_x	NC	NC	↓	↑	
		1	1	1	0	0	1	{57}	0	0	0	-i_x	NC	NC	NC	↓	
3	$\frac{V_{dc}}{2}$	1	1	1	0	0	0	{56}	0	0	0	0	NC	NC	NC	NC	
2	$\frac{V_{dc}}{3}$	1	1	0	0	0	0	{48}	0	i_x	0	0	NC	↑	NC	NC	
		1	0	1	0	0	0	{40}	i_x	-i_x	0	0	↑	↓	NC	NC	
		0	1	1	0	0	0	{24}	-i_x	0	0	0	↓	NC	NC	NC	$v_{xref} < 0$
1	$\frac{V_{dc}}{6}$	1	0	0	0	0	0	{32}	i_x	0	0	0	↑	NC	NC	NC	
		0	1	0	0	0	0	{16}	-i_x	i_x	0	0	↓	↑	NC	NC	
		0	0	1	0	0	0	{8}	0	-i_x	0	0	NC	↓	NC	NC	
0	0	0	0	0	0	0	0	{0}	0	0	0	0	NC	NC	NC	NC	

Note: The charging/discharging effects in the FC are given assuming that i_x is positive ($i_x > 0$) with the following notation:
↑ Capacitor voltage increases.
↓ Capacitor voltage decreases.
NC No change in the capacitor voltage.

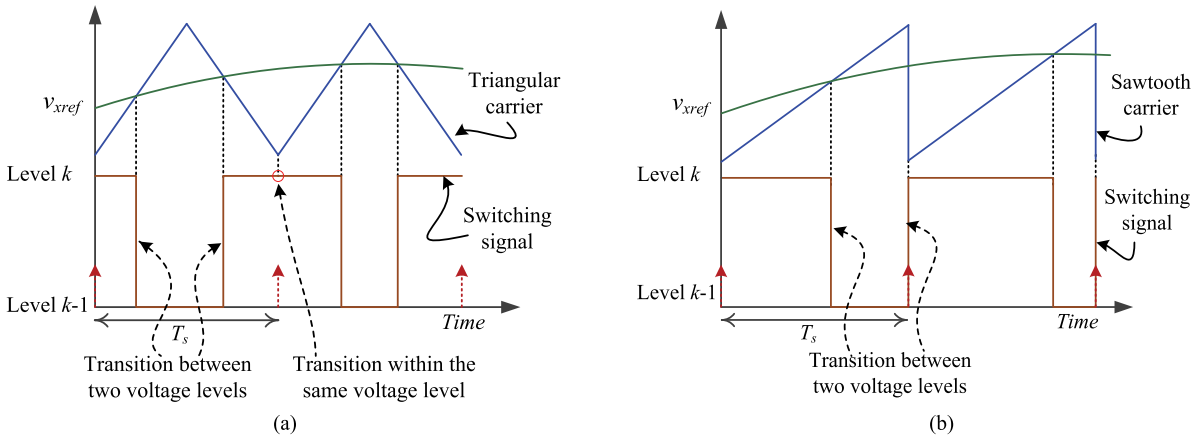


Fig. 2. Switching frequency reduction example: (a) transitions between two consecutive voltage levels and possible transitions within the same voltage level when using triangular carriers, and (b) transitions between two consecutive voltage levels using sawtooth carriers.

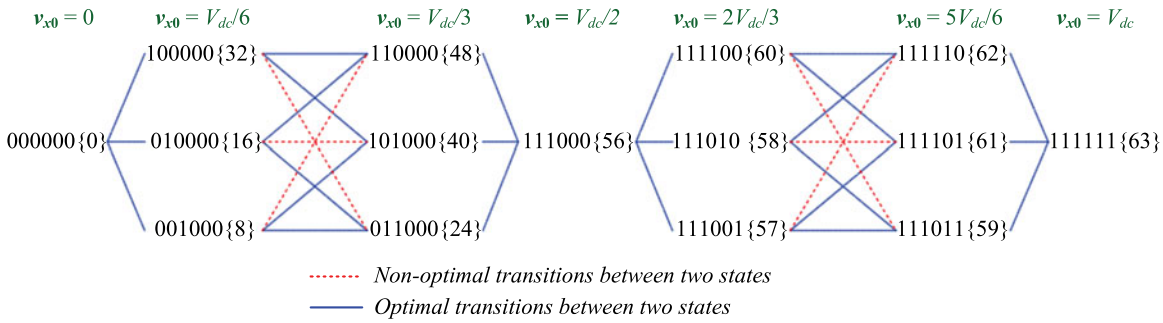
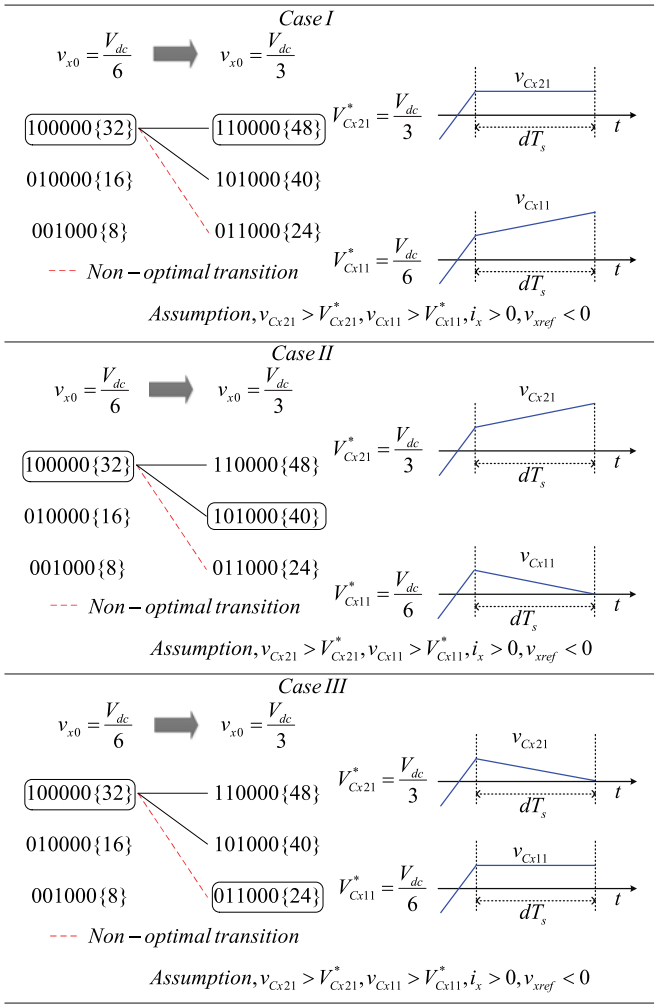


Fig. 3. Switching transitions between consecutive voltage levels in a seven-level 3×2 SMC.

TABLE II
CASE STUDY OF OSVB METHOD



the previous instant [see Fig. 2(a)]. Since the evaluation of the cost function is performed during the previous switching period and the new switching state is applied at the sampling instant, the selected switching state may change within the same level because of voltage balancing requirements, as it is shown in the example in Fig. 2(a). This fact leads to additional switching transitions in the power devices. This can be avoided by changing the shape of the carriers [29], [30]. Fig. 2(b) shows the case of using sawtooth-shaped carriers for the modulation. As it can be noted, no transition within the same voltage level can happen when changing from one switching period to the next one. On the contrary, the transitions are between consecutive levels. Hence, a significant amount of switching transitions can be avoided by using sawtooth carriers.

The switching transitions of the power devices can be further reduced by avoiding the nonoptimal transitions between consecutive voltage levels. However, avoiding the nonoptimal transitions will worsen the FC voltage balance. This effect is shown in the example in Table II, where three cases are given. In all the case study, the duty cycle and the sinusoidal voltage reference signal are denoted by d and $v_{x\mathrm{ref}}$, respectively. In the Case I, the converter is switching from State $100000\{32\}$ to State $110000\{48\}$, and in Case II the switching is from State $100000\{32\}$ to State blue$101000\{40\}$. Both Cases I and II are optimal transitions, however, none of the final states provide optimum voltage balance, since the voltage in one of the FCs increases and tends to go far beyond the reference value (capacitors C_{x11} and C_{x21} in the Cases I and II, respectively). On the other hand, in the Case III, the switching transition is from State $100000\{32\}$ to State $011000\{24\}$, which is a nonoptimal one. However, the State $011000\{24\}$ is the best from the point of view of voltage balancing, since none of the voltages in the FCs deviates further from the reference values. Therefore, if this state is avoided because it produces additional switching transitions, and either of the two states in Case I or II are chosen, the voltage balancing will be less effective. This can be partially compensated by using a modulation method that chooses the optimal transition considering the two states simultaneously, and not only the optimal states separately. As a result, the FC voltage balance will improve.

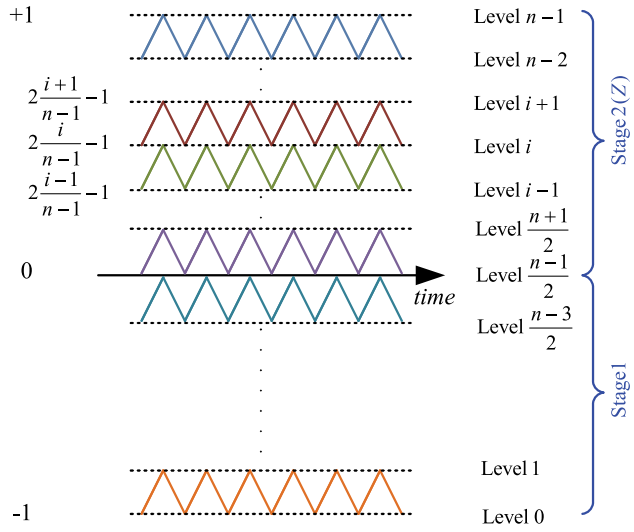


Fig. 4. Carriers in PD-PWM.

A similar analysis can be performed if the output current is negative. In such a case, the current through the capacitors will produce the opposite charging/discharging effect on them, i.e., the signs of the slopes of the voltage waveforms in Table II will change.

The cost function in [25], [29], and[30] is modified to select the switching transitions between two states of different voltage levels and is given as [28], [31]

$$J_{xz\,si-si+1} = J_{xz\,si}d_i + J_{xz\,si+1}d_{i+1}, \tag{4}$$

where x identifies the phase $(x=\{a,b,c\})$, i is the first state, $i+1$ is the second state, $d_i \in [0,1]$ is the duty cycle of the first state, and $d_{i+1} \in [0,1]$ is the duty cycle of the second state. As shown in Fig. 4, the duty cycle of an output voltage level using PD-PWM can be obtained as follows:

$$\text{for} \quad 2\frac{i}{n-1}-1 \le v_{x\mathrm{ref}} \le 2\frac{i+1}{n-1}-1: \quad d_i = (i+1)-(n-1)\frac{v_{x\mathrm{ref}}+1}{2} \tag{5}$$

$$\text{and for} \quad 2\frac{i-1}{n-1} - 1 \leq v_{x\text{ref}} \leq 2\frac{i}{n-1} - 1: \quad d_i = (n-1)\frac{v_{x\text{ref}}+1}{2} - (i-1) \tag{6}$$

$$\text{otherwise} \quad d_i = 0, \tag{7}$$

where n is the number of levels ($n = (Z \times Y + 1)$), in this paper $Z = 2$, $Y = 3$, and therefore, $n = 7$. And $v_{x\text{ref}}$ is the reference signal that ranges in the interval $[-1, 1]$ under linear operation mode. When $v_{x\text{ref}}$ is positive $z = 2$, otherwise $z = 1$.

The cost function of the transitions between two different voltage levels is positively defined, and if all the FC voltages are regulated at their reference value, it becomes zero. Hence, in order to achieve voltage balance, this cost function needs to be minimized at any switching period using differentiation. Thus, differentiation of 4, gives the following expression:

$$\frac{d}{dt}J_{xz\,si-si+1} = \sum_{j=1}^{Y-1} \Delta v_{Cxjz}(i_{Cxjz}d_i + i_{Cxjz}d_{i+1}) \leq 0, \tag{8}$$

where $i_{Cxjz\,si}$ and $i_{Cxjz\,si+1}$ are the capacitor currents of the corresponding states of the Stage z. They depend on the load currents and the redundant switching states, as shown in Table I. The terms Δv_{Cxjz} are the voltage deviations of the FCs ($\Delta v_{Cxjz} = v_{Cxjz} - V^*_{Cxjz}$).

When the modulator defines two particular voltage levels for the following switching period at the Stage z, the cost function is evaluated for all the redundant optimum switching transitions available for those levels. Based on the calculated values, the switching transition that provides the minimum value to the cost function is selected

$$\min\left[\sum_{j=1}^{Y-1} \Delta v_{Cxjz}\,(i_{Cxjz}d_i + i_{Cxjz}d_{i+1})\right]. \tag{9}$$

In order to avoid additional switching events, all the nonoptimal transitions are disregarded in the selection process. Once the optimal switching transition is selected, the two consecutive switching states are determined, which define the gating signals of the SMC. Fig. 5, shows a block diagram for the implementation of the proposed voltage balance method. In this block diagram, the measured FC voltages and load current are sampled at the carriers frequency and used for the calculation of the cost functions.

IV. Comparison Analysis Using OSVB and OTVB

Simulation analysis is conducted on the three-phase 3×2 SMC shown in Fig. 1. A medium-power converter in the range of 250 kVA is selected for the simulations. The dc voltage is $V_{\text{dc}} = 3$ kV and a three-phase sinusoidal current source of $I_{x\text{rms}} = 80$ A is connected to the converter output. The value of the FCs is $C = 1800$ μF. The fundamental and the carrier frequencies are $f = 50$ Hz and $f_s = 5$ kHz, respectively. The analysis is done in terms of switching transitions, capacitor voltage ripples, and power losses.

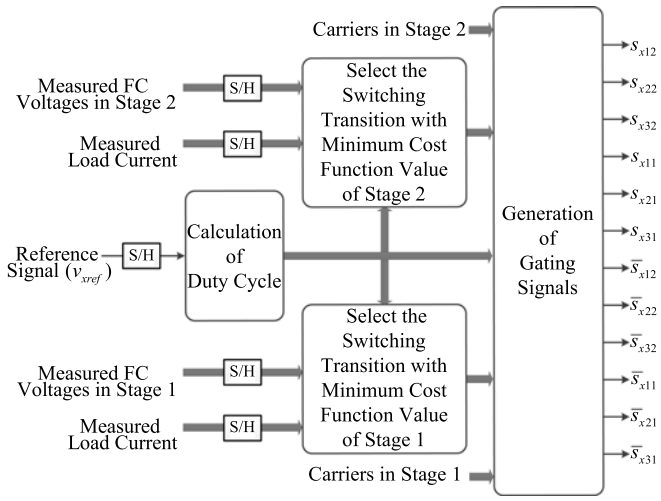


Fig. 5. Block diagram of the proposed OTVB method.

TABLE III
Relationship Between k and Modulation Index in an n-Level SMC

k	**Modulation Index,** m
1	$(n-3)/(n-1) < m \leq 1$
2	$(n-5)/(n-1) < m \leq (n-3)/(n-1)$
3	$(n-7)/(n-1) < m \leq (n-5)/(n-1)$
$(n-3)/2$	$2/(n-1) < m \leq 4/(n-1)$
$(n-1)/2$	$0 < m \leq 2/(n-1)$

TABLE IV
Minimum Number of Switching Transitions in a Seven-Level SMC

k	**Modulation Index,** m	N_{min}
1	$2/3 < m \leq 1$	212
2	$1/3 < m \leq 2/3$	208
3	$0 < m \leq 1/3$	204

A. Switching Transitions and FC Voltage Ripples

In the case of an SMC with an odd number of levels, the minimum number of switching transitions using PD-PWM can be calculated as

$$N_{\text{min}} = 2\frac{f_s}{f} + 2[n - (2k-1)], \tag{10}$$

where f_s is the carrier frequency, f is the fundamental frequency, n is the number of levels, and $k = 1, 2, ..., (n-1)/2$ that depends on the modulation index. In (10), the term $2f_s/f$ represents the number of crossings of a constant reference signal with a carrier, while the term $2[n-(2k-1)]$ represents the switching count due to the reference signal crossing the carrier bands of the PD-PWM. Table III shows the dependence of k with the modulation index in the general case of an n-level SMC. Table IV shows the particular case of a seven-level SMC ($n = 7$) and carrier and output frequencies of $f_s = 5$ kHz and $f = 50$ Hz, respectively. In order to achieve the maximum amplitudes of the output voltage fundamentals under linear mode, a zero

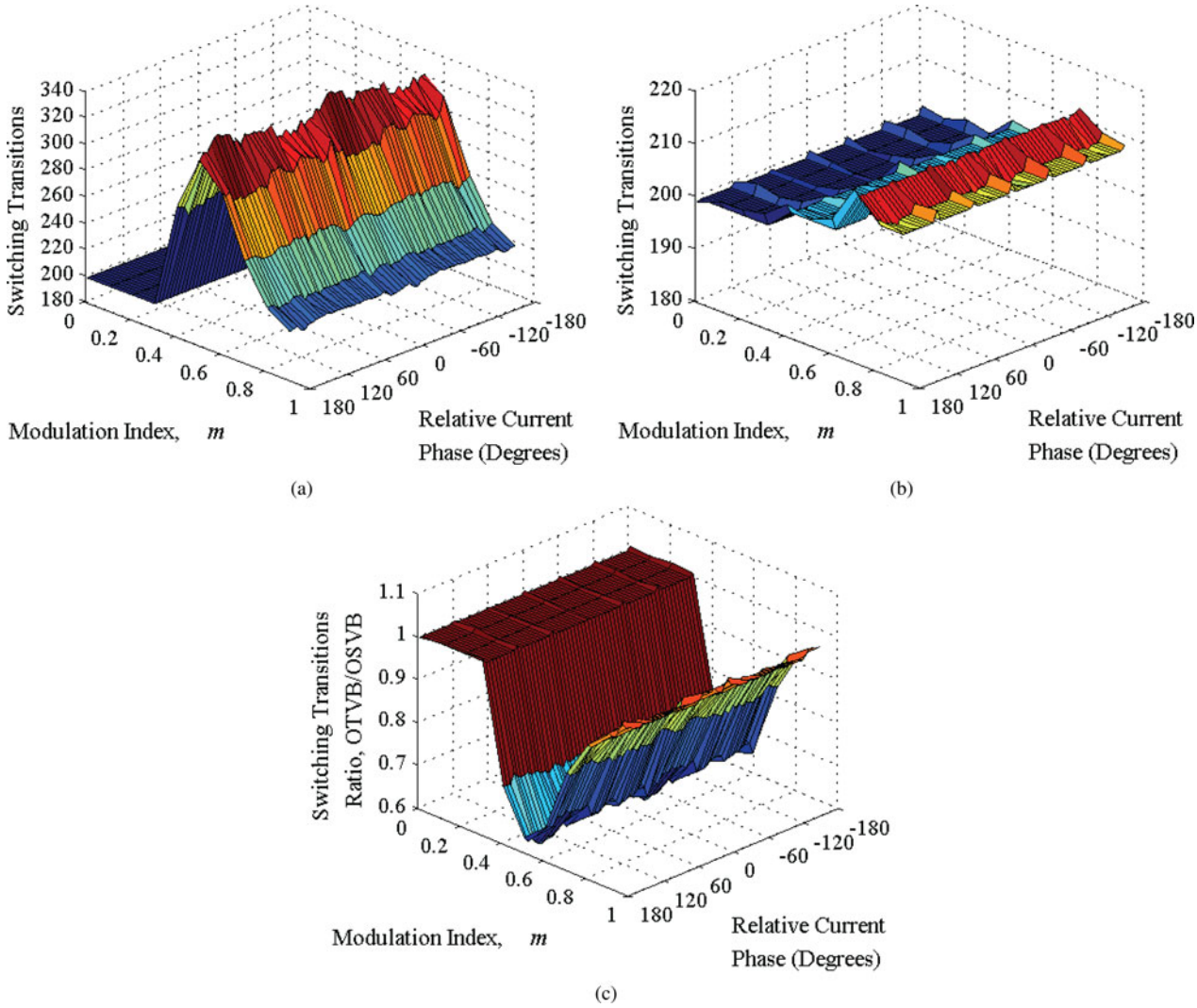


Fig. 6. Analysis of switching transitions using: (a) OSVB, (b) OTVB, and (c) ratio of OTVB over OSVB.

sequence has been added to the modulation signals of the converter. The zero sequence is given by $-(v_{x\mathrm{ref\,max}} + v_{x\mathrm{ref\,min}})/2$, where $v_{x\mathrm{ref\,max}}$ and $v_{x\mathrm{ref\,min}}$ are the maximum and minimum values of the modulation signals of the converter, respectively [32]. The addition of this zero sequence to the reference signals may increase the number of switching transitions a little for some modulation indices because the reference signals will cross the carrier bands more times, however, this increase in the minimum number of switching transitions is practically insignificant.

Fig. 6(a) and (b) shows the number of switching transitions of both voltage balancing methods, i.e., OTVB and OSVB, respectively, for all modulation indices and output current angles. It can be remarked that the number of switching transitions using the OTVB method practically matches the minimum theoretical values given in Table IV. In fact, the number of switching transitions is even lower in the simulation results. This is because some very narrow pulses are skipped in the process of simulation, and therefore, those switching transitions are not counted. On the other hand, a significant increase in the number of switching transitions is observed using the OSVB method.

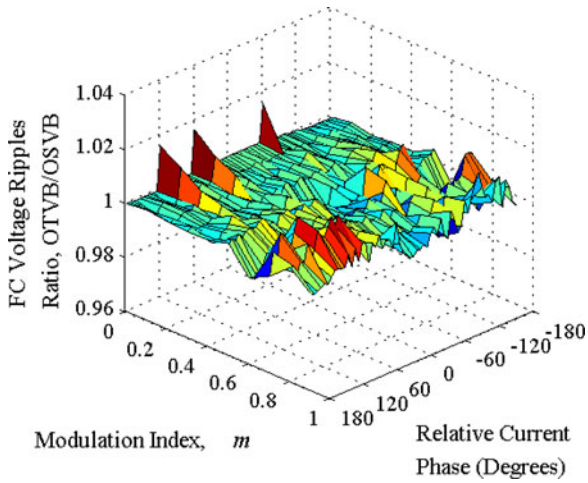


Fig. 7. FC voltage ripples ratio OTVB/OSVB.

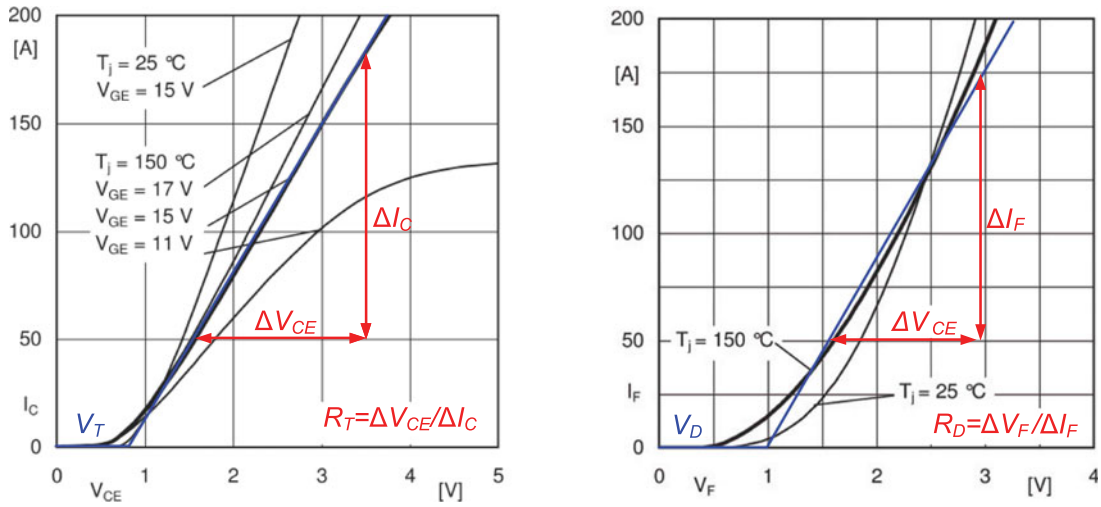


Fig. 8. SKM100GB12T4 power device characteristics: (a) $V_{\rm CE}$ versus I_C curves of the IGBT and (b) V_F versus I_F curves of the diode.

TABLE V
PARAMETERS OF THE LINEARIZED MODEL FOR THE CALCULATION OF CONDUCTION LOSSES

Parameter of the Linearized Model	Value
V_T (IGBT threshold voltage)	0.83 V
R_T (IGBT on-state resistance)	14.1 mΩ
V_D (Diode threshold voltage)	1 V
R_D (Diode on-state resistance)	11.43 mΩ

TABLE VI
$\rm E_{on}$, $\rm E_{off}$, AND $\rm E_{rr}$ POINTS

Curve	Current, $\rm I_C$ (A)	Energy(mJ)
$\rm E_{on}$	[25 50 100 150 200]	[3.57 7.14 15.18 35 55.36]
$\rm E_{off}$	[25 50 100 150 200]	[3.57 5.36 10.71 14.29 19.64]
$\rm E_{rr}$	[25 50 100 150 200]	[3.21 4.11 5.71 6.43 6.79]

TABLE VII
$\rm E_{on}$, $\rm E_{off}$, AND $\rm E_{rr}$ APPROXIMATION

Switching	Expression
$\rm E_{on}\,(\mu J)$	$\frac{V_{\rm off}}{600}(-0.0045\,I_C^3 + 2.7621\,I_C^2 - 121.5400\,I_C + 5556)$
$\rm E_{off}\,(\mu J)$	$\frac{V_{\rm off}}{600}(0.0010\,I_C^3 - 0.3183\,I_C^2 + 118.4000\,I_C + 579.2)$
$\rm E_{rr}\,(\mu J)$	$\frac{V_{\rm off}}{600}(0.00014\,I_C^3 - 0.1694\,I_C^2 + 52.1100\,I_C + 1979)$

Fig. 6(c) shows the switching transition ratio of OTVB over OSVB. It can be noted that there is a reduction of the switching transitions of about 5% for very high modulation indices. Such a reduction in the switching transitions is significantly larger (up to 35%) for modulation indices around 0.5.

Fig. 7 shows the FC voltage ripples ratio OTVB over OSVB. It can be noted that with the OTVB method the increase in the voltage ripples is very small (less than 2%) for all the operating conditions and modulation index range from 0 to 1.

In summary, using the OTVB method, a reduction of about 5% of the switching transitions in the power devices for high modulation indices can be achieved at the expense of slightly increasing the FC voltage ripples.

B. Power Losses in the Power Devices

In this section, the power losses associated with all the switches in the three-phase seven-level SMC are analytically estimated. The power device used in this study is the SKM100GB12T4 from SEMIKRON, rated at 1200 V and 100 A.

The power losses are classified into conduction and switching losses for both the transistors and freewheeling diodes. The power losses calculation method used in this paper is similar to the one discussed in [32]–[35], which is based on extrapolating the information from the manufacturer's data sheet for conduction ($V_{\rm CE}$ versus I_C) and switching curves (E versus I_C). For the calculation of the conduction losses, the curves of the devices (the transistors and freewheeling diodes) are linearized by an on-state resistance and a threshold voltage. Fig. 8(a) and (b) shows the estimation of the parameters for the insulated gate bipolar transistor (IGBT) and the freewheeling diode, respectively, using the device SKM100GB12T4 from SEMIKRON. The values of threshold voltage and the on-state resistance of the IGBT and the transistor are given in Table V. It is important to consider the junction temperature and the gate voltage. In this analysis, the gate voltage is assumed to be 15 V (typical gate driver voltage) and the worst case temperature of 150 °C is considered.

Once the parameters have been obtained, the conduction losses of the power devices, i.e., transistors and freewheeling diodes, can be approximated as

$$P_{\rm Cl\_T} = \frac{1}{T}\int_0^T (V_T + i_F\,R_T)i_F\,dt \qquad (11)$$

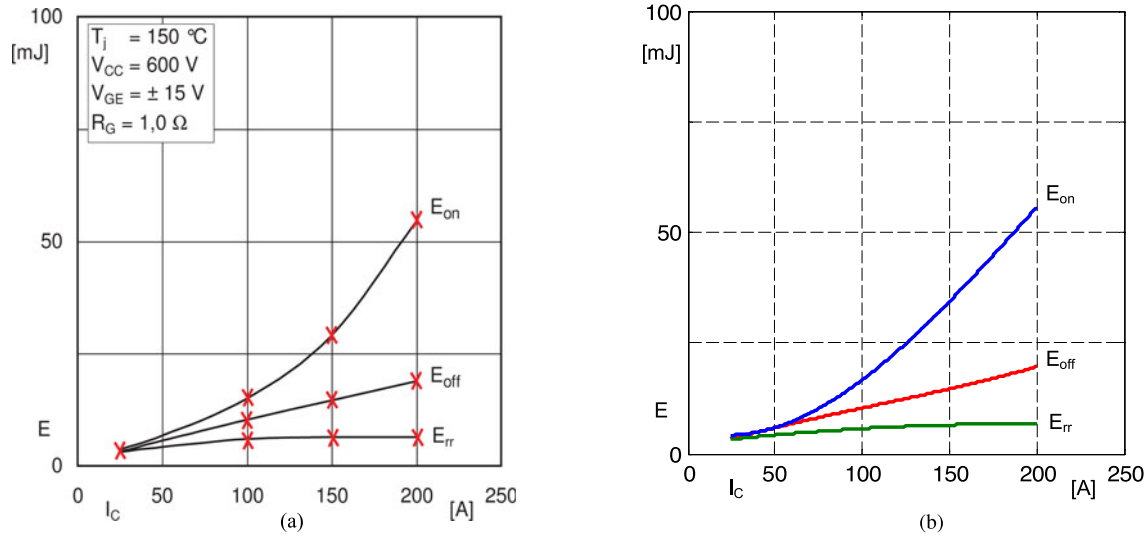


Fig. 9. SKM100GB12T4 power device–Switching Losses approximation: (a) (E versus I_C) curves from datasheet and (b) (E versus I_C) estimated curves.

$$P_{\mathrm{Cl\_D}} = \frac{1}{T}\int_0^T (V_D + i_F\, R_D) i_F\, dt \tag{12}$$

where $P_{\mathrm{Cl\_T}}$ and $P_{\mathrm{Cl\_D}}$ are the conduction losses of the transistor and diode, respectively, V_T and V_D are the threshold voltage of the transistor and diode, respectively, R_T and R_D are the on-state resistance of the transistor and diode, respectively, i_F is the forward current in the device (transistor and diode), and T is the period of the fundamental frequency.

For the calculation of the switching losses, the energy curves provided in the manufacturer's data sheet are approximated by using a MATLAB curve fitting tool (polyfit) [36]. The procedure is listed in the following steps:

1) *Step 1:* Extrapolate data points from the manufacturer's data sheet (E versus I_C) curves. An example is shown in Table VI, where some characteristic points have been selected.
2) *Step 2:* Using Step 1 along with a MATLAB curve fitting tool (polyfit) [36], an approximated curve is obtained. An example of estimated switching losses is shown in Table VII.
3) *Step 3:* The switching losses approximation equations obtained in Step 2 are checked with the original curves for verification. Fig. 9 shows the comparison of the original (E versus I_C) curves and the estimated (E versus I_C) curves.

Once the energy curves have been approximated, they are used to calculate the switching power losses at any transition. The switching losses for the transistor/diode can be calculated by

$$P_{\mathrm{sw\_T}} = \frac{1}{T}\sum_{j=1}^{nt} [E_{\mathrm{on}j}(i_F, v) + E_{\mathrm{off}j}(i_F, v)] \tag{13}$$

$$P_{\mathrm{sw\_D}} = \frac{1}{T}\sum_{j=1}^{nt} E_{rrj}(i_F, v) \tag{14}$$

where $P_{\mathrm{sw\_T}}$ and $P_{\mathrm{sw\_D}}$ are the switching losses of the transistor and diode, respectively, nt is the number of transitions in a fundamental period T, E_{on} and E_{off} are the energies dissipated during the turn-on and turn-off processes of the transistor, respectively. E_{rr} is the energy dissipated during the turn-off process of the diode. This information is available on the power device data sheet in the form of switching curves (E versus I_C). These values depend on the voltage v in the off-state and the current i_F in the on-state of the power device. According to the data sheet, the energy dissipated in the diode during the turn-on process is very small; therefore, it has been neglected in this study.

Fig. 10 shows the conduction power losses for the three-phase seven-level 3×2 SMC using OSVB and OTVB, respectively. As it can be observed, the conduction power losses are more or less the same for both methods.

Fig. 11 shows the switching losses for the three-phase seven-level 3×2 SMC when OSVB and OTVB are applied. All possible relative current phase angles and modulation indices have been considered in these representations. A zero sequence has been added to the modulation signals of the three-phase system to extend the range of the modulation index under linear operation mode [32]. Fig. 11(c) shows the switching losses ratio of OTVB over OSVB. This ratio is equal or lower than the unity for all the operating conditions, which means that OTVB produces lower switching losses than OSVB. The reduction is significant for modulation indices around 0.5 (about 35%). This is because the number of switching transition of the power devices is much lower with the OTVB since it avoids the use of nonoptimal transitions.

Fig. 12 shows the total power losses (conduction and switching losses) for the three-phase seven-level 3×2 SMC when OSVB and OTVB are applied. Fig. 12(c) shows the ratio of the total power losses of OTVB over OSVB. As it can be observed, this ratio is equal or lower than the unity for all the operating conditions, which means that OTVB produces lower total power

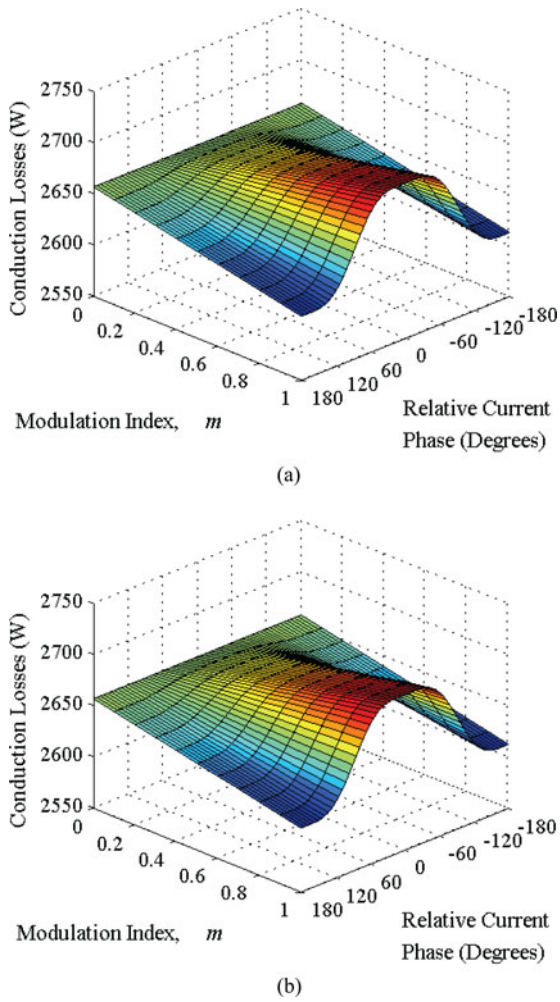


Fig. 10. Conduction power losses in a three-phase seven-level 3×2 SMC using: (a) OSVB and (b) OTVB.

losses than OSVB. This is because the switching transitions of the power devices is significantly lower (up to 35%) for modulation indices around 0.5, when applying OTVB. The results also show that the slightly increase in the capacitor voltage ripples when OTVB is applied does not have a significant impact on the power losses of the converter. This is because the voltage ripples are relatively small when compared to the average capacitor voltage values.

C. Computation Burden

In order to estimate and compare the computation burden for both methods, OSVB and OTVB, the number of cost function calculations that need to be performed in a phase-leg of seven-level SMC are determined and shown in Table VIII. For a fair comparison, one cost function calculation is associated to a single switching state. For example, in the case of OTVB and when switching between the levels $V_{\rm dc}/6 \rightarrow V_{\rm dc}/3$ (see Fig. 3), if the original state is 001000{8}, two optimal transitions for the level $V_{\rm dc}/3$ are available, i.e., switching to the states 011000{24} or 101000{40}. In addition, the returning transition to the original level $(V_{\rm dc}/6)$ has to be considered. In other words, the optimal transitions available are

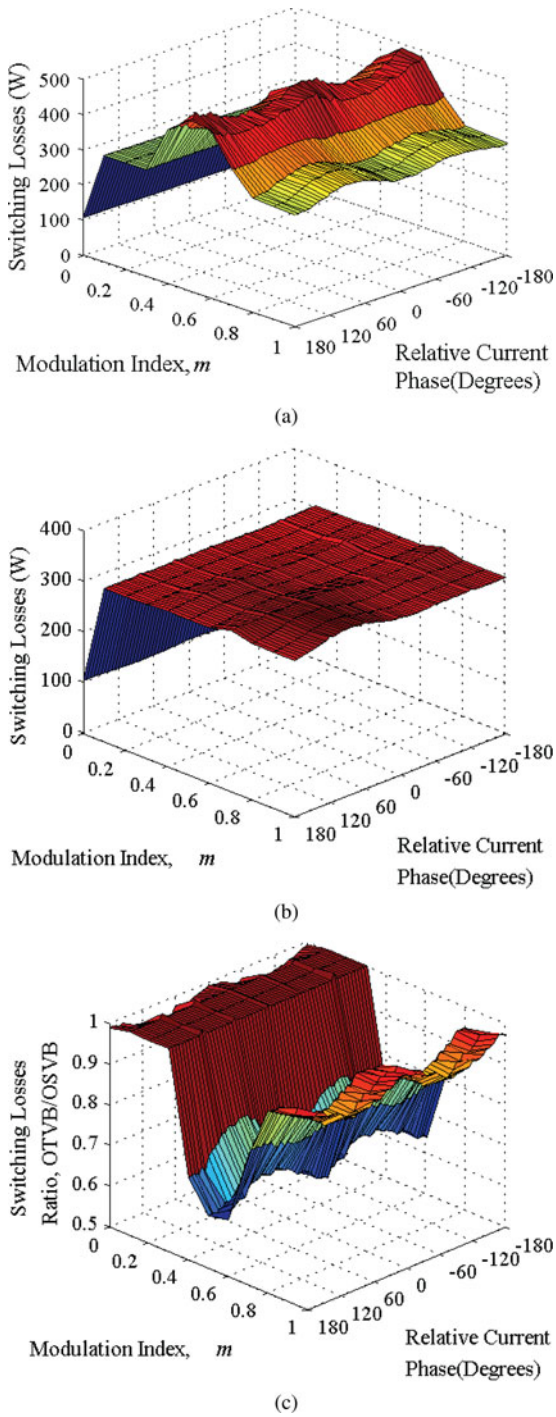


Fig. 11. Switching power losses of a three-phase seven-level 3×2 SMC using: (a) OSVB, (b) OTVB, and (c) Ratio of OTVB over OSVB.

001000{8}–011000{24}–001000{8}, 001000{8}–011000{24}–010000{16}, 001000{8}–101000{40}–001000{8}, and 001000{8}–101000{40}–100000{32}. Therefore, the cost function has to be calculated for the switching states 001000{8}, 010000{16}, 011000{24}, 100000{32}, and 101000{40}, i.e., five switching states in total. The final value of the cost function is calculated by adding the individual switching state cost function values weighted by the duty cycles of each voltage level according to 4. In the case of OSVB,

TABLE VIII
NUMBER OF CALCULATIONS OF THE STATE COST FUNCTION IN A SEVEN-LEVEL 3×2 SMC

	Transitions of the Output Voltage, $\mathbf{v_{x0}}$					
	$0 \leftrightarrow V_{\rm dc}/6$	$V_{\rm dc}/6 \leftrightarrow V_{\rm dc}/3$	$V_{\rm dc}/3 \leftrightarrow V_{\rm dc}/2$	$V_{\rm dc}/2 \leftrightarrow 2V_{\rm dc}/3$	$2V_{\rm dc}/3 \leftrightarrow 5V_{\rm dc}/6$	$\mathbf{5}V_{\rm dc}/6 \leftrightarrow V_{\rm dc}$
OSVB	4	6	4	4	6	4
OTVB	4	5	4	4	5	4

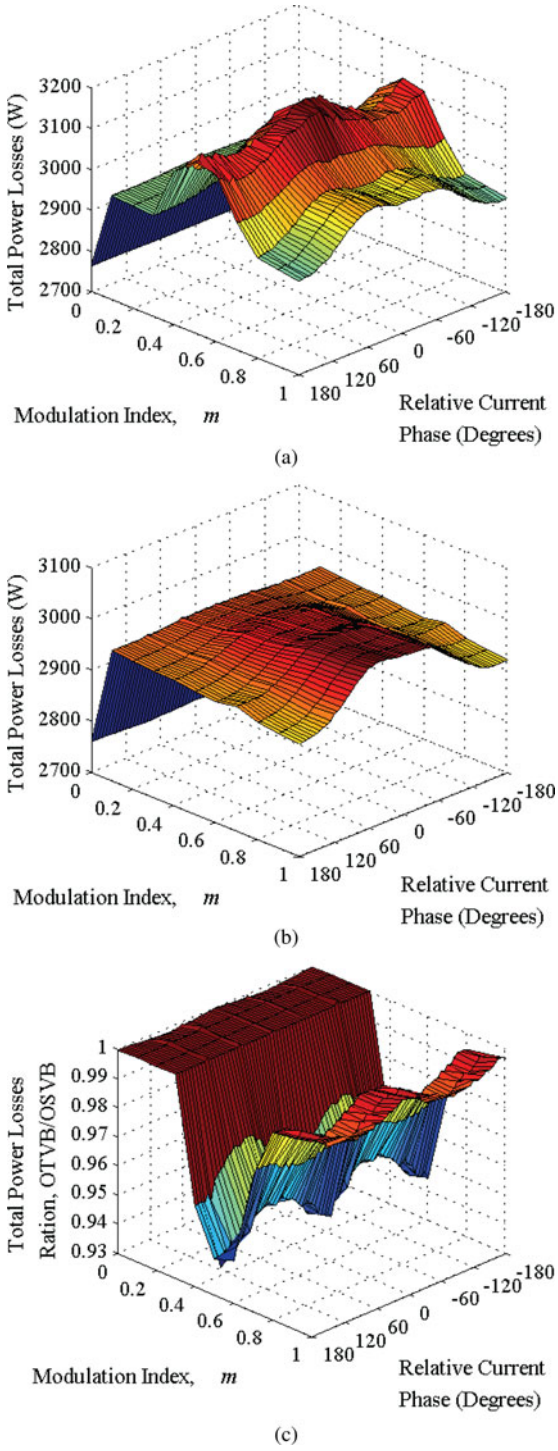


Fig. 12. Total power losses of a three-phase seven-level 3 × 2 SMC using: (a) OSVB, (b) OTVB, and (c) Ratio of OTVB over OSVB.

TABLE IX
SMC CONVERTER PARAMETERS

Circuit Parameter	Value
DC Bus Voltage, $V_{\rm dc}$	100 V
DC Bus Capacitors (C_1 and C_2)	6000 μF
FCs, C_{x11}, C_{x12}, C_{x21}, and C_{x22}	220 μF
Linear Load, RL	R=22 Ω, L= 6 mH
Nonlinear Load (Three-Phase Rectifier with RC)	R=44 Ω, C= 30 μF
Carrier Frequency, f_s	5 kHz
Fundamental Frequency, f	50 Hz

the number of calculations of the cost function is the same as the number of redundant switching states involved in the levels $V_{\rm dc}/6$ and $V_{\rm dc}/3$, which is six in this example. Table VIII shows the number of switching state cost function calculations to be performed with OSVB and OTVB. One can conclude that OTVB requires less computational effort than OSVB.

V. SIMULATION AND EXPERIMENTAL RESULTS

Simulation and experimental tests have been performed on a three-phase seven-level 3 × 2 SMC. The converter has been simulated using MATLAB/Simulink [36] and PLECS Toolbox [37]. The converter prototype is shown in Fig. 13. The dc bus is generated by two dc voltage sources connected in series of $V_{\rm dc}/2$ each of them together with dc bus capacitors, providing the neutral-point connection. The parameters of the converter are shown in Table IX. The proposed voltage balancing method has been implemented using a DSPACE 1006 with integrated DS 5203 FPGA board. This offers modular design flexibility for the control. The main components are shown in Fig. 14. The control is further divided into several components, which are as follows:

1) a computer that uses Control Desk real-time interface software provided by DSPACE; this software communicates with the DS1006 processor;
2) a DSPACE 1006 processor, which is also responsible for the communication with the DS5203 FPGA and DS2004 A/D boards;
3) a DS5203 FPGA board used to generate high speed PWM signals through a digital output port;
4) a DS2004 A/D high-speed board used to convert the measured signals from analog to digital; the digital signals are further processed by the DS1006 processor and send to the computer for data acquisition.

The performance of the proposed voltage balancing method operating with a linear load (RL) is shown in Fig. 15. The

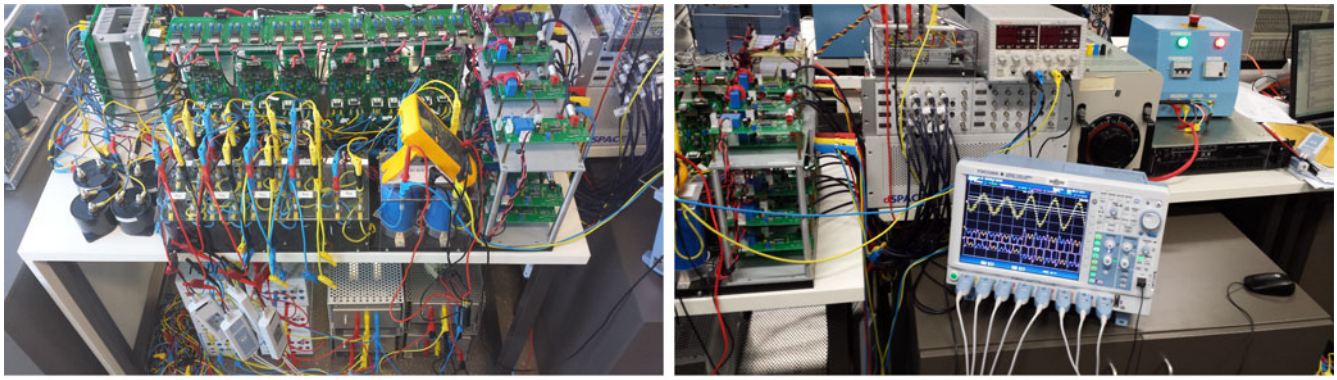


Fig. 13. Hardware prototype: (a) three-phase seven-level 3×2 SMC and (b) control hardware based on a dSpace unit.

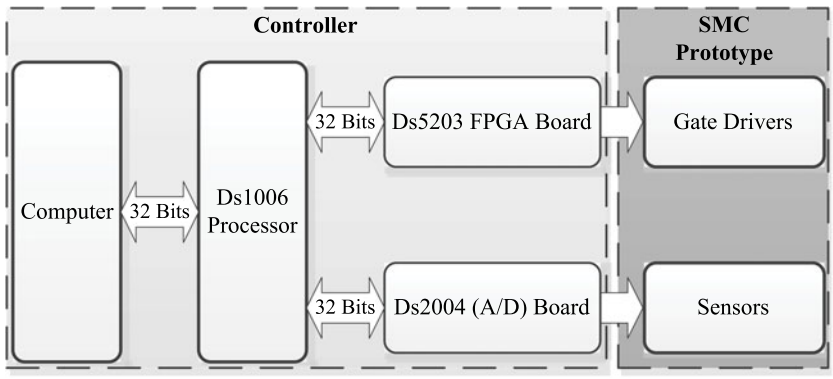


Fig. 14. Architecture of the digital controller.

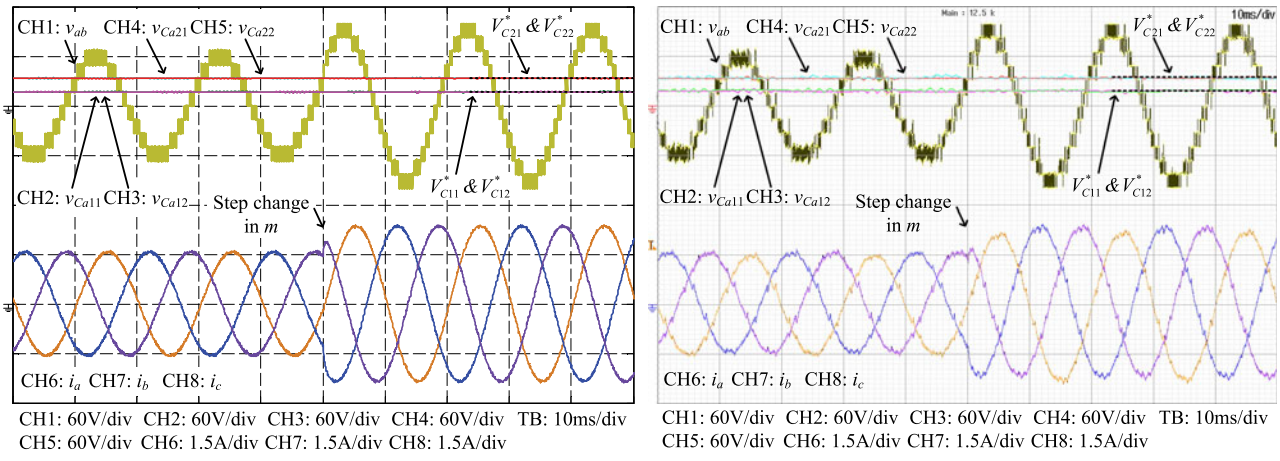


Fig. 15. Proposed voltage balancing method applied to a seven-level 3×2 SMC operating with a linear load (RL). At t=50 ms, the modulation index changes from $m = 0.6$ to $m = 0.9$. The waveforms presented are a line-to-line voltage, the FC voltages, and the load currents: (a) simulation and (b) experimental results.

line-to-line voltage v_{ab} and the FC voltages ($v_{Ca\,11}$, $v_{Ca\,12}$, $v_{Ca\,21}$, and $v_{Ca\,22}$) obtained from simulations are shown in Fig. 15(a). Initially the converter is in the steady-state condition, i.e., the FC voltages are at the reference values ($v_{Ca\,11} = 16.67$ V, $v_{Ca\,12} = 16.67$ V, $v_{Ca\,21} = 33.33$ V, and $v_{Ca\,22} = 33.33$ V). At $t = 50$ ms, there is a step change in the modulation index from $m = 0.6$ to $m = 0.9$. It can be seen that during this transient, the voltages in the FCs remain unaffected. A similar behavior can be observed during the same transient condition in the experimental results shown in Fig. 15(b). Fig. 15(a) and (b) also shows the load currents from simulations and experimental results, respectively. The proposed voltage balancing method proves to be robust

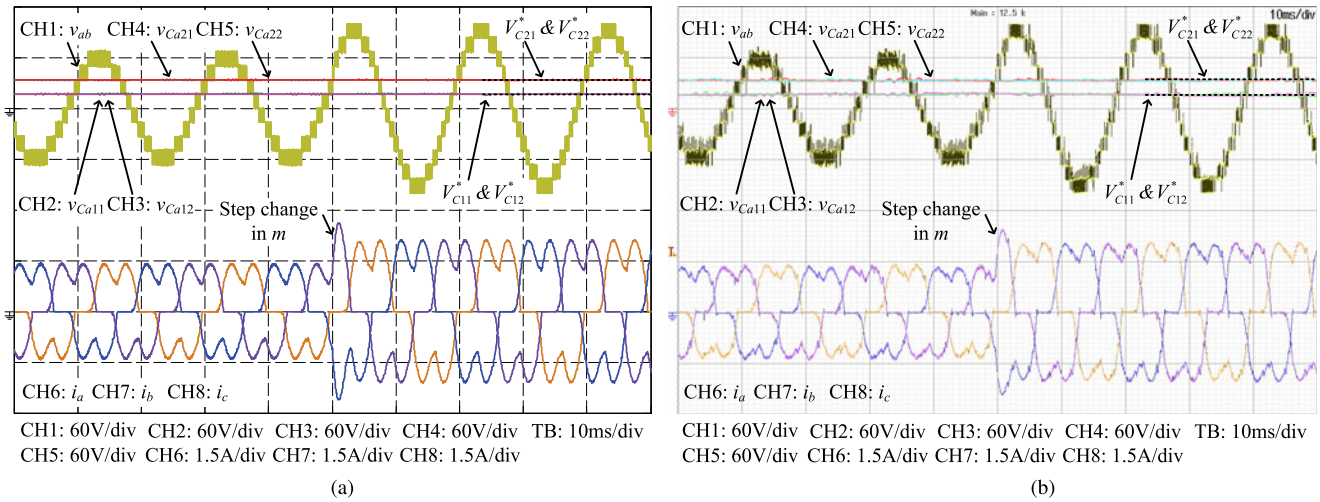


Fig. 16. Proposed voltage balancing method applied to a seven-level 3×2 SMC operating with a non-linear load. At t=50 ms, the modulation index changes from $m = 0.6$ to $m = 0.9$. The waveforms presented are a line-to-line voltage, the FC voltages, and the load currents: (a) simulation and (b) experimental results.

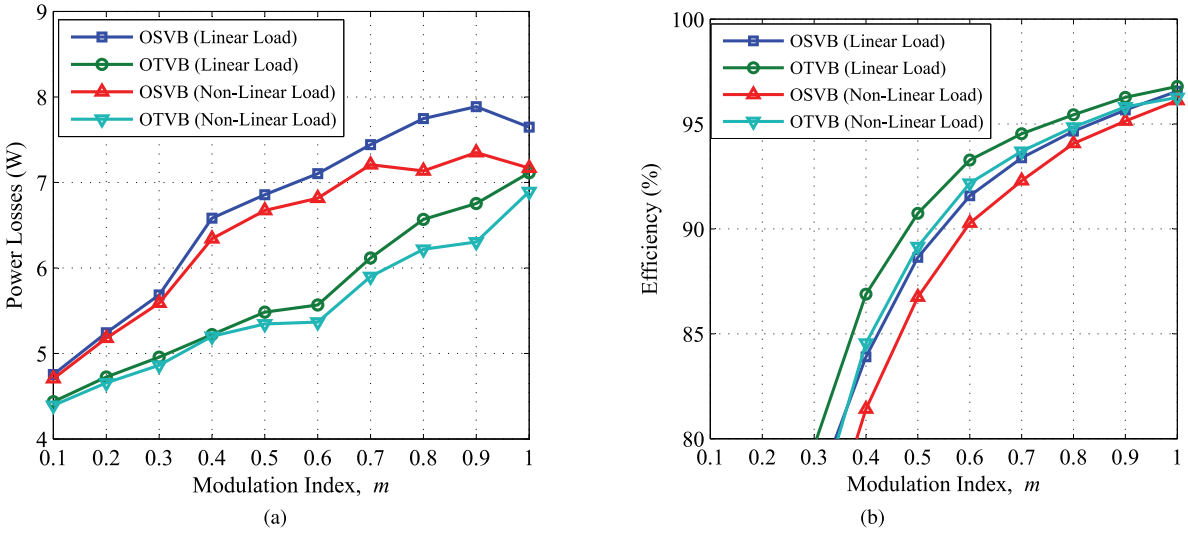


Fig. 17. Power analysis of the three-phase seven-level 3×2 SMC from experimental prototype: (a) power losses and (b) efficiency.

under modulation index changes when operating with a linear load.

The performance of the SMC operating with a nonlinear load is shown in Fig. 16. A three-phase diode rectifier with a dc-side filter capacitor of 30 μF and load resistor of 44 Ω, is used as a nonlinear load. The performance of the proposed voltage balancing method is verified by simulation and experiment. At $t = 50$ ms, the modulation index changes from $m = 0.6$ to $m = 0.9$. Observe that during this process, the FC voltages maintain the desire reference value in both cases, i.e., simulation [see Fig. 16(a)] and experimental [see Fig. 16(b)] tests. As expected, the currents are highly distorted and they increase with the modulation index. The proposed voltage balancing method is very robust operating with this strong nonlinear load and modulation index changes, since the FC voltages are maintained at their reference values at all times.

Fig. 17(a) shows the power losses of the seven-level 3×2 SMC for the linear and nonlinear loads (as shown in Table IX). The power analyzer device used in this experiment is Yokogawa WT3000. As observed from Fig. 17(a), the power losses using the OTVB method for both loads (linear and nonlinear) are lower when compared to the OSVB method. This is because in the OTVB, the nonoptimal transitions that produce higher switching frequencies are skipped and only the optimal ones are selected. As a result, lower switching frequency is produced, providing lower power losses.

Fig. 17(b) shows the efficiency of the experimental SMC prototype for the two different loads, i.e., linear and nonlinear (as shown in Table IX). It can be seen that the efficiency of the converter improves using the OTVB method when compared with the OSVB one for both loads. The efficiency improvement in this laboratory prototype is in the range of 2–4% for low

modulation indices ($m < 0.6$) and in the range of 0.5–2% for high modulation indices ($m > 0.6$). Hence, the proposed OTVB method reduces the power losses, and therefore, increases the overall efficiency of the converter.

The proposed voltage balancing method has also been tested with unbalanced loads (not included in this paper). It also performs very well under such conditions. This is because the cost function that selects the optimal transitions is calculated independently for each phase of the converter, therefore, there is no interaction among the phases.

VI. Conclusion

This paper has presented a voltage balancing method for SMCs using reduced switching transitions. The method is based on calculating a cost function considering the FC voltage deviations and the output currents. The proposed cost function evaluates only those redundant transitions between consecutive voltage levels that produce minimum switchings. The one that gives the lower value to the cost function is selected and applied to the converter. The proposed method has been implemented in a seven-level 3×2 SMC and tested against linear and nonlinear loads, and transients. It performs very well in regulating the FC voltages to the desired levels. The results have been compared with a modulation method that does not avoid nonoptimal transitions and optimizes switching states instead of transitions, i.e., OSVB. The results show that for high modulation indices, the switching transitions of the power devices are reduced by about 5% when using the proposed OTVB method. Consequently, the total power losses are also reduced, which also improves the efficiency of the converter. This reduction comes at the cost of slightly increasing the FC voltage ripples.

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