Investigating a MOSFET Driver (Buffer) Circuit Transition Ringings Using an Analytical Model

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***Abstract*—In this paper, a new analytical model introduced extracting from datasheet of a MOSFET and developed a MATLAB code for simulating a MOSFET driver circuit is proposed in the literature to observe the ringings of its output for capacitively loaded case. The output waveform is studied only for high-to-low transition. Gate drive resistance, wiring parasitics of the printed circuit board layout, and the characteristic properties of the MOSFET affect both the delay time of the MOSFET to become ON and performance of the driver circuit. Also, voltage stress of the MOSFET and therefore safe operating range for the circuit all depend on these effects. These effects are all considered in the design stage. The simulation results obtained from CST Design Studio software are compared with the results of experimental work. The analytical modeling results solved in the MATLAB are found congruent with the simulation results and experimental results as well. The simulation work showed that developed MATLAB code along with extracted models from datasheets has less convergence problems and also requires less simulation time.**

***Index Terms*—CMOS buffer circuit, gate drive resistance, MOSFET modeling.**

I. Introduction

CHOOSING a semiconductor switching element and managing the circuit wiring parasitics are important points to decrease the losses and thus increasing the switching performance of switched-mode power conversion. MOSFETs are commonly used as fast switching elements due to the low on-state losses depending on the low on-state resistance and fast switching speed because of the majority carrier devices [1], [2]. Although they are preferred as switching elements, the unfavorable effects of the three interelectrode capacitances, the inductances of the drain and source leads, and the (distributed) resistance of the gate of the MOSFET should be taken into consideration during the design phase of a circuit.

Higher switching frequency of the power processing circuits (converters, inverters) is preferred nowadays because of the smaller circuit size, lower cost, and higher power density. Turn-on and turn-off times for a switching element should be low to achieve higher switching frequencies. For this reason, higher voltage and/or current changing rates and thus wiring parasitics may have prominence effect on switching waveforms. On the other hand, high switching losses, current/voltage stresses, possible oscillations during the transitions and high electromagnetic interference (EMI) caused by high current and voltage peaks during switching actions are inevitable failures in consequence of the switching frequency increment.

To overcome these failures, the circuit should be analyzed and possible overvoltages and overcurrents should be observed in the design stage before the implementation. Even though the precise calculation is necessary for estimating working waveforms, it may not give exact results for the analysis, especially during transitions. What is really important is to consider the effect of both characteristics of the elements used in the circuit and parasitics caused by the connecting wires for analayzing the circuit behavior and losses, unless circuit parasitics are taken into account [3]–[14]. The effect of the MOSFET parasitic capacitances and inductances, circuit stray inductances, and reverse current of the freewheeling diode and switching performance in a test circuit with an inductive load is given in [3] and in a buck converter is given in [4]. The switching operation of a half-bridge converter with parasitic elements is developed by an analytical model and verified with both simulation and experimental results in [13]. The effect of the parasitic elements in a boost converter with RCD snubber configuration is modeled analytically and compared with simulation and experimental results and offer an optimum design with MOSFET snubber diode configuration in [6]. Analytical model for a buck converter with a current source driver is investigated and verified with simulation and experimental results in [10] and [14]. An improved layout, by rearranging the location of supply decoupling capacitance for minimizing the effective loop inductance, is proposed in [14].

As known, SPICE programs may exhibit convergence problems. The situation has become worsened when working pulse-type waveforms in the circuit including semiconductor devices. Relative accuracy of all voltage and currents is increased and the absolute current error tolerance is set to a value to the tolerable limits to solve the convergence problems in these programs [15]. In this paper, analytical model of a buffer circuit is developed and then solved in MATLAB by using a type of the iterative method called the Runga Kutta method for the purpose of obtaining a different point of view. Linear devices capacitances are used instead of nonlinear capacitances in this proposed model. Also, the analysis is fulfilled by using first-order differential equations, since discontinuties for the currents occur while making analysis with second-order differential equations in MATLAB.

The aim of this paper is to obtain design considerations of the driver circuit of Fig. 1 for achieving less output voltage and current ringings when output is loaded with a capacitor. In

Manuscript received June 8, 2014; accepted October 16, 2014. Date of publication October 30, 2014; date of current version April 15, 2015. This work was supported by The Scientific and Technological Research Council of Turkey (TUBITAK), under Project # 112E258. Recommended for publication by Associate Editor A. Lindemann.

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Digital Object Identifier 10.1109/TPEL.2014.2366431

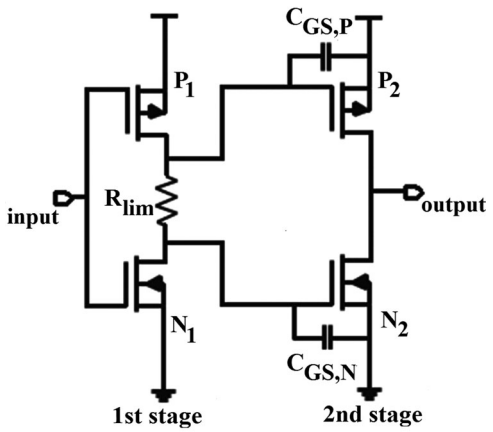

Fig. 1. Partly analyzed CMOS buffer circuit, the transistor N_2 behavior is analyzed for output transition high to low, load, and is assumed a simple capacitor element with an initial charge of Q.

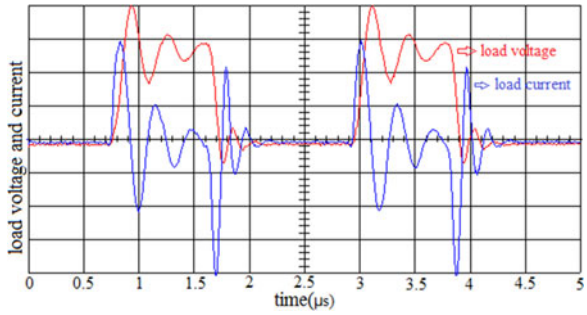

Fig. 2. Practical waveforms of MOSFET driver (buffer) circuit, output voltage waveform 5 V/div (red one), load current waveform measured with P6022 current probe 1 A/div (blue one).

fact, this capacitor represents the Miller input capacitance of the driven MOSFET; here, to simplify the operation and to get better insight on the parasitics caused ringings along with actually connected devices, a ceramic capacitor of 10 nF is used as load. Beside this, effect of the gate resistance on the switching waveforms is studied by using analytical, simulation, and experimental techniques. The modeling and simulation technique proposed here poses less convergence problems when today's SPICE packages used along with manufacturers SPICE models. The reason is that device parasitic capacitances were handled as constant-valued capacitances. Although this approach may introduce some errors on simulation results, simulation works in the proposed driver circuit. It is concluded that for this application, the difference in results obtained by using a SPICE package and proposed technique is not much. On the other hand, the proposed technique requires less computational time while having significantly less convergence problems.

II. Topology of the CMOS Buffer Circuit

There are several circuit topologies for amplifying the input current and obtaining enough driving current for fast switching of a MOSFET element. A comparison of performances of the various buffer driver circuits and schematics is given in [16]. CMOS buffer structure for the purpose of high-speed driving large MOSFETs shown in Fig. 1 is suggested in that paper as well. The practical work performed that this topology gives very promising results as claimed in the literature [16]. The experimental work also shows that this buffer circuit is very robust when compared with the commercial high current ultrafast MOSFET driver ICs.

In Fig. 1, $C_{\mathrm{GS},N}$ and $C_{\mathrm{GS},P}$ are the internal gate–source capacitances of the MOSFETs. R_{lim} is the limiting resistor. When input voltage of the circuit seen in Fig. 1 becomes high, P_1 reaches turn-off state and N_1 becomes ON. Therefore, N_2 becomes OFF and P_2 becomes ON. On the other hand, when low voltage (below threshold voltage level) is applied to the input of the circuit, N_1 becomes OFF and P_1 becomes ON with a delay time determined by the time constant $\tau_1 = R_{\mathrm{lim}} C_{\mathrm{GS},P}$. Consequently, P_2 becomes OFF and N_2 becomes ON after a delay time determined by time constant $\tau_2 = R_{\mathrm{lim}} C_{\mathrm{GS},N}$. These time delays are provided by the resistor R_{lim} together with the equivalent gate capacitances of the MOSFETs starting to conduct. In this paper, the reasons of the turn-on delay and especially the effect of the gate drive resistance are investigated when output stage becomes zero.

This circuit is demonstrated in the laboratory and gives excellent switching times as seen in Fig. 2 even though the switching frequency is about 450 kHz. In Fig. 2, the circuit is capable of obtaining acceptable driving waveforms up to 800 MHz with a load consisting of a 10 nF ceramic capacitor again. The ringings, however, were high and by analyzing and simulating this circuit topology we aimed to understand the circuits' operation better and possibly mitigate the ringings. In this paper, transition of the high-side MOSFET from ON to OFF and low-side MOSFET from OFF to ON of the second stage of the buffer is analyzed by considering the MOSFET characteristics and wiring inductances of the loads and also the effect of the gate drive resistance is especially emphasized. A detailed new simulation model was established using MATLAB; another simulation is also performed by using CST Design Studio software, and finally practical results of the circuit are compared with analytical and simulation results. Additionally, the same implementation circuit is set up with different gate drive resistances and checked against the performance of the circuit.

This buffer circuit is analyzed for low-to-high input transition case only. The output load here is assumed to be a constant capacitance of the driven MOSFET by this buffer circuit. Actually, this capacitance value changes with the time during transition in intended application of this circuit; it is here assumed to be constant as 10 nF for simplification purpose.

III. Equivalent Circuit Model of the Buffer Circuit for the High-to- Low Input Transition

When upper side P_2 MOSFET of Fig. 1 is turned OFF, which is expected to be very fast since no or very low gate driving resistance (in fact R_{ds} of the P_1 MOSFET), lower side MOSFET N_2 is expected to start turning on later and somehow slowly since R_{lim} resistor acts as a gate driving resistance at this instant.

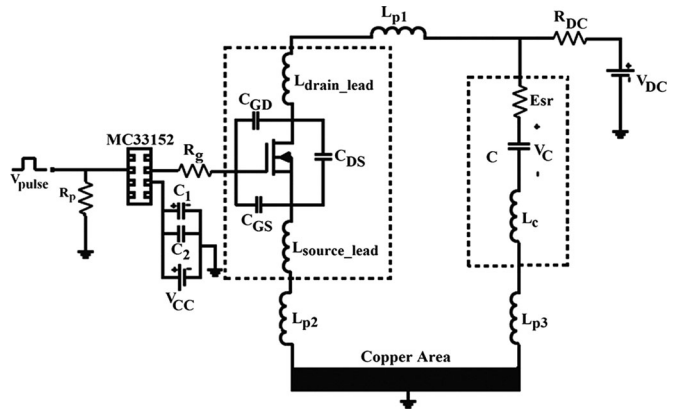

Fig. 3. Buffer circuit's second stage's model for its output transition 1 to 0, here actually the MOSFET device seen is the N_2 transistor of Fig. 1.

Gate resistance allied with gate–source capacitance affects the charge and discharge times of the MOSFETs. This effect plays an important role in determining the delay time of the MOSFET to become ON. On the other hand, output capacitor keeps the dc voltage constant at this transition time interval.

A simplified equivalent circuit of the buffer circuit for considering only N_2 MOSFET transition with parasitic elements could be constructed as seen in Fig. 3. Here, the transistor shown in figure is N_2 of the previous circuit of Fig. 1. Clock pulse with 100 kHz frequency is applied to the input of the MOSFET driver of the circuit of Fig. 3. This circuit is implemented using an IRF540Z power MOSFET. Parameters and abbreviations used in analysis for this MOSFET are given in Table I. A commercial predriver IC is used to drive the circuit of Fig. 3. The input signal of this predriver is provided by a laboratory signal source via a twin cable whose characteristic impedance (Z_0) is around $220\,\Omega$ .To suppress the ringings of the cable far end is loaded with a R_p as seen in Fig. 3 and value of this resistor is selected as $220\,\Omega$. Stray inductance can be calculated as given in the literature [17], and are chosen 8 nH/cm for the analyzed circuit layout. The parameters of the MOSFET related to turn-on and turn-off behavior have been read from the datasheet. The $R_{\rm g}$ resistor of Fig. 3 actually represents the $R_{\rm lim}$ component of Fig. 1.

$L_{\rm source\_lead}$: Internal source inductance.
$L_{\rm drain\_lead}$: Internal drain inductance.
R_g : Driver external resistance + driver internal resistance.
L_{p1} : Parasitic inductance of the wire from drain lead to the capacitor positive lead.
L_{p2} : Parasitic inductance of the wire from source lead to the ground.
L_{p3} : Parasitic inductance of the wire from capacitor negative lead to the ground.
$E_{\rm sr}$: Equivalent series resistance.
L_c : Equivalent series inductance.
$V_{\rm CC}$: DC supply voltage.
C_1, C_2 : DC supply capacitors.

TABLE I
PARAMETERS AND ABBREVIATIONS USED IN ANALYSIS

Parameters	Abbreviations of the parameters	Values
Switching frequency	$f_{\rm sw}$	100 kHz
Pulse voltage	$V_{\rm pulse}$	20 V
Electrostatic resistance of capacitive load	$E_{\rm sr}$	0.18 Ω
Electrostatic inductance of capacitive load	L_C	1 nF
Capacitive load	C	10 nF
Gate–drain capacitance of MOSFET ($V_{\rm DS}$ = 23 V)	$C_{\rm GD}$	111 pF
Gate–drain capacitance of MOSFET ($V_{\rm DS}$ = 23 V)	$C_{\rm GS}$	1770 pF
Gate–drain capacitance of MOSFET ($V_{\rm DS}$ = 23 V)	$C_{\rm DS}$	166 pF
Gate–drain capacitance of MOSFET ($V_{\rm DS}$ = 1 V)	$C_{\rm GD2}$	330 pF
Gate–drain capacitance of MOSFET ($V_{\rm DS}$ = 1 V)	$C_{\rm GS2}$	1770 pF
Gate–drain capacitance of MOSFET ($V_{\rm DS}$ = 1 V)	$C_{\rm DS2}$	400 pF
Forward transconductance (cut-off region)	$g_{\rm fs}$	0
Forward transconductance (saturation region)	$g_{\rm fs1}$	1 S
Internal gate resistance	$R_{g\_\rm int}$	6 Ω
Internal drain inductance	L_d	7.5 nH
Internal source inductance	L_s	4.5 nH
Threshold voltage of MOSFET	$V_{\rm th}$	3.2 V
MOSFET drain–source on resistance	$R_{\rm ds\_on}$	0.15 Ω

The circuit shown in Fig. 3 is implemented by using surface mount components in order to reduce the layout parasitics and thus EMI and losses. Load capacitor's parasitics are considered while performing the analysis. A dc voltage source as seen in Fig. 3 is connected through a resistor ($R_{\rm DC}$) so as to generate initial dc voltage value for the output capacitor. The value of $R_{\rm DC}$ is chosen as $250\,\Omega$ by taking following considerations.

1) It provides a reasonable charging time along with load capacitance value *C*.
2) When the MOSFET of Fig. 3 starts to conduct, nearly almost MOSFET drain current comes from the charged load capacitor then by limiting the current provided by $V_{\rm DC}$ in the transition interval.

IV. PARAMETERS USED IN ANALYSIS

Although obtaining more accurate results dictates taking into all account wiring parasitics and more detailed component models, for the sake of simplification, the following assumptions are made.

1) Forward transconductance and drain–source resistance of the MOSFET are taken as constant [3]. In fact, this resistance is varied with gate–source voltage of the MOSFET as shown in the manufacturer's datasheet [18].
2) Actually, it is seen that reverse recovery effect is a negligible parameter in this circuit. In fact, the cause of the oscillations is the leakage result of the inductance in the circuit. This situation limits the reverse recovery current.

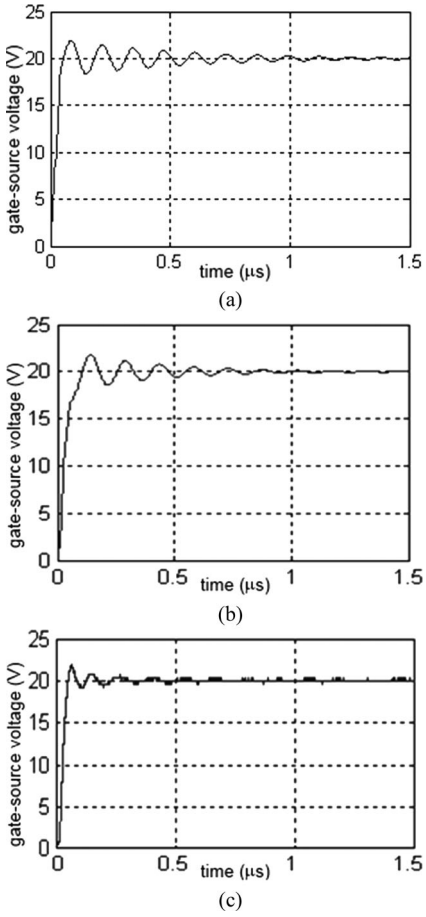

Fig. 4. Waveforms of $V_{\rm GS}$ (V) of the N_2 MOSFET for low to high with 2.2 Ω gate resistance. (a) CST Design Studio result. (b) Proposed model result. (c) Experimental result (500 ns/div, 5 V/div).

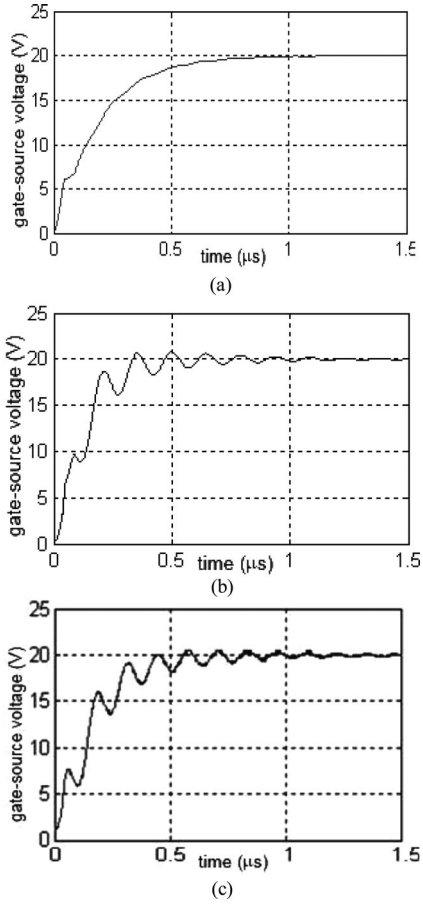

Fig. 5. Waveforms of $V_{\rm GS}$ (V) of N_2 of Fig. 3 for low to high with 47 Ω gate resistance. (a) CST Design Studio result. (b) Proposed model result. (c) Practically obtained results (500 ns/div, 5 V/div). Note that proposed model and developed code simulation gives more realistic results.

Additionally, the current which flows over parasitic diode is again limited because MOSFET's channel region is in its conduction mode. Because of these two reasons, reverse recovery current is not taken into account. Also, the simulation and experimental results prove that this assumption is correct.

3) Layout stray capacitances and stray resistances are neglected.
4) Stray inductance of the MOSFET gate path is neglected since driver-integrated circuit is placed to the gate resistor (R_g) as close as possible to minimize the oscillations caused by this parasitic inductance.

$$\text{Forward transconductance} = g_{\rm fs} = \left.\frac{di_d(t)}{dv_{\rm GS}}\right|_{V_{\rm DS}=\text{constant}}.$$

And, obtained from $V_{\rm GS}$ and I_d graph. For cut-off region, $g_{\rm fs}$ is taken zero value since no current is flowing through the drain of the MOSFET.

Drain–source resistance R_d of the MOSFET is obtained from drain-to-source current graph.

In the model circuit of Fig. 3, the capacitor *C* is represented with its parasitic resistance and inductance.

V. Analytical Model of the Switching Behavior of a MOSFET With Capacitive Load

Three techniques generally used for predicting and verifying the performance of a circuit: simulation, experimental, and analytical methods. In this paper, all these techniques are used and the results of them are compared.

In this part, the analytical approach is followed when the lower side MOSFET N_2 becomes ON.

Turn-on switching transition of a MOSFET switch could be divided into three regions:

Region 1: Eventhough gate signal is applied to the MOSFET, MOSFET is in cut-off region till the gate–source voltage value passes the threshold voltage level. Drain voltage is equal to capacitor's initial voltage, and no current flows. Input capacitance of the gate terminal begins to charge up in this period. Input capacitance when drain and source terminals are shorted is equal to the gate–source capacitance and gate–drain capacitance. If the internal source and drain inductances and parasitic inductances are neglected, the gate–source voltage $V_{\rm gs}$ is equal to the

$$V_{\rm GS} = V_{\rm pulse}[1 - e^{-(t_1 - t_0)/\tau}] \quad \tau = R_g(C_{\rm GS} + C_{\rm GD}) \quad (1)$$

where $R_g = R_{\rm gate\_resistance} + R_{g\_\rm int}$ and $R_{g\_\rm int}$ is the internal resistance of the MOSFET. However, source lead and parasitic

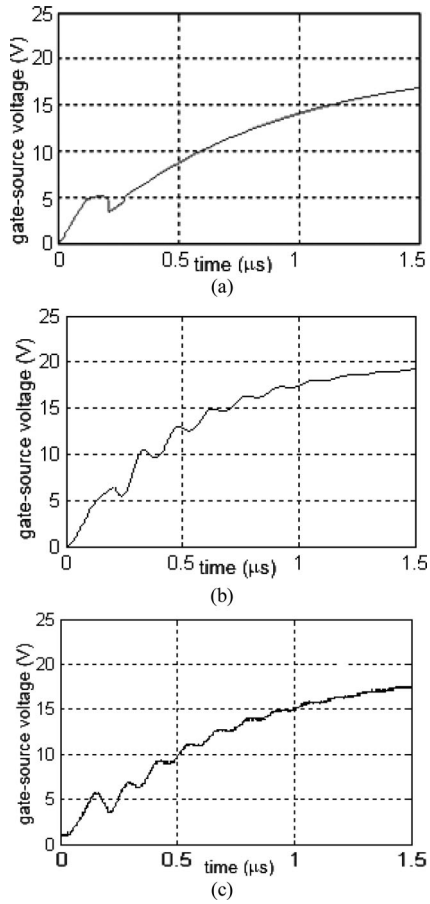

Fig. 6. Waveforms of $V_{\rm GS}$ (V) of N_2 of Fig. 3 for low to high with 220 Ω gate resistance. (a) CST Design Studio. (b) Proposed model result. (c) Implemented result (500 ns/div, 5 V/div). Note that the proposed model and developed code simulation give more realistic results.

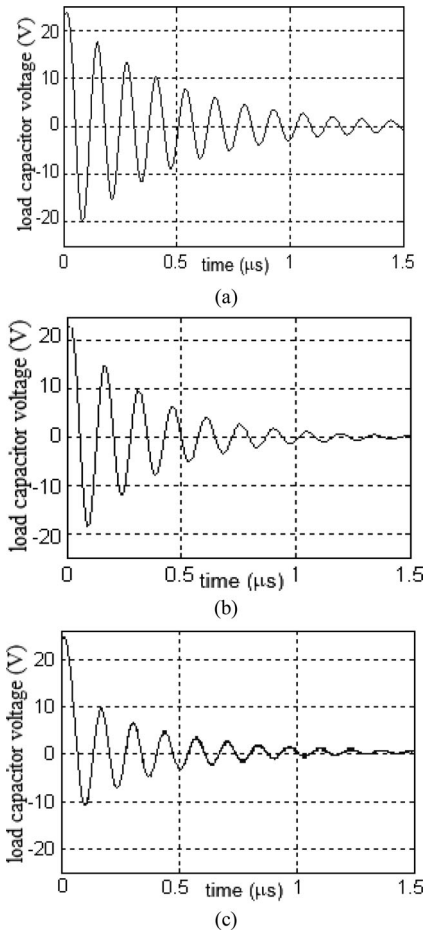

Fig. 7. Load capacitor voltage waveform with 2.2 Ω gate resistance. (a) CST Design Studio result. (b) Proposed model and MATLAB code results. (c) Practically obtained result (500 ns/div, 10 V/div).

inductances should be taken into account even if the circuit is in cut-off region. Current will flow through these inductances during charging of the gate–source capacitance. This current flow takes more time to turn on the MOSFET.

Regions 2 and 3: When $V_{\rm gs}$ reaches the threshold level, MOSFET begins to conduct, drain current (i_d) starts to increase, and drain–source voltage starts to decrease. The load capacitor voltage begins to decrease from its initial charged voltage level as well.

When Kirchoff's current law is applied to the gate, drain, and source of the MOSFET of Fig. 3, current equations can be written as follows:

$$i_g(t) = C_{\rm GD}\frac{dv_{\rm GD}}{dt} + C_{\rm GS}\frac{dv_{\rm GS}}{dt} \tag{2}$$

$$i_C(t) = (i_{\rm GD}(t) - i_d(t) - i_{\rm DS}(t)) \tag{3}$$

$$i_{\rm DS}(t) + i_{\rm GS}(t) + i_d(t) - i_L(t) = 0 \tag{4}$$

where

$$i_L(t) = i_g(t) - i_C(t).$$

When Kirchoff's voltage law is applied to the circuit, voltage equations are obtained as follows:

$$v_{\rm GD} = v_{\rm GS} - v_{\rm DS} \tag{5}$$

$$-V_{\rm pulse} + R_g i_g(t) + v_{\rm GS} + L_S\frac{d(i_L(t))}{dt} = 0 \tag{6}$$

$$-V_c - R_c i_c(t) + L_d\frac{di_c(t)}{dt} + v_{\rm DS} + L_S\frac{d(i_L(t))}{dt} = 0 \tag{7}$$

where

$$L_s = L_{\rm source\_lead} + L_{p2}$$
$$L_d = L_{\rm drain\_lead} + L_{p3} + L_c.$$

By differentiating (5) and putting into (2), gate current is obtained as follows:

$$i_g(t) = (C_{\rm GD} + C_{\rm GS})\frac{dv_{\rm GS}}{dt} - C_{\rm GD}\frac{dv_{\rm DS}}{dt}. \tag{8}$$

Voltage across L_d and L_s is written by using (5)–(7) as follows:

$$L_S\frac{d(i_L(t))}{dt} = V_{\rm pulse} - [R_g(C_{\rm GD} + C_{\rm GS})]\frac{dv_{\rm GS}}{dt} - [R_g C_{\rm GD}]\frac{dv_{\rm DS}}{dt} - v_{\rm GS} \tag{9}$$

$$-L_S\frac{d(i_L(t))}{dt} = -V_c - R_c i_c(t) + v_{\rm DS} + L_d\frac{di_c(t)}{dt}. \tag{10}$$

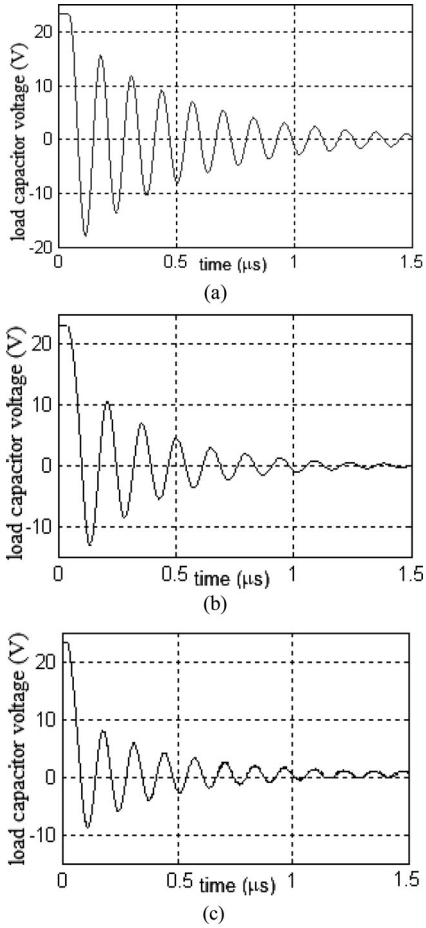

Fig. 8. Load capacitor voltage waveform with 47 Ω gate resistance. (a) CST Design Studio result. (b) Proposed model result. (c) Practically obtained result (500 ns/div, 10 V/div).

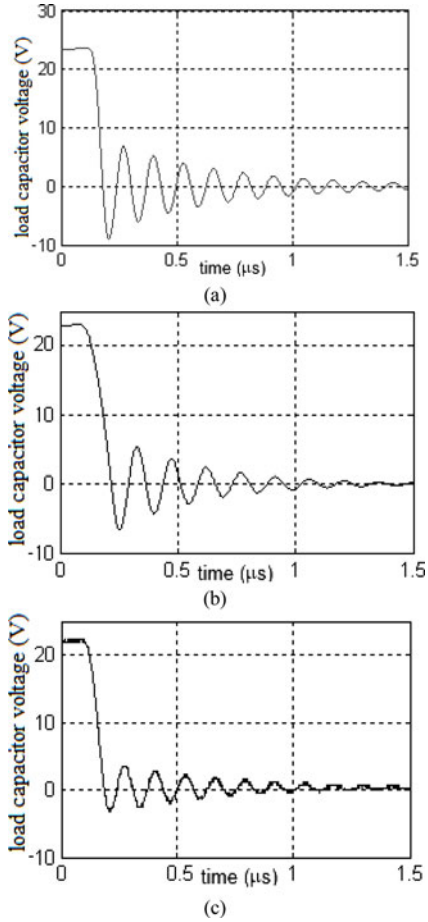

Fig. 9. Load capacitor voltage waveform upon 220 Ω gate resistance. (a) CST Design Studio result. (b) Proposed model result. (c) Practically obtained result (500 ns/div, 10 V/div).

Equations given earlier are valid for both saturation region and ohmic region of the MOSFET since Kirchoff's laws and governing equations of elements are used only for driving them.

A. Distinctive Features for Region 2

When $V_{\rm GS} \geq V_{\rm th}$ and $V_{\rm DS} \geq V_{\rm GS} - V_{\rm th}$, MOSFET is in saturation region and acts as a current source. Drain current of the MOSFET can be written as follows:

$$i_d(t) = g_{\rm fs}[v_{\rm GS} - V_{\rm th}]. \tag{11}$$

If the drain current is integrated into (3) and (4), current flowing through the drain–source capacitance and capacitive load is obtained

$$C\frac{dv_c}{dt} = C_{\rm GD}\frac{dv_{\rm GS}}{dt} - [C_{\rm GD} + C_{\rm DS}]\frac{dv_{\rm DS}}{dt} - [g_{\rm fs}(v_{\rm GS} - V_{\rm th})] \tag{12}$$

$$C_{\rm DS}\frac{dv_{\rm DS}}{dt} = C_{\rm GS}\frac{dv_{\rm GS}}{dt} - [g_{\rm fs}(v_{\rm GS} - V_{\rm th})] + i_L. \tag{13}$$

B. Distinctive Features for Region 3

When $V_{\rm GS} > V_{\rm th}$ and $V_{\rm DS} < V_{\rm GS} - V_{\rm th}$, MOSFET is in linear (ohmic) region and acts as a voltage-dependent resistance ($R_{\rm ds\_on}$). This resistance is varied with

$$R_{\rm ds\_on} = \frac{v_{\rm DS}}{i_d(t)}$$

$$C\frac{dv_c}{dt} = C_{\rm GD}\frac{dv_{\rm GS}}{dt} - [C_{\rm GD} + C_{\rm DS}] \times \frac{dv_{\rm DS}}{dt} - \frac{v_{\rm DS}}{R_{\rm ds\_on}} \tag{14}$$

$$C_{\rm DS}\frac{dv_{\rm DS}}{dt} = C_{\rm Gs}\frac{dv_{\rm GS}}{dt} - \frac{v_{\rm DS}}{R_{\rm ds\_on}} + i_L. \tag{15}$$

In ohmic region, drain current depends on the drain–source voltage and the curve of the drain current and drain–source voltage is approximately linear.

VI. Comparison of Analytical, Simulation, and Experimental Models

The governing equations for transition of N_2 MOSFET from "OFF" to "ON" state are derived earlier. The circuit is modeled analytically in MATLAB by using these equations with

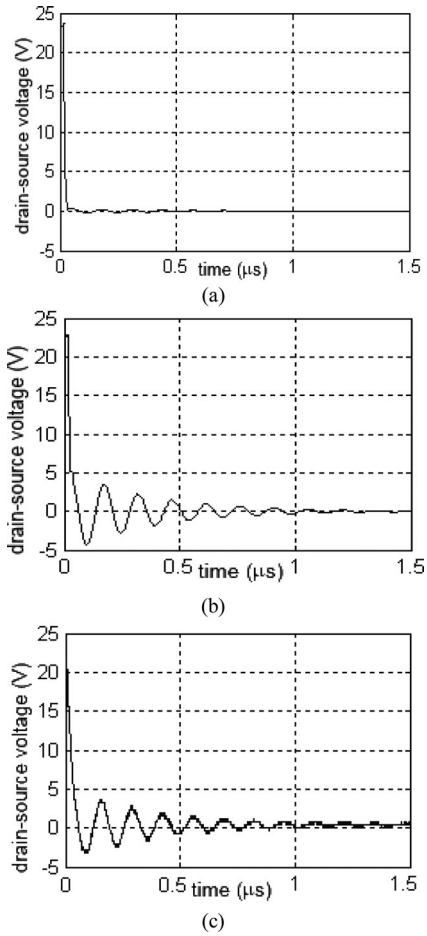

Fig. 10. MOSFET drain–source voltage waveform with 2.2 Ω gate resistance. (a) CST Design Studio result. (b) Proposed model result. (c) Practically obtained result (500 ns/div, 5 V/div).

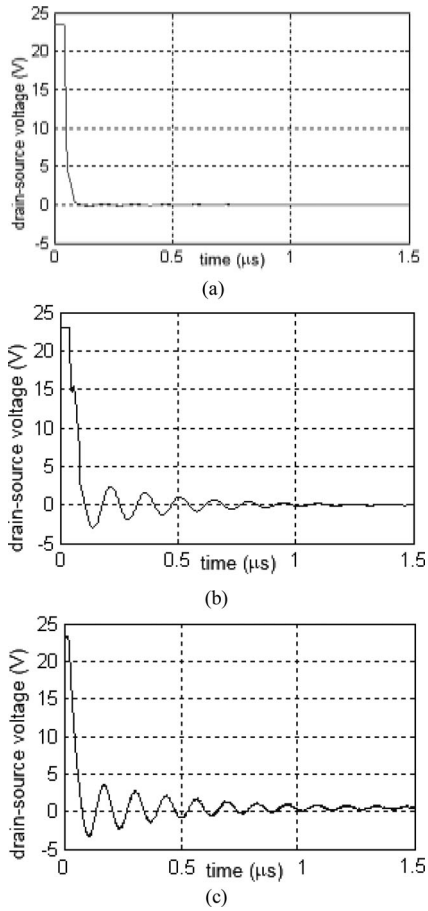

Fig. 11. MOSFET drain–source voltage waveform with 47 Ω gate resistance. (a) CST Design Studio result. (b) Proposed model result. (c) Practically obtained result (500 ns/div, 5 V/div).

an iterative method, and simulated with MATLAB/Simulink. Gate–source voltage of the MOSFET, load capacitor voltage, and drain–source voltage of the MOSFET waveforms are compared with the analytical, simulation, and experimental results.

The differences between the analytical model and the experimental model for the ringing frequencies and the magnitudes of the waveforms are within reasonable bounds. The differences are due to the assumptions that are given in analytical model calculations and also the parasitic resistances occurring on the component pins by soldering. But when simulation results with circuit elements block models are observed, it is seen that some parameters were not taken into account though the manufacturer model is used. Due to this, explicit differences occur in simulation results.

Gate voltage increases from threshold value to higher value levels in the time which required charging the input capacity combined with gate–source and gate–drain capacitances of the MOSFET. Gate–source capacitance is charged very quickly, when gate–source voltage of the MOSFET is very small (2.2 Ω), as shown in Fig. 4.

The MOSFET of Fig. 3 voltage waveforms between gate–source terminals with 47 Ω gate resistance is shown in Fig. 5 while obtaining this voltage-source lead inductance and internal gate resistance are included in analytical model. But it is seen that these values are not specified in the MOSFET model (in CST Design Studio) used for simulation. Application result shows that inductance and resistance in the inner structure of MOSFET also have important effect to observe the oscillations in the terminals of the MOSFET.

When gate resistance value is increased to 220 Ω, obtained gate–source voltage waveforms are as shown in Fig. 6. Again, the ringing of the signals cannot be observed in simulation results when a commercial package is used. Charging times for gate–source and gate–drain capacitances increase due to the gate resistance increment. Variation of the gate resistance becomes crucial at this point. As mentioned before, gate–source voltage must be higher than threshold value to become ON, but by the increment in gate resistance turn-on delay takes longer. Gate–source voltage is also expected to reach pulse voltage value, 20 V, in a short time. It reaches this value very quickly for 2.2 Ω gate resistance, beside this it takes longer time when the gate resistance increased. This is because of the time constant which is determined by the gate resistance.

The load capacitor voltage waveforms for 2.2 Ω gate resistance are seen in Fig. 7. As seen, magnitude of the undesirable oscillation is very high in this case. This high oscillatory driving waveform may cause failures of the driven MOSFET.

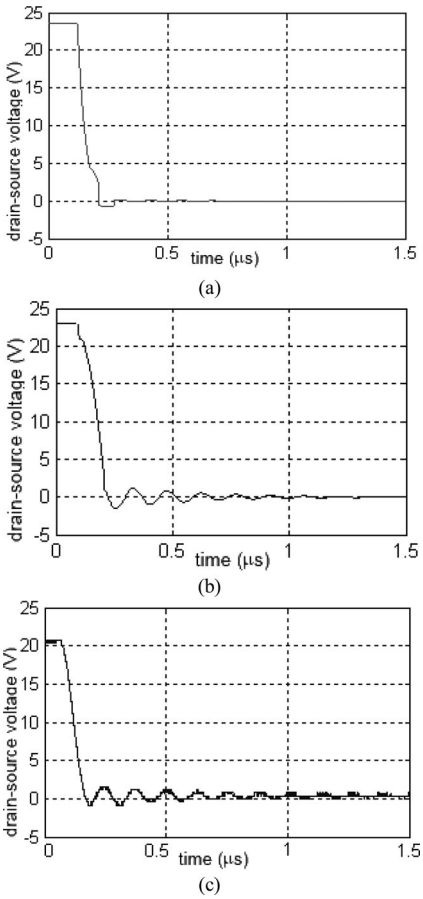

Fig. 12. MOSFET drain–source voltage waveform with 220 Ω gate resistance. (a) CST Design Studio result. (b) Proposed model result. (c) Practically obtained result (500 ns/div, 5 V/div).

In Fig. 8, load capacitor (C) voltage waveforms for 47 Ω gate resistance are seen. When higher side MOSFET P_2 of Fig. 1 becomes ON and N_2 becomes OFF, a transient current flows through the output capacitor, and thus capacitor voltage reaches to the 23 V and keeps this level. After P_2 turns off, the capacitor maintains its charge. The capacitor begins to discharge the voltage on itself, after N_2 becomes ON. But, N_2 cannot become ON at the same time; a delay occurs in order to be on state.

When gate resistance is increased to 220 Ω, ringing of the output signal (seen on load capacitor) is decreased. Actually, this damping is required to decrease the dv/dt ratio.

Oscillatory waveforms seen in Figs. 7–9 may cause the MOSFET to be driven to conduct temporarily just after it is turned-off, since load capacitor voltage represents in fact $V_{\rm GS}$ voltage of the MOSFET switch connected next to the driver circuit.

In Fig. 10, drain–source voltage for 2.2 Ω gate resistance is seen. Analytical model and experimental model results are compatible to each other as shown in figures. Magnitude of the simulation result is very low compared to other results.

Drain–source voltage of N_2 is seen in Fig. 11. For 47 Ω gate resistance, the ringing frequencies of the signals are observed approximately 6 MHz analytical model and 6.66 MHz in experimental results. While investigating the drain–source voltage of the MOSFET, both drain and source internal lead inductances should be considered. Despite the most prominent properties are considered in the MOSFET model, the internal inductances are not mentioned and this prevents to observe the voltage oscillations seen in the experimental and analytical results.

As shown earlier, in Fig. 12, when gate resistance is increased to the 220 Ω, the magnitude of the oscillation decreases. The magnitude of the drain–source voltage ringings seen in the CST Design Studio simulation results is low; this is possibly caused by the model of the MOSFET.

VII. Conclusion

An accurate analytical model of a driver circuit is developed with the assumption of constant MOSFET interelectrode capacitances. However, in each operating region of the MOSFET, the assumed capacitance values are changed in the model as read from datasheets. This proposed method brings a simplified approach and the performance of the driver is investigated without any convergence problems. Analytical model used and along with developed code in MATLAB gives realistic approach to the circuit behavior, since it takes into account the switching element's nonideal properties (MOSFET's parasitic capacitances, internal resistances, and lead inductances), gate driver, and printed circuit board layout parasitics effects. It is known that the accuracy of a simulation study is very sensitive to the models used. Many models can be developed for the same semiconductor element based on the parameters given in its datasheet and/or the results of the measurements conducted to extract model parameters. The analytical model proposed here worked very well for the driver circuit studied. Although it is a high speed driver, oscillations on waveforms may be inevitable. To investigate the reasons of these oscillations and find solutions for mitigating them, this proposed model gives fast and more accurate results than those of some commercial software.

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