Indirect Matrix Converter-Based Topology and Modulation Schemes for Enhancing Input Reactive Power Capability

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***Abstract*—A new topology based on indirect matrix converter (IMC) is proposed to enhance the input reactive power capability. This topology consists of a conventional IMC and an auxiliary switching network (ASN), which is connected to the dc-link of the IMC in parallel. With the aid of ASN, an implicit current source converter-based static synchronous compensator can be embedded into an IMC, which lays a foundation for the input reactive power control. Based on the proposed topology, two modulation schemes are presented, and the formations of the output voltage and input reactive current are decoupled in both of them. To minimize power loss and improve input current quality, a double closed-loop control algorithm is introduced, in which the current through the dc inductor in ASN is controlled to be minimum. Different from the conventional IMC, the input reactive power of the topology is independent of its load condition without considering the practical constraints. The effectiveness of the proposed topology and modulation scheme is confirmed by experimental results.**

***Index Terms*—Indirect matrix converter (IMC), input reactive power, SVM, STATCOM.**

I. Introduction

MATRIX converters, featured by the advantages such as sinusoidal input and output currents, bidirectional energy flow, controllable input power factor as well as a compact design, have received increasingly attention in recent years [1]–[4]. After decades of effort, they have found many applications in adjustable-speed drives, power supply, wind energy conversion system (WECS), flexible ac transmission system (FACTS), and so on [5]–[8]. In most applications, the operation of unity input power factor is preferred for matrix converters. However, in some specific situations, such as WECS and FACTS, the capability to generate and absorb input reactive power should be paid more attention because the completely controllable reactive power generated by matrix converters will be helpful to reduce real power losses in transmission lines and improve voltage stability.

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Due to the characteristics of compact structure, matrix converters are suited to be applied in WECS. For such applications, many researchers have studied the related topologies, modeling, control [5], [9], [10], stability [11], and so on. With the increasing penetration of wind turbines into power grid, the wind generator response to the grid voltage faults may affect the power system normal operation [10]. According to the new grid codes, wind turbines should be able to provide appropriate reactive power to support the grid voltage under abnormal network conditions. In [12], the reactive power control issue is investigated in a WECS fed by a matrix converter, where the reactive power capability is also discussed. However, its reactive power capability is limited and cannot satisfy the requirement of the grid code for WECS. In addition, matrix converter can be viewed as an alternative to unified power flow controller (UPFC). As a FACTS device is the most versatile and potential, the conventional UPFC is the combination of a static synchronous compensator (STATCOM) and a static synchronous series compensator, both of them can control the reactive power freely [13]. Compared with the UPFC based on back-to-back converter, the matrix converter-based UPFC has smaller volume and better reliability [14], [15]. In [15], a direct power control for matrix converter-based UPFC is presented to increase its dynamic response. In such kind of UPFC, the task of STATCOM will be undertook by the input side of matrix converter, Therefore, it is necessary to investigate the input reactive power capability of matrix converter. However, due to the nonlinear relations among the voltage transfer ratio, load properties, and modulation methods, it is not easy to control the input reactive power of the matrix converter.

Since the matrix converter topology was first proposed in 1976, many modulation methods have been presented [16]–[18], such as the optimum-amplitude method [16] and space vector modulation (SVM) [17]. Different modulation methods may reflect different input reactive power capability. In [19], the reactive power limitations with the optimum-amplitude method and SVM are investigated for different operating conditions, which greatly rely on the load displacement angle and output current amplitude. Thus, to cope with the reactive power limitation, a modulation strategy based on mathematical construction is proposed accordingly in [19]. Furthermore, a hybrid modulation scheme is proposed in [20] and [21], which can extend the reactive power control range with low computational effort. For the same purpose, the literature [22] also presents a three-vector modulation scheme for a FACT device based on matrix converter. With these solutions above, the input reactive power

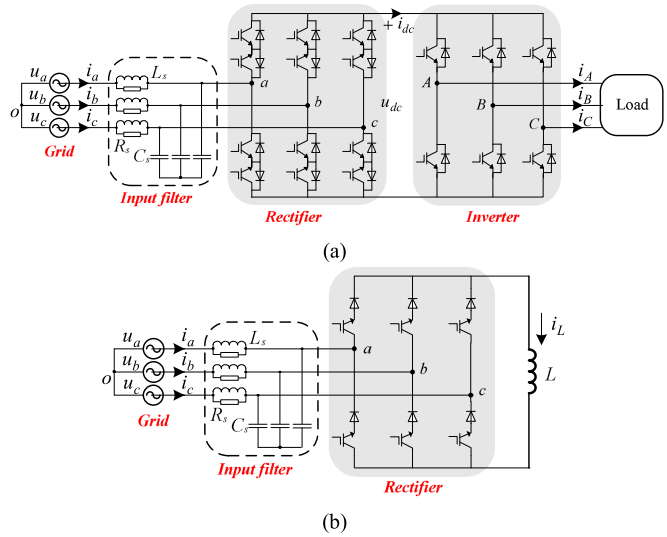


Fig. 1. Schematic diagram of IMC and CSC-based STATCOM.

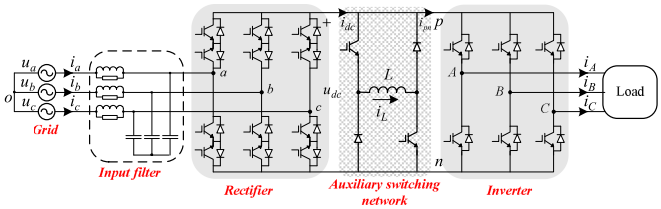


Fig. 2. Circuit diagram of the proposed topology for IMC.

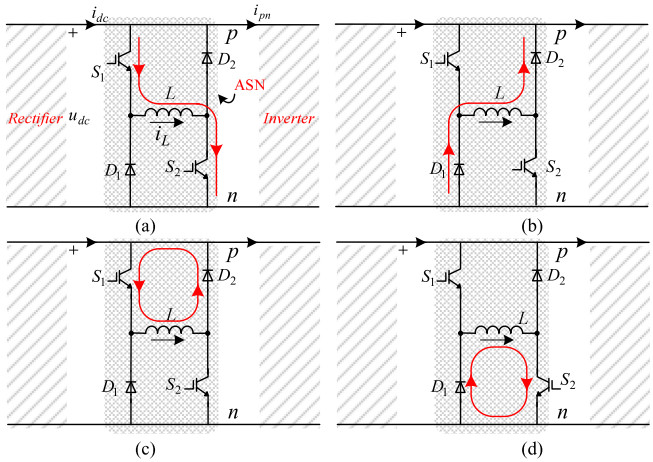


Fig. 3. Operating states for the ASN.

range has been enlarged greatly but the dependence on the load properties remains as usual.

Except for the modulation schemes, the input reactive power capability of matrix converter is also related to the topologies, which are mainly classified into indirect and direct ones [2]. As shown in Fig. 1(a), the indirect matrix converter (IMC) consists of a current source rectifier (CSR) and a voltage source inverter (VSI) connected via a physical dc link [23]. In IMCs, the zero-current commutation can be realized, which leads to lower switching losses and better reliability. Usually, the indirect SVM is employed in the IMC. With the modulation method, the input reactive power capability of the IMC is inferior to that of the conventional matrix converter because of the limitation of the instantaneous dc-link voltage. Moreover, the input reactive power cannot be produced for purely inductive load.

However, the physical dc link of the IMC offers a convenient interface to form other new topologies [24]. A current source converter (CSC)-based STATCOM shown in Fig. 1(b) is a kind of device that can control reactive power freely [25], [26], though it also has some limitations [27]. From Fig. 1, it can be found that the rectifier stage of the IMC is similar to the STATCOM. Thus, if the STATCOM is integrated into the IMC without affecting the inverter stage, the reactive power limitation problem of the IMC would be solved to a certain extent. Based on this idea, a novel topology for the IMC is proposed in this paper, where an auxiliary switching network (ASN) is connected to the physical dc link in parallel, as shown in Fig. 2. Its related modulation schemes based on the indirect SVM is presented to enhance the input reactive power capability.

The remainder of this paper is organized as follows: Section II introduces the topology and modulation schemes. In Section III, the analysis of input reactive power for matrix converter is described. In Section IV, ASN design and the associated control methods are introduced. In Section V, the experimental results are presented, and finally, the main points of this paper are summarized in Section VI.

II. Topology and Modulation Schemes

A. Topology

The proposed circuit topology in Fig. 2 mainly consists of a second-order (*LC*) input filter, an IMC switching circuit, and an ASN located at the dc link. In this converter, the input filter is used to prevent the high-frequency harmonic current from propagating into the grid. For enhancing the system stability, the damping resistors (R_s) are in parallel with the filtering inductors (L_s). The ASN includes two insulated gate bipolar transistors ($S_1 - S_2$) and two diodes ($D_1 - D_2$) and a dc inductor (L), which works implicitly as a STATCOM combined with the CSR.

According to different switching combinations, the ASN has four operating states as shown in Fig. 3(a)–(d), respectively. In the state shown in Fig. 3(a), the inductor L will be charged, and the energy from dc link is stored in the inductor temporarily. In the state shown in Fig. 3(c) or (d), D_1 or D_2 provides a freewheeling path for the dc inductor current i_L, where the energy in inductor almost remains unchanged. In the state shown in Fig. 3(b), the inductor will be discharged, and the energy stored in inductor returns back to dc link. Since the charged energy equals to the discharged, the current i_L maintains a constant. In the states shown in Fig. 3(a) and (b), i_L serves as the function of the dc current of the STATCOM to help to generate input reactive power.

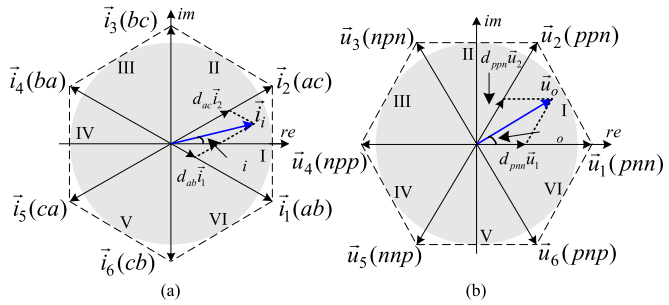


Fig. 4. Space vector diagrams for the modulation of the (a) rectifier and (b) inverter stages.

B. SVM Strategy for the Conventional IMC

Before introducing the modulation strategy for the proposed topology, the indirect SVM strategy for the traditional IMC is first reviewed briefly. For convenience, the input filter influence is not emphasized here. Since the IMC shown in Fig. 1(a) can be divided into two sections: CSR and VSI, the SVM techniques can be utilized in the CSR and VSI stages of matrix converter, respectively. The space vector diagrams for the modulation of the two stages are shown in Fig. 4, where there are six active switching vectors ($\vec{i}_1 \sim \vec{i}_6$ or $\vec{u}_1 \sim \vec{u}_6$) dividing the complex plane into six sectors, respectively. When the desired output voltage/input current vector lies in a certain sector, it can be synthesized by its two adjacent active vectors. Thus, the duty cycles of these adjacent active vectors can be calculated in each switching period, according to capacitor charge balance or volt–second balance principle.

First, assume the input voltage vector is $\vec{u}_{\text{in}} = u_{im}\, e^{j\alpha}$.

Without loss of generality, considering the desired input current vector $\vec{i}_i$ lying within sector I ($\varphi_i \in [-\pi/6, \pi/6]$) shown in Fig. 4(a), the duty cycles of the adjacent active vectors ($\vec{i}_1$ and $\vec{i}_2$) in each switching period are

$$\begin{cases} d_{ab} = m_i \sin(\pi/6 - \varphi_i) \\ d_{ac} = m_i \sin(\pi/6 + \varphi_i) \end{cases} \tag{1}$$

where φ_i is the angular position of the input current vector, m_i is the modulation index, and $0 \le m_i \le 1$.

The duty cycle of zero vectors can be calculated as

$$d_{r0} = 1 - d_{ab} - d_{ac}. \tag{2}$$

As shown in Fig. 4(b), assume that the desired output voltage vector $\vec{u}_o = q u_{im}\, e^{j\theta_o}$ also lies in section I ($\theta_o \in [0, \pi/3]$), where q is the voltage transfer ratio. Then, the corresponding duty cycles of the two active vectors ($\vec{u}_1$ and $\vec{u}_2$) that are used to synthesize it are given by

$$\begin{cases} d_{pnn} = m_o \sin(\pi/3 - \theta_o) \\ d_{ppn} = m_o \sin(\theta_o) \\ d_{i0} = 1 - d_{pnn} - d_{ppn} \end{cases} \tag{3}$$

where θ_o is the angular position of the output voltage vector and m_0 is the modulation index, and $0 \le m_o \le 1$. But for convenience of analysis, let $m_o = 1$ in this paper.

After the combination of the rectifier and inverter modulations, the final duty cycles are as follows:

$$\begin{cases} d_{ab(pnn)} = d_{ab} d_{pnn} = m_i \sin(\pi/6 - \varphi_i) \sin(\pi/3 - \theta_o) \\ d_{ab(ppn)} = d_{ab} d_{ppn} = m_i \sin(\pi/6 - \varphi_i) \sin(\theta_o) \\ d_{ac(pnn)} = d_{ac} d_{pnn} = m_i \sin(\pi/6 + \varphi_i) \sin(\pi/3 - \theta_o) \\ d_{ac(ppn)} = d_{ac} d_{ppn} = m_i \sin(\pi/6 + \varphi_i) \sin(\theta_o). \end{cases} \tag{4}$$

To get the desired output voltage, the modulation indexes should satisfies

$$\boldsymbol{m}_i = \frac{2q}{\sqrt{3}\cos(\Phi_i)} \tag{5}$$

where Φ_i is the input displacement angle and $\Phi_i = \alpha - \varphi_i$.

Generally, to reduce commutation times in each modulation period, only two input line-to-line voltages are used in the rectifier stage and the zero vectors do not appear explicitly. Therefore, d_{r0} should be distributed to d_{ab} and d_{ac} as follows:

$$\begin{cases} d'_{ab} = d_{ab} + d^{ab}_{r0} \\ d'_{ac} = d_{ac} + d^{ac}_{r0} \\ d'_{ab} + d'_{ac} = 1 \end{cases} \tag{6}$$

where d'_{ab} and d'_{ac} are the modified duty cycles of $\vec{i}_1$ and $\vec{i}_2$ after distribution, respectively, and d^{ab}_{r0} and d^{ac}_{r0} should meet the following constraints:

$$\begin{cases} d_{r0} = d^{ab}_{r0} + d^{ac}_{r0} \\ d^{ab}_{r0} \ge 0, d^{ac}_{r0} \ge 0. \end{cases} \tag{7}$$

One most commonly-used way to distribute zero vectors is that d_{r0} is divided into d^{ab}_{r0} and d^{ac}_{r0} in proportion [2], [22] as

$$\begin{cases} d^{ab}_{r0} = \dfrac{d_{ab}}{d_{ab} + d_{ac}} d_{r0} \\ d^{ac}_{r0} = \dfrac{d_{ac}}{d_{ab} + d_{ac}} d_{r0}. \end{cases} \tag{8}$$

However, such a way may lead to the narrow pulse problem [28], which degrades the quality of input currents and output voltages.

In such a manner, the formation of the dc-link voltage and current is shown in Fig. 5.

C. SVM Strategy for the Proposed Topology

In this section, two modulation methods (method I and method II) for the proposed topology are presented, which can regulate the input reactive power independently when synthesizing the expected output voltages. In these methods, the inverter modulation remains the same as that of the conventional IMC mentioned previously, while the rectifier modulation needs to be modified to undertake the task of adjusting the reactive power together with the ASN.

According to the instantaneous reactive power theory, the input current vector could be decomposed into the active and reactive current components. The active current $\vec{i}_{id}$ is in phase with the input voltage, which is orthogonal to the reactive current $\vec{i}_{iq}$. In this paper, both $\vec{i}_{id}$ and $\vec{i}_{iq}$ are viewed as the reference

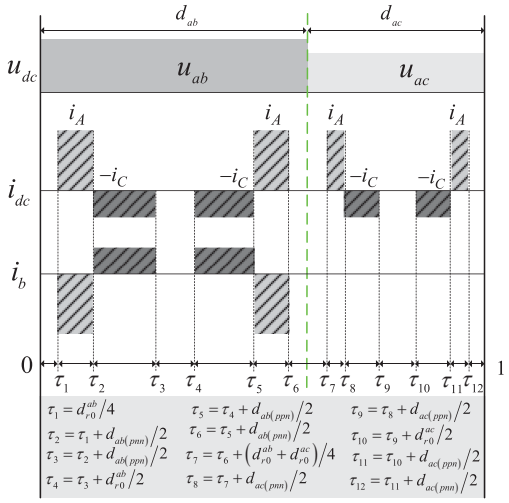


Fig. 5. Pulse diagram of the dc-link variables for the traditional SVM during one switching period.

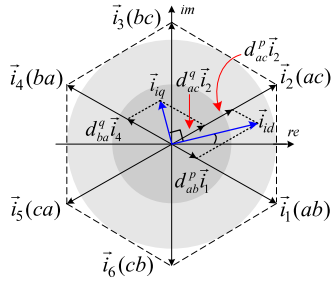


Fig. 6. Space vector diagrams for input current formation using method I.

as shown in Fig. 6, instead of the input current $\vec{i}_i$. Moreover, $\vec{i}_{id}$ is synthesized by the rectifier and inverter of the proposed converter, while $\vec{i}_{iq}$ is only synthesized by the rectifier and ASN, which has nothing to do with the inverter.

1) Formation of the Active Current and Output Voltage: For the active current formation shown in Fig. 6, the related duty ratios of $\vec{i}_1(ab)$ and $\vec{i}_2(ac)$ are rewritten as follows marked with the superscript "*p*"

$$\begin{cases} d_{ab}^p = m_i \sin(\pi/6 - \alpha) \\ d_{ac}^p = m_i \sin(\pi/6 + \alpha) \end{cases} \tag{9}$$

where m_i is the modulation index.

To obtain the required output voltage shown in Fig. 4(b), the expressions for the related duty ratios ($m_o = 1$) are the same with those in (6). Considering the target of extending the input reactive current, m_i takes the minimum value q/q_{max} here ($q_{\max} = \frac{\sqrt{3}}{2}$).

Thus, the effective duty cycles for the output voltage synthesis can be calculated as follows:

$$\begin{cases} d_{ab(pnn)}^p = d_{ab}^p d_{pnn} = \dfrac{q}{q_{\max}} \sin(\pi/6 - \alpha)\sin(\pi/3 - \theta_o) \\ d_{ab(pnn)}^p = d_{ab}^p d_{ppn} = \dfrac{q}{q_{\max}} \sin(\pi/6 - \alpha)\sin(\theta_o) \\ d_{ac(pnn)}^p = d_{ac}^p d_{pnn} = \dfrac{q}{q_{\max}} \sin(\pi/6 + \alpha)\sin(\pi/3 - \theta_o) \\ d_{ac(pnn)}^p = d_{ac}^p d_{ppn} = \dfrac{q}{q_{\max}} \sin(\pi/6 + \alpha)\sin(\theta_o) \end{cases} \tag{10}$$

From (10), these duty cycles are uniquely determined by q, α, and θ_o.

2) Formation of the Input Reactive Current for Method I: The desired reactive current vector $\vec{i}_{iq}$ can be synthesized by different combinations of switching vectors. In this method, $\vec{i}_{iq}$ is synthesized by two vectors with phase difference of 120° of the six basic active vectors. To make it clear, assume that $\vec{i}_{id}$ lies in section I, it is synthesized by $\vec{i}_1(ab)$ and $\vec{i}_2(ac)$. Then, $\vec{i}_{iq}$ may be located in sector II or III, which will yield a leading power factor angle; otherwise, it may also be in sector V or VI, leading to a lagging power factor angle. In other words, the position of $\vec{i}_{iq}$ determines the input reactive power type (inductive or capacitive).

As illustrated in Fig. 6, to synthesize $\vec{i}_{iq}$ located in sector III, in theory, there are two pairs of active vectors ($\vec{i}_2(ac)$ and $\vec{i}_4(ba)$, $\vec{i}_3(bc)$, and $\vec{i}_5(ca)$) available. However, only the vectors $\vec{i}_2(ac)$ and $\vec{i}_4(ba)$ are employed in this method, which also applies to the situation when $\vec{i}_{iq}$ lies in sector II. From the input current point of view, $\vec{i}_4(ba)$ could be replaced by $\vec{i}_1(ab)$ with the dc-link current of opposite direction, which can be realized by changing the operating states of the ASN easily. In addition, the negative dc-link voltage u_{ba} that would lead to short circuit via the free-wheeling diodes in inverter stage can be avoided. Therefore, we could synthesize the desired $\vec{i}_{id}$ and $\vec{i}_{iq}$ with the two vectors $\vec{i}_1(ab)$and $\vec{i}_2(ac)$, simultaneously.

For the reactive current formation shown in Fig. 6, the related duty cycles of $\vec{i}_1(ab)$ and $\vec{i}_2(ac)$ marked with the superscript "*q*" can be expressed as

$$\begin{cases} d_{ab}^q = n_i \sin(\pi/3 + \alpha) \\ d_{ac}^q = n_i \sin(\pi/3 - \alpha) \end{cases} \tag{11}$$

where $0 \le n_i \le \frac{1}{\sqrt{3}}$.

When $\vec{i}_1(ac)$ is used, the ASN will operate in the state as shown in Fig. 3(a), and the related duty cycle is $d_\alpha = d_{ac}^q$. When $\vec{i}_1(ab)$ is applied, the ASN will work in the state as shown in Fig. 3(b) and the duty cycle is $d_\beta = d_{ab}^q$. Over the rest of time, the ASN would work in the states as shown in Fig. 3(c) and (d), whose duty cycles are equal.

Considering the operating limit, the following constraint must be always satisfied

$$d_T = \max(d_{ab}^p, d_{ab}^q) + \max(d_{ac}^p, d_{ac}^q) \le 1. \tag{12}$$

Substitute (9) and (11) into (12), after some manipulations (please refer to the Appendix for details), we can get the maximum n_i with regard to q, which is

$$n_{i\max} = \begin{cases} \dfrac{1}{\sqrt{3}}, & 0 \le q \le q_{c1} \\ 1 - q, & q_{c1} < q \le q_{\max} \end{cases} \tag{13}$$

where q_{c1} is the critical point, and $q_{c1} = 0.423$.

Note that, in most cases, $d_T < 1$. Thus, to reduce the commutation times, it is necessary to distribute the zero vector time of

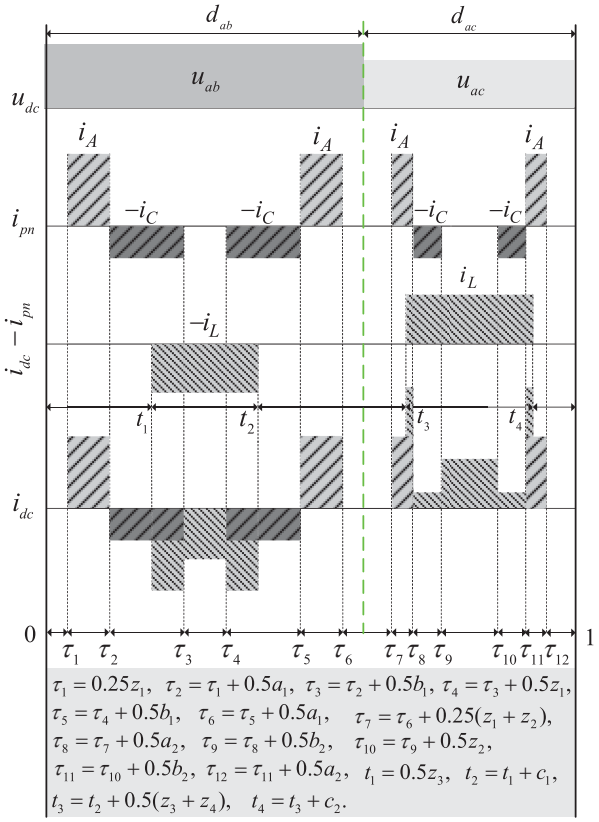


Fig. 7. Pulse diagram of the dc-link variables for method I during one modulation period, $z_1 = d_{ab} - a_1 - b_1$, $a_1 = d^p_{ab(pnn)}$, $b_1 = d^p_{ab(ppn)}$, $z_2 = d_{ac} - a_2 - b_2$, $a_2 = d^p_{ac(pnn)}$, $b_2 = d^p_{ac(ppn)}$, $z_3 = d_{ab} - c_1$, $c_1 = d^q_{ab}$, $z_4 = d_{ac} - c_2$, $c_2 = d^q_{ac}$.

the CSR ($d_{r0} = 1 - d_T$) to the active vectors. For instance, in this case, the duty cycles of the active vectors $\vec{i}_1(ab)$ and $\vec{i}_2(ac)$ after the zero vector time being distributed can be expressed as follows:

$$\begin{cases} d_{ab} = \max(d^p_{ab}, d^q_{ab}) + \dfrac{d_{r0}}{2} \\ d_{ac} = \max(d^p_{ac}, d^q_{ac}) + \dfrac{d_{r0}}{2} \end{cases}. \tag{14}$$

Fig. 7 illustrates the corresponding pulse diagram of the dc-link variables during one modulation period. As seen, two line-to-line input voltages u_{ab} and u_{ac} are applied to form the dc-link voltage $u_{\rm dc}$. The dc-link current i_{dc} is constituted by adding the dc-link current i_{pn} with the inverted or noninverted inductor current i_L. Obviously, the zero current commutation in the rectifier could still be guaranteed, leading to low switching losses and high reliability.

3) Formation of the Input Reactive Current for Method II: In method I, $\vec{i}_{iq}$ is synthesized by two vectors with phase difference of 120°, and the dc-link voltage is formed by two line-to-line voltages. In fact, if $\vec{i}_{id}$ lies in section I and $\alpha > 0$ as shown in Fig. 8, $\vec{i}_{iq}$ could also be synthesized by its two adjacent vectors $\vec{i}_3(bc)$ and $\vec{i}_4(ba)$. Still, $\vec{i}_4(ba)$ would be replaced by $\vec{i}_1(ab)$ in the modulation process, and the dc-link current should also be reversed by changing the switching states of the ASN. Note that,

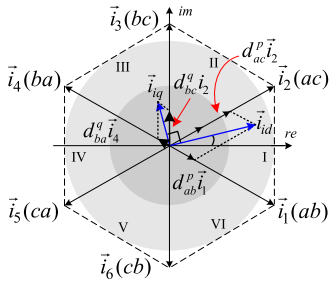


Fig. 8. Space vector diagrams for input current formation using method II.

if the case of $\alpha < 0$ appears, $\vec{i}_{iq}$ will lie in section II. In this case, $\vec{i}_{iq}$ would be synthesized by its two adjacent vectors $\vec{i}_3(bc)$ and $\vec{i}_2(ac)$, and $\vec{i}_3(bc)$ would be replaced by $\vec{i}_6(cb)$. Without loss of generality, we only consider the case of $\alpha > 0$ here.

According to Fig. 8, the duty cycles of $\vec{i}_3(bc)$ and $\vec{i}_4(ba)$ can be expressed as follows:

$$\begin{cases} d^q_{bc} = n_i \sin(\pi/3 - \alpha) \\ d^q_{ab} = n_i \sin(\alpha) \end{cases} \tag{15}$$

where $0 \le n_i \le 1$.

Similarly, when $\vec{i}_3(bc)$ is used, the ASN will operate in the state as shown in Fig. 3(a), and $d_\alpha = d^q_{bc}$; when $\vec{i}_1(ab)$ is applied, the ASN will work in the state as shown in Fig. 3(b) and $d_\beta = d^q_{ab}$.

To complete the entire modulation method, the following constraint must be always satisfied:

$$d_T = \max(d^p_{ab}, d^q_{ab}) + d^q_{bc} + d^p_{ac} \le 1. \tag{16}$$

Substitute (9) and (15) into (16), after some manipulations (please refer to the Appendix for details), we can get the maximum n_i with respect to q, which is

$$n_{i\max} = \begin{cases} 1 - q, & 0 \le q \le q_{c2} \\ \dfrac{2\sqrt{3}}{3} - \dfrac{4}{3}q, & q_{c2} < q \le q_{\max} \end{cases} \tag{17}$$

where $q_{c2} = 0.464$.

By analogy, to avoid using zero vector in rectifier, it is also necessary to distribute the zero vector time of the CSR ($d_{r0} = 1 - d_T$) to the active vectors. Therefore, the duty cycles of the active vectors $\vec{i}_1(ab)$, $\vec{i}_2(ac)$, and $\vec{i}_3(bc)$ after the zero vector time being distributed can be expressed as follows:

$$\begin{cases} d_{ab} = \max(d^p_{ab}, d^q_{ab}) + \dfrac{d_{r0}}{3} \\ d_{ac} = d^p_{ac} + \dfrac{d_{r0}}{3} \\ d_{bc} = d^q_{bc} + \dfrac{d_{r0}}{3}. \end{cases} \tag{18}$$

Fig. 9 illustrates the pulse diagram of the dc-link variables for method II accordingly. As seen, there are three line-to-line input voltages u_{ab}, u_{ac}, and u_{bc} being applied to form the dc-link voltage $u_{\rm dc}$. Moreover, the dc-link current $i_{\rm dc}$ is constituted by adding the dc-link current i_{pn} with the inverted or noninverted inductor current i_L.

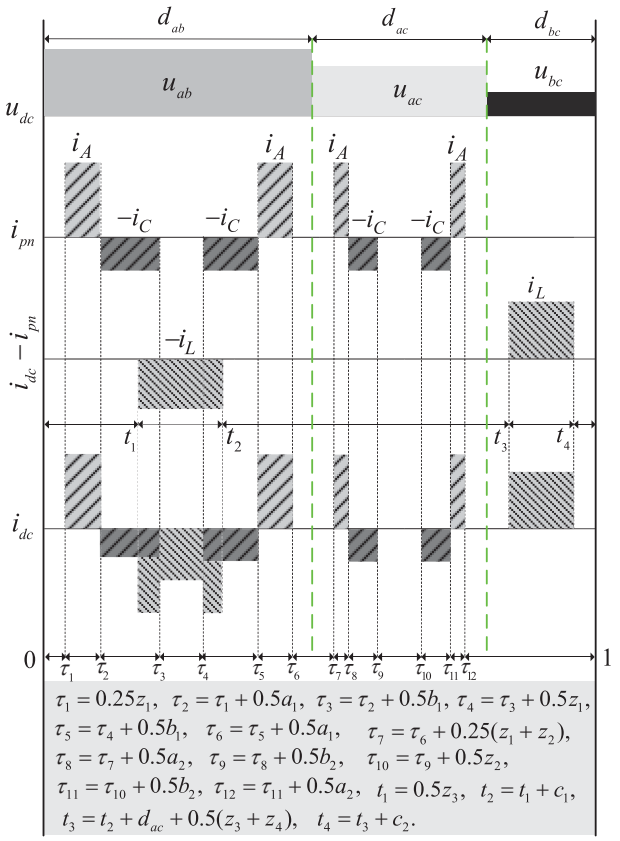


Fig. 9. Pulse diagram of the dc-link variables for method II during one switching period, $z_1 = d_{ab} - a_1 - b_1, a_1 = d^p_{ab(pnn)}, b_1 = d^p_{ab(ppn)}, z_2 = d_{ac} - a_2 - b_2,\ a_2 = d^p_{ac(pnn)},\ b_2 = d^p_{ac(ppn)},\ z_3 = d_{ab} - c_1,\ c_1 = d^q_{ab},\ z_3 = d_{bc} - c_2, c_2 = d^q_{bc}$.

III. Analysis of Input Reactive Power

A. Reactive Power of the Conventional IMC

Based on the modulation strategy for conventional IMC, the input reactive power of the IMC can be expressed as

$$Q_i = 1.5u_{im}\left|\vec{i}_i\right|\sin(\Phi_i) = P_i\tan(\Phi_i) \tag{19}$$

where $P_i = 1.5u_{im}\left|\vec{i}_i\right|\cos(\Phi_i)$ denotes the input active power and $|\Phi_i| \le \frac{\pi}{6}$.

Due to the lack of storage element in the IMC, the active power at the input and output sides are equal, ignoring the power loss of switching devices. Thus, the active power can also be written as

$$P_i = P_o = 1.5qu_{im}\left|\vec{i}_o\right|\cos(\Phi_o) \tag{20}$$

where Φ_o is the load displacement angle, and $\vec{i}_o$ is the output current vector.

Combining (19) and (20), it leads to

$$Q_i = 1.5qu_{im}\left|\vec{i}_o\right|\cos(\Phi_o)\tan(\Phi_i) \tag{21}$$

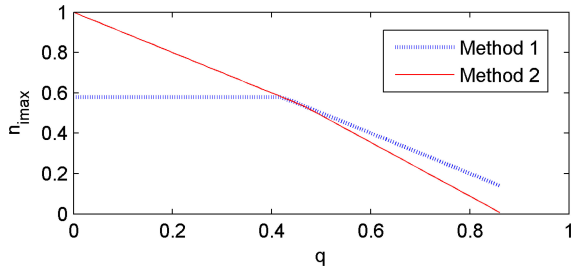


Fig. 10. Maximum feasible modulation index versus voltage transfer ratio.

where the voltage transfer ratio q should satisfy the constraint $q \le \frac{\sqrt{3}\cos(\Phi_i)}{2}$. It is clear that the reactive power is related to the load properties, and the relation is very complicated.

B. Reactive Power for the Proposed Schemes

As for the proposed topology and modulation schemes, the input reactive power is expressed as

$$Q_i = \frac{3}{2}u_{im}\left|\vec{i}_{iq}\right| = \frac{3}{2}u_{im}n_i i_L. \tag{22}$$

It is obvious that the input reactive power Q_i is related to i_L and n_i, which are independent of the active power transfer and the load properties, such as the load displacement angle. Though n_i is restricted by (13) or (17), any desired input reactive power can be attained if i_L is large enough (with the physical limitations neglected). However, to reduce power loss and enhance the quality of input currents and voltages, let n_i equals to its maximum value as in (13) or (17), then, i_L would be viewed as a free variable. In that case, the inductor current would be a minimum value that can meet the requirement of input reactive power.

According to (13) and (17), the maximum feasible modulation index $n_{i\max}$ of two methods with respect to q is illustrated in Fig. 10. As seen, $n_{i\max}$ in method I is greater than that in method II when $q \le q_{c1} = 0.432$. That is to say, the maximum reactive capability of method I is greater than that in method II with the same i_L. Moreover, $n_{i\max}$ in method I is equivalent to that in method II when $q_{c1} < q \le q_{c2} = 0.464$, and it is smaller than that in method II when $q > q_{c2}$. Therefore, it is not difficult to combine the two methods to form a hybrid method.

IV. ASN Design and Control Method

A. ASN Design

In the proposed topology, the ASN including a dc inductor is an important component. The design of the ASN involves the selection of switching devices and dc inductor. Both of the switching devices and dc inductor are related to the maximum allowable dc inductor current, which is determined by the required input reactive power capacity. If the maximum allowable dc inductor current has been determined, the next step is to determine the inductance L. Usually, a low inductance means less weight and lower cost. However, it also means large current ripple, which will result in bad input current quality [29]. Hence,

L could be calculated based on the given maximum allowable current ripple.

For method I, without loss of generality, assume $\vec{i}_{id}$ lies in Section I. Then, the current ripple is expressed as

$$\begin{aligned}\Delta i_L &= \max_{\alpha}\{u_{ac}d_{ac}^{q}T/L\} \\ &= \max_{\alpha,n_i}\{\tfrac{\sqrt{3}}{2}u_{im}n_i[\cos(2\alpha)-\cos(\tfrac{2\pi}{3})]T/L\} \quad (23)\end{aligned}$$

where $-\frac{\pi}{6}\le\alpha\le\frac{\pi}{6}$, $0\le n_i\le\frac{1}{\sqrt{3}}$, T is the modulation period. When $\alpha=0$ and $n_i=\frac{\sqrt{3}}{3}$, the maximum current ripple occurs. Therefore, for a given maximum allowable current ripple Δi, L should satisfy

$$L\ge\frac{3u_{im}T}{4\Delta i}. \quad (24)$$

For method II, assume that $\vec{i}_{id}$ lies in section I, the current ripple is

$$\begin{aligned}\Delta i_L &= \max_{\alpha}\{u_{bc}d_{bc}^{q}T/L\} \\ &= \max_{\alpha,n_i}\left\{\frac{\sqrt{3}}{2}u_{im}n_i\left[\cos\left(2\alpha-\frac{\pi}{3}\right)-\cos\left(\frac{\pi}{3}\right)\right]T/L\right\}\end{aligned} \quad (25)$$

where $-\frac{\pi}{6}\le\alpha\le\frac{\pi}{6}$, $0\le n_i\le 1$, it is clear that the maximum current ripple occurs when $\alpha=0$ and $n_i=1$.

Therefore, L should satisfy

$$L\ge\frac{\sqrt{3}u_{im}T}{4\Delta i}. \quad (26)$$

Taking into account the two cases above, L is selected from the range $L\ge\frac{3u_{im}T}{4\Delta i}$.

As known, the CSC-based back-to-back converter also has a dc inductor, where the inverter stage is a CSC. According to the related mathematic relation between the inductor current ripple and inductance, the selection principle of the dc inductance L in the proposed topology and CSC-based converter are basically identical but the rated inductor currents are different. The rated inductor current of the CSC-based converter depends on the rated converter capacity, while the rated current of the proposed converter is mainly related to the required input reactive power [30]. Thus, the cost and volume of dc inductor in the proposed converter would be less than those in the CSC-based back-to-back converter.

B. Control Method for ASN

The control of the ASN is essential for the proposed input reactive power control. According to Fig. 3, the dynamic equation of the inductor current is given by

$$L\frac{di_L}{dt}=d_\alpha u_{\rm dc}^{\alpha}-d_\beta u_{\rm dc}^{\beta} \quad (27)$$

where d_α and d_β denote the duty ratios of state (a) and state (b) in Fig. 2, respectively, $u_{\rm dc}^{\alpha}$ is the dc-link voltage when the ASN is working in the state (a), and $u_{\rm dc}^{\beta}$ is the dc-link voltage when the ASN is working in state (b). For example, for the case shown in Fig. 6, where $d_\alpha=d_{ac}^{q}$, $u_{\rm dc}^{\alpha}=u_{ac}$ and $d_\beta=d_{ab}^{q}$, $u_{\rm dc}^{\beta}=u_{ab}$.

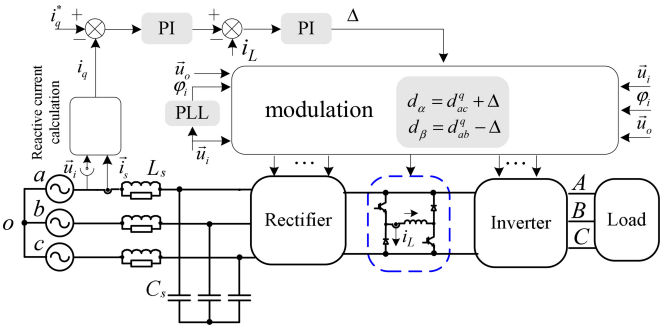


Fig. 11. Schematic Diagram of the modulation scheme for the proposed topology.

TABLE I
PARAMETERS USED IN THE EXPERIMENTS

Input voltage/filter/load	value
u_i	65 V(rms)
ω_i	314 rad/s
L_s	0.6 mH
C_s	50 μF
R_s	4.8 Ω
L	5 mH
L_d	3 mH
R_d	25 Ω

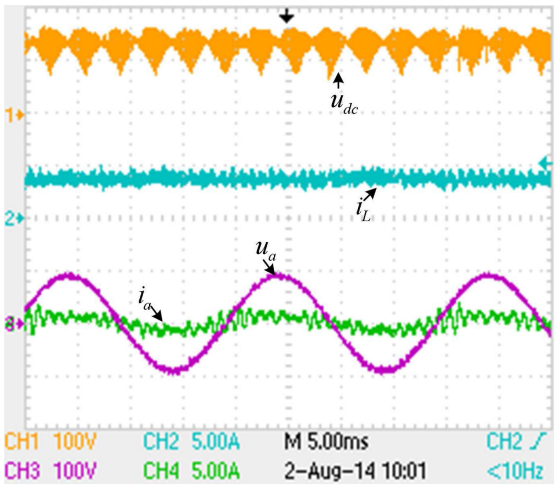
In theory, i_L could be maintained to be a constant value because of $d_\alpha u_{\rm dc}^{\alpha}=d_\beta u_{\rm dc}^{\beta}$. However, an extra closed-loop control is needed to stabilize or regulate it due to the power loss and varying set-point. The overall control scheme is proposed as shown in Fig. 11. The PLL is used to track the position of the input voltage vector, which helps to determine the sector for the active and reactive current references. A proportional-integral controller is employed to control the inductor current i_L, whose output Δ is used to compensate the power loss. In steady state, Δ is very small.

Based on the analysis on modulation scheme in previous section, if the desired output voltage vector and input reactive power is given, it is not difficult for the proposed method to be implemented.

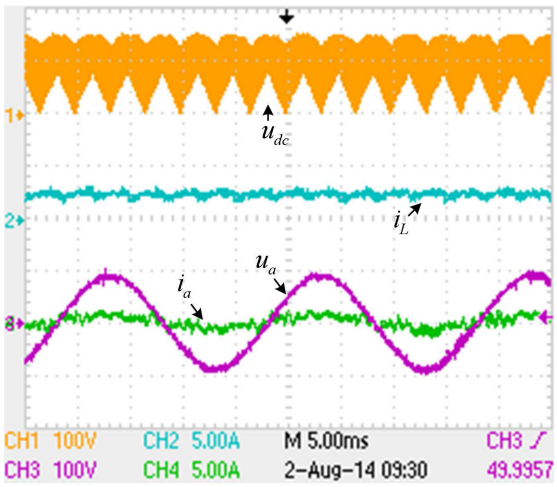
V. EXPERIMENTAL RESULTS

To validate the proposed topology and modulation methods experimentally, a prototype has been built in our laboratory. The parameters of the input voltages (u_i and ω_i), input filter (L_s, C_s, and R_s), dc-link inductor (L) in the ASN and inductive load (L_d,R_d) are listed in Table I. Besides, the modulation period is set to be $1e^{-4}$ s, and the output voltage frequency is 40 Hz in all cases.

The selection of the dc inductor is a very important step, which is related to the power quality and system efficiency. However, it is difficult to obtain a precise mathematical relationship between the total harmonic distortion of input currents and the dc current ripple in this case. According to the working principles, the design of the dc inductor for the proposed converter is similar with that of the CSC-based STATCOM. Usually, by making a

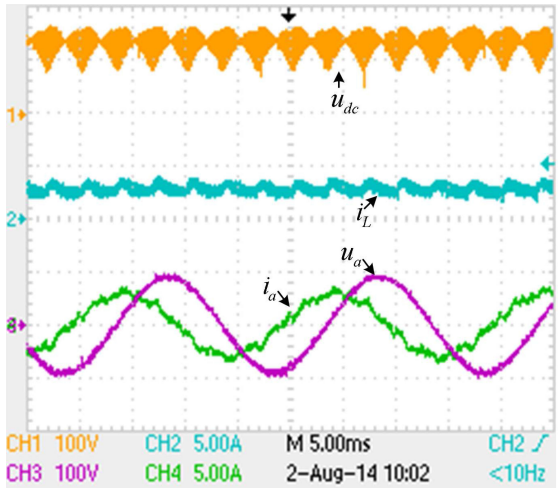


(a)

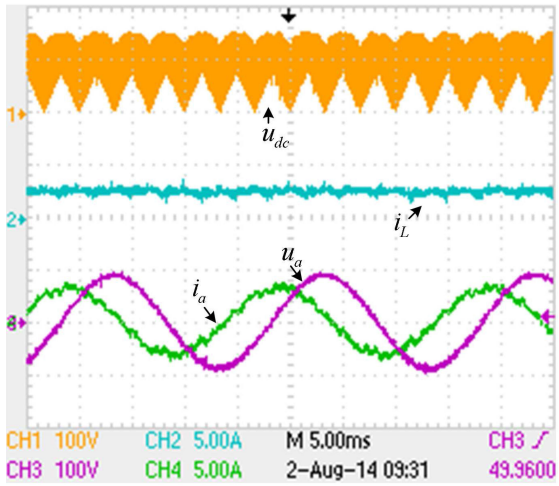


(b)

Fig. 12. Measured waveforms at $m_i = 0.3$ and $i_q = 0$ A: (a) method I; (b) method II.



(a)



(b)

Fig. 13. Measured waveforms with $m_i = 0.3$ and $i_q^* = 3$ A: (a) method I; (b) method II.

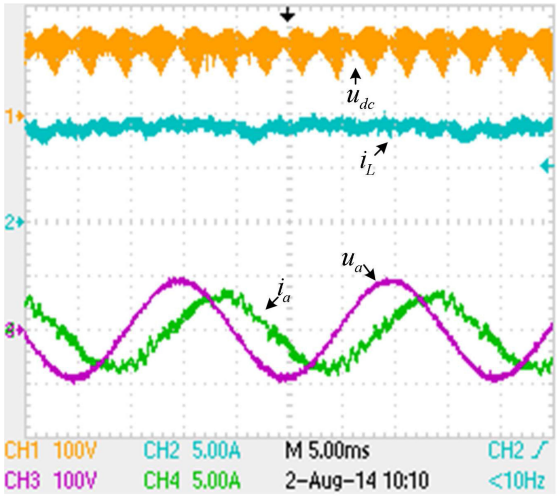
tradeoff between costs and power quality, an acceptable dc-link current ripple is selected as about 10% of the average value in CSC-based STATCOM [29], [31]. In the experiment, the average value of the dc-link current is 15 A, according to (26), the dc inductance value is 4.4 mH. Meanwhile, a dc inductor of 5 mH/20 A happens to be available in the lab. So an inductor of 5.0 mH is selected here.

The experiments are carried out in the following cases:

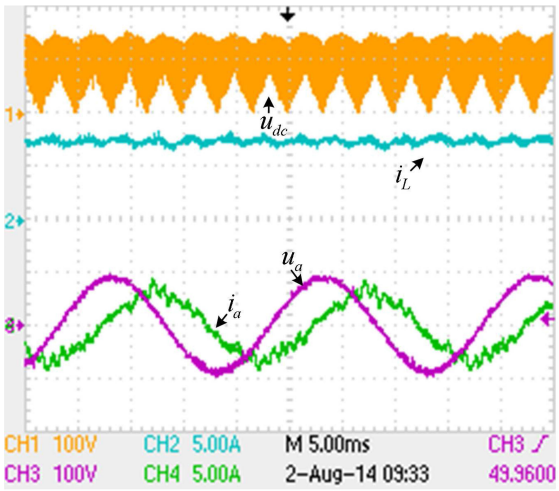
1) $m_i = 0.3$, and i_q=0, 3, −3 (A), respectively;
2) $m_i = 0.7$, and i_q=0, 3, −3 (A), respectively;
3) $m_i = 0.5$, i_q is changed from 0 to −3 A;
4) $m_i = 0$, and i_q= − 3 A, n_i=1, respectively.

The experimental waveforms of the input voltage u_a, input current i_a, dc-link voltage $u_{\rm dc}$, and inductor current i_L with methods I and II at $m_i = 0.3$ and $i_q = 0A$ are shown in Fig. 12(a) and (b), respectively. It is clear that the matrix converter operates at unity input power factor with the two methods. The main difference between Fig. 12(a) and (b) is the dc-link voltage waveform. In method I, two higher line-to-line voltages are used, and the minimum dc-link voltage is larger than zero at any time. However, three line-to-line voltages are employed in method II during each sampling interval, the minimum dc-link voltage is almost close to zero. In addition, it can be found that the current ripple of dc inductor in method I is larger than that in method II, which is in good agreement with the calculation results in Section IV.

Under the condition of $m_i = 0.3$ and $i_q^* = 3$A, the associated experimental waveforms with methods I and II are shown in Fig. 13(a) and (b), respectively. As seen from the experimental results, the input currents lead the input voltages in both methods, which means the input capacitive reactive power could be generated. Moreover, Fig. 14(a) and (b) illustrate the corresponding experimental waveforms with methods I and II at $m_i = 0.3$ and $i_q^* = -3$A, respectively. As seen, the input currents are behind the input voltages. i.e., the inductive reactive power is generated. Compared the results in Fig. 13 with those in Fig. 14, it can also be found that the inductor currents i_L in Fig. 13 are smaller than those in Fig. 14. It is easy to understand, when the capacitor reactive power induced by the filtering capacitor is taken into account. Meanwhile, in Fig. 13 or in Fig. 14,

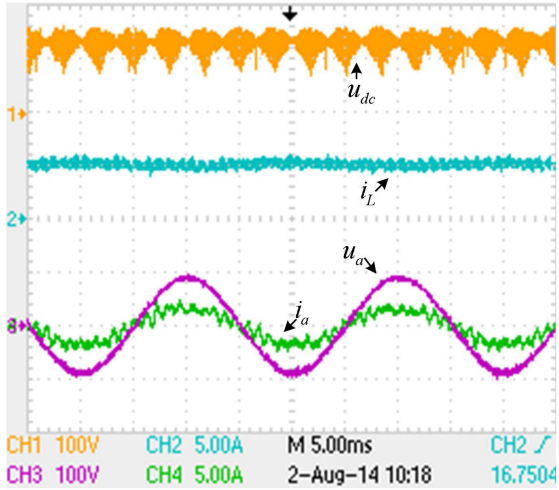


(a)

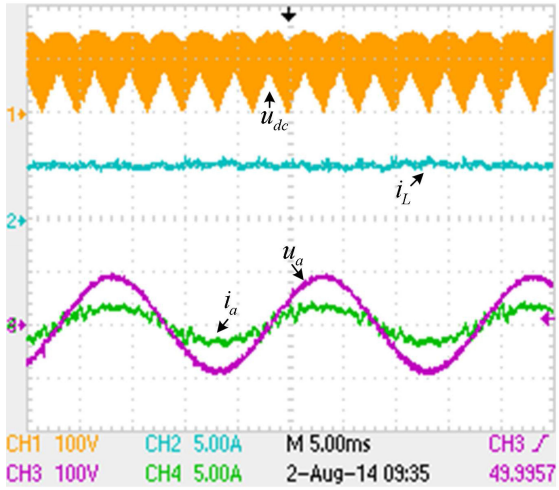


(b)

Fig. 14. Measured waveforms with $m_i = 0.3$ and $i_q = -3$ A: (a) method I; (b) method II.



(a)



(b)

Fig. 15. Measured waveforms with $m_i = 0.7$ and $i_q^* = 0$ A: (a) method I; (b) method II.

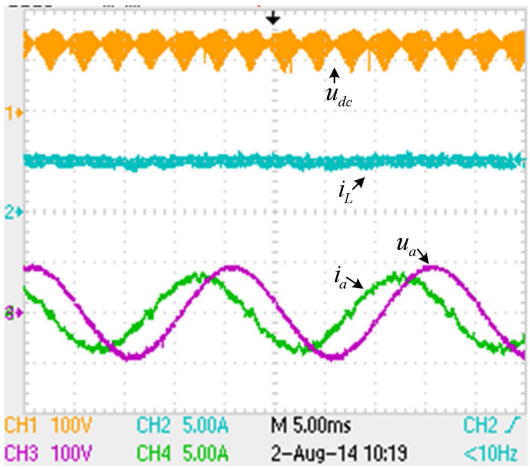
the inductor current i_L with method I is slightly larger than that with method II because refer to (22) and Fig. 10, only a larger i_L in method I can obtain the same reactive current i_q as that in method II at $m_i = 0.3$.

The experimental waveforms with methods I and II at $m_i = 0.7$ and $i_q^* = 0$ are illustrated in Fig. 15(a) and (b), respectively. As seen, the input voltages are in phase with the input currents. Compared with the results in Fig. 12, it is found that the current inductor currents i_L in Fig. 15 are larger than those in Fig. 12, which indicates that as m_i increases, the reactive power capacity decreases.

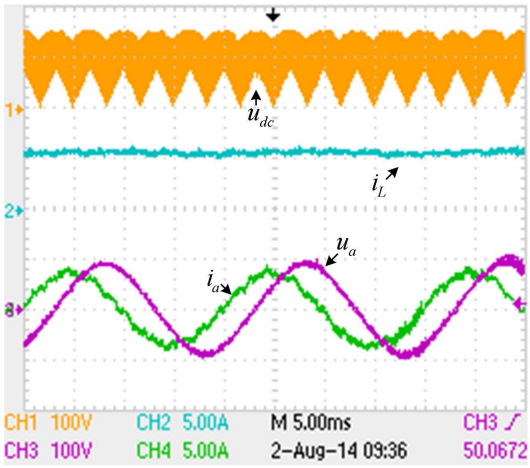
At $m_i = 0.7$, the experimental waveforms for $i_q = 3$ A with methods I and II are illustrated in Fig. 16(a) and (b), respectively. Fig. 16(c) shows the waveforms of the conventional IMC when $m_i = 0.7$ and maximum input reactive power is obtained. As seen, for a given output voltage, the input reactive power of the conventional IMC cannot be regulated like the proposed topology and it is determined by modulation, voltage transfer ratio, and load condition. Fig. 17(a) and (b) show the experimental results for $i_q = -3$A, respectively. By comparisons, it can be found that the inductor currents at $m_i = 0.7$ are larger than those at $m_i = 0.3$, and the inductor currents with method I are slightly smaller than those with method II, which agree well with the theoretic analysis before.

Fig. 18 shows the experimental results when the reactive current reference i_q is changed from 0 to -3 A at $m_i = 0.5$. As seen, to keep the current inductor current i_L minimum for any given input reactive current reference, the current inductor currents are also changed in both methods. The output current i_A with the frequency of 40 Hz does not affected by the change of reactive current reference, which means the output current of the topology is independent of its input reactive current.

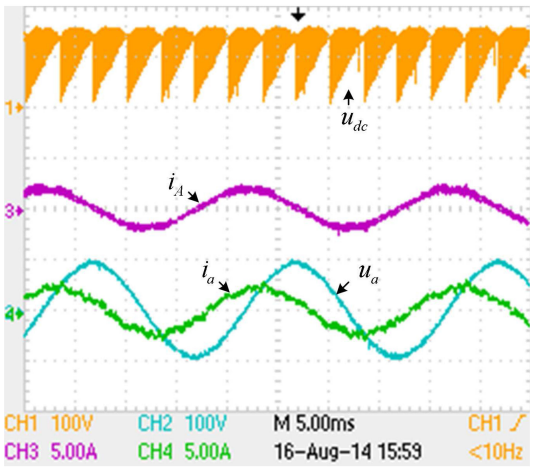
Fig. 19(a) and (b) show the measured waveforms with methods I and II in the case of $m_i = 0$ and $i_q = -3$ A, respectively. Since the output voltages and currents are zero, there is no active power consumed by the load. Only the input reactive power is regulated. As seen, the measured input reactive power is close to the calculated value. The measured active power is



(a)



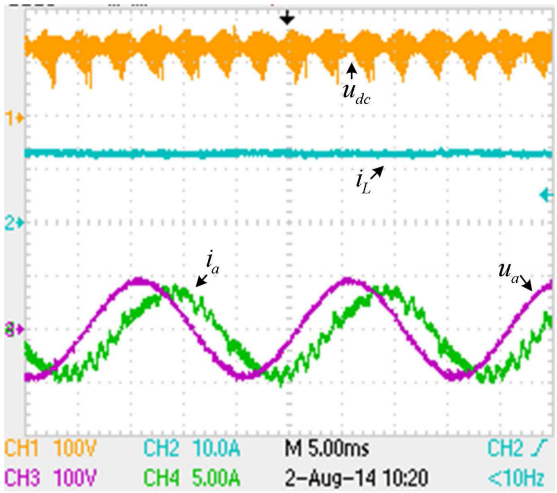
(b)



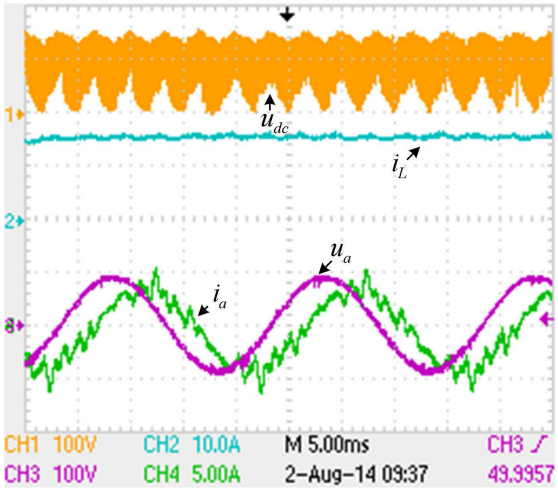
(c)

Fig. 16. Measured waveforms with $m_i = 0.7$ and $i_q^* = 3$ A: (a) method I; (b) method II; (c) conventional IMC.

not zero, which is due to the power loss of the converter. In our design, the maximum allowable dc inductor i_L is 15 A. Fig. 20 shows the experimental results with method II when the maximum capacitive reactive power compensation capacity is achieved ($m_i = 0$, $n_i = 1$). According to the experimental



(a)



(b)

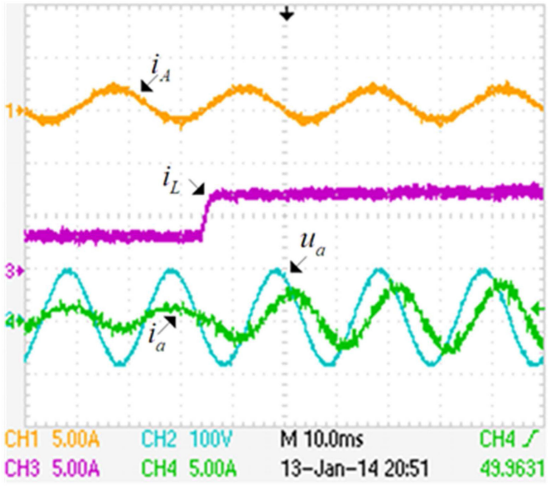
Fig. 17. Measured waveforms with $m_i = 0.7$ and $i_q^* = -3$A: (a) method I; (b) method II.

results above, it is obvious that the input reactive power of the topology is independent of its load condition

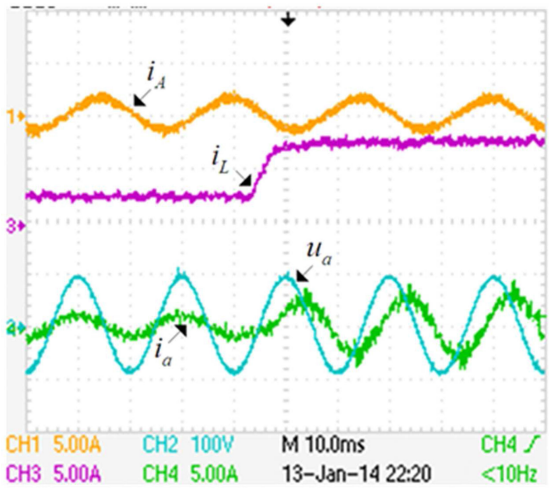
VI. Conclusion

In this paper, a new topology based on the IMC is proposed, which places an additional ASN connected to the dc link of IMC. Two modulation methods based on SVM are presented. In method I, the dc-link voltage of the proposed circuit topology is composed of two input line-to-line voltages, while in method II, the dc-link voltage is composed of three input line-to-line voltages. Both of the modulation methods could generate input reactive power freely without effecting the formation of output voltages. According to the theoretical analysis, considering the limitation of power loss and switching stress, method I have advantage over method II when the voltage transfer ratio is higher than 0.432. However, in the low transfer ratio region, method II is preferred.

Compared with the conventional IMC, the proposed converter (with dc inductor) can obtain the input reactive power

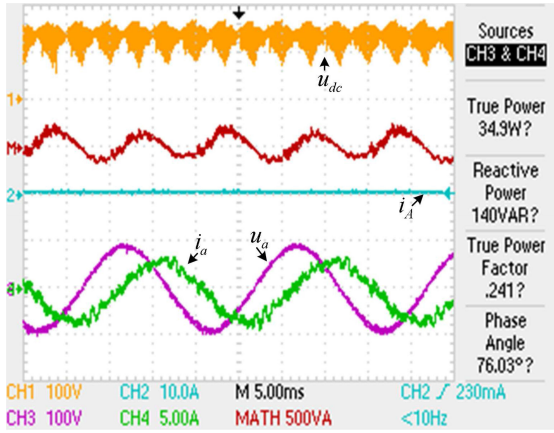


(a)

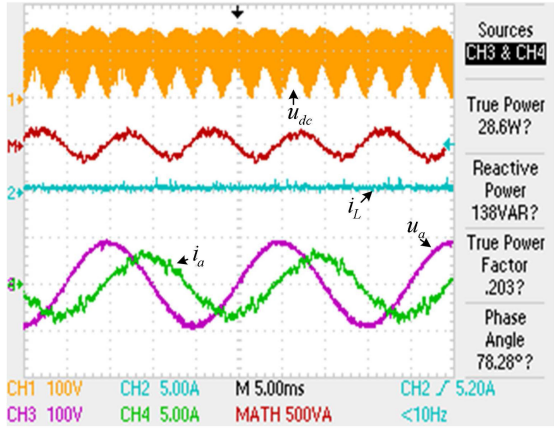


(b)

Fig. 18. Transient waveforms at $m_i = 0.5$ and with reference current changing from $i_q = 0$ to $i_q^* = -3$A: (a) method I; (b) method II.



(a)



(b)

Fig. 19. Measured waveforms with $m_i = 0$ and $i_q^* = -3$ A: (a) method I; (b) method II.

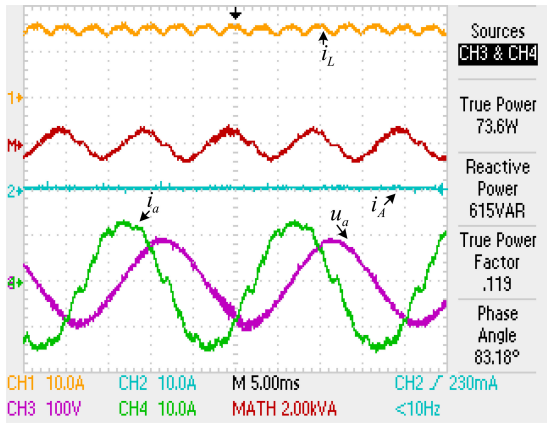


Fig. 20. Measured waveforms with method II when $m_i = 0$ and $n_i = 1$.

independent of the load conditions, without considering practical constraints such as switching capacity, efficiency, and cost. In fact, in the case of high voltage transfer ratio, the required inductor current may be very large to obtain the given input reactive power, which would result in serious switching stress and degrade input current quality. Therefore, from a practical point of view, the converter is mainly suitable for the applications where the voltage transfer ratio is not too high but the required input reactive power is large.

APPENDIX

For (12), it can be transformed into such a problem to find a maximum n_i when satisfying the following constraints

$$\begin{cases} n_i \sin(\pi/3+\alpha) + n_i \sin(\pi/3-\alpha) \le 1 \\ m_i \sin(\pi/6-\alpha) + n_i \sin(\pi/3-\alpha) \le 1 \\ n_i \sin(\pi/3+\alpha) + m_i \sin(\pi/6+\alpha) \le 1 \end{cases} \tag{28}$$

where $-\frac{\pi}{6} \le \alpha \le \frac{\pi}{6}$. Simplifying (28), it yields

$$\begin{cases} n_i \le \dfrac{1}{\sqrt{3}\cos(\alpha)} \\ n_i \le \dfrac{1}{\sin(\pi/3-\alpha)}\left[1 - m_i \sin(\pi/6-\alpha)\right] \\ n_i \le \dfrac{1}{\sin(\pi/3+\alpha)}\left[1 - m_i \sin(\pi/6+\alpha)\right] \end{cases}. \tag{29}$$

To satisfy (29), the maximum feasible n_i is written as

$$n_{i\max} = \min\left\{\min_{\alpha}\frac{1}{\sin(\pi/3+\alpha)+\sin(\pi/3-\alpha)}\right.$$
$$\min_{\alpha}\frac{1}{\sin(\pi/3-\alpha)}\left[1-m_i\sin(\pi/6-\alpha)\right]$$
$$\left.\min_{\alpha}\frac{1}{\sin(\pi/3+\alpha)}\left[1-m_i\sin(\pi/6+\alpha)\right]\right\}. \quad (30)$$

Simplifying (30), it yields

$$n_{i\max} = \min\left\{\frac{1}{\sqrt{3}}, 1-\frac{\sqrt{3}}{2}m_i\right\}. \quad (31)$$

It is obvious that $q=\frac{\sqrt{3}}{2}m_i = 1-\frac{1}{\sqrt{3}}$ is a critical point, and $n_{i\max}$ could also be expressed as (13).

For (16), it can be stated as the problem to find a maximum n_i when satisfying the following constraints:

$$\begin{cases} n_i\sin(\alpha)+n_i\sin(\pi/3-\alpha)+m_i\sin(\pi/6+\alpha)\le 1 \\ m_i\sin(\pi/6-\alpha)+n_i\sin(\pi/3-\alpha)+m_i\sin(\pi/6+\alpha)\le 1 \end{cases} \quad (32)$$

where $0\le\alpha\le\frac{\pi}{6}$.

Equation (32) is simplified as

$$\begin{cases} n_i \le \dfrac{1-m_i\sin(\pi/6+\alpha)}{\cos(\alpha-\pi/6)} \\ n_i \le \dfrac{1-m_i\cos(\alpha)}{\sin(\pi/3-\alpha)}. \end{cases} \quad (33)$$

To satisfy (33), the maximum feasible n_i are

$$n_{i\max}=\min\left\{\min_{\alpha}\frac{1-m_i\sin(\pi/6+\alpha)}{\cos(\alpha-\pi/6)}, \min_{\alpha}\frac{1-m_i\cos(\alpha)}{\sin(\pi/3-\alpha)}\right\}. \quad (34)$$

Simplifying (34), it yields

$$n_{i\max} = \min\left\{1-\frac{\sqrt{3}}{2}m_i, \frac{2}{\sqrt{3}}(1-m_i)\right\}. \quad (35)$$

If $1-\frac{\sqrt{3}}{2}m_i = \frac{2}{\sqrt{3}}(1-m_i)$, then the critical point is solved as $q_{c2}=2\sqrt{3}-3$, and $n_{i\max}$ could also be expressed as (17).

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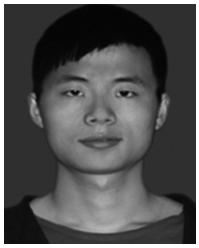

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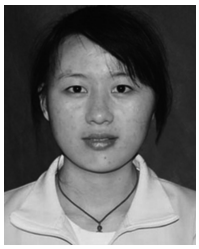

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