Conceptual Study of Sub-600 V IGBTs

Friedhelm D. Bauer, *Senior Member, IEEE*

***Abstract*—Very low voltage, 60–600 V insulated-gate bipolar transistors (IGBTs) were compared to power MOSFETs with conventional and superjunction drift layers of identical voltage classes using mixed-mode numerical device simulation. This study was done in the light of forthcoming 400 V class IGBTs for use in electric vehicle/hybrid electric vehicle: the 600 V borderline, which previously separated the bulk of power MOSFET from IGBT applications, has become fragile recently. We find that the 400 V class must not represent a lower limit for IGBTs based on silicon: in fact, LV IGBTs could offer lower losses down to the 60–100 V level. Most importantly, low-voltage IGBTs may outperform power MOSFETs not only with respect to on-state voltage drop but also regarding switching offering up to 30% lower turn-off losses. This paper presents physics-based arguments focusing on the device transconductance to augment these projections. LV IGBTs or hybrid devices (monolithic integration of MOSFET plus IGBT) could become lower cost, high performance alternatives to SJ power MOSFETs thanks to short development cycles common in mature silicon technologies.**

***Index Terms*—Emitter efficiency, insulated-gate bipolar transistor (IGBT), power MOSFET, superjunction (SJ) power MOSFET, technology tradeoff.**

I. Introduction

In recent years, the 600 V boundary has become a major borderline across the landscape of power semiconductor devices separating power MOSFET and insulated-gate bipolar transistor (IGBT) territories going by device characteristics, performance, and applications. It emerged as a result of technological evolution of both device concepts driven by user requirements in the field of power electronics. Invented in the late 1970s, the vertical power MOSFET went through a succession of structural modifications of the MOS gate debuting with a V-shaped gate geometry [1]. Back then, this concept failed to satisfy manufacturing requirements and was soon replaced by devices with planar MOS gate geometries [2]. Adopting trench etching processes from the microelectronics industry, this device generation was superseded by U-shaped trench-gate power MOSFETs [3] eliminating the parasitic JFET resistance [4]. The trench-gated power MOSFET has become the cornerstone for low-voltage power semiconductor switches making possible a continued reduction of on-resistance $R_{D\mathrm{Son}}$ by means of cell shrinking techniques [5], [6]. The period of successfully increasing cell densities stopped several years ago, realizing that further minimization of the on-resistance also involved an adverse behavior affecting device capacitances and switching losses [7].

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The author is with ABB Switzerland, Ltd., Corporate Research Center, Baden CH-5405, Switzerland (e-mail: friedhelm.bauer@ch.abb.com).

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Conceptually, on-resistance and breakdown voltage are both strongly depending on the drift layer doping concentration [2] resulting in a strong power law dependence of $R_{D\mathrm{Son}}$ on V_{br} (breakdown voltage) [8]. With silicon as the semiconductor material, this law precludes the design of higher voltage power MOSFETs ($>$500 V) with technically appealing characteristics. Positioning power MOSFETs at and slightly above the 600 V borderline thus required the invention and commercialization of the superjunction (SJ) power MOSFET [9]. With these device geometries, the charge compensation principle helps increasing doping concentrations in the drift layer paving the way for HV power MOSFETs in the 600 V class; nevertheless, only few commercial offerings with V_{br} as high as 900 V have become available in the past. The penetration of the 600 V borderline has remained weak compared to the continuing expansion of the SJ technology toward lower power MOSFET voltage classes as low as 30 V [10].

In the first place, the concept of the IGBT was derived from the power MOSFET in the 1980s [11], [12]. Owing to its bipolar conduction mechanism providing very low on-state voltage drop by means of excess base charge, the IGBT evolved from the 300 to 600 V range to the 6.5 kV voltage level [13]. Similar to the case of the power MOSFET, this evolution proceeded from lower to higher blocking voltages passing the milestones of trench-gate IGBTs [14] and the field-stop concept [15]. Owing to its focus on higher blocking voltages, the IGBT did not experience a similar miniaturization process of the cell layout as was the case with the power MOSFET. While the design of power MOSFETs with low blocking voltages required the epitaxial growth of a thin drift layer on top of a thick, highly doped wafer substrate and early IGBTs were structured in the same way, most IGBTs are presently manufactured using wafers of varying thicknesses with relatively low doping ($\sim 10^{14}$ cm^{-3}). For 600 V IGBTs, the challenge of handling thin (60–70 μm) wafers with 200 or even 300 mm wafer diameter has been mastered by the industry [16].

At present, the well-established landscapes of power MOSFETs and IGBTs begin to experience pressure from wide bandgap (WBG) power semiconductor devices made using materials such as SiC and GaN [17]. The properties of some WBG semiconductors (critical breakdown field, saturated drift velocity, and thermal conductivity) allow conceiving new power semiconductor devices with largely superior performance. This fact is known since more than two decades [18] but a noticeable market appearance of WBG power devices is just about to happen these days [19]. Given the long time scale for developing disruptive WGB power device technologies, it is evident that mature silicon based technologies will successfully compete with WBG devices for a number of years to come. The SJ power MOSFET [9] is a prominent example illustrating this situation; presented for the first time around 1995 when WBG-related research started, the technology is about to become a multibillion market these

days supported by most major players in the power semiconductor business.

A similar event is likely to happen in the future with IGBTs [20], [21] thanks to the soaring demand in automotive power semiconductors and white goods. Major companies are preparing for the pending commercialization of 40-μm-thick 400-V field-stop IGBTs expected to take place in 2014. To meet low cost targets, a market leader will use a 300 mm wafer fab for the first time in the history of power semiconductor device manufacturing [16], [22]. Some market studies predict a massive penetration of IGBTs into the power MOSFET domain stopping short of 200 V [22]. These trends could initiate a likely paradigm change in the perception of power MOSFETs versus IGBTs on both sides of the 600 V borderline.

The investigation presented in this paper is aimed at gaining a broader, device physics-based understanding of the present and future transformations of power MOSFET and IGBT landscapes. As per the current developments [20], IGBTs are no longer the slow switches they were taken for only some years ago. We offer arguments backed by extensive numerical device simulations for a penetration of IGBTs into the MOSFET domain down to the 100 V range. We see a likelihood that IGBTs might challenge SJ power MOSFETs not only with respect to on-state voltage drop but also in terms of turn-off switching losses. Further on, a new class of hybrid device concepts featuring monolithically integrated MOSFET and IGBT structures could emerge at very low blocking voltages.

We observed first evidence for fast switching IGBTs in the context of a comparison of SJ IGBTs and SJ power MOSFETs [23]. This study revealed that the p-emitter injection efficiency not only affects turn-off losses via an impact on tail currents and $dV_{\rm ce}/dt$ during turn-off [24] (domain of high p-emitter injection efficiencies: technology tradeoff curves $E_{\rm off}(V_{\rm ce})$ characterized by negative slope $dE_{\rm off}/dV_{\rm ce} < 0$). IGBT tail currents result from slow recombination of charge carriers during the charge storage phase at the end of the turn-off transient. The transconductance g_m and the slope of the collector current density dJ_c/dt during turn-off [25] are also strongly affected by p-emitter properties. Accordingly, SJ IGBTs with comparatively weak p-emitters can rival SJ MOSFETs of the 600 V class even in terms of $E_{\rm off}$. Weak p-emitters give rise to IGBT tradeoff curves with anomalous slopes $dE_{\rm off}/dV_{\rm ce} > 0$ [23].

This paper shows that similar p-emitter effects can be expected in conventional IGBT geometries. It discusses the transition from predominantly unipolar to strongly bipolar characteristics in conventional LV IGBTs. These IGBT structures were compared by means of numerical device simulation to conventional and SJ power MOSFETs using the Sentaurus Device simulator from Synopsys, Inc. [26]. Given the broad range of device geometries and voltage classes and the lack of experimental investigations, numerical device simulation represents a convenient, well-suited tool for the purpose of technological forecasting. Section II offers an introduction to the simulation setup including the details of the device geometries; the mixed-mode simulation turn-off conditions are also discussed here. Highlighting 600 V devices, Section III-A presents the change of transient IV characteristics resulting from a broad variation of the p-emitter injection efficiency. Continuing with the presentation of results in Section III-B, the main contributions to the total turn-off loss ($E_{\rm off}$) during the Miller interval, the voltage ($V_{\rm ce}$) rise and the current (J_c) fall period are analyzed with respect to their dependence on p-emitter properties and for a number of voltage classes. The comparison of LV IGBT losses with conventional and SJ power MOSFET losses follows in Section III-C. The discussion in Section IV touches on a number of related aspects discussing transconductance and turn-off dJ_c/dt models in order to back up the interpretation of the numerical results. The remaining part of Section IV is dedicated to a discussion of technological aspects of LV power devices. This paper is concluded in Section V.

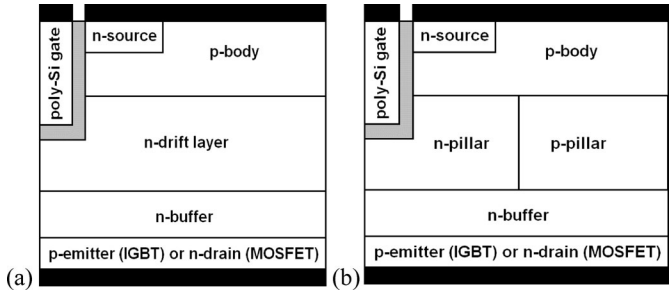

Fig. 1. Schematic half-cell cross sections of vertical trench-gate power semiconductor devices with (a) conventional and (b) SJ drift layer. IGBTs and conventional MOSFETs have structures as shown in (a) while SJ power MOSFETs and SJ IGBTs are represented by the geometry in (b).

II. Simulation Experiment

Fig. 1 presents schematic device cross sections of power MOSFETs/IGBTs (half-cell geometries) with conventional [see Fig. 1(a)] and SJ drift layers [see Fig. 1(b)]; to facilitate comparisons, all geometries feature the same MOS trench gate (1 μm wide, 5 μm deep, gate oxide thickness: 0.1 μm). Four groups (voltage classes: 60, 120, 300, and 600 V) are created with total device thicknesses of 10, 15, 30, and 50 μm, respectively. The respective drift layer doping concentrations are 1×10^{15}, 6×10^{14}, 2×10^{14}, and 1×10^{14} cm^{-3}. The cell pitch is 20 μm for all geometries; with our choice of the cell design, there is a realistic chance to make short-circuit failure modes controllable even with the lowest IGBT voltage classes and to improve the ruggedness as well.

All devices are of the field-stop type and share the same n-doped buffer layer design (5 μm width with peak concentration of 8×10^{16} cm^{-3}). The IGBT p-emitter is a p-doped layer (thickness: 0.5 μm) with Gaussian dopant distribution and peak concentrations varying from 1×10^{17} to 1×10^{19} cm^{-3} at the anode surface. This is equivalent with a range of p-emitter injection efficiencies γ_e spanning the range from quasi-unipolar to strong bipolar characteristics. All power MOSFET geometries feature a drain layer with a peak doping concentration of 4.5×10^{18} cm^{-3} and a thickness of 0.5 μm. Bulk carrier lifetimes are 8 and 2 μs (400 K) for electrons and holes, respectively, for all device structures. Conventional power MOSFET and IGBT geometries share the same drift layer doping concentrations.

The SJ MOSFETs feature a typical symmetrical design for the n- and p-doped pillars [see Fig. 1(b)] with equal pillar widths of 10 μm and doping concentrations of 3×10^{15} cm^{-3}. Total device thicknesses are the same for SJ MOSFETs and for conventional MOSFETs/IGBTs. SJ geometries with narrower pillars and higher pillar doping were also examined, however, on a selective basis. The same applies to SJ IGBTs. Based on a standard circuit for hard, inductive switching $J_c(t)$ and $V_{\rm ce}(t)$ traces were simulated at $T = 400$ K to derive $E_{\rm off}$ data (integration interval: 20 μs). Turn-off current densities were varied from 25 to 200 A/cm^2. The dc-link voltages $V_{\rm DC}$ were set to 30, 80, 200, and 350 V for the blocking voltage classes 60, 120, 300, and 600 V. The gate resistor for a 1 cm^2 die had a fixed value of 20 Ω to allow simple comparisons among different devices. Identical values for the circuit inductance (30 nH) and the common emitter inductance (4 nH) were used in all simulations. Furthermore, the default Sentaurus parameter file was used and the following models were active: Shockley–Reed–Hall and Auger recombination, carrier mobility including high field saturation, normal electric field dependence and carrier-carrier scattering. The default impact ionization model based on Van OverStraeten parameters was equally activated [26].

III. Results

A. Variation of p-Emitter Injection Efficiency: 600 V Range

Fine-tuning IGBT emitter characteristics to match device performance to application requirements is a widely used technique among IGBT manufacturers. The best compromise between strong minority carrier injection (holes) into the drift layer (low on-state voltage drop) and fast extraction of the excess base charge during turn-off (transparency of the p-emitter for electrons) is targeted. The impact of a variation of the p-emitter injection efficiency on $V_{\rm ce,on}$ and $E_{\rm off}$ is often portrayed in technology tradeoff curves $E_{\rm off} = f(V_{\rm ce})$. There are several techniques available to change the injection efficiency of a bipolar emitter: thickness and peak doping concentration have the strongest impact and are well controllable technology parameters. Other IGBT design parameters affecting the injection efficiency are the doping density and width of the n-buffer layer as well as carrier lifetimes.

We used the variation of the p-emitter surface concentration to evaluate the effect of the injection efficiency on the major contributions to the turn-off losses. The injection efficiency was obtained from the ratio of hole current density to total collector current (100 A/cm^2 at 400 K in Fig. 2) at the interface between p-emitter and anode metallization; this yields a minimal deviation (<5%) from the textbook definition for γ_e, which would require electron and hole currents to be evaluated at the depletion boundaries of the forward biased PN junction. Given the shallow depth (0.5 μm) of the p-emitter layer, recombination losses in the neutral emitter region are negligible even for the highest p-emitter surface concentrations. Thus, the simplified evaluation of γ_e does not compromise precision of the analysis. Fig. 2 shows some quintessential collector current and collector–emitter voltage transients of 600 V IGBTs with high, medium, and low γ_e. The initial turn-off phase coincides with

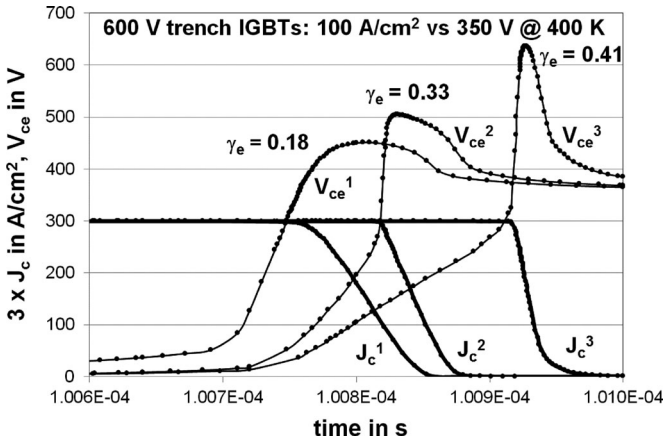

Fig. 2. $J_c(t)$ and $V_{\rm ce}(t)$ traces during hard inductive turn-off for 600 V trench IGBTs (100 A/cm^2); the p-emitter injection efficiency increases from the left ($V_{\rm ce}^1$, J_c^1 with $\gamma_e = 0.18$; quasi-unipolar behavior) to the right ($V_{\rm ce}^3$, J_c^3 with $\gamma_e = 0.41$; typical bipolar behavior). For the traces $V_{\rm ce}^2$, J_c^2 with $\gamma_e = 0.33$, minimum turn-off losses are observed.

the gate voltage plateau (100.6–100.7 μs in Fig. 2) when the gate–source capacitance is discharged. $V_{\rm ce}$ rises slowly from the on-state voltage to a value of some tens of volts. The impact of injection efficiency on turn-off losses during this interval is rather small; with increasing γ_e, the Miller interval becomes longer; however, $V_{\rm ce}$ will also be smaller resulting in an approximately constant contribution to the total turn-off losses.

The second phase is characterized by a fast rise of the collector–emitter voltage controlled by the excess charge extraction from the n-drift region. The effect of turn-off current and temperature on $dV_{\rm ce}/dt$ during IGBT turn-off was discussed in [24]; the same analytical model can be extended to explain the effect of the injection efficiency on $dV_{\rm ce}/dt$ as apparent in Fig. 2. With the collector current being constant during phase 2, the respective turn-off loss contribution will rise strongly with γ_e. The third and final phase is governed by the decay of the collector current. Fig. 2 implies that dJ_c/dt and the corresponding losses will increase for low emitter injection efficiencies. At high injection efficiencies, the loss contribution from phase 3 will increase due to the appearance of tail currents of bipolar origin. This leads to a U-shaped dependence of the loss contributions associated with the collector current decay. Fig. 3 shows these three $E_{\rm off}$ contributions with the total turn-off losses as a function of the injection efficiency γ_e for the 600 V IGBTs and the turn-off conditions corresponding to Fig. 2. Plotting the $E_{\rm off}$ data from Fig. 3 as technology tradeoff curves ($E_{\rm off} = f(V_{\rm ce})$) as shown in Fig. 4 reveals that a second curve section characterized by $dE_{\rm off}/dV_{\rm ce} > 0$ emerges for low injection efficiencies in addition to the common, well-known branch with $dE_{\rm off}/dV_{\rm ce} > 0$. This new branch was first observed in a study on SJ IGBTs [23]; according to Fig. 4, the injection efficiency variation has a similar effect in conventional and SJ IGBTs. The data constituting the right-hand side curves in Fig. 4 (very low γ_e or high $V_{\rm ce,on}$) serve as representatives of unipolar devices (power MOSFETs). Thus, we conclude that $E_{\rm off}$-optimized IGBTs should be able to switch faster (lower $E_{\rm off}$) than comparable power MOSFETs.

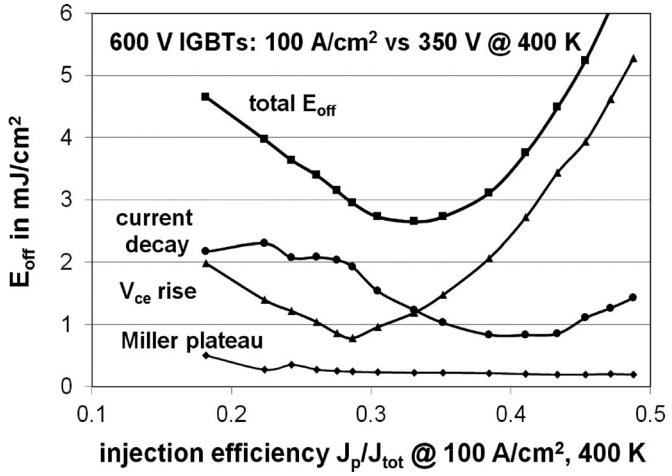

Fig. 3. Turn-off switching loss contributions (600 V class IGBTs) from initial period (Miller phase: 0–15 V), voltage rise interval (15–350 V) and current decay phase (350 V—total) and total turn-off losses plotted versus p-emitter injection efficiency.

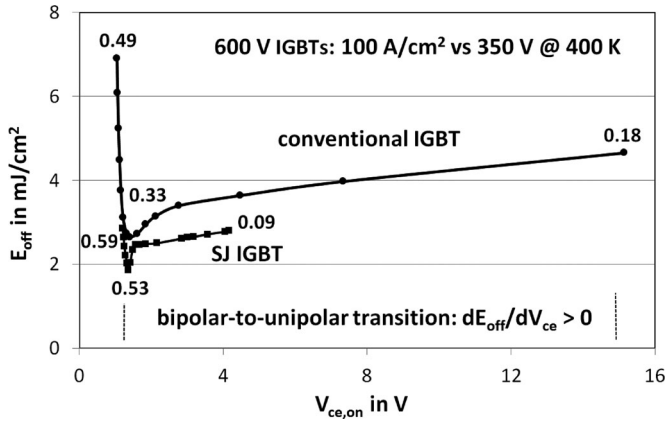

Fig. 4. Technology tradeoff curves for 600 V IGBTs (conventional and SJ drift layers). Numbers indicate p-emitter injection efficiencies. Conventional IGBT: 0.49—strong bipolar behavior: 0.33—minimum $E_{\rm off}$: 0.18—quasi-unipolar characteristics. The results for the SJ IGBT were taken from [23].

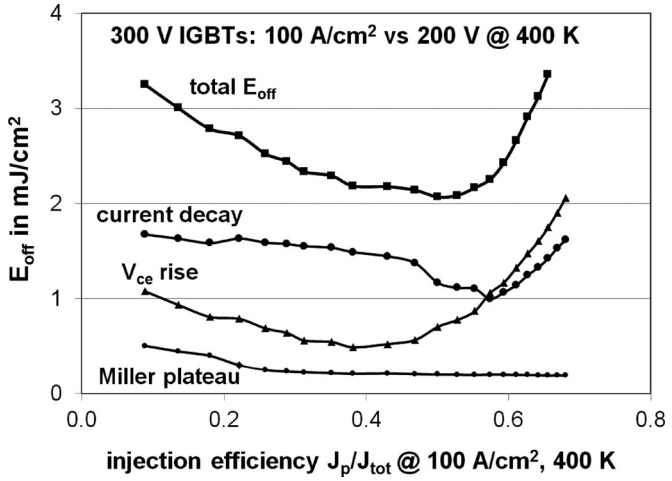

Fig. 5. Turn-off switching loss contributions (300 V class IGBTs) from initial period (Miller phase: 0–15 V), voltage rise interval (15–200 V) and current fall phase (200 V—total) and total turn-off losses plotted versus p-emitter injection efficiency.

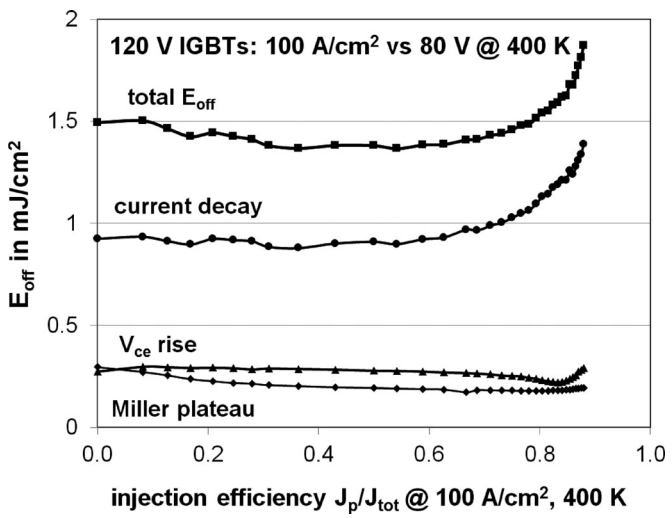

Fig. 6. Turn-off switching loss contributions (120 V class IGBTs) from initial period (Miller phase: 0–15 V), voltage rise interval (15–80 V) and current fall phase (80 V—total) and total turn-off losses plotted versus p-emitter injection efficiency.

B. Low-Voltage IGBTs

This section presents results of an analogous analysis of IGBTs with blocking voltages far below 600 V. Applying the same injection efficiency variation to 120 and 300 V IGBTs, plots of the three major turn-off loss contributions versus γ_e are shown in Fig. 5 (300 V) and Fig. 6 (120 V). The turn-off current density was kept constant for the three voltage classes. Given that all devices share the same MOS cell geometry, it is comprehensible that the turn-off loss contribution from phase 1 (Miller plateau) has similar values for the three voltage classes. Turn-off losses generated during the fast rise of the emitter–collector voltage (phase 2) decrease for low voltage IGBTs as a result of the reduced thickness of the n-drift layer. Likewise, the amount of excess charge will be smaller in low-voltage IGBTs giving rise to a less pronounced effect of the tail currents appearing at high γ_e. Turn-off loss contributions from phase 3 (decay of the collector current) become dominant for low-voltage layouts. Total turn-off losses show a distinct minimum at $\gamma_e = 0.33$ (600 V, Fig. 3) and at $\gamma_e = 0.5$ (300 and 120 V). For the 120 V case, the total $E_{\rm off}$ curve (see Fig. 6) assumes a flat, broad minimum along the γ_e-axis ($\gamma_e = 0$–0.8). Putting this result in relation with power MOSFETs, emitter injection efficiencies of IGBTs could be increased up to 0.8 without exceeding the turn-off losses of the corresponding power MOSFET. In addition, at large γ_e, the IGBT will also offer drastically lower on-state voltage drop.

C. Comparison With Power MOSFETs

Given the broad penetration of SJ power MOSFETs into the sub-600 V landscape, an objective comparison of LV IGBTs with power MOSFETs has to consider conventional MOSFET

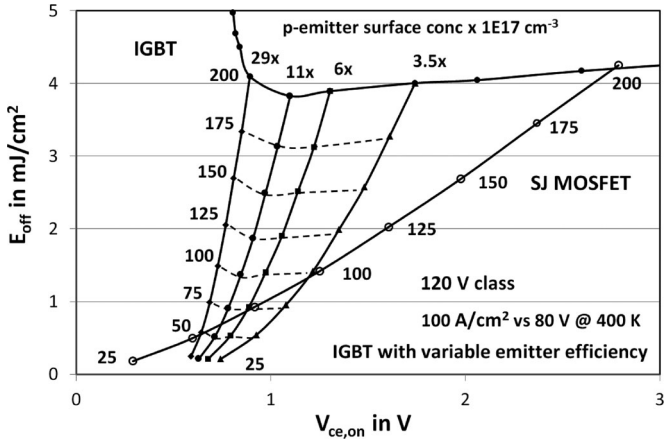

Fig. 7. Technology tradeoff curves for 120 V IGBTs (conventional n-drift layer, four different p-emitter surface concentrations) for various turn-off current densities from 25 to 200 A/cm^2. Corresponding turn-off data ($E_{\rm off}$, $V_{\rm ce}$) for a 120 V SJ power MOSFET are included for comparison.

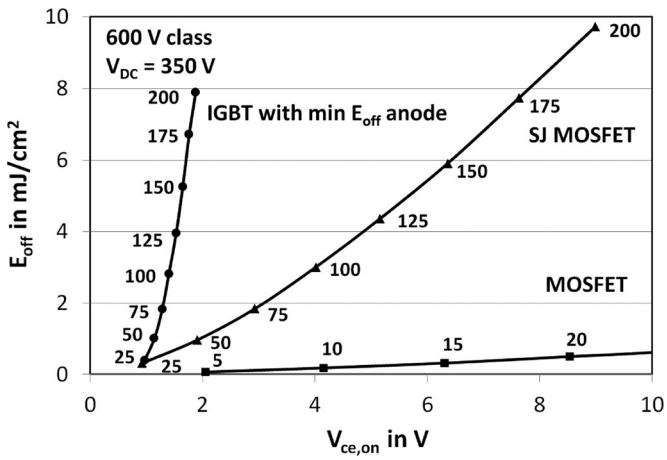

Fig. 8. Comparison of 600 V class devices: numbers refer to turn-off current densities (hard, clamped inductive turn-off at $V_{\rm DC} = 350$ V, 400 K).

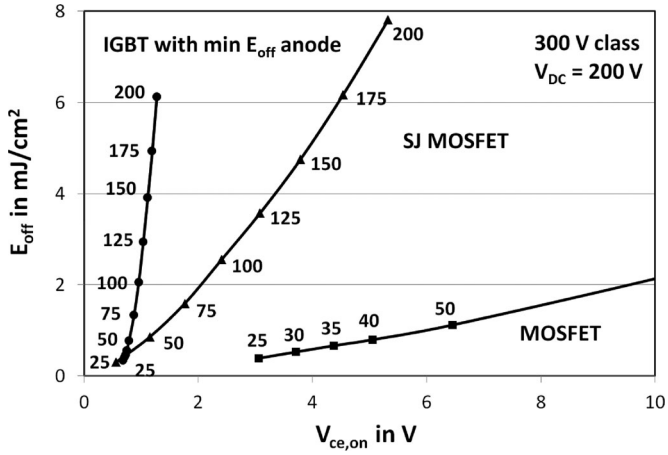

Fig. 9. Comparison of 300 V class devices: numbers refer to turn-off current densities (hard, clamped inductive turn-off at $V_{\rm DC} = 200$ V, 400 K).

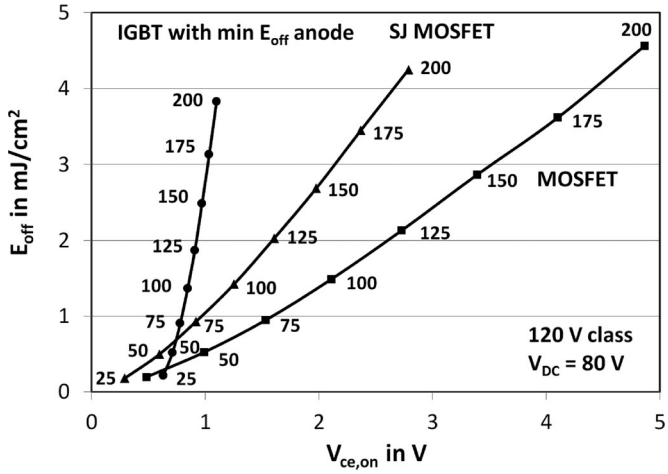

Fig. 10. Comparison of 120 V class devices: numbers refer to turn-off current densities (hard, clamped inductive turn-off at $V_{\rm DC} = 80$ V, 400 K).

geometries as well as SJ MOSFETs. To keep the number of design variables low, one single, state-of-the-art SJ configuration was selected for the bigger part of this comparison (see Section II). SJ geometries with thinner pillars were only investigated selectively to back up the interpretation of the results. Fig. 7 serves the purpose to illustrate this comparison presented in Figs. 8–10.

For the case of 120 V class devices, IGBT technology tradeoff curves (dashed lines) are plotted in Fig. 7 for turn-off current densities from 25 to 200 A/cm^2 (25 A/cm^2 steps). Minimum $E_{\rm off}$ is reached for a p-emitter surface concentration of 1.1×10^{18} cm^{-3}. $E_{\rm off}$–$V_{\rm ce}$ data for different turn-off current densities are merged into a characteristic curve for a particular p-emitter. In this way, four characteristic curves are generated for the 120 V IGBTs in Fig. 7 with one curve highlighting the minimum $E_{\rm off}$ design. Pairs of values ($E_{\rm off}$–$V_{\rm ce}$) resulting from turn-off simulations of a 120 V SJ power MOSFET (design details in Section II) at the same conditions as used for the IGBTs are included in Fig. 7. This procedure was applied to all device groups in the voltage classes considered (conventional IGBT, conventional power MOSFET, SJ power MOSFET). Fig. 8 presents the results for devices in the 600 V class; given a PN junction built-in voltage for silicon of about 0.7 V, minimum on-state voltage drop for IGBTs will be limited by this value. For 600 V design rules in particular, power MOSFETs acquire significant contributions to the on-resistance from the comparatively thick and low doped n-drift layer: conventional 600 V power MOSFETs will not be able to compete with IGBTs. Due to its increased doping concentration of the pillars, the SJ power MOSFET is in a better position: however, as indicated by the crossover of the IGBT and SJ MOSFET curves in Fig. 8, it can outperform the IGBT only at turn-off current densities below 25 A/cm^2. The data given in Figs. 8–11 correspond to an operating temperature of 400 K. Arguably, the IGBT advantage will increase at even higher operating temperatures. Moving on from the 600 V class to 300 V (see Fig. 9) and further on to 120 V (see Fig. 10) shows that the limitation of power MOSFETs arising from the drift layer resistance will become weaker as expected. We observe a shift of the crossover point (equal on-state drop

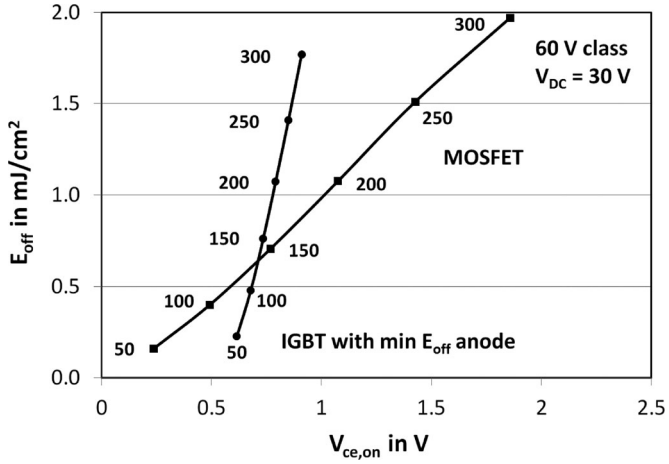

Fig. 11. Comparison of 60 V class devices: numbers refer to turn-off current densities (hard, clamped inductive turn-off at $V_{\rm DC} = 30$ V, 400 K). For 60 V devices, the SJ power MOSFET geometry was discarded from the comparison.

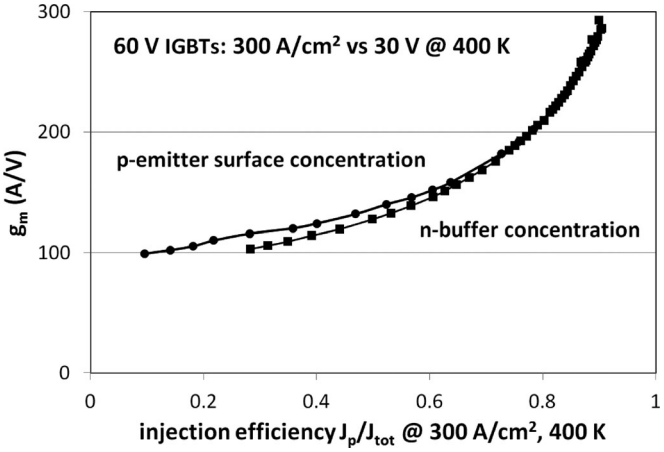

Fig. 12. Impact of p-emitter injection efficiency on IGBT transconductance at 300 A/cm^2, 400 K, $V_{\rm ce} = 30$ V (relevant condition at the beginning of the current decay phase). Similar curve shapes result independent of the technological approach used for the emitter efficiency variation.

and turn-off loss for both IGBT and power MOSFET) toward higher turn-off current densities (35 A/cm^2 for 300 V class devices, Fig. 9 and 60 A/cm^2 for 120 V devices, Fig. 10). For 60 V class design rules, drift layers of conventional devices are only a few microns thick; doping concentrations approach or even exceed levels of 1×10^{15} cm^{-3}. The advantage of SJ designs with respect to conventional drift layers will thus vanish in the 60 V class and below. Thus, only 60 V devices with conventional drift layers were considered (see Fig. 11). 60 V IGBTs should show significantly better performance that power MOSFETs starting with current densities around 150 A/cm^2. Note that IGBTs show persistently lower turn-off losses across the full voltage range from 60 to 600 V. As a last remark, as shown in Fig. 7, IGBT on-state voltage drop can be further reduced by slightly increasing the emitter injection efficiency beyond the minimum-$E_{\rm off}$ value. The resulting increase of $E_{\rm off}$ may not exceed a few percent.

IV. Discussion

A. Transconductance

Simple analytical models state that the transconductance g_m of IGBTs can be expressed using the respective formula for the MOSFET and a prefactor [8]

$$g_m^{\rm IGBT} = \frac{1}{1-\alpha_{\rm pnp}} \bullet \frac{\mu_{\rm ch} \bullet C_{\rm ox} \bullet Z}{L_{\rm ch}} \bullet (V_{\rm ge} - V_{\rm th}). \quad (1)$$

The prefactor $1/(1-\alpha_{\rm pnp})$ reflects the impact of the bipolar gain $\alpha_{\rm pnp}$ of the IGBT on g_m. All variables in (1) have their usual meaning: channel mobility $\mu_{\rm ch}$, oxide capacitance $C_{\rm ox}$, channel length $L_{\rm ch}$, channel width Z, gate–emitter voltage $V_{\rm ge}$, and threshold voltage $V_{\rm th}$. In its simplest representation, $\alpha_{\rm pnp}$ is a product of emitter injection efficiency γ_e and the base transport factor α_T yielding a simple analytical relation of IGBT and MOSFET transconductances

$$g_m^{\rm IGBT} = \frac{g_m^{\rm MOSFET}}{1-\alpha_T \bullet \gamma_e}. \quad (2)$$

According to (2), IGBT tranconductance can be substantially larger than that of power MOSFETs with the same MOS gate structure depending on the emitter design. Taking into consideration a slightly more sophisticated model for α_T which accounts for the carrier diffusion lengths in the carrier plasma, it is also apparent from (2) that strong carrier lifetime reduction would be counterproductive when high IGBT transconductance is the goal. For 60 V devices, the simulation results suggest that g_m can be increased by a factor of 3 (see Fig. 12) through an increase of the p-emitter injection efficiency from 0.1 to 0.9. As mentioned before, p-emitter properties can be affected in different ways resulting in similar $g_m = f(\gamma_e)$ relationships as shown in Fig. 12 for two cases (variation of p-emitter surface concentration versus peak doping concentration variation of the n-buffer layer). Note that this discussion relates to the transconductance g_m evaluated at $V_{\rm ce} = V_{\rm DC}$.

B. dJ_c/dt at Turn-Off

The control theory for MOS-controlled power devices provides simple models for the rates of current and voltage transitions during switching [25]; (3) is the relevant equation for dJ_c/dt at turn-off with the gate resistor R_g, circuit stray inductance L_s, gate–collector capacitance $C_{\rm gc}$, gate–emitter capacitance $C_{\rm ge}$, off-state gate voltage $V_{\rm EE}$, and turn-off current density J_c

$$\frac{{\rm d}J_{c,\rm off}}{{\rm d}t_{t=0}} = \frac{g_m \bullet \left[V_{\rm EE} - \left(V_{\rm th} + \frac{J_c}{g_m}\right)\right]}{R_g \bullet (C_{\rm gc} + C_{\rm ge}) + R_g \bullet g_m \bullet L_s}. \quad (3)$$

Neglecting the inductive factor and the effect of the gate bias $V_{\rm EE}$ and inserting g_m from (2) yields a relation between the rate of change of the collector current per time and the p-emitter injection efficiency

$$\frac{{\rm d}J_{c,\rm off}}{{\rm d}t_{t=0}} = -\frac{1}{R_g \bullet (C_{\rm gc} + C_{\rm ge})} \bullet \left(\frac{g_m^{\rm MOSFET} \bullet V_{\rm th}}{1-\gamma_e} + J_c\right). \quad (4)$$

TABLE I
COMPARISON OF MOSFET ON-RESISTANCES FOR VARIOUS VOLTAGE CLASSES (400 K)

Commercial dies		Simulated geometries	
Voltage class	R_{DSon} (mΩ·cm^2)	Voltage class	R_{DSon} (mΩ·cm^2)
75 V	1.5	60 V (conv)	6
100 V	1.5–2.4	120 V (SJ)	13
250 V	30	300 V (SJ)	27
600 V	50	600 V (SJ)	40

For a variation of γ_e, the prediction of (4) reflects the simulated turn-off curve traces shown in Fig. 2—increasing γ_e causes an increase of the absolute value of $dJ_{c,\mathrm{off}}/dt$. As for the case of the IGBT turn-off dV_{ce}/dt and its temperature dependence [24], a charge extraction capacitance should be considered in (4) to model the IGBT $dJ_{c,\mathrm{off}}/dt$ more precisely. However, its impact on $dJ_{c,\mathrm{off}}/dt$ may be lower than its effect on dV_{ce}/dt as a result of the high collector–emitter voltage (V_{ce}–V_{DC}).

C. Power MOSFET Versus IGBT Technology

The results shown in Figs. 7–11 allow the derivation of specific 400 K on-resistance values for the respective conventional and SJ power MOSFET geometries. These data were compared to specific on-resistances of commercial bare die MOSFETs from a US manufacturer at 300 K (datasheets provide essential die size information) after compensation for the temperature difference (multiplication of 300 K values by a factor of 1.5). The comparison shown in Table I yields increasingly large differences up to a factor of 5 for the lower voltage classes between simulated and commercial power MOSFETs. In fact, low-voltage power MOSFETs use significantly smaller feature sizes (cell pitch, trench depth, gate oxide thickness, and channel length) than those used in the simulation experiment. With reference to (2) (see Section IV-A), it can be argued that similarly downscaled LV IGBTs could rival their MOSFET counterparts also regarding the on-resistance.

An alternative path of LV IGBT development could focus on device ruggedness and SOA criteria profiting from the emerging cost pressure on SJ MOSFET technologies. Ultimately, triggering of the parasitic bipolar transistor in power MOSFETs (avalanche behavior) and the thyristor in IGBTs (SOA, short-circuit capability and avalanche capability) proceeds via similar mechanisms. In both devices, these parasitic effects can be addressed using similar design approaches. Compared to power MOSFET designs, a low-cost LV IGBT technology could employ more relaxed design rules partly trading off minimum IGBT on-state drops against short-circuit capability, better avalanche behavior, and eventually also against lower gate charge. These arguments affected our choice of a comparatively wide cell pitch in the simulation experiment. In principle, technologies for reverse conducting IGBTs would allow the implementation of integrated body diodes. However, cost and application requirements will play the decisive role in the choice of optimum freewheeling diodes (SiC diodes versus Si diodes). In some cases, integrating body diodes together with the switch may lead to design tradeoffs.

D. SJ Versus Conventional Geometries

At the 600 V level, a competition between fast IGBTs and SJ power MOSFETs has already started [20]. In the light of our study, IGBTs with conventional drift layers could have a chance to compete with SJ power MOSFETs even in the 100 V class (see Fig. 10), both in terms of on-state voltage drop and turn-off losses, and in particular at high collector current densities. With some likelihood, these benefits would be available at lower component cost (conventional versus SJ technology). The performance of SJ power MOSFETs is improved using higher doping concentrations for the p- and n-doped pillars; this, however, accentuates the requirements regarding the charge balance in the columns of the SJ MOSFET. Moreover, the width of the pillars must be reduced appropriately. These technological challenges have been limiting the pace at which SJ MOSFET technology further proceeds toward better performance. Below 600 V, pure SJ IGBT concepts [23] will progressively lose their attraction for a number of reasons: in SJ IGBTs, high pillar doping levels favor lower conduction and switching losses as they can compensate for a significant amount of excess base charge present in the conventional structure. This effect is powerful in SJ IGBTs for 600 V and above. LV IGBTs would be particularly interesting at very high current densities (>200 A/cm^2). This calls for large amounts of excess base charge where the advantage brought about by the SJ geometry becomes negligible.

E. Hybrid Device Concepts

For the lowest MOSFET blocking voltage classes (60 V and below), SJ drift layers progressively lose their attractiveness. This is caused by two effects: first, p-type pillars are not accessible to majority carriers (electrons), when the MOSFET is in the on-state. This is synonymous with a reduction of the active device area. Second, doping concentrations in conventional drift layers will differ less from the doping concentrations in the pillars of respective SJ MOSFETs unless their width is brought close to the 1 μm scale [10]. Accordingly, planar power MOSFET geometries (non SJ concepts) seem to dominate the present development of 20–30 V power MOSFETs [27], [28]. For this reason, we considered only device geometries with conventional drift layers in the 60 V class comparison (see Fig. 11). With decreasing thickness of the drift layer, the IGBT penalty of the PN junction built-in voltage (approximately 0.7 V at room temperature) becomes more prominent. Our simulations indicate that the crossover current density (equal conduction and turn-off losses) reaches 150 A/cm^2. At 300 A/cm^2, the 400 K on-state voltage drop of a 60 V IGBT should not exceed 1 V (see Fig. 11). Considering state-of-the-art 600 V IGBTs with maximum rated current densities approaching 200 A/cm^2, running 60 V IGBTs at 300–500 A/cm^2 or even higher current densities would not seem unrealistic (hypothetical dual pack with 1 kA current capability). To harvest the most valuable characteristics of LV power MOSFETs and IGBTs in this lowest voltage segment would call for a monolithic integration of both functionalities on a single

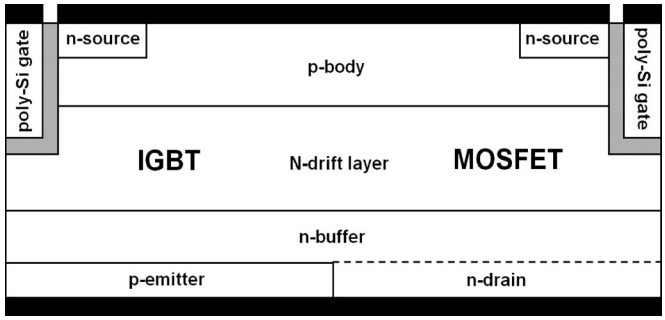

Fig. 13. Monolithically integrated, hybrid power semiconductor device containing IGBT-type and power MOSFET cells (schematic representation, the wafer substrate is not shown).

wafer/die as illustrated schematically in Fig. 13 (MOSFET mode at low current densities and predominantly IGBT mode at high current densities). Such a hybrid structure would also allow using the MOSFET body diode for freewheeling diode purposes.

F. Wafer Substrate and p-Emitter Efficiency

Historically, IGBTs were first fabricated using epitaxially grown drift layers on thick wafer substrates (500 μm) [11], [12]. Among other things, this implementation was abandoned due to problems related to strong carrier lifetime control needed for tailoring the emitter injection efficiency. In contrast, highly doped wafer substrates have remained a commonplace in the manufacture of LV power MOSFETs. Modern thin wafer processing technologies have made possible a reduction of the substrate thickness to approximately 50 μm. Because of the impact on series resistance, the power MOSFET industry is presently working on solutions to further reduce the substrate thickness to 20 μm or even less. In a radical approach to solve this problem, power MOSFETs on metal substrates have been proposed recently [29]. Considering these new trends together with the global trend of semiconductor technologies toward thin wafer processing, it is not unrealistic to assume that sufficient emitter efficiency control could be applied to LV IGBTs even with the presence of thin substrates. As illustrated in Fig. 6 (120 V class), thinner drift layers tend to significantly relax the requirements on low p-emitter injection efficiency; in this example, $E_{\rm off}$ remains fairly constant up to emitter efficiencies of 0.8. A further increase of γ_e to 0.9 (strong p-emitter) will result in an $E_{\rm off}$ increase of only 20%.

V. Conclusion

Market volume is one of the most powerful drivers for technological innovation. Thus, it is not surprising that the highlights of IGBT evolution such as trench MOS-gates and field-stop geometries were first implemented in 600 V and 1.2 kV IGBTs. At present, these two voltage classes occupy the lion's share (about 80%) of the total IGBT market [30]. In 2011, both power MOSFET (predominantly discrete devices) and IGBT markets (modules and discrete devices) had a value of close to 6 billion US dollars and contributed about two thirds of the world's total power semiconductor device market. This sheer size of the market up to 600 V makes it rather attractive for a number of IGBT manufacturers. At present, the move of IGBTs below the 600 V borderline [22] is facilitated by new, emerging applications having power-hungry requirements as needed for example in the electric vehicle/hybrid electric vehicle development. The first 400 V automotive IGBTs have been released recently (IGBT components FS215R04A1E3D and AUIRGP35B60PD-3). These new IGBTs can satisfy current handling requirements which are not easily met by existing power MOSFETs. Should this trend proceed successfully, it might trigger a market driven push toward even lower voltage IGBTs or hybrid MOSFET/IGBTs ending just short of the lowest blocking voltages of present day power MOSFETs. This analysis predicts that such very low voltage IGBTs must not be plagued by higher switching losses than offered by the MOSFET competition. Moreover, LV IGBTs could become a low-cost alternative to SJ MOSFETs. Historically, most power semiconductor devices evolved from lower toward higher blocking capability. Eventually, IGBTs could become a first, rare exception to this rule: while the main development trend toward high voltages seems to lose some of its initial thrust (not counting the efforts toward multi-kV SiC IGBTs), the device concept might soon enter a second technological life cycle pointing into the opposite direction, i.e., leading toward blocking voltages much below the capability of IGBTs three decades ago.

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Friedhelm D. Bauer (M'97–SM'09) received the M.S. and Ph.D. degrees in electrical engineering from Rheinisch Westfälische Technische Hochschule Aachen, Germany, in 1979 and 1984, respectively.

From 1986 to the present, he has been involved in the research and development of high-voltage high-power semiconductor switches such as MOS-controlled thyristors, integrated gate-commutated thyristors, and insulated-gate bipolar transistors at ABB Corporate Research, Switzerland, and later at ABB Semiconductors AG, Lenzburg, Switzerland. Since 2004, he has been a Senior Principal Scientist with the Corporate Research Center, ABB Switzerland, Ltd., Baden-Dättwil, Switzerland. He is the author of a number of scientific papers in the field of modern power semiconductor devices. He is also the holder of several patents in the same field.