Alleviation of Electromagnetic Interference Noise Using a Resonant Shunt for Balanced Converters

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***Abstract*—Balanced converter is an effective way to reduce the CM noise. However, the parasitic capacitance between the switch and heat sink leads to resonant problems, resulting in high noise in certain frequency range. This paper proposes a novel coupled inductor structure based on the balanced technique for the Boost converter to further reduce the CM noise at certain frequency range. A shunt resonant path is adopted to offer a maximum suppression. The analytical estimation for shunt winding's performance is provided for better design. Some simulation and experimental results of this new technique are presented to validate its effectiveness. The experiments about the capacitance unbalance, different load current, and reduction of the CM inductor size are also discussed for better understanding of this technique.**

***Index Terms*—Balanced converter, common mode (CM) noise, shunt resonant path.**

I. Introduction

BOOST converters have been widely used due to its simplicity of topology and ability to handle the input current. Typically, this kind of converter serves as the front end of a power supply (PS), and is connected with the power source/grid directly [1]–[6]. Hence, the electromagnetic compatibility (EMC) of such converters becomes a major concern [7]–[11]. The high electromagnetic interference (EMI) noise is induced by the rapid voltage change across a switch component. Since the heat sink of switch device will introduce large parasitic capacitance, the high EMI noise is dominated by the common mode (CM) one [12]. Therefore, extra EMI filters with bulky CM inductors are required to alleviate the noise in order to make the EMC performance of the PS to comply with the EMI standards.

To reduce the CM noise and the volume of CM inductors, a variety of balanced converters are presented [13]–[15]. Shoyama *et al.* presented a balanced boost converter to reduce the CM noise [16]. In this method, the inductor is divided equally into two parts. Then, the voltage of the drain and source change complementarily which confines the CM current within the converter, contributing to the CM noise reduction significantly.

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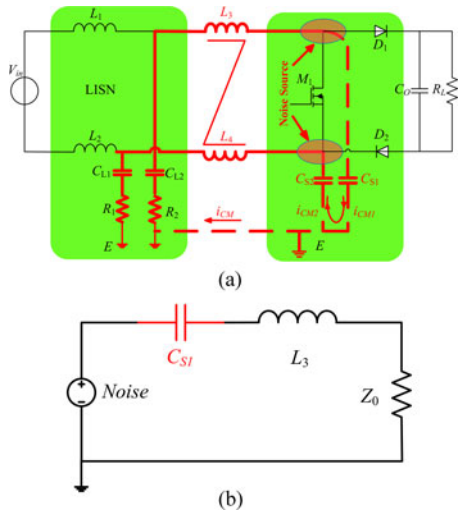

Fig. 1. Series resonant circuit. (a) The boost converter with LISN (b) The simplified circuit with the parasitic capacitance.

Wang *et al.* investigated the theory of boost converter modeling for EMI, and introduced a general balance concept to cancel the CM noise [17]. Some ways are discussed to improve the circuit balance such as splitting the boost inductor, keeping the ESL and ESR of the output capacitors as small as possible.

Kong *et al.* proposed two approaches based on the balance concept to minimize the CM noise [18]. One way is to add two more diodes and a gate drive transformer to achieve symmetric topology, another way is to add an inductor to achieve balance. The experimental results show that both approaches can reduce the CM noise up to 30 dB $\cdot \mu$V.

Deng *et al.* also proposed a balanced power factor correction converter, which integrated the differential mode (DM) inductor of the EMI filter into the boost inductors [19]. With the integration technique, it can significantly reduce the EMI noise, and the volume of the prototype can be reduced by 25%.

All of the methods above based on the balanced converter can mitigate the CM noise in most frequency range. However, there are always some noises, which are hardly to reduce by applying balanced topology, during special frequency interval. This scenario will be diagramed by the simplified schematic shown in Fig. 1. It is readily seen that a resonant path, which is comprised of a parasitic capacitor C_{s1}/C_{s2} and an inductor L_3/L_4 exists. In the case of two components working in series resonant mode, the impedance between the noise source and the line impedance stabilization network (LISN) equals to zero theoretically. Thus, the noise level of the frequencies in the vicinity of resonant point will be dramatically high. This frustrated result might not be properly deal with. The reason lies that the

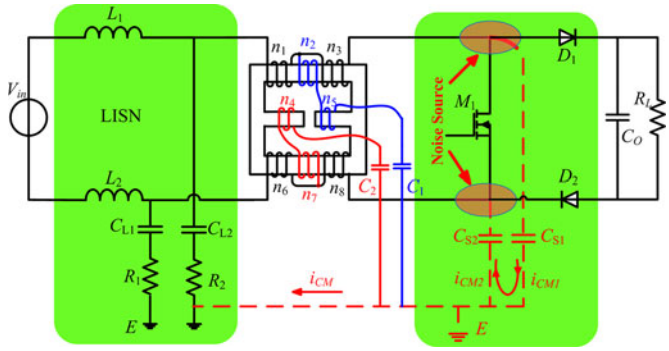

Fig. 2. Proposed scheme in boost converters.

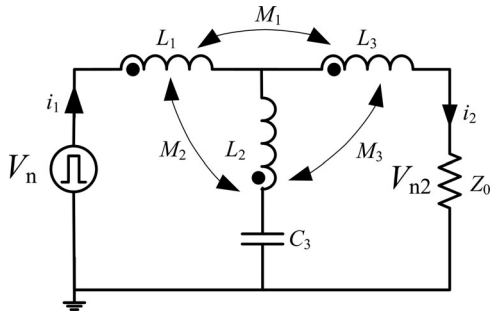

Fig. 3. Scheme for the proposed topology.

series resonant impedance is so small that even a tiny variation between balanced paths will contaminate the well-known cancellation effect of a balanced topology. At the same time, so many components such as inductors, parasitic capacitors, and coupling inductors are involved in this case, and fine tuning every components and their coupling relationship is a formidable task.

This paper presents a novel coupled inductor structure based on the balanced switching technique to reduce the CM noise as shown in Fig. 2. This new topology inherits all the advantages of the balanced switching technique and solves the resonant problem. It adopts shunt resonant paths to offer a maximum suppression for the noise at particular frequency range, where it is the resonance frequency here. Therefore, the performance of the balanced switching technique can be improved further with this novel topology.

This paper is organized as follows. Section II provides the concept of the shunt resonant paths, and Section III describes the implementation of the shunt resonant path. In Section IV, simulation and experimental results are presented. Discussion and conclusions are presented in Sections V and VI.

II. Concept of Shunt Resonant Path

A. Problem of the Balanced Switching Technique

Although balanced converters can achieve significant improvement in the CM noise suppression, their symmetrical topologies will introduce some resonant branch. We can take a balanced boost converter as an example to demonstrate this case, as shown Fig. 1(a). The ground E here is the LISN ground, which is connected with the thermal pad in this experiment. Since C_{S1} and C_{S2} are parasitic capacitors, which are distributed in the air, in order to distinguish from the real capacitor components, they are connected with dashed lines. A resonant branch, which is marked in red, consists of the parasitic capacitance C_{S1}, C_{S2} and the inductor. Then, the equivalent resonant branch is illustrated in Fig. 1(b), and the noise gain is given by

$$G_1 = \frac{V_R}{V_{\text{Noise}}} = \frac{Z_0}{Z_0 + sL_3 + \frac{1}{sC_{S1}}} = \frac{sZ_0C_{S1}}{s^2L_3C_{S1} + sZ_0C_{S1} + 1}. \quad (1)$$

At the frequency

$$f_1 = \frac{1}{2\pi\sqrt{L_3C_{S1}}} \quad (2)$$

the evaluation of the gain is

$$G_1 = \frac{V_R}{V_{\text{Noise}}} = 1. \quad (3)$$

Therefore, the inductor will not suppress the noise any more.

B. Principle of the Shunt Resonant Path

In order to reduce the noise at the resonant frequency f_1, a resonant path is added to offer a maximum suppression to reduce the CM noise as shown in Fig. 3 [20]. The path consists of a capacitor and an inductor, which is coupled with the power inductor in negative polarity. The source V_n is the noise produced by the floating voltage of the switch device.

The current gain is

$$G_2 = \frac{i_2}{i_1} = \frac{1 + s^2C_3(L_2 - M_1 - M_2 + M_3)}{1 + sC_3Z_0 + s^2C_3(L_2 + L_3 + 2M_3)} \quad (4)$$

where Z_0 is the equivalent output resistance, C_3 is the capacitance in the shunt resonant path, M_1 is the mutual inductance between L_1 and L_3, while M_2 is the one between L_1 and L_2, and M_3 is the one between L_2 and L_3.

Equation (4) illustrates that at the frequency

$$f_2 = \frac{1}{2\pi\sqrt{C_3(L_2 - M_1 - M_2 + M_3)}} \quad (5)$$

the numerator is approaching to zero and so is G_2.

Therefore, at this frequency, the path can afford a maximum suppression. Since the resonant frequency f_2 is related to the inductor L_2 in the resonant path which has a flexible value, the maximum suppression can also be chosen from a wide range. Here, the frequency f_2 is set at frequency f_1, where the parasitic capacitor and the inductor resonate.

To evaluate the performance of the shunt path, the function of its insertion loss (IL) is provided, which is described as a ratio of V_{n1} to V_{n2}. V_{n1} is the voltage across the resistor in the circuit without the shunt path connected as shown in Fig. 4, while V_{n2} is the one across the resistor in the circuit with the shunt path connected as shown in Fig. 3. It is assumed that the current i_1

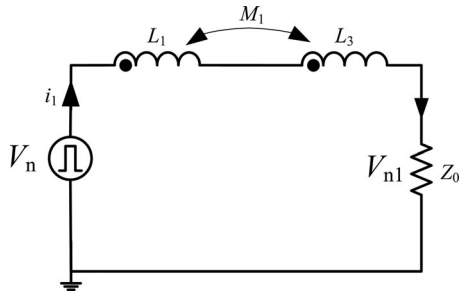

Fig. 4. Scheme without the proposed topology.

keeps constant. Then, IL is

$$\begin{aligned}\mathrm{IL_{CM}} &= 20\log\left|\frac{V_{n1}}{V_{n2}}\right| = 20\log\left|\frac{i_1 z_0}{i_2 z_0}\right| = 20\log\left|\frac{i_1}{i_2}\right| \\ &= 20\log\left|\frac{1+sC_3Z_0+s^2C_3(L_2+L_3+2M_3)}{1+s^2C_3(L_2-M_1-M_2+M_3)}\right|.\end{aligned} \tag{6}$$

Since the equivalent series resistance of the inductor L_2, R_{esr}, will worsen the performance of IL, a much more accurate model is given by

$$\begin{aligned}&\mathrm{IL_{CM}} \\ &= 20\log\left|\frac{1+sC_3Z_0+sC_3R_{\mathrm{esr}}+s^2C_3(L_2+L_3+2M_3)}{1+sC_3R_{\mathrm{esr}}+s^2C_3(L_2-M_1-M_2+M_3)}\right|.\end{aligned} \tag{7}$$

This model can be used to predict the performance of the shunt path.

The disadvantage of this topology is that at the frequency

$$f_3 = \frac{1}{2\pi\sqrt{C_3\,(L_2+L_3+2M_3)}} \tag{8}$$

the denominator will decrease and the IL of this topology will be worse. Therefore, the frequency f_3 should be selected at the range where the EMI noise is low enough.

III. Implementation of the Shunt Resonant Path

From the principle discussed above, a novel inductor structure based on the balanced structure is proposed as shown in Fig. 5. In order to reduce the size of the EMI filter, a structure which integrates the DM and CM inductors into the power inductor is adopted [21]. The derivation of its CM inductance and DM inductance is detailed in Appendix. The windings n_1, n_3, n_6, and n_8, acting as the power inductor, are wound on an E–E core. Besides, the other four coils n_2, n_4, n_5, and n_7, acting as the shunt resonant path which are coupled with the power inductor, are also wound on the core.

A. Implementation of the Shunt Resonant Path

1) Common Mode: Since it is based on the balanced structure, the path should have no influence on the balanced state of the inductor. In CM, the currents flow into the winding from ports 1 and 2. The fluxes produced by the two coils n_2 and n_7 will flow through the two side legs. Therefore, the fluxes in the two-side legs still equal, and the CM inductor keeps balanced.

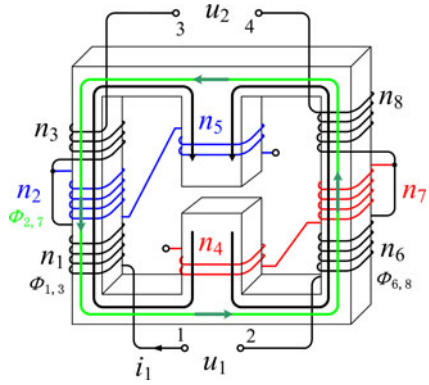

Fig. 5. Proposed inductor structure.

2) Differential Mode: In DM, the currents flow into the winding from ports 1 and 4 as shown in Fig. 5. The fluxes $\Phi_{1,3}$ and $\Phi_{6,8}$ shown as black lines are produced by the windings n_1, n_3, n_6, and n_8. Both of the fluxes flow through the center leg in the same direction. The flux $\Phi_{2,7}$ shown as green line is produced by the winding n_2 and n_7. It can be found that the flux produced by the windings n_2 and n_7 are in the same direction. The flux $\Phi_{1,3}$ and the flux $\Phi_{2,7}$ are in the opposite direction, while the flux $\Phi_{6,8}$ and the flux $\Phi_{2,7}$ are in the same direction. Therefore, the fluxes of the two-side legs do not equal with each other, which results in asymmetric structure.

In order to keep the structure balance, the flux linkage of the shunt resonant windings, caused by the DM current, should be zero. Therefore, the other two windings n_4 and n_5 are wound in the center leg

$$n_2\phi_2 - n_5\phi_5 = 0. \tag{9}$$

Since the DM flux in the center leg is twice of the one in the side leg

$$\begin{aligned}\phi_2 &= \phi_{\mathrm{DM}} \\ \phi_5 &= 2\times\phi_{\mathrm{DM}}.\end{aligned} \tag{10}$$

Therefore, the number ratio of the windings n_2 and n_5 should be $n_2/n_5 = 2/1$. As the structure is symmetrical, so is the ratio between n_7 and n_4.

3) Effects of the Shunt Resonant Path on the DM Noise: From the analysis above, the shunt resonant path contributes to the CM noise suppression within certain frequency range. However, its effect on the DM noise still needs to be discussed. The equivalent differential circuit of Fig. 1 is shown in Fig. 6.

The current gain equals

$$G_3 = \frac{i_2}{i_1} = \frac{1-s^2C_e(M_{D1}+M_{D6})}{1+s^2C_e(L_{D1}+L_{D6})+sC_eZ_0} \tag{11}$$

where C_e is the equivalent value of C_1 and C_2.

From the (11), it can be found that the IL of the DM will be changed thanks to the variation of C_e, L_{D1}, L_{D6}, M_{D1} and M_{D6}. To achieve the best performance, these parameters should be carefully chosen. Since the relationship among these

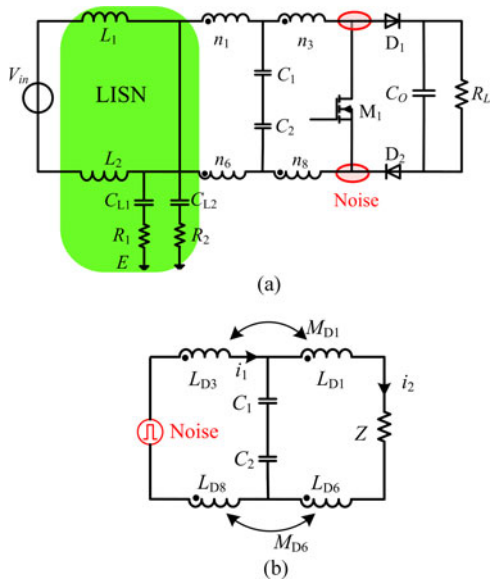

Fig. 6. Noise path for DM. (a) Equivalent circuit in boost convertor for DM. (b) Equivalent noise path for DM

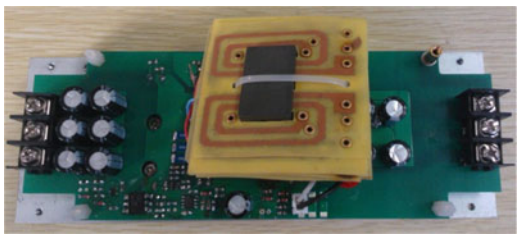

Fig. 7. Experiment setup.

parameters are complex, and our main objective of this paper is to demonstrate the novel magnetic structure and the idea of alleviation of the noise level by shunt branch, much work on the optimization of the shunt resonant path are fulfilled using simulation method.

IV. Simulation and the Experiment Results

A. Design of the Inductor

The experiment setup is shown in Fig. 7. The input voltage of the prototype is 35 V, while the output voltage is 53 V. Its switching frequency is 50 kHz. The inductance was designed to be 80 uH, the peak current is 11 A. Then, the energy-handling capability of the inductor was calculated

$$W = \frac{LI_{pk}^2}{2} = \frac{1}{2} \times 80 \times 10^{-6} \times 11^2 = 0.00484 \text{ (J)}. \quad (12)$$

Then the area product A_p was

$$A_p = \frac{2W \times 10^4}{B_m J K_u} = \frac{2 \times 0.00484 \times 10^4}{0.44 \times 0.4 \times 395} = 1.39 \,(\text{cm}^4). \quad (13)$$

Considering the A_p value and the structure of the inductor whose coils are balanced and wound on the two side legs, E32/6/20 of Planar EE core is chosen in this experiment. The

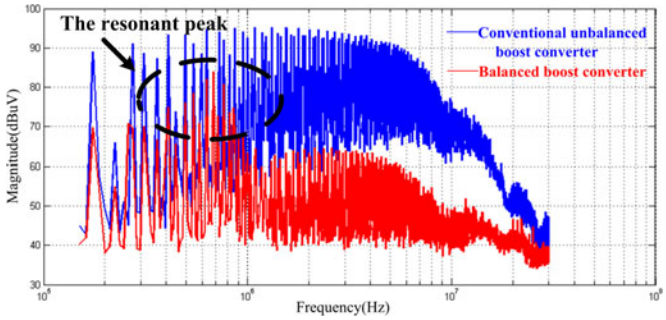

Fig. 8. Spectrum of the CM noise.

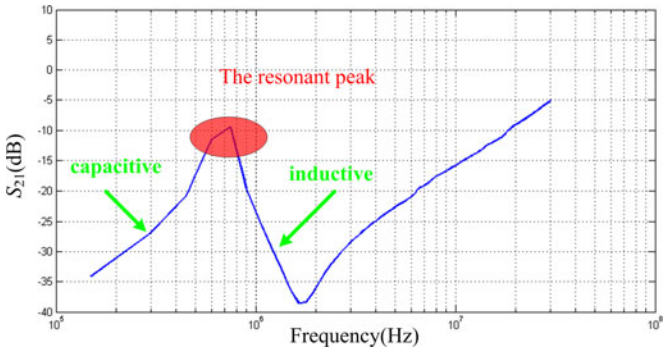

Fig. 9. Scattering parameter S_{21}.

turn number of each coil is 12 and the approximate air gap of the middle leg is 0.7 mm. Finally, the DM inductance is 72 μH and the CM coupled inductance is 0.86 mH.

B. Comparison of Conventional Unbalanced Boost Converter and Balanced Boost Converter

First of all, to confirm the CM noise reduction in the balanced converter, we conducted two experiments. One was the conventional unbalanced boost converter and the other was balanced boost converter. All of the prototypes presented in this section are tested without any EMI filter. The spectrum of CM noise was sensed by noise separator. Fig. 8 shows the experimental results, where the blue spectrum is the result of the conventional unbalanced converter and the red spectrum is the one of the balanced converter. From the comparison of the results, it can be found that the CM noise is reduced more than 20 dB from a large frequency range in the balanced converter. But it can also be found that there is a series resonant peak at the frequency about 700 kHz where the noise is much higher than the ones at other frequencies.

To verify the resonant problem, the scattering parameter S_{21}, which represents the energy transfer ratio between noise source and input power port, was also measured [22]. The result was presented in Fig. 9. It can be found that it exists a resonant peak around the frequency 700 kHz.

C. Shunt Resonant Path Experiments

1) Prediction of the Shunt Resonant Path: To further reduce the noise at the resonant frequency, the shunt resonant path was adopted. First, the IL is predicted according to (7). From (5) and

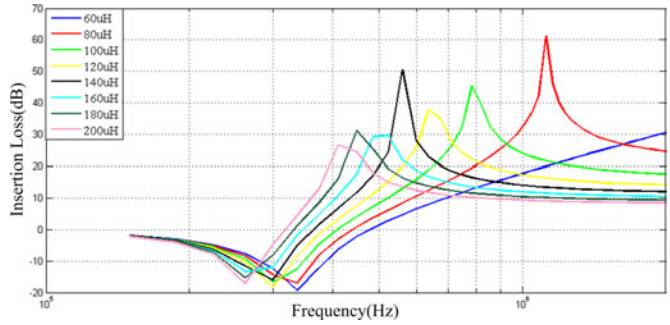

Fig. 10. CM IL with different L2.

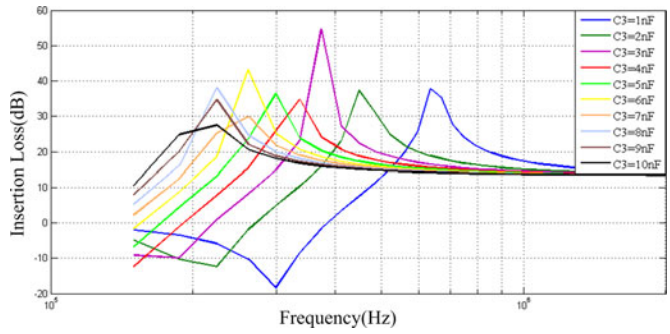

Fig. 11. CM IL with different C3.

(8), it can be found that the resonant frequency is complex for calculation since it relates to five variables. In order to simplify its calculation, the shunt resonant path in this experiment is connected in the middle of the power inductor, making M_2 equals to M_3. Then (5) can be simplified as

$$f_2 = \frac{1}{2\pi\sqrt{C_3(L_2 - M_1)}}. \tag{14}$$

To take advantage of the resonant path for its maximum suppression, f_2 should be greater than zero. Therefore

$$L_2 > M_1. \tag{15}$$

Since

$$\begin{aligned} M_2 &= M_3 \\ Z_0 &\gg R_{\text{esr}}. \end{aligned} \tag{16}$$

Then, (7) can be simplified

$$\text{IL} = \left| 20\log \frac{1 + sC_3Z_0 + s^2C_3\left(L_2 + L_3 + 2M_3\right)}{1 + sC_3R_{\text{esr}} + s^2C_3\left(L_2 - M_1\right)} \right|. \tag{17}$$

For easier analysis, (17) can be analyzed in frequency domain

$$\text{IL} = 20\log \left| \frac{1 + jwC_3Z_0 - w^2C_3\left(L_2 + L_3 + 2M_3\right)}{1 + jwC_3R_{\text{esr}} - w^2C_3\left(L_2 - M_1\right)} \right|. \tag{18}$$

We first selected a capacitor arbitrarily and increased the inductance L_2 from 60 to 200 uH. The calculation results of the IL were presented in Fig. 10. It can be found that the higher the value of the inductance L_2 is, the lower the IL at the resonant point.

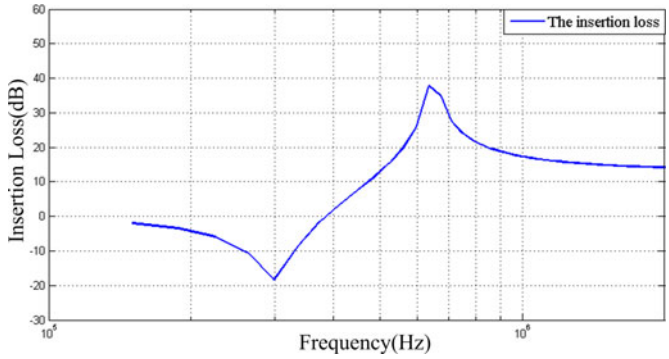

Fig. 12. CM IL of the shunt resonant path.

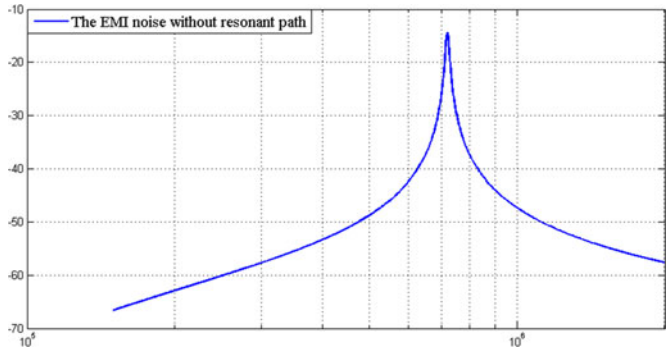

Fig. 13. EMI noise simulation without resonant path.

Then, we selected the inductance arbitrarily and increased the capacitance C_3, the results of the IL were presented in Fig. 11. It can be found that the capacitance value just changes the resonant frequency and its IL at the resonant point keeps constant.

Therefore, from the analysis above, the lower the inductance L_2 is, the better the performance is. The capacitor C_3 can be used to change the resonant frequency to the range where it needs.

Fig. 12 shows the IL applied to the real parameters in the experiment. It can be found that the shunt resonant path can gain 37-dB IL over the one without resonant path at the frequency 650 kHz. According to the (8), the noise will be worse at the frequency f_3, where it is at the frequency 300 kHz, as shown in Fig. 12.

2) Simulation of the Shunt Resonant Path: Then, we made several simulations to verify its effectiveness. First, we simulated the noise without the shunt resonant path, and the result is shown in Fig. 13. It can be found that it exists a series resonant peak at the frequency of 700 kHz, where the noise is much higher than the ones at other spots.

Next, simulations of the new topology were made with discrete inductors in Pspice to validate its effectiveness. In order to determine the value of the inductor L_2, we first selected a capacitor value arbitrarily, and simulated the circuit with different values of the inductor in the shunt resonant path. The results are presented in Fig. 14, which shows that a maximum suppression can be achieved whose frequency differs with the inductance value. In this experiment, the turn number of the

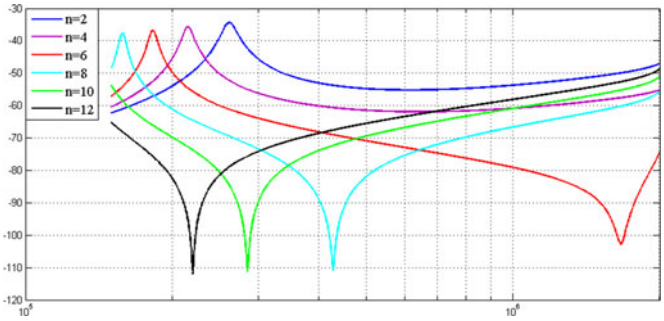

Fig. 14. EMI noise of simulation with different inductor values of the shunt path.

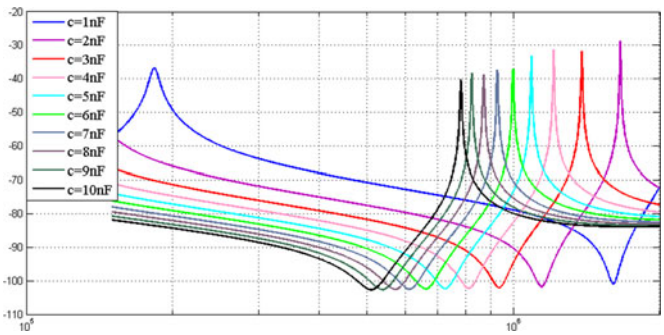

Fig. 15. EMI noise of simulation with different capacitor values of the shunt path.

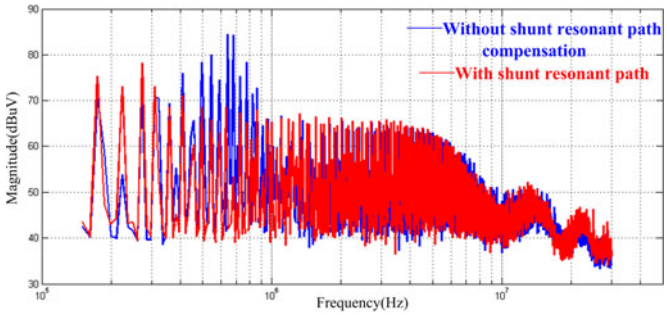

Fig. 16. CM noise of the balanced Boost converter.

inductor in the shunt path was 6. In fact, with the effect of the parasitic capacitance among the windings, the inductor will acts like a capacitor above the resonant frequency of the inductor, which is 1.8 MHz in this experiment and the simulation will be not effective. Therefore, we only concern the simulation results below 1.8 MHz.

Finally, the value of the capacitor should be determined. We simulated the circuit with different capacitor values, which was increased from 1 to 10nF. The results are shown in Fig. 15. It can be found that the capacitor value also affect the frequency of the maximum suppression. In this experiment, the selected capacitor value was 4 nF.

3) Experiment Results of the shunt Resonant Path: Then, the experiment was conducted. The results are shown in Fig. 16. The blue spectrum is the CM noise without the shunt resonant path,

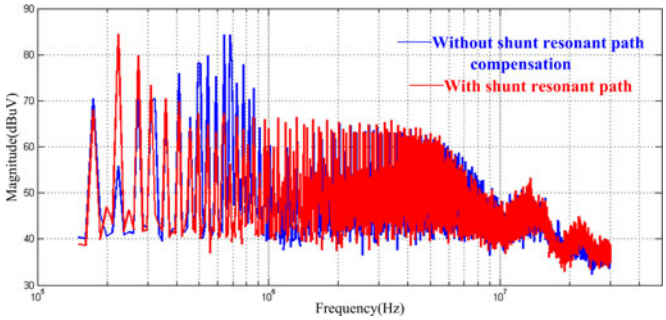

Fig. 17. DM noise of the balanced Boost converter.

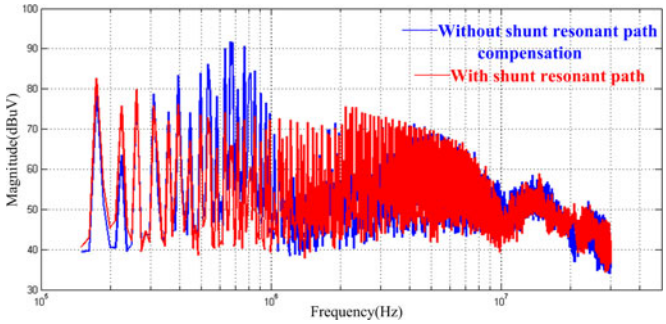

Fig. 18. Total noise of the balanced boost converter.

while the red spectrum is the result with the shunt resonant path. It can be found that the shunt resonant path provides suppression as high as 15 dB at the frequency 500– 900 kHz.

Since the shunt resonant path will also affect the differential IL, the total performance of circuit is also measured. The results are shown in Figs. 17 and 18. Obviously, the noise peak at the frequency of 700 kHz, which is caused by the series resonant of CM inductor and capacitors, is now been attenuated. The energy loss that the shunt resonant path consumed is only 0.2 W.

V. Discussion

A. Effects of the Shunt Path Windings

Since the shunt path conducts only the noise current, the path can use very small conductors and occupies little space. However, the added windings may have some impact on the parasitic parameters of inductor, which might decrease the suppression performance. We conducted two compared experiments, one was the coupled inductor without the shunt path, and the other was the coupled inductor with the shunt path wound on the inductor but leave it floating. The results which are the total noise of the circuits are presented in Fig. 19. It shows that with the added windings which is even not connected with the inductor, its performance still deteriorated in a small degree. But compared to the performance of the shunt path at the resonant frequency which can achieve 15-dB attenuation, this deterioration is acceptable.

B. Effects of the Parasitic Capacitors of the MOSFET

Since the winding of the inductor is equally split into two parts, the voltage of both drain and source of the MOSFET

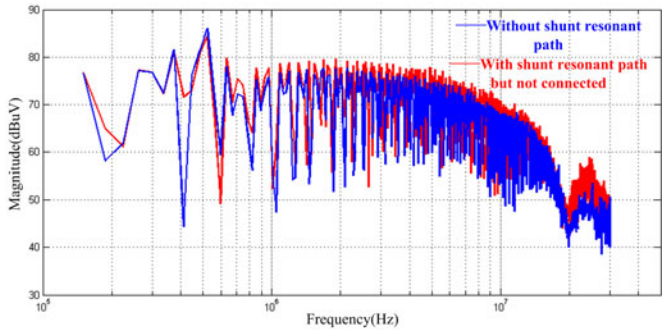

Fig. 19. Effect of the added windings.

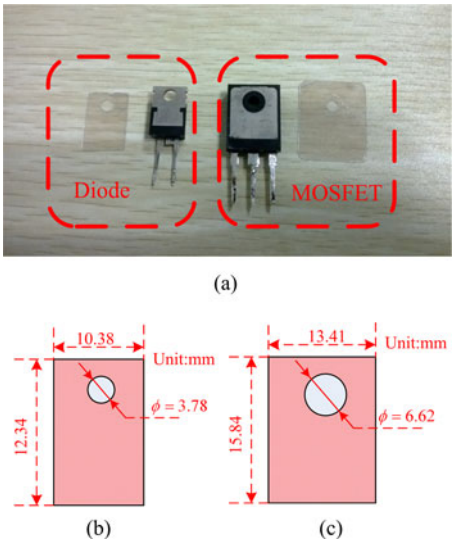

Fig. 20. Dimension of the diode and the MOSFET. (a) MOSFET and diode. (b) Thermal pad of the diode. (c) Thermal pad of the MOSFET

change complementarily. Then, the CM current equals

$$i_{\mathrm{CM}} = i_{\mathrm{CM1}} - i_{\mathrm{CM2}} = (C_{S1} - C_{S2})\frac{du}{dt} \tag{19}$$

where C_{S1} and C_{S2} are the parasitic capacitors of the MOSFET. Therefore, the CM noise can be significantly reduced if the parasitic capacitance C_{S1} and C_{S2} equals which helps to reduce the size of the EMI filter.

From the (19), it is found that the lower difference of the capacitances C_{S1} and C_{S2}, the smaller the CM current is. Therefore, we first calculated the parasitic capacitance of the PCB where our experiments operate. The parasitic capacitance C_{S1} consists of two parts. One is caused by the drain pin of the MOSFET, and the other part is caused by the copper on the PCB. Considering the cooling requirement in case of flowing large current, the MOSFET is a through-hole component and a heat sink is used with the MOSFET. The type of the MOSFET is IRFP4332 and its package type is TO-247 as shown in Fig. 20(a). Since the drain pin of the MOSFET is connected with the thermal pad, which is insulated with the heat sink only through a thin mica isolation pad, the parasitic capacitance caused by the drain pin of the MOSFET is quite large. The dimension of the MOSFET is presented in Fig. 20(c) and the area of its heat sink

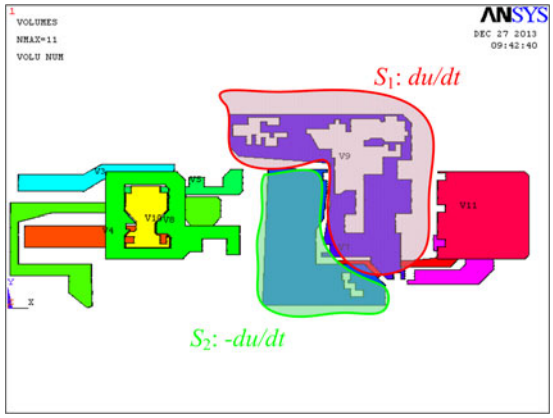

Fig. 21. Parasitic capacitance simulation in ANSYS.

is

$$\mathrm{S}_1 = 15.84 \times 13.41 - \pi \times 6.62^2/4 = 177.99\,\mathrm{mm}^2. \tag{20}$$

The thickness of the mica pad is 0.14 mm and the relative permittivity of the mica is 7, the parasitic capacitance of the thermal pad is

$$\mathrm{C}_1 = \varepsilon_0\varepsilon_r \times \mathrm{S}_1/\mathrm{d} = 78.75\ \mathrm{pF} \tag{21}$$

where ε_0 is 8.85×10^{-12}, and d is the thickness of the insulator.

The other part of the parasitic capacitance is introduced by the copper S_1 on the PCB connecting with the drain of the MOSFET as shown in Fig. 21. In order to calculate this capacitor value, we simulated the PCB in ANSYS. The capacitor we simulated is 3.5 pF. Therefore, the total capacitance C_{S1} is 82.25 pF.

The parasitic capacitance C_{S2} is similar to C_{S1}, which also consists of two parts. One is the cathode-to-ground capacitance of D_2 in Fig. 2, and the other part is also caused by the copper on the PCB S_2 as shown in Fig. 21.

The area of the thermal pad of the diode D_2 connecting with the cathode pin, as shown in Fig. 20 (b), is

$$\mathrm{S}_2 = 10.38 \times 12.34 - \pi \times 3.78^2/4 = 116.87\ \mathrm{mm}^2. \tag{22}$$

The cathode-to-ground capacitance is

$$\mathrm{C}_2 = \varepsilon_0\varepsilon_r \times \mathrm{S}_2/\mathrm{d} = 51.73\ \mathrm{pF}. \tag{23}$$

From the analysis in ANSYS, the copper parasitic capacitance of C_2 is 4.7 pF. Therefore, the total capacitance C_{S2} is 56.43 pF.

It can be found that there is a big difference between the parasitic capacitance C_{S1} and C_{S2}. In order to reduce the difference, a thin sheet of copper which is of the same size as the thermal pad of the MOSFET was added between the diode and the heat sink. Thus, it can ensure that the cathode-to-ground capacitance C_2 is the same with the capacitance C_1 caused by the MOSFET thermal pad [23]. Then, the difference of the parasitic capacitance of C_{S1} and C_{S2} can be reduced greatly and the final difference is only 1.2 pF which is caused by the area difference of the copper on the PCB.

Then, the experiment of the parasitic capacitance compensation was conducted. The result is shown in Fig. 22 where the blue spectrum is the CM noise after parasitic capacitance

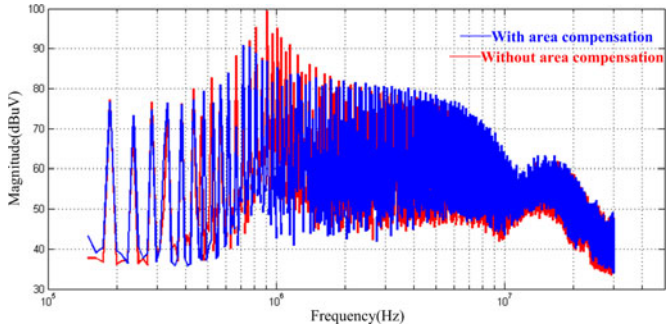

Fig. 22. Experiment result of parasitic capacitance compensation.

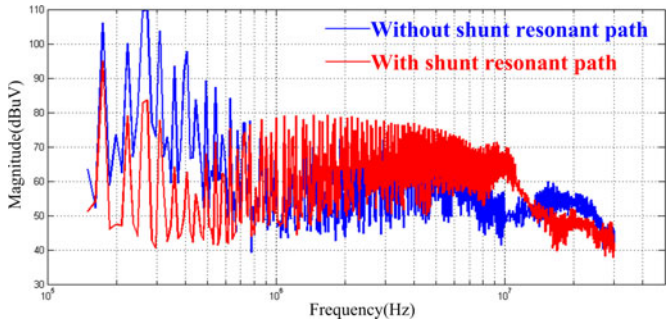

Fig. 23. Effect of shunt resonant path with capacitance unbalance.

compensation and the red one is the CM noise without capacitance compensation.

C. Effectiveness of the Shunt Path in the Case of a Dramatic Difference Between Parasitic Capacitances

In order to verify the effectiveness of the shunt path, the experiment with unbalanced structure was also conducted. One of the parasitic capacitance was increased much larger than the other deliberately. The value of C_{S1} is 582.25 pF, while the one of C_{S2} is 83.45 pF. Its experimental results are presented in Fig. 23. It can be found that the capacitance unbalance leads to much larger noise in low-frequency range. Since the capacitance in the resonant path was increased, its resonant frequency decreased to 250 kHz. The experiment result shows that the shunt resonant path is still effective.

D. Reduction for the CM Inductor With the Shunt Resonant Path

To the best of our knowledge, the state-of-art balanced converters cannot meet the EMC rule requirements without EMI filters. Thus, a front stage EMI filter must be adopted to attenuate the CM noise further, and how to reduce the EMI filter size/cost by fine tuning the converter is the motivation of this paper. It is well known that the size/cost of a CM inductor with a fixed inductance is dominated by its self-resonance frequency (SRF). At the same time, the more CM noise locates at high frequency, the higher SRF CM inductors have to be used to wardoff the noise. In other words, the CM inductor will be much bigger. As stated in this paper, the noise locating at frequency around

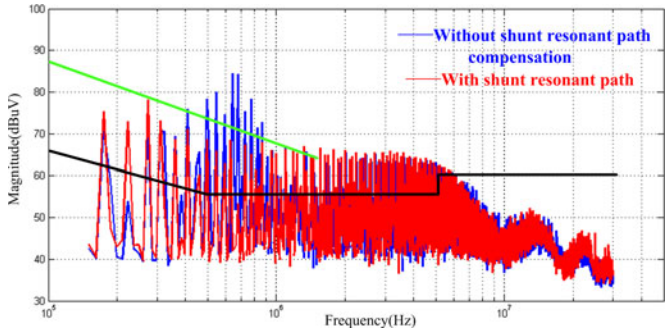

Fig. 24. CM noise in our experiment.

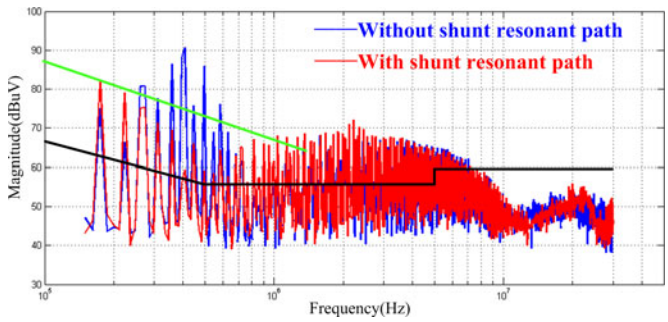

Fig. 25. CM noise with larger inductance.

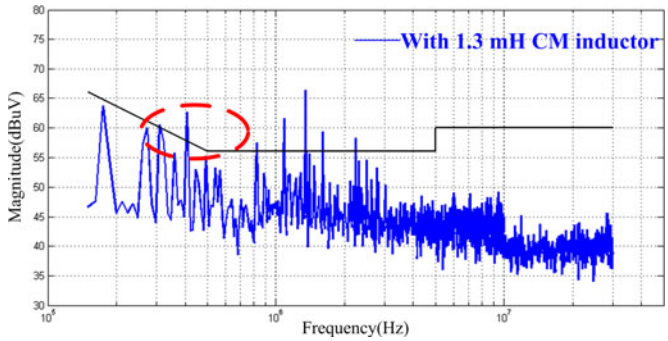

Fig. 26. Noise without the shunt resonant path connecting 1.3 mH CM inductor.

700 kHz is mainly induced by the series resonant of the coupled boost inductor and parasitic CM capacitances. In case we distribute the CM noise around 700 kHz to lower frequency, a CM inductor with low SRF can fulfill the noise alleviation task. The low-SRF CM inductor may be fabricated by thick winding method, and leave the issue of equivalent parallel capacitance alone. As a result, the volume of CM inductor will be shrunk. In addition, some cheaper manufacturing method/core type such as multiple layers, banking windings, and E–E cores rather than toroid cores may be used.

For better understanding of this technique, the reduction of the CM inductor will be discussed. Since the performance of the EMI filter at high frequency depends on the parasitic parameters. Here, we only consider the noise in the low-frequency range, which dominates the size of the CM inductor. Therefore, we will concentrate our mind on the frequency below 1 MHz. The CM noise is presented in Fig. 24. The black line in figure is the

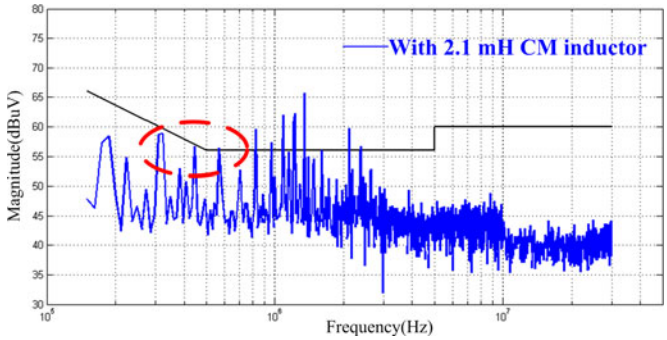

Fig. 27. Noise without the shunt resonant path connecting 2.1-mH CM inductor.

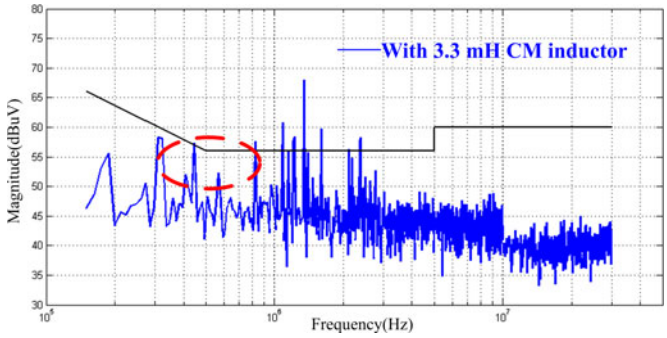

Fig. 28. Noise without the shunt resonant path connecting 3.3-mH CM inductor.

standard of CISPR 22B, while the green one is the IL that the CM inductor should provide which is usually 20 dB per decade.

It shows that, without the shunt resonant path, the highest noise is at the frequency 700 kHz. A high SRF of CM inductor will also be needed. However, with the shunt resonant path, it can be found that the highest noise which exceeds the standard is around the frequency 300 kHz. Therefore, the SRF of the CM inductor can be decreased as well as the size of the CM inductor.

To further reduce the size of the CM inductor, according to the SRF of the CM inductor mentioned above, we could increase the power inductor and make the resonant frequency lower. It must be pointed out that this variation contributes little change to the volume of the converter since the core size of the inductor does not alter. The experimental result is presented in Fig. 25. It can be found that with a larger inductance, the resonant frequency was decreased to 400 kHz. After applying the shunt resonant path, the noise exceeding the standard also moved to 150 kHz. Then, the CM inductor with a lower SRF can be applied to reduce its size.

A series of experiments were also conducted to illustrate the reduction of the CM inductor with the shunt resonant path. In these experiments, the EMI filter topology as well as values of its components except the CM inductor was kept the same, and different CM inductors were applied for comparison. In order to fully demonstrate the advantage of shunt path, a larger power inductor was adopted for a lower resonant frequency (about 400 kHz).

First, we made the experiments without the shunt resonant path. It can be found that, when the inductance of the EMI filter

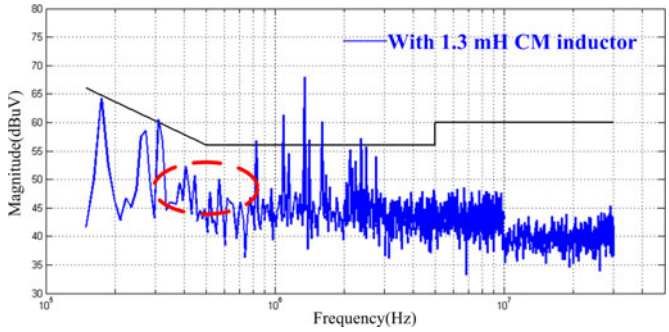

Fig. 29. Noise with the shunt resonant path connecting with 1.3-mH CM inductor.

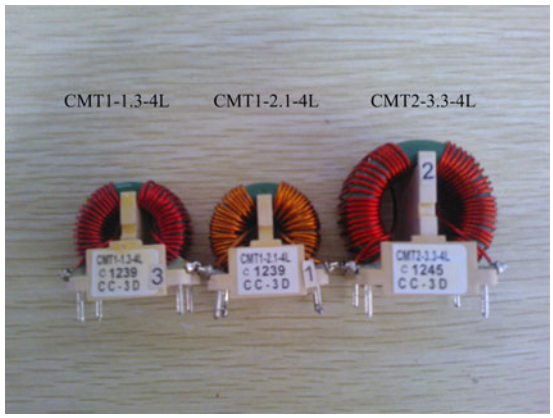

Fig. 30. Comparison of the inductors in the EMI filters.

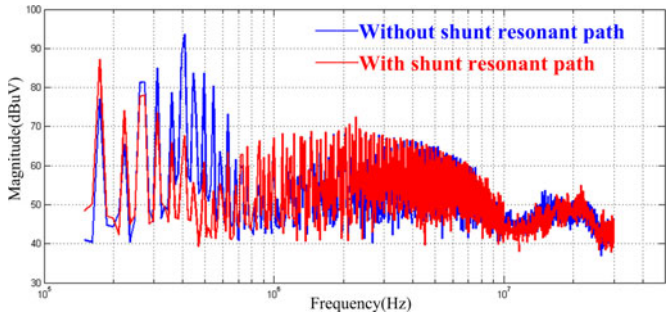

Fig. 31. Noise with 1.77-A load current.

is 1.3 mH, the noise at the resonant frequency 400 kHz still exceeds the standards as shown in Fig. 26. Then, the inductance was increased to 2.1 mH, the noise in the low frequency can be decreased and satisfy the standards as shown in Fig. 27. To get better performance, the inductance was increased to 3.3 mH. The result is also presented in Fig. 28 and shows that the noise around the frequency 600 kHz gets better. Since the noise above 1 MHz does not include the content of this paper; therefore, we only care the noise in the low frequency range.

Then, we conducted the experiment with the shunt resonant path. When the inductance is 1.3 mH, the noise in the low frequency has satisfied the standards as shown in Fig. 29. It can

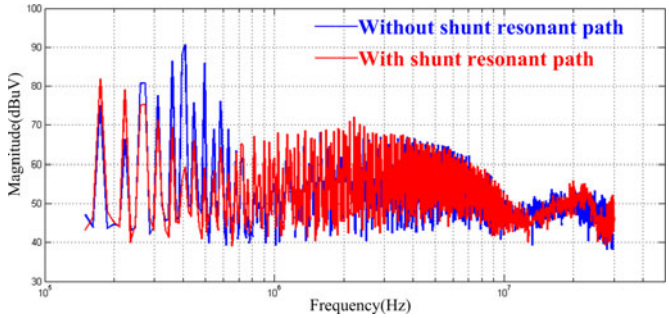

Fig. 32. Noise with 2.65-A load current.

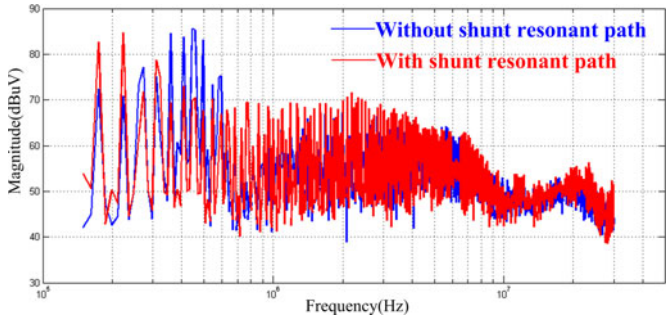

Fig. 33. Noise with 3.53-A load current.

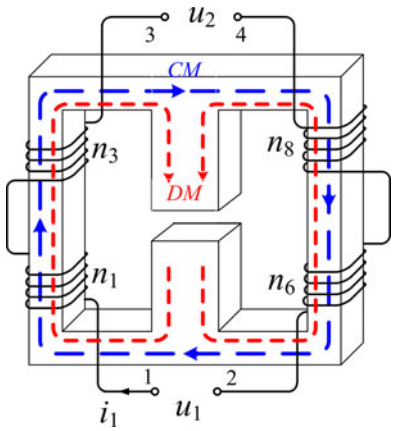

Fig. 34. Flux direction in DM and CM mode.

be found that the noise in the frequency range between 400 and 700 kHz is much lower than the one in the experiment without the shunt resonant path.

The inductors used in these experiments are COILCRAFT CMT1-1.3-4L, CMT1-2.1-4L, and CMT2-3.3-4L as shown in Fig. 30. It is clearly shown that a balanced converter provided with the shunt path will gain much benefit over the one without a shunt path in view of size/cost of EMI filter.

E. Effect of the Load Current

Since some parasitic parameters of nonlinear devices, such as diode junction capacitance and permeability of the core material, will be affected by the operating conditions of the converter, which will also affect the validity of this technique [24]. In order

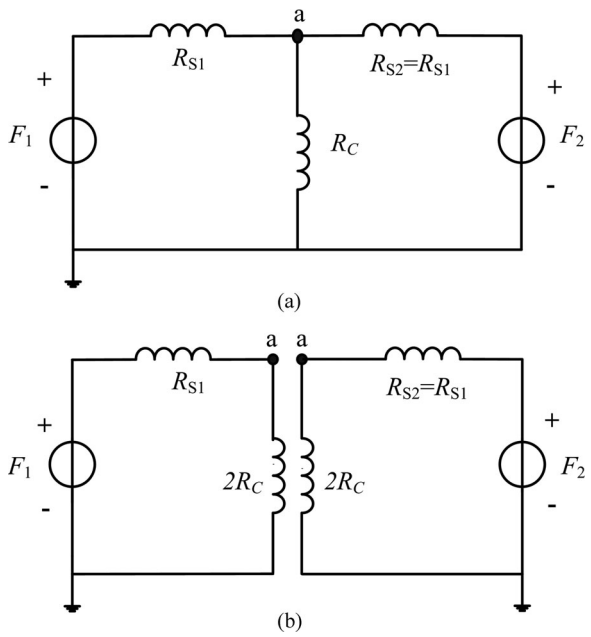

Fig. 35. DM reluctance model of the coupled inductor. (a) DM reluctance model (b) Equivalent magnetic circuit.

to validate the functionality of the shunt path in different load cases, the EMI performance of the converter without a filter are measured with load of 30, 20, and 15 Ω, respectively. The corresponding load current is 1.77, 2.65, and 3.53 A. The experiment results are presented in Figs. 31–33, respectively. It can be found that the performance of the shunt path does be worsened in larger load current circumstance due to junction capacitance variation and decreasing in permeability of the material.

VI. Conclusion

In this paper, a new inductor structure based on the balanced technique is presented. The noise problem caused by the resonant path comprising the parasitic capacitor C_{s1}/C_{s2} and the inductor L_1/L_3 is discussed. A shunt resonant path based on the balanced structure is studied as well as its implementation. With the new added path, a maximum suppression can be achieved to suppress the noise at a certain frequency. The function of IL is provided to evaluate its performance, along with its simulation results. Experimental results show that the auxiliary circuit can gain more than 15-dB IL at the frequency where it resonates. Furthermore, the experiments of this technique on capacitance unbalance condition and different load current also validates its effectiveness. Finally, the CM inductor size comparison is provided, and the experiments show that the converter with the shunt path will gain much benefit over the one without the path in view of the size of EMI filter.

Appendix

A. Principle of the Coupled Inductor

1) Common Mode: For easier understanding, the principle of the coupled inductor, without the shunt resonant paths as shown in Fig. 34, is analyzed. In CM, the CM currents flow into

the windings from ports 1 and 2. From the right-hand rule, the two magnetic fluxes produced in two windings are in the same direction and flow only through two side legs as the blue dotted lines shown in Fig. 34. Since the CM currents value is very small, the CM inductor will not saturate. The self-inductance of winding n_1 and n_3 is

$$L_{11} = (n_1 + n_3)^2 \frac{\mu A_S}{l_S} \tag{24}$$

where μ is the core of permeability, A_S is the cross-sectional area of the side legs, and l_S is the mean flux path length. Since the inductor is symmetrical, the inductance of winding n_6 and n_8 is equal to L_{11}.

The mutual inductance between the windings wound on the two side legs is

$$M_{12} = (n_1 + n_3)(n_6 + n_8)\frac{\mu A_S}{l_S} = (n_1 + n_3)^2 \frac{\mu A_S}{l_S}. \tag{25}$$

Therefore, the inductance of the CM inductor is

$$L_{\mathrm{CM}} = 2 \times (L_{11} + M_{12}) = 4(n_1 + n_3)^2 \frac{\mu A_S}{l_S}. \tag{26}$$

2) Differential Mode: In DM, the DM currents flow into the windings from ports 1 and 4. The fluxes produced by the windings are shown as the red dotted lines in Fig. 34. Consequently, the mmf's of the windings n_1, n_3 and n_6, n_8 tend to set up flux in the center leg in the same direction. Since the DM current is usually very large, an air gap is employed preventing the inductor from being saturation.

As the magnetic circuit is analogous to electrical circuit, voltage and current are replaced by mmf and magnetic flux, while the resistance is the counterpart of reluctance. The equivalent DM reluctance model is displayed in Fig. 35(a).

As shown in Fig. 35(b), because the power inductors are designed in a symmetric way, the reluctance of middle leg can be divided into two equivalent parts and each part of reluctance has a value of $2R_C$. In addition, the reluctances of two side legs are equal as well. We deduce the value of inductance in the entire magnetic circuit as follows:

$$L_{\mathrm{DM}} = 2 \times L_{1,3} = \frac{2N^2}{R_{S1} + 2R_C} = \frac{2(n_1 + n_3)^2}{R_{S1} + 2R_C} \tag{27}$$

$$R_{S1} = \frac{l_S}{\mu A_S} \tag{28}$$

$$R_{S1} = \frac{l_S}{\mu A_S} \tag{29}$$

where μ is the core of permeability, A_S is the cross-sectional area of the side legs, l_S is the mean flux path length, μ_0 is the air gap of permeability, A_C is the cross-sectional area of the center leg, and l_C is the air length.

Under the assumption that the reluctance of the core is negligible as compared to that of the air gap, the inductance of the windings n_1 and n_3 is equal to

$$L_{\mathrm{DM}} = \frac{2(n_1 + n_3)^2}{R_{S1} + 2R_C} \approx \frac{2(n_1 + n_3)^2}{2R_C} = \frac{(n_1 + n_3)^2 \mu_0 A_C}{l_C}. \tag{30}$$

From the analysis above, the power inductor can be used not only as CM inductor, but also the DM inductor at the same time.

REFERENCES

[1] B. York, Y. Wensong, and L. Jih-Sheng, "An integrated boost resonant converter for photovoltaic applications," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1199–1207, Mar. 2013.

[2] R. Jun, D. Yuejiao, Z. Min, and C. Xi, "Modeling and simulation of boost hard switching converter in power factor correction circuit," in *Proc. 3rd Int.Conf. Consum. Electron., Commun. Netw.*, 2013, pp. 396–399.

[3] H. Bodur, H. Yesilyurt, and H. Ozel, "An improved lossless passive snubber cell for PFC boost converter," in *Proc. 3rd Int. Conf. Electr. Power Energy Convers. Syst.*, 2013, pp. 1–6.

[4] L. Yu-Kang, L. Chung-Yi, C. Huang-Jen, C. Shih-Jen, and L. Jing-Yuan, "Analysis and design of a push-pull quasi-resonant boost power factor corrector," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 347–356, Jan. 2013.

[5] K. Jungmoon and K. Chulwoo, "A DC-DC boost converter with variation-tolerant MPPT technique and efficient ZCS circuit for thermoelectric energy harvesting applications," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3827–3833, Aug. 2013.

[6] N. Altintas, A. F. Bakan, and I. Aksoy, "A novel ZVT-ZCT-PWM boost converter," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 256–265, Jan. 2014.

[7] D. K. W. Cheng, X. C. Liu, and Y. S. Lee, "A new improved boost converter with ripple free input current using coupled inductors," in *Proc. 7th Int. Conf. Power Electron. Variable Speed Drives*, 1998, pp. 592–599.

[8] W. Chuanyun, X. Ming, F. C. Lee, and L. Bing, "EMI study for the interleaved multi-channel PFC," in *Proc. IEEE Power Electron. Spec. Conf.* , 2007, pp. 1336–1342.

[9] D. Cochrane, D. Y. Chen, and D. Boroyevic, "Passive cancellation of common-mode noise in power electronic circuits," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 756–763, May 2003.

[10] H. Li, W. K. S. Tang, Z. Li, and W. A. Halang, "A chaotic peak current-mode boost converter for EMI reduction and ripple suppression," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 6, pp. 763–767, Aug. 2008.

[11] Y. Fei, R. Xinbo, J. Qing, and Y. Zhihong, "Input differential-mode EMI of CRM boost PFC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1177–1188, Mar. 2013.

[12] G. Xun and J. A. Ferreira, "Investigation of conducted EMI in SiC JFET inverters using separated heat sinks," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 115–125, Jan. 2014.

[13] M. R. Yazdani, N. A. Filabadi, and J. Faiz, "EMI examination of symmetric forward converter," in *Proc. 4th Power Electron., Drive Syst. Technol. Conf.*, 2013, pp. 367–371.

[14] I. H. Hung and S. Sheng-Fang, "Techniques for reduction of common-mode EMI based on the concepts of current balance on the power transformer windings," in *Proc. 1st Int. Conf. Future Energy Electron.*, 2013, pp. 558–561.

[15] F. Dianbo, W. Shuo, K. Pengju, F. C. Lee, and H. Daocheng, "Novel techniques to suppress the common-mode EMI noise caused by transformer parasitic capacitances in DC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4968–4977, Nov. 2013.

[16] M. Shoyama, G. Li, and T. Ninomiya, "Balanced switching converter to reduce common-mode conducted noise," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 1095–1099, Dec. 2003.

[17] S. Wang, P. Kong, and F. C. Lee, "Common mode noise reduction for boost converters using general balance technique," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1410–1416, Jul. 2007.

[18] P. Kong, S. Wang, and F. C. Lee, "Common mode EMI noise suppression for bridgeless PFC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 291–297, Jan. 2008.

[19] C. Deng, M. Chen, P. Chen, C. Hu, W. Zhang, and D. Xu, "A PFC converter with novel integration of both the EMI filter and boost inductor," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4485–4489, Sep. 2014.

[20] R. S. Balog and P. T. Krein, "Coupled-inductor filter: A basic filter building block," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 537–546, Jan. 2013.

[21] X. W. Dehong Xu and Y. Zhang, "EMI filter with an integrated structrue of common-mode inductors and differential-mode capacitors realized by flexible printed circuit board," U.S. Patent 7 999 633 B2, Aug. 16, 2011.

[22] A. Ales, J. Schanen, D. Moussaoui, and J. Roudet, "Impedances identification of DC/DC converters for network EMC analysis," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6445–6457, Dec. 2014.
[23] R. Robutel, C. Martin, C. Buttay, H. Morel, P. Mattavelli, D. Boroyevich, and R. Meuret, "Design and implementation of integrated common mode capacitors for SiC-JFET inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3625–3636, Jul. 2014.
[24] D. Yu, W. Jun, W. Gangyao, and A. Q. Huang, "Modeling of the high-frequency rectifier with 10-kV SiC JBS diodes in high-voltage series resonant type DC/DC converters," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4288–4300, Aug. 2014.

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