A High-Efficiency PFM Half-Bridge Converter Utilizing a Half-Bridge *LLC* Converter Under Light Load Conditions

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***Abstract*—Recently, the various types of the half-bridge (HB) converters with the output inductor have been developed, and they exhibit a good performance in medium power applications such as the server power supplies and personal computer power supplies requiring high output current. However, they have common problems such as the primary and secondary switch turn-off losses and snubber loss in the secondary side caused by the output inductor, which degrades light load efficiency. To relieve these limitations of the conventional HB converters, a new HB converter, which employs one additional switch and capacitor in the secondary side, is proposed for a high efficiency under light load conditions in this paper. Since the proposed converter operates like the HB *LLC* converter with below operation by turning on additional switch under light load conditions, the switch turn-off losses and snubber loss can be minimized, and the zero-voltage switching (ZVS) capability can be improved. Consequently, the proposed converter can achieve a high efficiency under light load conditions. To confirm the operation, features, and validity of the proposed converter, a 330–400 V input and 12 V/300 W output laboratory prototype is built and tested.**

***Index Terms*—Asymmetrical half-bridge (AHB) converter, half-bridge (HB) *LLC* converter, hold-up time, light load efficiency.**

I. Introduction

THE energy conversion efficiency in the server power supplies and personal computer (PC) power supplies has become a very important issue in these days as the amount of electricity consumed in the data centers and offices remarkably increases [1]–[4]. Especially, the necessity of the power supplies with a high efficiency is emphasized on medium power (300–600 W) supplies due to the server infrastructure for small companies and demand for the office computer. As a result, many dc/dc topologies with a high efficiency have been developed for these medium power applications, which require the hold-up time conditions [5]–[7] and high output current. Especially, as the climate savers computing initiative [8] recently requires higher efficiency at 10% and 20% load conditions than before to achieve 80 PLUS titanium-certification, the importance of the efficiency at 10% and 20% load conditions has been highlighted.

The conventional asymmetrical half-bridge (AHB) converter is one of suitable candidates for medium power applications requiring high output current due to low primary and secondary RMS currents caused by its output inductor and low voltage stresses on the primary switches [9]–[13]. However, the AHB converter has some limitations caused by the hold-up time conditions where its output voltage should be regulated during 20 ms after ac line is lost. The hold-up time conditions make the AHB converter to operate with asymmetrical switching at nominal input. It results in many problems such as a large transformer dc-offset current and narrow ZVS range. Moreover, the primary and secondary switch turn-off losses and snubber loss in the secondary side, caused by the output inductor, have a deteriorative influence on light load efficiency.

In order to overcome aforementioned drawbacks caused by asymmetrical switching operation in the AHB converter, several researches have been progressed on the symmetrical half-bridge (SHB) converters. In [14] and [15], one additional switch and diode are added to remove the transformer dc-offset current and improve the ZVS capability. However, due to additional devices, driving circuitry becomes more complex. Moreover, since the SHB converters have the output inductor, the switch turn-off losses and snubber loss still degrade light load efficiency like the AHB converter.

To decrease the primary conduction losses maintaining the advantages of the SHB converters without additional devices, the PFM HB converter has been proposed in [16]. The PFM HB converter controls its output voltage by varying the voltage across the blocking capacitor C_B according to the switching frequency. Since it has higher voltage conversion ratio compared with the AHB and SHB converters, it increases the transformer turns ratio, and thus, the conduction losses in the primary switches are decreased. However, the switch turn-off losses and snubber loss are still burdened under light load conditions like the AHB and SHB converters. Moreover, to achieve the ZVS of the primary switches under light load conditions, large transformer leakage inductor is required, which can degrade medium and heavy load efficiency. Consequently, although the converters with the output inductor can achieve a high efficiency under medium and heavy load conditions due to low primary and secondary RMS currents, they have common problems such as the primary and secondary switch turn-off losses and snubber loss in

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the secondary side, which degrades light load efficiency. Moreover, they have poor ZVS capability at light load conditions.

To improve light load efficiency in the converters with the output inductor, several researches have been presented [17]–[19]. In [17], a method to improve light load efficiency has been proposed by periodically turning OFF the converter to reduce the switching-related losses. While the converter is turned OFF, the required output power is supplied from the snubber capacitor in the secondary side. As a result, the switching losses in the primary side and transformer core loss can be reduced. However, this method needs large size snubber capacitors to supply the energy. Therefore, it is difficult to apply this method to the server power supplies and PC power supplies requiring a high power density. In [18], a gate driving method to improve light load efficiency is proposed. This method reduces the gate driving voltage of the switches and operating voltage of the controller ICs under light load conditions by adjusting auxiliary output voltage of the standby converter. Therefore, the gate driving losses on the switches and losses on the controller ICs can be decreased. However, since the gate driving losses and losses on the controller ICs occupy a small portion in total losses at 10% and 20% load conditions, the efficiency improvement is small at these conditions. In [19], a control method, which has wide dead time under light load conditions, is proposed. By enlarging the dead time between the primary switches at light load conditions, the ZVS range of the primary switches can be wide, and thus, the primary switch turn-on losses are reduced. However, this method does not guarantee a full ZVS capability of the primary switches due to small energy stored in the transformer leakage inductor. Therefore, this method still generates the switch turn-on losses. Moreover, since it has the output inductor, the switch turn-off losses and snubber loss still degrade light load efficiency.

Meanwhile, the conventional HB *LLC* converter is also one of the popular converters in medium power applications because of no transformer dc-offset current, wide ZVS range, and low voltage stresses on the primary switches. Moreover, since it has no output inductor, the snubber loss in the secondary side is eliminated. In addition, since it is generally designed in resonant or below region to achieve a full ZVS capability of the primary switches and minimize the switch turn-off losses, it achieves a high efficiency especially under light load conditions [20]. However, due to no output inductor, its primary and secondary RMS currents and the number of the output capacitor are considerably increased compared with the PFM HB converter. Therefore, the HB *LLC* converter is limited in medium power applications with high output current, although it has merits such as low switch turn-off losses and no snubber loss.

In order to achieve a high efficiency over entire load conditions for wide input voltage and high output current applications such as the server power supplies and PC power supplies, a new HB converter, which employs one additional switch Q_A and capacitor C_A, is proposed as shown in Fig. 1. The primary switches Q_{p1} and Q_{p2} of the proposed converter are turned ON and OFF by the PFM with a 50% fixed duty cycle, and Q_A is turned ON or OFF according to the input voltage or output load conditions. The proposed converter has following operations

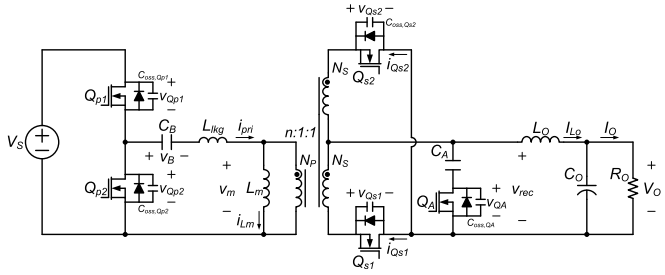


Fig. 1. Circuit diagram of the proposed converter.

and advantages according to the input voltage or output load conditions.

1) From full-load conditions to 30% load conditions at nominal input, the proposed converter operates like the PFM HB converter by turning OFF Q_A. At these conditions, the proposed converter controls its output voltage by varying the voltage across the blocking capacitor C_B. Since the proposed converter has the output inductor, it features low primary and secondary RMS currents. Therefore, the proposed converter can achieve a high efficiency at these conditions, where the conduction loss is a dominant factor at the efficiency.
2) On the other hand, below 30% load conditions at nominal input, the proposed converter operates like the HB *LLC* converter with below operation by turning ON Q_A. Therefore, at these conditions, it has low switch turn-off losses, no snubber loss, and wide ZVS range compared with the PFM HB converter, which improves light load efficiency.
3) During the hold-up time, the proposed converter operates like the PFM HB converter to regulate the output voltage by turning OFF Q_A.

This paper is organized as follows: The operational principle and analysis of the proposed converter are discussed in Sections II and III, respectively. A 330–400 V input and 12 V/300 W output laboratory prototype is built and tested to verify the effectiveness of the proposed converter in Section IV.

II. Operational Principles

Fig. 1 shows the circuit diagram of the proposed converter. Compared with the conventional PFM HB converter, one additional switch Q_A and capacitor C_A are employed in the secondary side for the topology change according to the input voltage or output load conditions. Fig. 2(a) shows the secondary circuit of the proposed converter above 30% load conditions at nominal input or during the hold-up time. During these conditions, the proposed converter operates like the PFM HB converter by turning OFF Q_A. In addition, Fig. 2(b) shows the secondary circuit of the proposed converter below 30% load conditions at nominal input. During these conditions, the proposed converter operates like the HB *LLC* converter with the output *CLC* filter by turning ON Q_A. The gates of Q_{p1} and Q_{p2} are complementarily turned ON and OFF by the PFM with a 50% fixed duty cycle. Since the output current is large, two secondary switches $Q_{\rm s1}$ and $Q_{\rm s2}$ are adopted. For the

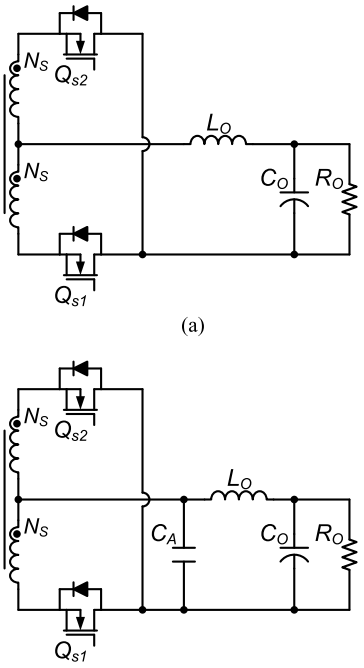


Fig. 2. Secondary circuits according to input voltage or output load conditions. (a) Above 30% load conditions at nominal input or during hold-up time. (b) Below 30% load conditions at nominal input.

convenience of the mode analysis in steady-state conditions, several assumptions are made as follows.

1) All parasitic components are ignored except for the output capacitor $C_{\mathrm{oss},QA}$ of Q_A.
2) The transformer leakage inductor L_{lkg} is considered only below 30% load conditions at nominal input.
3) The output inductor L_O is large enough to be considered as a constant current source.
4) The output voltage V_O is constant.
5) The dead time T_d between the primary switches is small enough to be ignored.

Each switching cycle can be divided into two half cycles $t_0 - t_1$ and $t_1 - t_2$ above 30% load conditions at nominal input or during the hold-up time, and $t_0 - t_2$ and $t_2 - t_4$ below 30% load conditions at nominal input. Due to symmetric operation, each first half cycle is only explained. The operational key waveforms for each case are, respectively, shown in Fig. 3(a) and (b), and each equivalent circuit is, respectively, shown in Figs. 4 and 5.

A. Above 30% Load Conditions at Nominal Input or During Hold-Up Time

In these conditions, the proposed converter operates like the PFM HB converter by turning OFF Q_A.

Mode 1 [t_0–t_1]: When Q_{p1} and Q_{s1} are turned ON at t_0, mode 1 begins. The input power is transferred to the output as shown in Fig. 4. Since Q_{s1} is conducted, the load current I_O is reflected to the primary side of the transformer. At the same time, $V_S - v_B(t)$ is applied to the magnetizing inductor

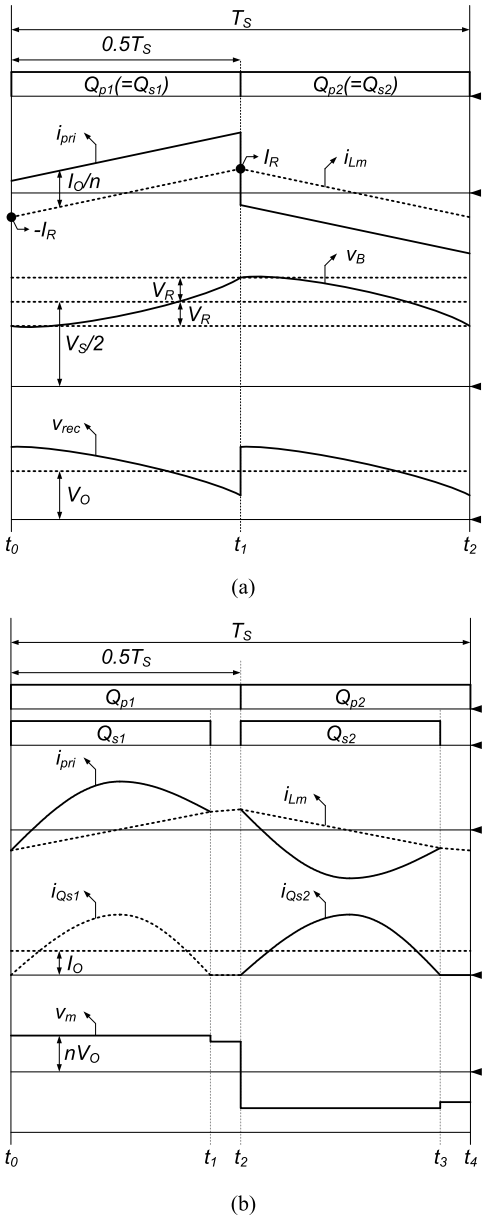


Fig. 3. Operational key waveforms of the proposed converter. (a) Above 30% load conditions or during hold-up time. (b) Below 30% load conditions.

L_m. Therefore, the magnetizing inductor current $i_{Lm}(t)$ and primary current $i_{\mathrm{pri}}(t)$ are, respectively, expressed as follows:

$$i_{Lm}(t) = i_{Lm}(t_0) + \left(\frac{V_S - v_B(t)}{L_m}\right)(t - t_0) \tag{1}$$

$$i_{\mathrm{pri}}(t) = i_{Lm}(t) + \frac{I_O}{n}. \tag{2}$$

The voltage $v_B(t)$ across the blocking capacitor C_B is charged by $i_{\mathrm{pri}}(t)$ as follows:

$$v_B(t) = v_B(t_0) + \int_{t_0}^{t} i_{\mathrm{pri}}(t)dt. \tag{3}$$

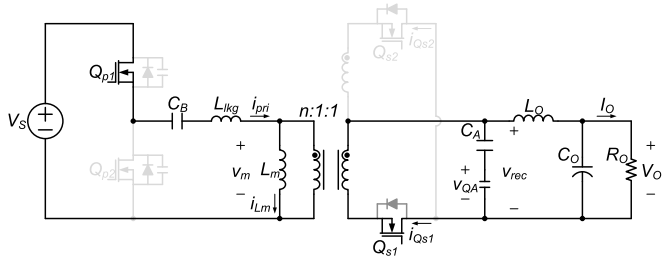


Fig. 4. Equivalent circuits of mode 1 above 30% load conditions or during hold-up time.

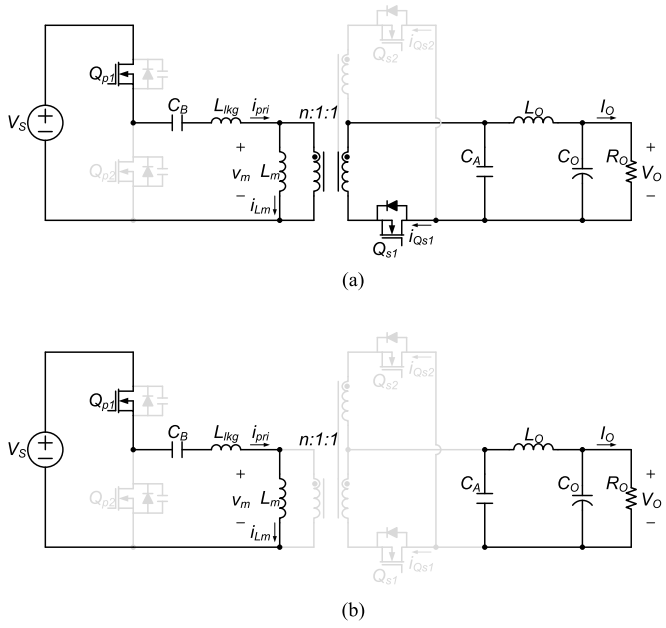


Fig. 5. Equivalent circuits below 30% load conditions. (a) mode 1 ($t_0 - t_1$). (b) mode 2 ($t_1 - t_2$).

During this mode, since Q_A is turned OFF, $C_{\mathrm{oss},QA}$ is connected to C_A in series. Since $C_{\mathrm{oss},QA}$ is sufficiently small compared with C_A, the voltage $v_{QA}(t)$ across Q_A becomes almost equal to $(V_S - v_B(t))$/n, i.e., $v_{\mathrm{rec}}(t) = (V_S - v_B(t))/\mathrm{n}$.

B. Below 30% Load Conditions at Nominal Input

In these conditions, to improve light load efficiency, the proposed converter operates like the HB *LLC* converter with below operation by turning ON Q_A.

Mode 1 [t_0–t_1]: When Q_{p1} and Q_{s1} are turned ON at t_0, mode 1 begins. Since Q_{s1} is turned ON, $i_{Lm}(t)$ is linearly increased with a slope of nV_O/L_m, and the resonant operation transfers the power to the output through Q_{s1} as shown in Fig. 5(a).

Mode 2 [t_1–t_2]: At time t_1, $i_{\mathrm{pri}}(t)$ becomes equal to $i_{Lm}(t)$, and Q_{s1} is turned OFF. At this mode, since $v_B(t)$ charged by $i_{\mathrm{pri}}(t)$ is large, the body diode of Q_{s1} is not conducted as shown in Fig. 5(b). Therefore, L_m, L_{lkg}, and C_B begin to resonate.

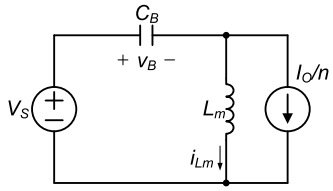


Fig. 6. Equivalent circuit in mode 1 above 30% load conditions or during hold-up time.

III. Analysis of the Proposed Converter

A. Voltage Conversion Ratio

To simplify the analysis of the voltage conversion ratio above 30% load conditions at nominal input or during the hold-up time, L_{lkg} and T_d are small enough to be ignored.

Fig. 6 is an equivalent circuit in mode 1 above 30% load conditions at nominal input or during the hold-up time. As shown in this figure, a resonant $L_m C_B$ circuit is formed. From this figure, two equations are obtained as follows:

$$C_B \frac{dv_B(t)}{dt} = i_{Lm}(t) + \frac{I_O}{n} \tag{4}$$

$$V_S = v_B(t) + L_m \frac{di_{Lm}(t)}{dt} \tag{5}$$

where the initial values of $v_B(t)$ and $i_{Lm}(t)$ are respectively expressed as follows:

$$v_B(t_0) = \frac{V_S}{2} - V_R \tag{6}$$

$$i_{Lm}(t_0) = -I_R. \tag{7}$$

Therefore, $v_B(t)$ and $i_{Lm}(t)$ are obtained from (4), (5), (6), and (7) as follows:

$$v_B(t) = -(V_S - v_B(t_0))\cos\omega_O t + Z\left(\frac{I_O}{n} + i_{Lm}(t_0)\right) \sin\omega_O t + V_S \tag{8}$$

$$i_{Lm}(t) = \left(i_{Lm}(t_0) + \frac{I_O}{n}\right)\cos\omega_O t + \left(\frac{V_S - v_B(t_0)}{Z}\right) \sin\omega_O t - \frac{I_O}{n} \tag{9}$$

where the characteristic impedance Z and resonant angular frequency ω_O are defined as

$$Z = \sqrt{\frac{L_m}{C_B}} \tag{10}$$

$$\omega_O = \frac{1}{\sqrt{L_m C_B}}. \tag{11}$$

After a half switching cycle, $v_B(t)$ and $i_{Lm}(t)$ become $V_S - v_B(t_0)$ and $-i_{Lm}(t_0)$. As a result, the initial values of $v_B(t)$ and $i_{Lm}(t)$ are respectively obtained as

$$v_B(t_0) = \frac{V_S}{2} - V_R = \frac{V_S}{2} - \frac{I_O Z}{n}\frac{(1 - \cos(0.5\,\omega_O/f_S))}{\sin(0.5\,\omega_O/f_S)}$$

(12)

$$i_{Lm}(t_0) = -I_R = -\frac{V_S}{2Z}\frac{\sin(0.5\,\omega_O/f_S)}{(1+\cos(0.5\,\omega_O/f_S))} \tag{13}$$

where f_S is the switching frequency.

As shown in Fig. 3(a), since the average of $v_{\rm rec}(t)$ is equal to V_O, V_O can be expressed as follows:

$$V_O = \frac{1}{T_S/2}\int_0^{T_S/2}\frac{1}{n}(V_S - v_B(t))dt. \tag{14}$$

Therefore, from (8), (12), (13), and (14), the voltage conversion ratio of the proposed converter above 30% load conditions at nominal input or during the hold-up time is obtained as follows:

$$M = \frac{nV_O}{V_S} = \frac{f_S}{\pi f_O}\frac{\sin(\pi f_O/f_S)}{1+\cos(\pi f_O/f_S)} \tag{15}$$

where $f_O = 1/[2\pi(L_m C_B)^{0.5}]$.

From (15), it can be seen that the voltage conversion ratio is dependent on n, f_O, and f_S.

Meanwhile, since the proposed converter operates like the HB *LLC* converter below 30% load conditions at nominal input, its voltage conversion ratio below 30% load conditions can be represented as follows [21]:

$$M = \frac{nV_O}{V_S} = \frac{1}{2\sqrt{\left\{1+\frac{1}{K}\left[1-\left(\frac{f_R}{f_S}\right)^2\right]\right\}^2 + \left[\left(\frac{f_S}{f_R}-\frac{f_R}{f_S}\right)\frac{\pi^2}{8n^2}Q\right]^2}} \tag{16}$$

where $K = L_m/L_{\rm lkg}$, $f_R = 1/[2\pi(L_{\rm lkg}C_B)^{0.5}]$, and $Q = (L_{\rm lkg}/C_B)^{0.5}/R_O$.

B. Zero-Voltage Switching

Since the switching operations of Q_{p1} and Q_{p2} are symmetrical, only Q_{p2} is considered. To analyze the ZVS operations in detail, the output capacitors $C_{{\rm oss},Qp1}$ and $C_{{\rm oss},Qp2}$ of the primary switches, output capacitor $C_{{\rm oss},Qs2}$ of the secondary switch $Q_{\rm s2}$, and transformer equivalent capacitor $C_{\rm eq,trans}$ are considered. Fig. 7 shows the key waveforms during the ZVS operations of Q_{p1} and Q_{p2} above 30% load conditions at nominal input. At time t_0, Q_{p1} is turned OFF. Fig. 8(a) shows the equivalent circuit between t_0 and t_1 in Fig. 7, where $2C_{{\rm oss},Qp}$, total equivalent output capacitor of the primary switches, and $C_{{\rm oss},Qs2r}$, reflected output capacitor of the secondary switch $Q_{\rm s2}$, are figured out to be $2C_{{\rm oss},Qp} = C_{{\rm oss},Qp1} + C_{{\rm oss},Qp2}$ and $C_{{\rm oss},Qs2r} = 4C_{{\rm oss},Qs2}/n^2$. $C_{\rm eq,trans}$, which results from the stray capacitors among the windings in the transformer, can be placed in parallel with the transformer. Provide that the effect of $L_{\rm lkg}$ is sufficiently small between t_0 and t_1, $i_{Lm}(t_0)$ and I_O/n, considered as a current source, would discharge $2C_{{\rm oss},Qp}$, $C_{{\rm oss},Qs2r}$, and $C_{\rm eq,trans}$. Thus, $v_{Qp2}(t)$ is linearly decreased and reaches $V_S/2 + V_R$ at t_1, and the voltage $v_{C{\rm eq,trans}}(t)$ across

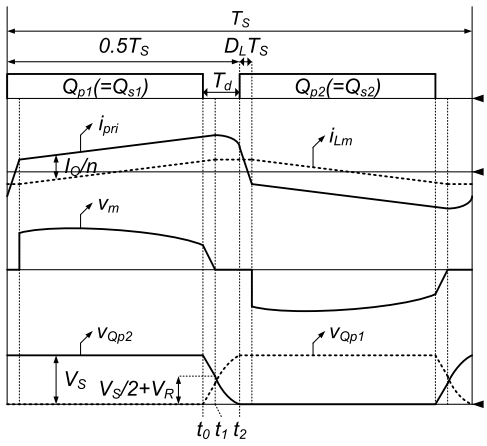


Fig. 7. Key waveforms during ZVS operations above 30% load conditions.

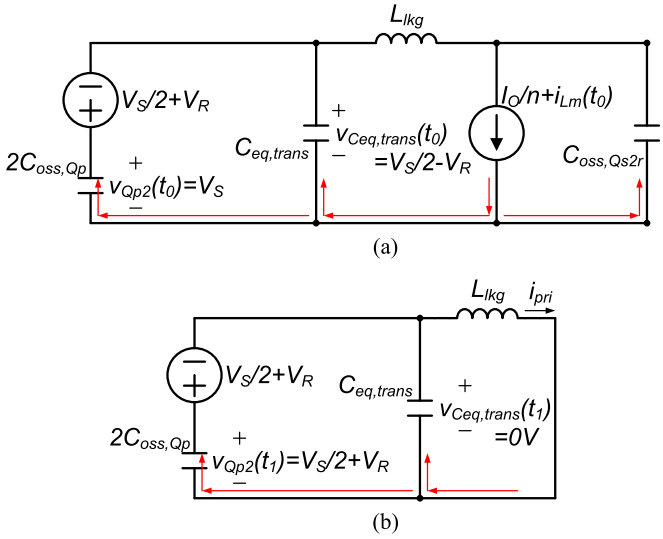


Fig. 8. Equivalent circuits in Fig. 9 above 30% load conditions. (a) $t_0 - t_1$. (b) $t_1 - t_2$.

$C_{\rm eq,trans}$ and voltage $v_{Qs2}(t)$ across $Q_{\rm s2}$ simultaneously become 0 V at t_1. If the effect of the transformer leakage inductor $L_{\rm lkg}$ is sufficiently small, $v_{Qp2}(t)$ can be expressed during t_0 – t_1 as follows:

$$v_{Qp2}(t) = V_S - \frac{i_{Lm}(t_0) + I_O/n}{2C_{{\rm oss},Qp} + C_{{\rm oss},Qs2r} + C_{eq,{\rm trans}}}(t - t_0). \tag{17}$$

However, $v_{Qp2}(t)$ is not completely discharged yet. Since the body diode of $Q_{\rm s2}$ is conducted between t_1 and t_2, the voltage $v_m(t)$ across L_m maintains 0 V. Therefore, the energy stored in $L_{\rm lkg}$ discharges the rest of $v_{Qp2}(t)$, and it also decreases $v_{C{\rm eq,trans}}(t)$ from 0 to $-V_S/2 - V_R$ V as shown in Fig. 8(b). Therefore, the ZVS conditions of Q_{p2} can be expressed as follows:

$$\frac{1}{2}L_{\rm lkg}i_{\rm pri}(t_1)^2 \geq \frac{1}{2}(2C_{{\rm oss},Qp} + C_{eq,{\rm trans}})\,(0.5V_S + V_R)^2\,. \tag{18}$$

In the conventional PFM HB converter, since $i_{\rm pri}(t_1)$ is small below 30% load conditions, large $L_{\rm lkg}$ is required to achieve a full ZVS capability, which causes large duty cycle loss D_L in Fig. 7 and degrades medium and heavy load efficiency. If the method in [19] to improve the light load efficiency by enlarging the dead time under light load conditions is applied to the PFM HB converter, the ZVS range of the primary switches can be wide, and thus, the switch turn-on losses are reduced. However, this method does not guarantee a full ZVS capability of the primary switches due to small energy stored in the transformer leakage inductor.

On the other hand, below 30% load conditions in the proposed converter, since the ZVS of the primary switches is achieved by the energy stored in L_m, the ZVS capability is very excellent, which improves light load efficiency compared with the PFM HB converter and PFM HB converter with [19].

C. Switch Turn-off Losses and Snubber Loss Below 30% Load Conditions

In this section, the switch turn-off losses and snubber loss in the proposed converter are compared with those in the conventional PFM HB converter below 30% load conditions. The switch turn-off losses and snubber loss in the PFM HB converter with [19] are the same as those of the PFM HB converter.

Fig. 9(a) and (b) shows the primary and secondary currents and voltages across the secondary switches in the conventional and proposed converter below 30% load conditions. The switch turn-off loss is mainly determined by the switch current at the turn-off instant [22]. In the conventional converter, the turn-off current $i_{Q\rm s1}(t_1)$ of the secondary switch $Q_{\rm s1}$ is I_O due to L_O as shown in Fig. 9(a). Moreover, the turn-off current $i_{\rm pri}(t_1)$ of the primary switch Q_{p1} is $i_{Lm}(t_1)+I_O/n$, since I_O is reflected to the primary side of the transformer. Meanwhile, in the proposed converter, since it operates like the HB *LLC* converter with below operation below 30% load conditions, the turn-off current $i_{\rm pri}(t_2)$ of Q_{p1} is equal to $i_{Lm}(t_2)$ as shown in Fig. 9(b). Moreover, since $i_{Q\rm s1}(t)$ is the difference between $i_{\rm pri}(t)$ and $i_{Lm}(t)$, the turn-off current $i_{Q\rm s1}(t_1)$ of $Q_{\rm s1}$ becomes 0 A. Consequently, the turn-off currents of the primary and secondary switches in the proposed converter are, respectively, reduced and eliminated compared with those in the conventional converter. Therefore, the switch turn-off losses in the proposed converter are reduced.

The isolated converters, employing the output inductor, suffer from a voltage ringing across the secondary switches as shown in Fig. 9(a), since the transformer leakage inductor and output capacitor of the secondary switch are interacted after the commutation between the secondary switches [23], [24]. The ringing increases the voltage stresses on the secondary switches and, thus, two RCD snubbers are required to prevent additional voltage stresses, which degrades light load efficiency. Therefore, the conventional converter employing the output inductor has the snubber loss. Meanwhile, in the proposed converter, the voltage stresses across the secondary switches are clamped to $2\,V_O$ due to the output *CLC* filter as shown in Fig. 9(b). Therefore, the snubber loss is eliminated in the proposed converter, which improves the efficiency below 30% load conditions.

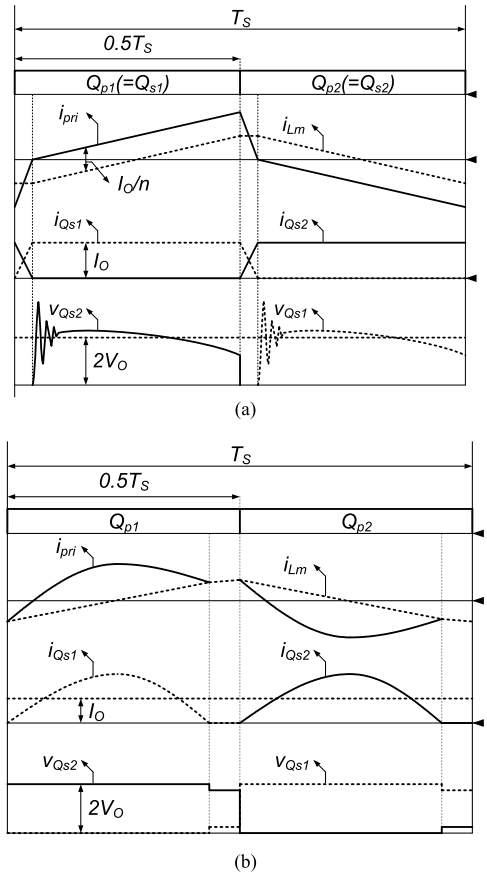


Fig. 9. Comparison of current and voltage waveforms below 30% load conditions. (a) Conventional PFM HB converter. (b) Proposed converter.

D. Design Considerations

In this paper, to verify the feasibility of the proposed converter, a design example of resonant tank is presented. The proposed converter has the following specifications: input voltage = 330 ∼ 400 V, output voltage = 12 V, and rated power = 300 W.

1) Transformer Turns Ratio n: Fig. 10 shows the voltage conversion ratio of the proposed converter above 30% load conditions at nominal input or during the hold-up time. As shown in this figure, as the switching frequency is increased, the output voltage approaches $0.5\,V_S/n$ [25]. Therefore, to obtain the output voltage, $0.5\,V_{S,\max}/n$ should be smaller than the output voltage, which can be expressed as follows:

$$n \geq \frac{V_{S,\max}}{2V_O}. \tag{19}$$

For example, if *n* is 16, $0.5\,V_{S,\max}/n$ is 12.5 V, and thus, the desired output voltage cannot be obtained at nominal input 400 V. From (19), it can be seen that *n* should be over 16.67 to regulate the output voltage. If *n* is increased, f_S/f_O is decreased as shown in Fig. 10. As a result, the switching frequency can be

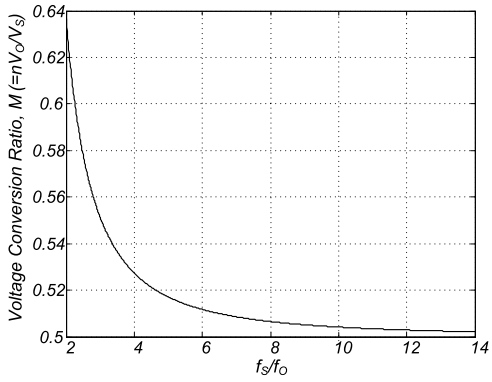


Fig. 10. Voltage conversion ratio above 30% load conditions or during hold-up time.

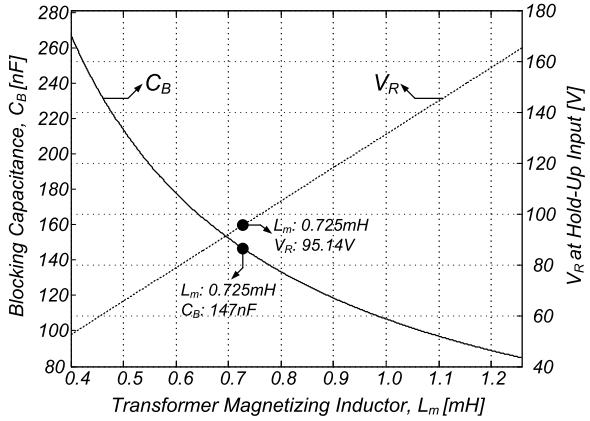


Fig. 11. V_R at hold-up input and C_B according to L_m.

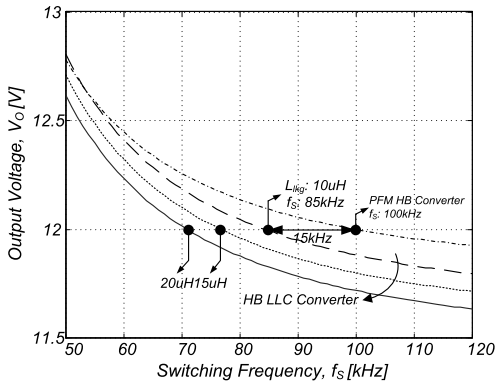


Fig. 12. Output voltage at 30% load conditions according to $L_{\rm lkg}$.

extremely decreased at the hold-up input 330 V, which increases the size of the transformer. Therefore, *n* is chosen as 17.

2) Transformer Magnetizing Inductor L_m and Blocking Capacitor C_B: Because of $n = 17$, f_S/f_O is calculated as 6.49 at nominal input, and f_S/f_O is calculated as 2.11 at the hold-up input from (15). Assuming that the switching frequency at nominal input is chosen as 100 kHz, considering the overall system efficiency and volume, the minimum switching frequency at the hold-up input is calculated as 32.5 kHz. Meanwhile, if V_R exceeds $0.5\,V_S$, the proposed converter cannot properly operate. Therefore, V_R should be smaller than $0.5\,V_{S,\min}$ at full-load conditions, which can be expressed as follows:

$$\frac{I_O Z}{n}\frac{(1-\cos(\pi f_O/f_S))}{\sin(\pi f_O/f_S)} \le \frac{V_{S,\min}}{2}. \tag{20}$$

From (10), (11), and (20), L_m is calculated as follows:

$$L_m \le \frac{nV_{S,\min}\sin(\pi f_O/f_S)}{4\pi f_O I_O(1-\cos(\pi f_O/f_S))} = 1.258\,mH. \tag{21}$$

Fig. 11 shows V_R at the hold-up input and C_B according to the variation of L_m. As shown in this figure, as L_m is increased, C_B is decreased, and thus V_R at the hold-up input is increased. To prevent the proposed converter from operating improperly, L_m is chosen as 725 μH, and C_B is calculated as 147 nF from (11).

3) Transformer Leakage Inductor $L_{\rm lkg}$: To obtain a high efficiency over entire load conditions at nominal input, the ZVS of the primary switches should be achieved. Since the ZVS of the primary switches is achieved by the energy stored in L_m below 30% load conditions at nominal input, the ZVS capability is very excellent at these conditions. Meanwhile, the ZVS of the primary switches is achieved by the energy stored in $L_{\rm lkg}$ above 30% load conditions at nominal input. As a result, to ensure the ZVS at these conditions, the required minimum leakage inductor can be determined from (18) as

$$L_{\rm lkg} \ge (2C_{{\rm oss},Qp} + C_{eq,{\rm trans}})\left(\frac{0.5\,V_S + V_R}{i_{\rm pri}(t_1)}\right)^2. \tag{22}$$

Since the primary switches used in the experiment are IPP60R385CP with the effective output capacitance 36 pF, the minimum leakage inductor is calculated as 6.27 μH from (22).

Fig. 12 shows the output voltage at 30% load conditions according to the variation of $L_{\rm lkg}$ above 6.27 μH. From this figure, it is noted that the operating switching frequency of the HB *LLC* converter approaches that of the PFM HB converter as $L_{\rm lkg}$ decreases. However, since very small $L_{\rm lkg}$ degrades the ZVS capability of the PFM HB converter, it is difficult to extremely decrease $L_{\rm lkg}$. To decrease the variation of the switching frequency, $L_{\rm lkg}$ is chosen as 10 μH. Since the difference between their operating switching frequencies in transient mode is small, the output voltage control loop can compensate the difference between their operating switching frequencies.

4) Design of Output CLC Filter: Since the output voltage ripple is the largest at full-load conditions, the output filter should be designed at full-load conditions. Since the proposed converter operates like the PFM HB converter at full-load conditions, the output inductor L_O and output capacitor C_O should be designed in advance. For the sake of the analysis, T_d is ignored, and it is assumed that $v_B(t)$ is linearly charged and discharged by $i_{\rm pri}(t)$. Fig. 13 shows simplified voltage and current waveforms above 30% load conditions at nominal input. Since $v_{\rm rec}(t)$ is $(V_S - v_B(t))/n$ as explained in mode 1, the peak-to-peak output inductor current ripple Δi_{Lo} can be

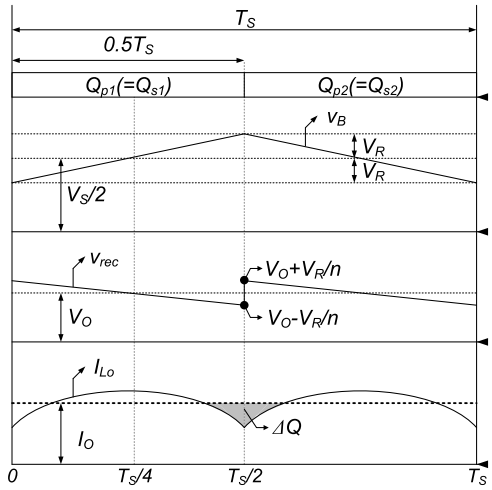


Fig. 13. Simplified voltage and current waveforms above 30% load conditions.

approximated as follows:

$$\Delta i_{Lo} \simeq \frac{1}{L_O} \int_0^{T_S/4} (v_{\rm rec}(t) - V_O)dt = \frac{V_R}{8nL_O f_S}. \quad (23)$$

The output capacitor can be approximated by calculating ΔQ from Fig. 13 as follows:

$$C_O = \frac{\Delta Q}{\Delta V_O} \simeq \frac{0.008\, V_R}{nL_O \Delta V_O f_S^2} \quad (24)$$

where ΔV_O is the output voltage ripple.

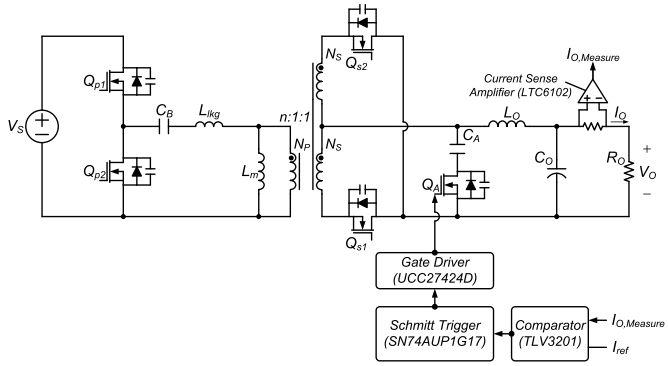
Meanwhile, since the proposed converter operates like the HB *LLC* converter with the output *CLC* filter below 30% load conditions, C_A should be designed. When the proposed converter operates in below region, C_A can be expressed as in (25) with the assumption that the output voltage ripple is neglected [26]

$$C_A = \frac{I_O}{8L_O \Delta i_{Lo}} \left(\frac{1}{4f_S^2} + \frac{1}{\pi f_S f_R} - \frac{1}{2f_S f_R} \right). \quad (25)$$

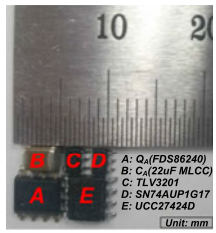
IV. Experimental Results

A. Implementation of the Proposed Converter

To verify the feasibility of the proposed converter, a 300 W prototype converter with the specifications of $V_S = 330 - 400$ V and $V_O = 12$ V has been built. Fig. 14(a) shows the implementation circuit of the proposed converter. In the proposed converter, one additional switch Q_A and multilayer ceramic capacitor C_A with very small size are employed in the secondary side for the topology change according to the input voltage or output load conditions. The current sense amplifier LTC6102, which is employed to protect over current in the secondary side, is used to measure the output load current. LTC6102 is located between the output capacitor and system capacitor to obtain the constant output load current. Since the server power supplies and PC power supplies require high output current, the sensing resistor in LTC6102 should have small value to reduce the conduction loss. Therefore, four sensing resistors with 1 mΩ in parallel are used, and the gain of LTC6102 is chosen as 750 by using the input and output resistors. To distinguish 30% output load current, measured output load current is compared with a reference $I_{\rm ref}$ by using a comparator TLV3201. However, although the output load current sensed by LTC6102 is constant, there may be an oscillation in the output of the comparator between the operation transfers. Since an oscillation causes abnormal operation of Q_A, a Schmitt trigger IC SN74AUP1G17 is utilized to eliminate the oscillation. The output of a Schmitt trigger is connected to the gate driver UCC27424D for Q_A. Due to these additional components, the size of the overall system may be slightly increased. However, since they are implemented with compact size as shown in Fig. 14(b), the power density of the proposed converter can be maintained compared with that of the conventional PFM HB converter. Fig. 15 shows a 300 W prototype of the proposed converter including the power



(a)



(b)

Fig. 14. Implementation of proposed converter. (a) Implementation circuit. (b) Size of additional components.

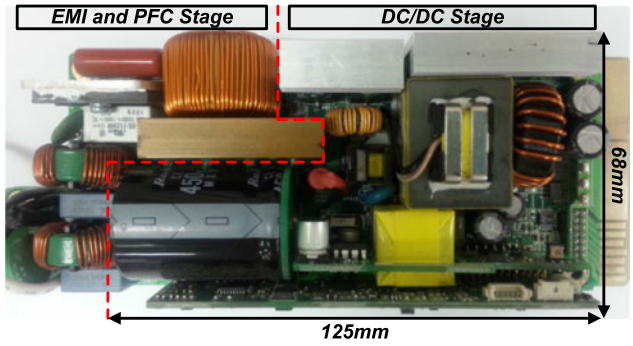
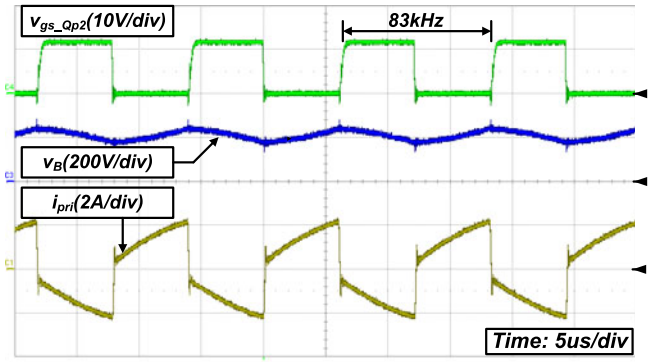


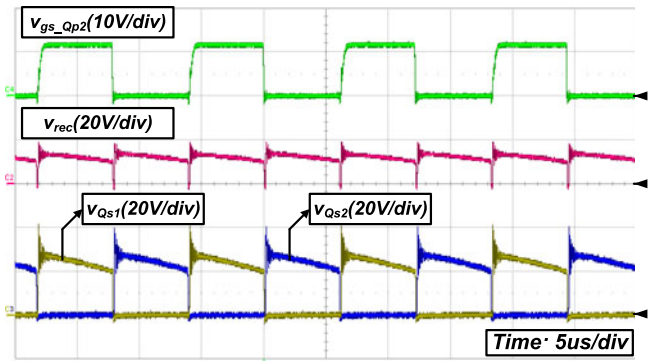
Fig. 15. 300 W prototype converter.

TABLE I
DESIGNED PARAMETERS

Components list	Conventional PFM HB converter	Proposed converter
Primary switches (Q_{p1}, Q_{p2})	IPP60R385CP(650V/9A)	IPP60R385CP(650 V/9 A)
Transformer	Core: PQ3220 L_m : 720 μH $L_{\rm lkg}$: 12.3 μH $N_P : N_S : N_S = 17 : 1 : 1$	Core: PQ3220 L_m : 720 μH $L_{\rm lkg}$: 12.3 μH $N_P : N_S : N_S = 17 : 1 : 1$
Blocking capacitor (C_B)	147 nF	147 nF
Secondary switches (Q_{s1}, Q_{s2})	IRFB3206GPBF (75 V, 120 A, $R_{ds,on}$: 3 mΩ)	IRFB3206GPBF (75 V, 120 A, $R_{ds,on}$: 3 mΩ)
Output inductor (L_O)	0.31 μH	0.31 μH
Additional capacitor (C_A)	–	22 μF
Output capacitor (C_O)	82 μF	82 μF



(a)



(b)

Fig. 16. Experimental key waveforms at full-load conditions. (a) v_{gsQp2}, v_B, and $i_{\rm pri}$ in primary side. (b) $v_{\rm rec}$, $v_{Q\rm s1}$, and $v_{Q\rm s2}$ in secondary side.

factor correction and dc/dc stages. The width, height length, and height of a 300 W prototype converter are 125, 68, and 30 mm, respectively. For the comparison, the prototypes of the PFM HB converter and PFM HB converter with [19] have also been implemented. The designed parameters are presented in Table I.

B. Experimental Key Waveforms and Measured Efficiency

Fig. 16(a) and (b) shows the primary and secondary key waveforms of the proposed converter at full-load conditions under nominal input conditions, respectively. As shown in Fig. 16(a), $v_B(t)$ is charged and discharged by $i_{\rm pri}(t)$. $v_B(t)$ changes $v_{\rm rec}(t)$, and the average of $v_{\rm rec}(t)$ is equal to V_O as shown in Fig. 16(b). From these figures, it can be seen that the required switching frequency to regulate the output voltage is 83 kHz. The switching frequency used in the experiment can have a slightly difference compared with the theoretical analysis due to the duty cycle loss resulting from $L_{\rm lkg}$.

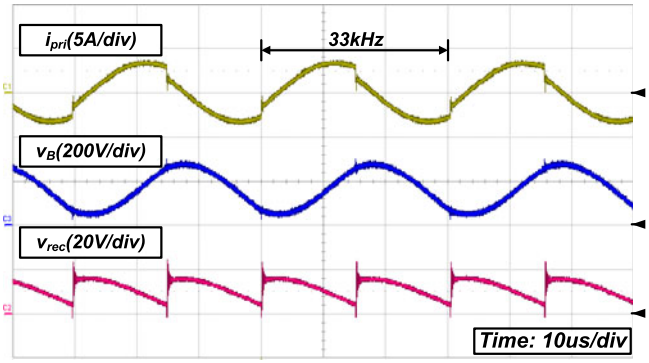


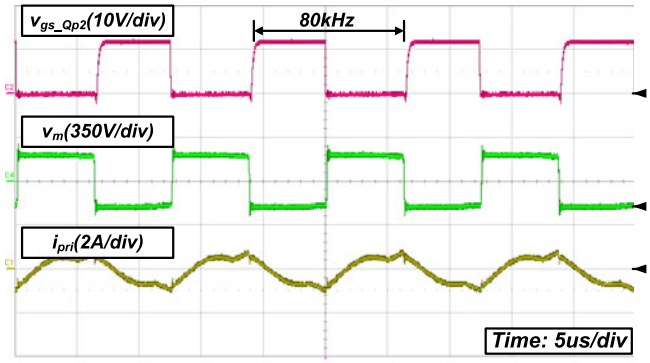
Fig. 17. Experimental key waveforms under hold-up time conditions.

Fig. 17 shows the operational key waveforms of the proposed converter at full-load conditions under the hold-up time conditions 330 V. As shown in this figure, the switching frequency is smaller than that at nominal input, which enables the variation of $v_B(t)$ to be increased. That is, to achieve higher gain under the hold-up time conditions, the switching frequency is decreased to 33 kHz.

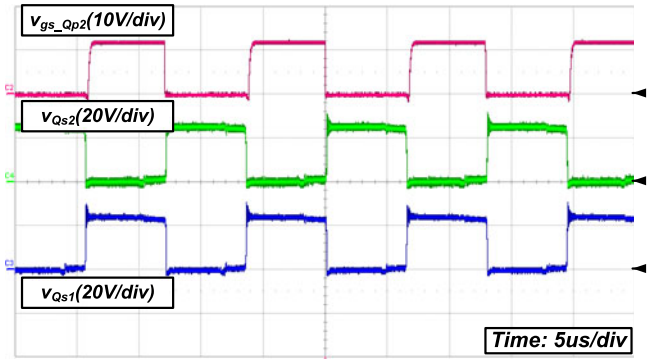
Fig. 18(a) and (b) shows the primary and secondary key waveforms of the proposed converter at 20% load conditions under nominal input conditions, respectively. From $i_{\rm pri}(t)$ in Fig. 18(a), it can be seen that the proposed converter operates like the HB *LLC* converter with below operation, which enables the primary and secondary switch turn-off losses to be minimized. Furthermore, from $v_{Q\rm s1}(t)$ and $v_{Q\rm s2}(t)$ in Fig. 18(b), it is noted that the voltage stresses across the secondary switches of the proposed converter are clamped to $2\,V_O$. Therefore, the proposed converter can improve the efficiency at 10% and 20% load conditions compared with the conventional PFM HB converter.

Figs. 19 and 20 show the ZVS waveforms of the primary switches Q_{p1} and Q_{p2} at 40% and 10% load conditions under nominal input conditions, respectively. As shown in Fig. 19, it is noted that the ZVS of the primary switches is achieved by the energy stored in $L_{\rm lkg}$ at 40% load conditions. Moreover, as shown in Fig. 20, the ZVS of the primary switches is achieved by the energy stored in L_m at 10% load conditions.

Fig. 21(a) shows the key waveforms while the output load current is changed from 11 to 6 A. From this figure, it is noted that the proposed converter is changed from the PFM HB converter to the HB *LLC* converter. When the proposed converter operates like the PFM HB converter at 11 A output load conditions, $v_{QA}(t)$ is almost $(V_S - v_B(t))/n$ due to much smaller $C_{{\rm oss},QA}$ than C_A. If Q_A is turned ON at 30% load conditions 7.5 A, $v_{QA}(t)$ is rapidly decreased to 0 V, and thus, $v_{\rm rec}(t)$

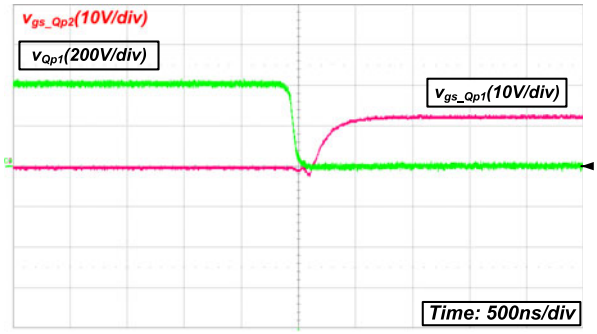


(a)

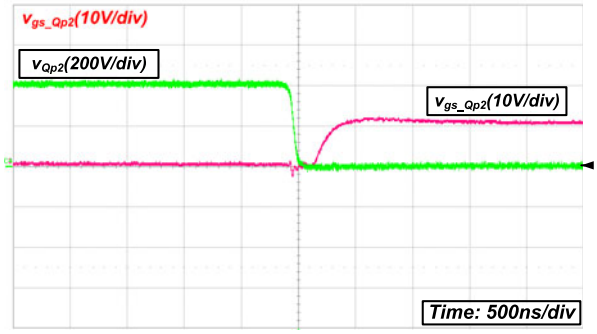


(b)

Fig. 18. Experimental key waveforms at 20% load conditions. (a) v_{gsQp2}, v_m , and $i_{\rm pri}$ in primary side. (b) v_{Qs1} and v_{Qs2} in secondary side.

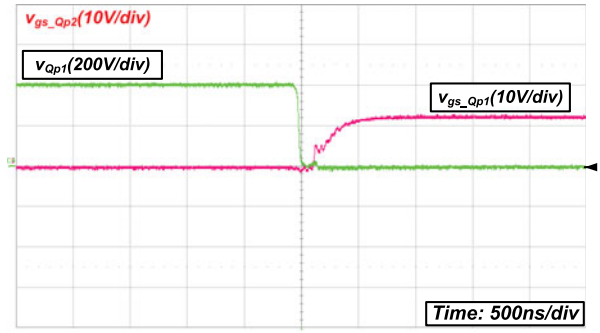


(a)

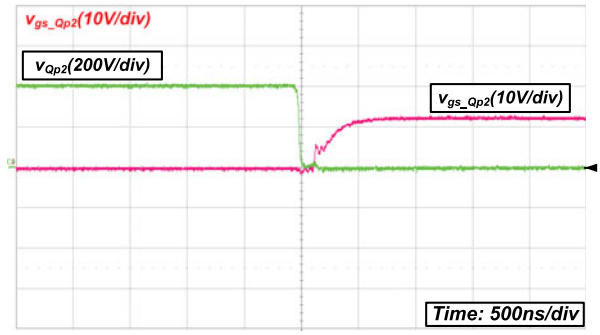


(b)

Fig. 19. ZVS waveforms. (a) Q_{p1} at 40% load. (b) Q_{p2} at 40% load.

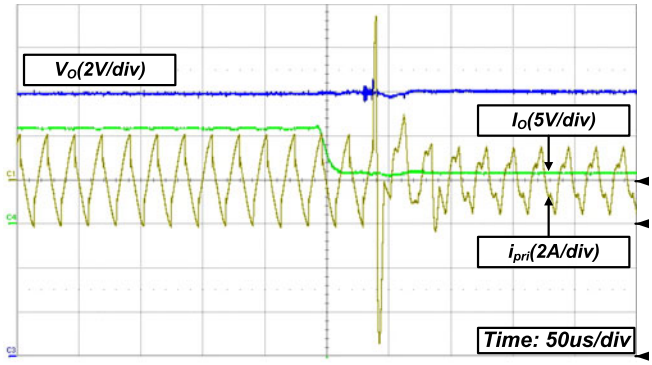


(a)

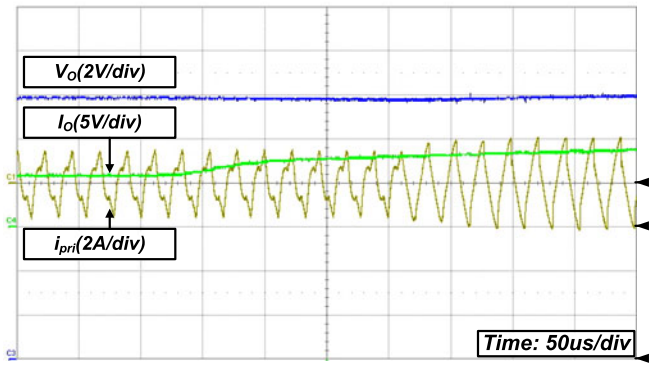


(b)

Fig. 20. ZVS waveforms. (a) Q_{p1} at 10% load. (b) Q_{p2} at 10% load.



(a)



(b)

Fig. 21. Key waveforms during operation mode transfer. (a) $I_{\rm O}$ (11 A) → $I_{\rm O}$ (6 A). (b) $I_{\rm O}$ (6 A) → $I_{\rm O}$ (11 A).

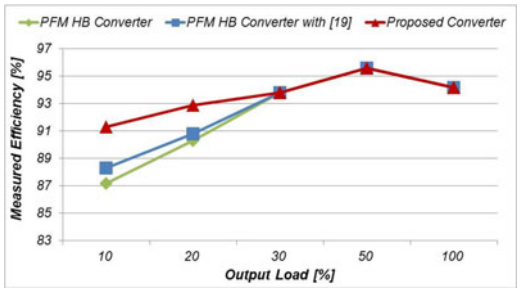


Fig. 22. Measured efficiency.

becomes 0 V. Since $v_{\rm rec}(t)$ should be increased to V_O to enable the proposed converter to operate with the HB *LLC* converter below 7.5 A, $i_{\rm pri}(t)$ and the output inductor current charges C_A. Therefore, as shown in Fig. 21(a), $i_{\rm pri}(t)$ is suddenly increased. However, since the output inductor current as well as $i_{\rm pri}(t)$ charges C_A with 22 μF, the voltage across C_A is increased to V_O for a short time. Fig. 21(b) shows the key waveforms, while the output load current is changed from 6 to 11 A. From this figure, it is noted that the proposed converter is changed from the HB *LLC* converter to the PFM HB converter. Since $v_{\rm rec}(t)$ has already reached V_O, $i_{\rm pri}(t)$ is smoothly changed.

Fig. 22 shows the measured efficiency of the conventional PFM HB converter, PFM HB converter with [19], and the proposed converter according to the output load at nominal input. From this figure, it is noted that the PFM HB converter with [19] has 1.1% and 0.5% higher efficiency at 10% and 20% load conditions compared with the PFM HB converter due to reduced switch turn-on losses. The proposed converter has 3% and 2.1% higher efficiency at 10% and 20% load conditions compared with the PFM HB converter with [19], since it has low switch turn-off losses, no snubber loss, and wide ZVS range.

V. Conclusion

In this paper, in order to improve light load efficiency of the conventional PFM HB converter, a new HB converter with one additional switch and capacitor in the secondary side is proposed for wide input voltage and high output current applications. From full-load conditions to 30% load conditions at nominal input, the proposed converter operates like the conventional PFM HB converter by turning OFF the additional switch. Since the proposed converter has the output inductor at these conditions, it features low primary and secondary RMS currents. Therefore, the proposed converter can achieve a high efficiency at these conditions, where the conduction loss is a dominant factor at the efficiency. On the other hand, to improve the efficiency at 10% and 20% load conditions at nominal input, the proposed converter operates like the HB *LLC* converter with below operation by turning ON additional switch. Therefore, at these conditions, it has low switch turn-off losses, no snubber loss, and wide ZVS range compared with the PFM HB converter with [19], which improves light load efficiency. Consequently, the proposed converter, respectively, shows 3% and 2.1% higher efficiency at 10% and 20% load conditions than that of the PFM HB converter with [19]. Since additional components can be implemented with compact size, the power density of the proposed converter can be maintained compared with that of the PFM HB converter.

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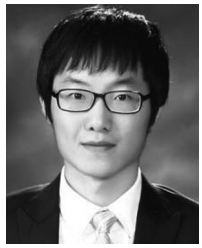

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