A Four-Switch Three-Phase SEPIC-Based Inverter

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***Abstract*—The four-switch three-phase (FSTP) inverter has been proposed as an innovative inverter design to reduce the cost, complexity, size, and switching losses of the dc–ac conversion system. Traditional FSTP inverter usually operates at half the dc input voltage; hence, the output line voltage cannot exceed this value. This paper proposes a novel design for the FSTP inverter based on the topology of the single-ended primary-inductance converter (SEPIC). The proposed topology provides pure sinusoidal output voltages with no need for output filter. Compared to traditional FSTP inverter, the proposed FSTP SEPIC inverter improves the voltage utilization factor of the input dc supply, where the proposed topology provides higher output line voltage which can be extended up to the full value of the dc input voltage. The integral sliding-mode control is used with the proposed topology to optimize its dynamics and to ensure robustness of the system during different operating conditions. Derivation of the equations describing the parameters design, components ratings, and the operation of the proposed SEPIC inverter is presented in this paper. Simulation model and experimental setup are used to validate the proposed concept. Simulations and experimental results show the effectiveness of the proposed inverter.**

***Index Terms*—Four-switch three-phase inverter (FSTP), integral sliding-mode control, single-ended primary-inductance converter (SEPIC) converter, sliding-mode control.**

I. Introduction

PREVIOUSLY, the conventional six-switch three-phase (SSTP) two-level voltage source inverter (VSI) has found widespread industrial applications in different forms such as motor drives, renewable energy conversion systems, and active power filters. However, in some low power range applications, reduced switch count inverter topologies are considered to alleviate the volume, losses, and cost.

Some research efforts have been directed to develop inverter topologies that can achieve the aforementioned goal. The results obtained showed that it is possible to implement a three-phase inverter with only four switches [1]. In four-switch three-phase (FSTP) inverter, two of the output load phases are maintained from the two inverter legs, while the third load phase is fed from the dc-link at the middle point of a split-capacitor bank as shown in Fig. 1. Recently, the FSTP inverter has attracted the most interests regarding its performance, control, and applications [2]–[17].

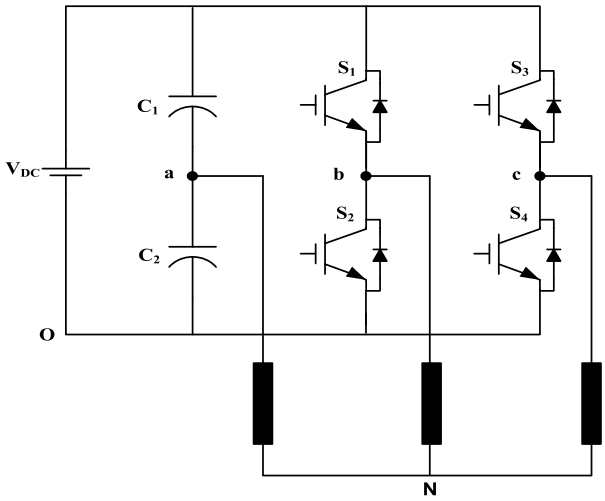

Fig. 1. Conventional FSTP voltage source inverter.

Compared to the traditional SSTP inverter, the FSTP inverter has some advantages such as reduced cost and increased reliability due to the reduction in the number of switches, reduced conduction and switching losses by 1/3, where one entire leg is omitted, and reduced number of interface circuits to supply PWM signals for the switches. The FSTP inverter can also be utilized in fault tolerant control to solve the open/short-circuit fault of the SSTP inverter [2], [8], [10]. However, there are some disadvantages of the conventional FSTP inverter which should be taken into consideration. Similar to the traditional SSTP inverter, the FSTP inverter performs only buck dc–ac conversion. Furthermore, the peak phase voltage of the FSTP inverter is reduced to $V_{\rm DC}/2\sqrt{3}$, where it is $V_{\rm DC}/2$ in the SSTP inverter. In order to boost up the phase voltage of the FSTP inverter to that of SSTP inverter, the typical solution is to insert a dc–dc boost converter between the dc input source and the FSTP inverter. However, this adds significant complexity and hardware to the power conversion system and wastes the merits of the reduced switch count. Also, the FSTP inverter topology is not symmetrical; while two load-phases are directly fed from the two inverter legs, the third load-phase is connected to the center tap of split dc-link capacitors. This forces the current of the third phase to circulate through the dc-link capacitors; hence, a fluctuation will inevitably appear in the two capacitors' voltages,

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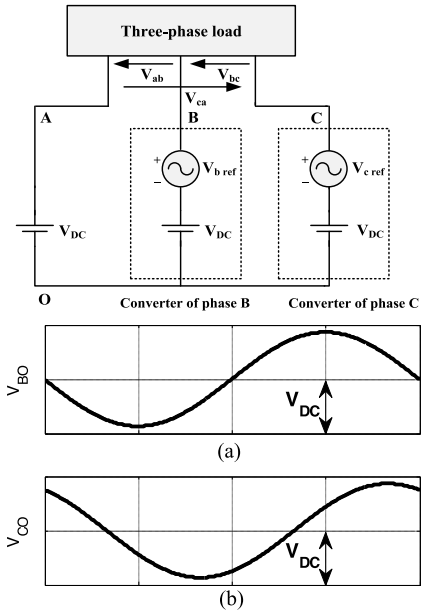


Fig. 2. Basic approach to achieve dc–ac conversion with four switches using two SEPIC dc–dc converters. (a) Reference output voltage of the first converter. (b) Reference output voltage of the second converter.

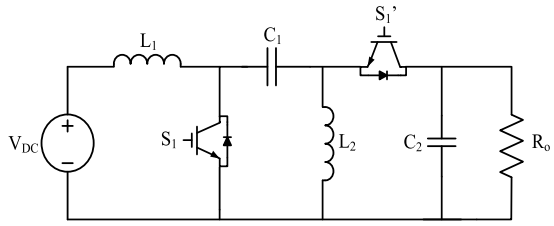


Fig. 3. Bidirectional SEPIC converter.

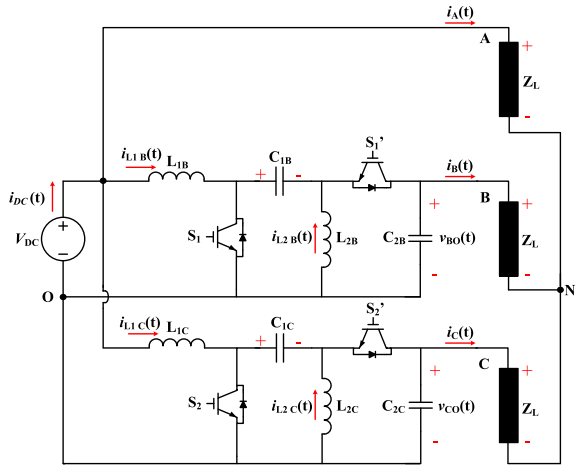


Fig. 4. Proposed FSTP SEPIC inverter.

which correspondingly distorts the output voltage [18]. Moreover, if the dc-link split-capacitors have not equal values, there is a possibility of overmodulation of the pulse-width modulation process in order to compensate this dilemma [16].

This paper proposes a novel design of the FSTP inverter topology based on the single-ended primary inductance converter (SEPIC). The SEPIC converter is a fourth-order nonlinear system that is extensively used in step-down or step-up dc–dc switching circuits, photovoltaic maximum power point tracking [19], [20], [21], and power factor correction circuits [22], [23] due to its promising features as the noninverting output voltage buck-boost capability and lower input current ripple content. Based on the aforementioned advantages, SEPIC converter has been recently researched by scholars in various topologies in many diversified studies [19]–[35].

Although the proposed FSTP SEPIC inverter has not a voltage boost capability, it can produce an output voltage higher than that of the conventional FSTP VSI by a factor of two, which improves the voltage utilization factor of the input dc supply. Another attractive feature of the proposed SEPIC inverter is that the output voltage is a pure sinusoidal wave, therefore reducing the filtering requirements at the output stage. Also, there is no vital need to insert a dead-band between the same-leg switches, which significantly reduces the output waveform distortion and gain nonlinearity.

II. Proposed FSTP SEPIC Inverter and its Principle of Operation

The proposed FSTP SEPIC inverter consists of two SEPIC converters, and achieves dc–ac conversion as explained in Fig. 2 by connecting two phases of the three-phase load to the output of two dc–dc SEPIC converters which are sinusoidally modulated [36], while the third phase is directly connected to the input dc source. Both SEPIC dc–dc converters produce a dc-biased sinusoidal wave output, so that each converter produces a unipolar voltage. To generate three-phase balanced load voltages, the sinusoidal modulation of each converter is 120° shifted and the dc-bias is exactly equal to the input dc voltage. Since the load is connected differentially across the two converters and the dc input supply, thus, whereas a dc bias appears at each end of the load with respect to ground, the differential dc voltage across the load is zero and the voltage generated across the load is bipolar voltage, which necessitates the dc–dc SEPIC converters to be current bidirectional. The bidirectional SEPIC dc–dc converter is shown in Fig. 3, while the detailed configuration of the proposed FSTP SEPIC dc–ac inverter is shown in Fig. 4.

As shown in Fig. 3, the bidirectional SEPIC converter includes dc input voltage V_{DC}, input inductor L_1, two complementary bidirectional power switches S_1, S'_1, coupling capacitor C_1, output inductor L_2 and output capacitor C_2 feeding a load resistance R_{o}. SEPIC operation core implies charging the inductors L_1 and L_2 during the ON state of the switching period taking the energy, respectively, from the input source and from the coupling capacitor C_1, and discharging them simultaneously into the load through the bidirectional switch S'_1 during the OFF state of the switching period. The output voltage of the SEPIC dc–dc converter may be less or more than the input voltage depending on the duty cycle. The relationship between the output

and input voltages is as follows:

$$V_o = \frac{D}{1-D} V_{\text{in}} \tag{1}$$

where D is the duty cycle, while V_{in} and V_o are the input and output voltage of the converter, respectively. The sinusoidal modulation of each SEPIC converter implies that the reference voltage of each converter with respect to the ground is given by

$$\begin{aligned} v_{BO}(t) &= V_{\text{DC}} + V_{\text{bref}} = V_{\text{DC}} - V_{\text{m}_{L-L}} \sin(\omega t) \\ v_{CO}(t) &= V_{\text{DC}} + V_{\text{cref}} = V_{\text{DC}} + V_{\text{m}_{L-L}} \sin(\omega t + 2\pi/3) \end{aligned} \tag{2}$$

where $V_{m_{L-L}}$ is the peak of the desired line to line output voltage, while ω is the desired radian frequency. Thus, based on Kirchhoff's voltage law in Fig. 4, the output line voltages across the load are given by

$$\begin{aligned} v_{\text{AB}}(t) &= V_{\text{DC}} - [V_{\text{DC}} - V_{m_{L-L}} \sin(\omega t)] = V_{m_{L-L}} \sin(\omega t) \\ v_{\text{BC}}(t) &= V_{\text{DC}} - V_{\text{m}_{L-L}} \sin(\omega \text{t}) - \big[V_{\text{DC}} \\ &\quad + V_{\text{m}_{L-L}} \sin(\omega + 2\pi/3)\big] = V_{m_{L-L}} \sin(\omega t - 2\pi/3) \\ v_{\text{CA}}(t) &= V_{\text{DC}} + V_{m_{L-L}} \sin(\omega t + 2\pi/3) - V_{\text{DC}} \\ &= V_{m_{L-L}} \sin(\omega t + 2\pi/3) \end{aligned} \tag{3}$$

Although the FSTP SEPIC inverter can give an output line voltage up to a value equals the voltage of the input source (V_{DC}) as indicated by (2), however, it is recommended to define $V_{m_{L-L}}$ lower than the value of the input dc voltage to avoid operating at zero duty cycle (i.e., minimum duty cycle is selected to be slightly higher than zero).

For successful dc–ac conversion, accurate selection of passive elements of SEPIC converter is necessary, and requires a knowledge of the instantaneous capacitors voltages and inductors currents. The voltage across the output capacitors has been given by (2). Based on the basics of dc–dc SEPIC converter, the average voltage across the coupling capacitor is equal to the input dc voltage, while the current through the output inductor is equal to the output load current as indicated in (4) and (5)

$$v_{C1B}(t) = v_{C1C}(t) = V_{\text{DC}} \tag{4}$$

$$i_{L2B}(t) = i_B(t), i_{L2C}(t) = i_C(t). \tag{5}$$

Referring to Fig. 4, i_{L2B}(t) and $i_{L2C}(t)$ are the output inductor currents of both SEPIC converters, while $i_B(t)$and $i_C(t)$ are the instantaneous load currents drawn by phase B and phase C, respectively. The load phase currents are given by (6)

$$\begin{aligned} i_A(t) &= I_m \sin(\omega t - \emptyset - \pi/6) \\ i_B(t) &= I_m \sin(\omega t - \emptyset - 5\pi/6) \\ i_C(t) &= I_m \sin(\omega t - \emptyset + \pi/2) \end{aligned} \tag{6}$$

where I_m is the peak value of load current, and $\emptyset$ is the phase of the load impedance (Z_L).

The input inductor current for both SEPIC converters can be obtained by applying energy balance rule for each SEPIC converter. Assuming ideal converters, the input inductor currents for both converters are given by

$$i_{L1B}(t) = \frac{i_B(t) v_{\text{BO}}(t)}{V_{\text{DC}}} = i_B(t) \frac{V_{\text{DC}} - V_{\text{m}_{L-L}} \sin(\omega t)}{V_{\text{DC}}} \tag{7a}$$

$$\begin{aligned} i_{L1C}(t) &= \frac{i_C(t) v_{\text{CO}}(t)}{V_{\text{DC}}} \\ &= i_C(t) \frac{V_{\text{DC}} + V_{\text{m}_{L-L}} \sin(\omega t + 2\pi/3)}{V_{\text{DC}}} \end{aligned} \tag{7b}$$

where $i_{L1B}(t)$ and $i_{L1C}(t)$ are the input inductor currents of both SEPIC converters connected to phase B and phase C, respectively, as shown in Fig. 4.

The input power drawn by each SEPIC could be obtained by calculating the average value of the input inductor current for each converter. The average values of the input inductor currents for both SEPIC converters (I_{L1B} and I_{L1C}) are given by

$$I_{L1B} = \bar{i}_{L1B} = \frac{-V_{m_{L-L}} I_m}{2V_{\text{DC}}} \cos(\emptyset + 5\pi/6) \tag{8a}$$

$$I_{L1C} = \bar{i}_{L1C} = \frac{V_{m_{L-L}} I_m}{2V_{\text{DC}}} \cos(\emptyset + \pi/6) \tag{8b}$$

From (8), it is clear that the average value of both input inductor currents are equal only at a unity power factor ($\emptyset = 0$, pure resistive load), in this case, both SEPIC converters will transfer the same amount of power to the load side. Otherwise, the average currents are not equal [according to (8)], i.e., SEPIC converters will transfer different amount of power to the load side.

Referred to Fig. 4, the dc input current of the proposed inverter topology [$i_{\text{DC}}(t)$] is equal to the summation of the load current drawn by phase A [$i_A(t)$], and the input inductors currents of both SEPIC converters [$i_{L1B}(t)$ and $i_{L1C}(t)$] as follows:

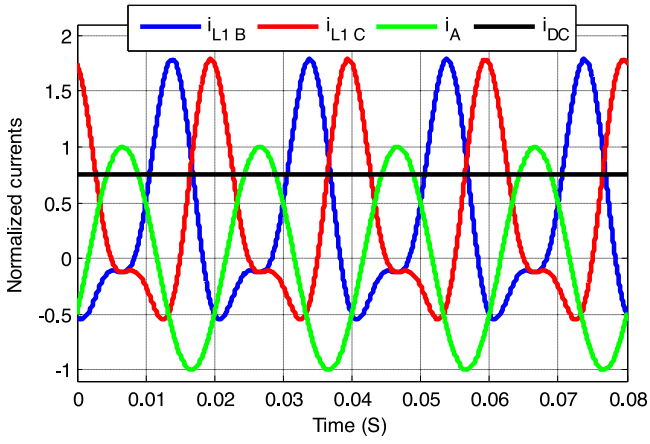
$$\begin{aligned} i_{\text{DC}}(t) &= i_A(t) + i_{L1B}(t) + i_{L1C}(t) \\ &= i_A(t) + i_B(t) \frac{V_{\text{DC}} - V_{\text{m}_{L-L}} \sin(\omega t)}{V_{\text{DC}}} \\ &\quad + i_C(t) \frac{V_{\text{DC}} + V_{\text{m}_{L-L}} \sin(\omega t + 2\pi/3)}{V_{\text{DC}}} \end{aligned} \tag{9}$$

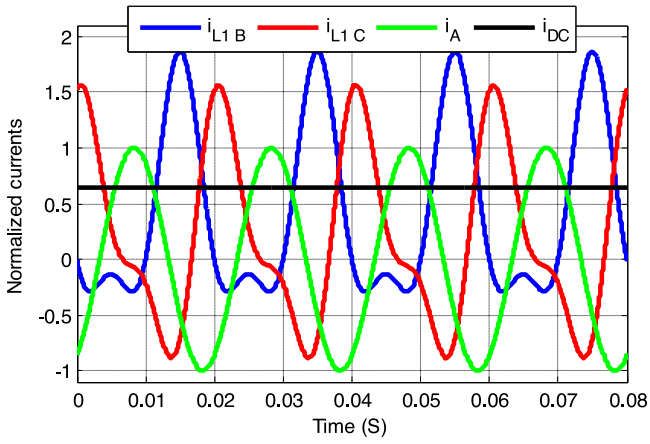
where $i_A(t)$ is the load current of phase A as described in (6), which is drawn directly from the dc input source. Substituting (6) into (9), the dc supply current could be given in the following form:

$$i_{\text{DC}}(t) = \frac{\sqrt{3} V_{m_{L-L}} I_m}{2V_{\text{DC}}} \sin(\emptyset + \pi/2) \tag{10}$$

Equation (10) shows that the dc supply current drawn by the proposed inverter topology is constant.

For line-to-line voltage peak of 86.66% of the dc input voltage, the normalized load current drawn by phase A [$i_A(t)/I_m$], normalized input inductor current for each SEPIC converter [$i_{L1B}(t)/I_m$ and $i_{L1C}(t)/I_m$], and the normalized dc input current [$i_{\text{DC}}(t)/I_m$] are shown in Fig. 5 for different load power factors. At unity power factor, the input currents of both SEPIC converters are symmetrical with the same average value as shown in Fig. 5(a). At lagging/leading power factors, the input currents of both SEPIC converters have different waveforms with unequal average value as shown in Fig. 5(b) and (c), respectively.





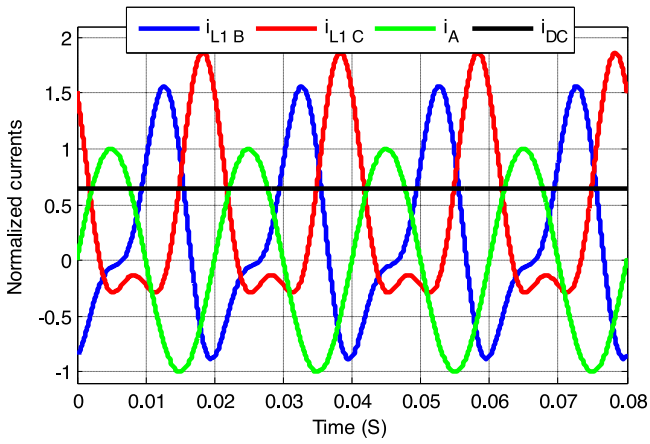


Fig. 5. Normalized waveforms of input inductor currents of each SEPIC converter, load current drawn by phase A, and the dc supply current of the SEPIC inverter at different power factors. (a) Unity power factor ($\emptyset = 0$). (b) Lagging power factor ($\emptyset = -\pi/6$). (c) Leading power factor ($\emptyset = +\pi/6$).

To assess the load deviation between the two active legs of the proposed SEPIC inverter, the RMS value of the input inductor current of both SEPIC converters at different load power factors is illustrated in Fig. 6 [for a unity RMS value of the output load current ($I_m = \sqrt{2}$)]. It can be noted that the maximum current drawn by converter B (i_{L1B}) occurs at a power factor of 0.866,

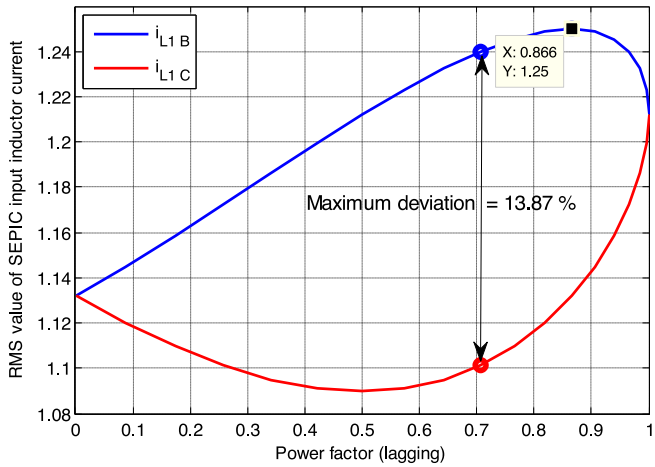


Fig. 6. Normalized RMS value of input inductor current of each SEPIC converter at different lagging power factors (line-to-line voltage peak = 86.66% of the dc input voltage).

while the maximum current drawn by converter C (i_{L1C}) occurs at unity power factor. The maximum deviation between the input currents of the two active legs is 13.87%, and occurs at a power factor of 0.7071.

Considering the unity power factor loading as the reference loading condition to select the IGBTs current rating, it can be noted that at a lagging power factor of 0.866, converter B has a deviation between its input current and the reference unity power factor current of 3.81%. Although the percentage of this deviation could be considered as a small ratio that does not imply the derating of the transistors, it is preferable to consider it in the selection of the IGBTs current rating.

III. Control Strategy

A robust control strategy is required to drive the proposed FSTP SEPIC inverter. This is due to the fact that the voltage of one of the three-output phases with respect to the common point is equal to the input dc voltage. Thus, any deviation in the output voltage of the two SEPIC dc–dc converters from the desired dc-biased sine-wave reference leads to a significant unbalance in the three-phase output line voltages.

A. SEPIC Modeling

To design a robust controller, a precise modeling is necessary. The conventional SEPIC converter has a complex model of fourth order, which is derived from the four passive components. This complex high-order system increases the difficulty of obtaining a precise model.

The best suitable mathematical model for the application of sliding-mode control (SMC) to the SEPIC is to use a nonlinear (large signal) state space representation. The converter is controlled through two complementary switches, having the control signal as its duty cycle, and is assumed to operate in continuous conduction mode (CCM). Hence, there are two state space representations during both ON and OFF states of the switch. The equivalent circuits of the SEPIC converter during ON and

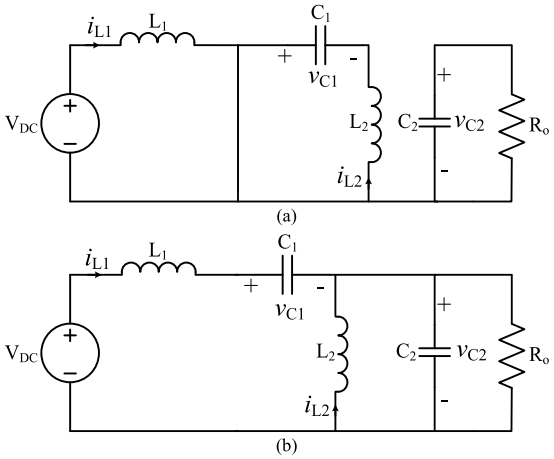


Fig. 7. SEPIC equivalent circuit for (a) switch ON and (b) switch OFF.

OFF states are shown in Fig. 7(a) and (b), respectively, where the basic converter equations are given as follows:

$$\text{Switch ON}\begin{cases} L_1\dfrac{di_{L1}}{dt} = V_{\rm DC} - i_{L1}r_{L1} \\ C_1\dfrac{dv_{C1}}{dt} = -i_{L2} \\ L_2\dfrac{di_{L2}}{dt} = v_{C1} - i_{L2}r_{L2} \\ C_2\dfrac{dv_{C2}}{dt} = -\dfrac{v_{C2}}{R_o} \end{cases} \tag{11a}$$

$$\text{Switch OFF}\begin{cases} L_1\dfrac{di_{L1}}{dt} = V_{\rm DC} - v_{C1} - v_{C2} - i_{L1}r_{L1} \\ C_1\dfrac{dv_{C1}}{dt} = i_{L1} \\ L_2\dfrac{di_{L2}}{dt} = -v_{C2} - i_{L2}r_{L2} \\ C_2\dfrac{dv_{C2}}{dt} = i_{L1} + i_{L2} - \dfrac{v_{C2}}{R_o} \end{cases} \tag{11b}$$

where r_{L1} and r_{L2} are the equivalent series resistance (ESR) of the inductors $L_1$and L_2, respectively. The two state space models can be written accordingly in the form

$$\frac{dX}{dt} = AX + BV_{\rm DC} \tag{12}$$

where *X* and $\frac{dX}{dt}$ are the vectors of the state variables and their time derivatives, respectively, given by

$$X = [x_1\, x_2\, x_3\, x_4]^T = [i_{L1}\, v_{C1}\, i_{L2}\, v_{C2}]^T \tag{13}$$

The elements of the matrices *A* and *B* are composed of the circuit parameters, ESRs, and the load resistance R_o. By introducing the discrete variable u as the switch status ($u = 1$ during ON state, while it equals zero during OFF state), the state space representations (11a) and (11b) can be written as

$$\begin{bmatrix} \dfrac{di_{L1}}{dt} \\ \dfrac{dv_{C1}}{dt} \\ \dfrac{di_{L2}}{dt} \\ \dfrac{dv_{C2}}{dt} \end{bmatrix} = \begin{bmatrix} -\dfrac{r_{L1}}{L_1} & \dfrac{u-1}{L_1} & 0 & \dfrac{u-1}{L_1} \\ \dfrac{1-u}{C_1} & 0 & \dfrac{-u}{C_1} & 0 \\ 0 & \dfrac{u}{L_2} & -\dfrac{r_{L2}}{L_2} & \dfrac{u-1}{L_2} \\ \dfrac{1-u}{C_2} & 0 & \dfrac{1-u}{C_2} & \dfrac{-1}{R_oC_2} \end{bmatrix} \times \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} [V_{\rm DC}] \tag{14}$$

The average state space model in CCM is obtained by averaging the state space matrices of the "ON" and "OFF" states of the switch over the switching period. By defining the duty cycle *D*, the averaged state space model of the SEPIC is obtained as

$$\begin{aligned} \frac{di_{L1}}{dt} &= -\frac{r_{L1}}{L_1}i_{L1} + \frac{(D-1)}{L_1}v_{C1} + \frac{(D-1)}{L_1}v_{C2} + \frac{1}{L_1}V_{\rm DC} \\ \frac{dv_{C1}}{dt} &= \frac{(1-D)}{C_1}i_{L1} - \frac{D}{C_1}i_{L2} \\ \frac{di_{L2}}{dt} &= \frac{D}{L_2}v_{C1} - \frac{r_{L2}}{L_2}i_{L2} + \frac{(D-1)}{L_2}v_{C2} \\ \frac{dv_{C2}}{dt} &= \frac{(1-D)}{C_2}i_{L1} + \frac{(1-D)}{C_2}i_{L2} - \frac{1}{R_oC_2}v_{C2} \end{aligned} \tag{15}$$

B. Sliding Mode Control

SMC is a nonlinear control theory which extends the properties of hysteresis control to multivariable environments. It is able to constrain the system status to follow trajectories which lie on a suitable surface in the state space (the sliding surface) [37]–[40]. The main advantages of SMC are the fast dynamic response and the guarantee of stability and robustness for large variations of system parameters and against perturbations [37]. Moreover, given its flexibility in terms of synthesis, SMC is relatively easy to be implemented compared to other types of nonlinear control. However, its application to power converters should be studied for each converter severally. As a control method, SMC has been applied to basic dc–dc converters [41], [42] and complex converters [37], [43], [44]. Although most authors mention the generalization of their developed methods to other high-order converters, this does not imply to all converters because the difference in circuit topology completely changes the system's behavior even if it is of the same order [45].

C. Sliding Surface

Although the output voltage v_{C2} of each SEPIC converter is the final control target, it will be impossible for the closed-loop-controlled system to reach stable motion on the sliding surface if v_{C2} is only selected to be the direct control target, thus the other variables should be chosen.

Then, it is proposed to increase the number of state variables as low as possible in the sliding surface. To avoid a large number of tuning gains, a surface containing the input current in addition to the output voltage could be chosen as given by (16)

$$s(i_{L1}, v_{C2}) = \alpha_1 e_1 + \alpha_2 e_2 \tag{16}$$

where coefficients α_1 and α_2 are gains, while e_1 and e_2 are the feedback errors of the state variables i_{L1}, and v_{C2}, respectively, and given by (17)

$$\begin{aligned} e_1 &= i_{L1\text{ref}} - i_{L1} \\ e_2 &= v_{C2\text{ref}} - v_{C2}. \end{aligned} \tag{17}$$

The reason for choosing i_{L1} instead of i_{L2} is to allow the sliding surface to directly control the input of each converter in addition to its output, which is more stable than the other cases.

At an infinitely high switching frequency, the SMC will ensure that both input inductor current and output capacitor voltage are regulated to follow exactly their instantaneous references i_{L1ref} and v_{C2ref}, respectively. However, in the case of finite frequency or fixed frequency SMCs, the control is imperfect, where steady-state errors exist in both inductor current and output capacitor voltage. A good method for suppressing these errors is to introduce an additional integral term of the state variables into the sliding surface. Therefore, an integral term of these errors is introduced into the SMC as an additional-controlled state-variable to reduce these steady-state errors. This is commonly known as integral sliding-mode control (ISMC) [46], and the sliding surface is selected as specified by (18).

$$s = \alpha_1 e_1 + \alpha_2 e_2 + \alpha_3 e_3 \tag{18}$$

where α_1, α_2, and α_3 represent the desired control parameters denoted sliding coefficients, while e_1,e_2 and e_3 are expressed as

$$\begin{aligned} e_1 &= i_{L1\text{ref}} - i_{L1} \\ e_2 &= v_{C2\text{ref}} - v_{C2} \\ e_3 &= \int (e_1 + e_2) dt \end{aligned} \tag{19}$$

The time derivative of the three-state errors is given by

$$\begin{aligned} \frac{de_1}{dt} &= \frac{d(i_{L1\text{ref}} - i_{L1})}{dt} \\ \frac{de_2}{dt} &= \frac{d(v_{C2\text{ref}} - v_{C2})}{dt} \\ \frac{de_3}{dt} &= e_1 + e_2 \end{aligned} \tag{20}$$

The inductor current reference is difficult to evaluate as it has a nonconventional form and generally depends on the load power demand, supply voltage, and load voltage. In practical implementation, the state variable error for the inductor current is obtained from the actual current either by using a high-pass filter to obtain the inductor current ripples at the switching frequency that simulates the error, or by using a low-pass filter to pass only the fundamental component of the inductor current then the actual current is subtracted from this reference signal to get the state error [39]. To avoid increasing the system order and altering the converter dynamics when such filters are used, the inductor current reference can be chosen as [39], [47]

$$i_{L1\text{ref}} = K(v_{C2\text{ref}} - v_{C2}) \tag{21}$$

where *K* is an amplifying gain of the converter output voltage error. Substituting (21) in (20) gives

$$\frac{de_1}{dt} = \frac{d(i_{L1\text{ref}} - i_{L1})}{dt} = \frac{d\left[K(v_{C2\text{ref}} - v_{C2}) - i_{L1}\right]}{dt} \tag{22}$$

Considering the time derivative of the output capacitor voltage

$$\frac{dv_{C2}}{dt} = \frac{i_{c2}}{C_2} \tag{23}$$

To simplify the calculation, assuming that $v_{C2\text{ref}}$ is constant, and substituting equations (15) and (23) in (22) gives

$$\begin{aligned} \frac{de_1}{dt} &= \frac{-K}{C_2} i_{c2} - \left[\frac{(D-1)(v_{C1} + v_{C2})}{L_1} - \frac{r_{L1}}{L_1} i_{L1} + \frac{V_{\text{DC}}}{L_1}\right] \\ \frac{de_2}{dt} &= \frac{d(v_{C2\text{ref}} - v_{C2})}{dt} = \frac{-i_{c2}}{C_2} \\ \frac{de_3}{dt} &= e_1 + e_2 = (K+1)(v_{C2\text{ref}} - v_{C2}) - i_{L1} \end{aligned} \tag{24}$$

where D is the equivalent control signal denoted as the duty cycle of the converter, which could be formulated using the invariance conditions by setting the time derivative of (18) to zero as follows [48]:

$$\frac{ds}{dt} = \alpha_1 \frac{de_1}{dt} + \alpha_2 \frac{de_2}{dt} + \alpha_3 \frac{de_3}{dt} = 0 \tag{25}$$

Solving for the equivalent control signal yields

$$\begin{aligned} D = \frac{1}{v_{C1} + v_{C2}} \big[& K_1(v_{C2\text{ref}} - v_{C2}) - K_2 i_{C2} - K_3 i_{L1} \\ & + r_{L1} i_{L1} + (v_{C1} + v_{C2} - V_{\text{in}}) \big] \end{aligned} \tag{26}$$

where $K_1 = \frac{\alpha_3}{\alpha_1} L_1 (K+1)$, $K_2 = \frac{L_1}{C_2}\left(K + \frac{\alpha_2}{\alpha_1}\right)$ and $K_3 = \frac{\alpha_3}{\alpha_1} L_1$ are the fixed gain parameters of the recommended ISMC. The block diagram of the ISMC given by (26) is illustrated in Fig. 8.

D. Double-Integral Sliding-Mode Control (DISMC)

To increase the effectiveness of the ISMC, an additional double-integral term of the state-variables error could be introduced in the sliding surface. This is the so-called DISMC [46]. Thus, the DISM controller has the following sliding surface:

$$s = \alpha_1 e_1 + \alpha_2 e_2 + \alpha_3 e_3 + \alpha_4 e_4 \tag{27}$$

where the state errors are defined by

$$\begin{aligned} e_1 &= i_{L1\text{ref}} - i_{L1} \\ e_2 &= v_{c2\text{ref}} - v_{c2} \\ e_3 &= \int (e_1 + e_2) dt \\ e_4 &= \iint (e_1 + e_2) dt \end{aligned} \tag{28}$$

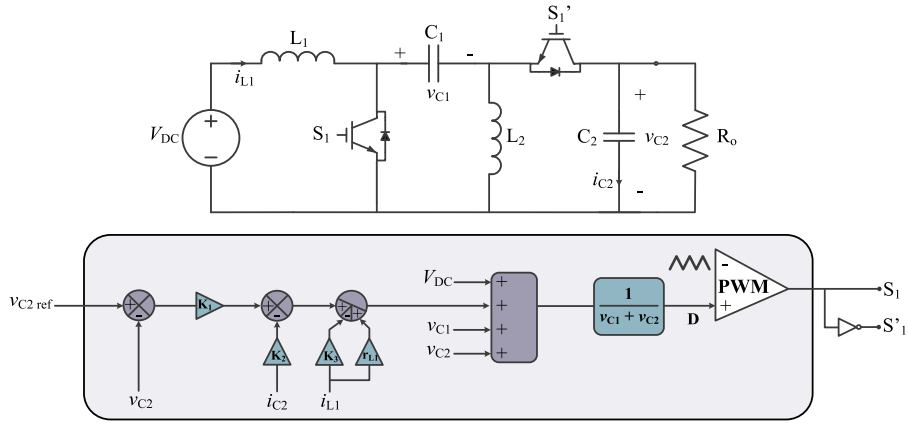


Fig. 8. ISMC for SEPIC converter.

Substituting the SEPIC state-space models under CCM into the time derivative of (28) gives the dynamical model of the system as

$$\begin{aligned}\frac{de_1}{dt} &= \frac{-K}{C_2}i_{C2} - \left[\frac{(D-1)(v_{C1}+v_{C2})}{L_1} - \frac{r_{L1}}{L_1}i_{L1} + \frac{V_{\rm DC}}{L_1}\right]\\ \frac{de_2}{dt} &= \frac{d(v_{C2\rm ref}-v_{C2})}{dt} = \frac{-i_{C2}}{C_2}\\ \frac{de_3}{dt} &= e_1+e_2 = (K+1)(v_{C2\rm ref}-v_{C2}) - i_{L1}\\ \frac{de_4}{dt} &= \int (e_1+e_2)dt \end{aligned} \tag{29}$$

The equivalent control signal deduced from setting the time derivative of (27) into zero gives

$$\begin{aligned} D = \frac{1}{v_{C1}+v_{C2}}\Big[&K_1(v_{C2\rm ref}-v_{C2}) - K_2 i_{C2} - K_3 i_{L1}\\ &+ r_{L1}i_{L1} + (v_{C1}+v_{C2}-V_{\rm in})\\ &+ \int K_4(v_{C2\rm ref}-v_{C2})dt\Big] \end{aligned} \tag{30}$$

where $K_1{=}\frac{\alpha_3}{\alpha_1}L_1(K+1)$,$K_2{=}\frac{L_1}{C_2}(K+\frac{\alpha_2}{\alpha_1})$, $K_3=\frac{\alpha_3}{\alpha_1}L_1$, and $K_4=\frac{\alpha_4}{\alpha_1}L_1$ are the fixed gain parameters in the recommended DISM controller.

(30) shows that the DISMC introduces an integral term of the capacitor voltage error component in the equivalent control, which allows to solve the problem of the significant steady-state errors in the ISMC algorithm.

The block diagram of the DISMC given by (30) is illustrated in Fig. 9.

E. Selection of DISM Control Parameters

The system behavior is completely determined by coefficientsK_i, which must be selected so as to satisfy the existence condition of the SMC and ensure stability and fast response even for large supply and load variations. The existence condition for the SMC consists of finding the regions of attraction given by $s\,(x)\,\frac{ds(x)}{dx}<0$ throughout the entire domain of operation which are imposed by the SMC strategy. These regions are found using the following inequalities [49]:

$$\begin{cases} u=1, & \dfrac{ds(x)}{dx}<0, \ \text{if } s(x)>0\\ u=0, & \dfrac{ds(x)}{dx}>0, \ \text{if } s(x)<0 \end{cases} \tag{31}$$

Detailing equation (31) leads to

Case 1: $s(x)>0$, $u=1$, then $\frac{ds(x)}{dx}<0$

$$\begin{aligned} &V_{\rm in} - K_1(v_{C2\rm ref}-v_{C2}) - \int K_4(v_{C2\rm ref}-v_{C2})dt + K_2 i_{C2}\\ &-(K_3-r_{L1})i_{L1} > 0 \end{aligned} \tag{32a}$$

Case 2: $s(x)<0$, $u=0$, then $\frac{ds(x)}{dx}>0$

$$\begin{aligned} &V_{in} - K_1(v_{C2\rm ref}-v_{C2}) - \int K_4(v_{C2\rm ref}-v_{C2})dt + K_2 i_{C2}\\ &-(K_3-r_{L1})i_{L1} < v_{C1}+v_{C2} \end{aligned} \tag{32b}$$

Since existence conditions are expressed by inequalities (32), there are some degrees of freedom in choosing coefficients K_i. The solutions giving stable and nonoscillatory response of all state variables can therefore be investigated. This can be obtained by finding the system eigenvalues as a function of the coefficients K_i in order to find the solutions having eigenvalues with negative real part and suitable dynamic behavior [50].

IV. Parameters and Ratings Selection for the Proposed SEPIC Inverter Components

In this section, a methodology to select suitable values of capacitances and inductances is presented, in addition to selection of all components ratings.

A. Inductors Selection

Retrieving equation (1), the relation between input, and output voltages and currents for SEPIC converter is as follows:

$$\frac{i_{in}(t)}{i_o(t)} = \frac{v_o(t)}{V_{\rm DC}} = \frac{D(t)}{1-D(t)} \tag{33}$$

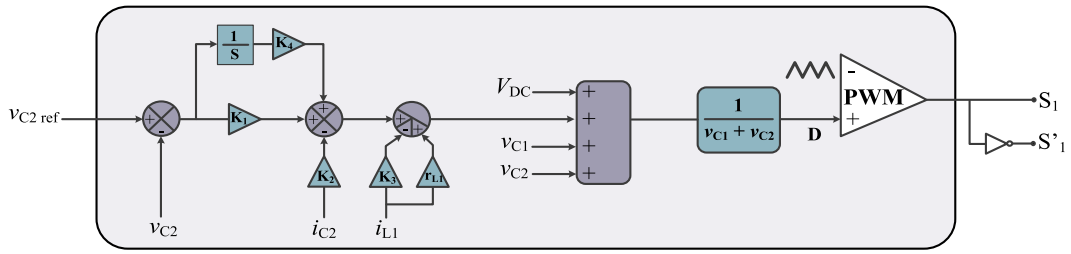


Fig. 9. DISMC for SEPIC converter.

where $D(t)$ is the instantaneous duty cycle, which can be expressed by (34)

$$D(t) = \frac{v_o(t)}{V_{\rm DC} + v_o(t)}. \tag{34}$$

Considering the first converter in the proposed SEPIC inverter topology, which is connected to phase B, and retrieving equations (2) and (6), i.e., $v_{BO}(t) = V_{\rm DC} - V_{m_{L-L}} \sin(\omega t)$ and $i_B(t) = I_m \sin(\omega t - \emptyset - 5\pi/6)$. Then, the instantaneous duty cycle for the first converter is calculated as follows:

$$D(t) = \frac{V_{\rm DC} - V_{m_{L-L}} \sin(\omega t)}{2V_{\rm DC} - V_{m_{L-L}} \sin(\omega t)} \tag{35}$$

To find the duty cycle at the highest output current, it is necessary to find the time at which the current becomes at its peak value. For the load current $i_B(t)$, it will be at the level of I_m when

$$\omega t = \frac{4\pi}{3} + \emptyset \tag{36}$$

Then, the duty cycle correspondent to this maximum current is $\hat{D}$, and could be found as follows:

$$D_{at I_m} = \hat{D} = \frac{V_{\rm DC} - V_{m_{L-L}} \sin(4\pi/3 + \emptyset)}{2V_{\rm DC} - V_{m_{L-L}} \sin(4\pi/3 + \emptyset)} \tag{37}$$

It is clear from (37) that the highest possible duty cycle occurs at $\emptyset = \frac{\pi}{6}$, which is not depending on the ratio of $(V_{m_{L-L}}/V_{\rm DC})$. The corresponding maximum duty cycle could be found by (38), and will be used in design which emulates the worst possible case

$$D_{\max \rm conv1} = \frac{V_{\rm DC} + V_{m_{L-L}}}{2V_{\rm DC} + V_{m_{L-L}}}. \tag{38}$$

For the second converter in the proposed SEPIC inverter topology, which is connected to phase C, i.e., $v_{CO}(t) = V_{\rm DC} + V_{m_{L-L}} \sin(\omega t + 2\pi/3)$ and $i_C(t) = i_m \sin(\omega t + \pi/2 - \emptyset)$. The instantaneous duty cycle is calculated as follows:

$$D(t) = \frac{V_{\rm DC} + V_{m_{L-L}} \sin(\omega t + 2\pi/3)}{2V_{\rm DC} + V_{m_{L-L}} \sin(\omega t + 2\pi/3)} \tag{39}$$

For the load current $i_C(t)$, it will be at the level of I_m when

$$\omega t = \emptyset \tag{40}$$

Then, the duty cycle correspondent to this maximum current is $\hat{D}$, and could be found as follows:

$$D_{at I_m} = \hat{D} = \frac{V_{\rm DC} + V_{m_{L-L}} \sin(2\pi/3 + \emptyset)}{2V_{\rm DC} + V_{m_{L-L}} \sin(2\pi/3 + \emptyset)} \tag{41}$$

It is clear from (41) that the highest possible duty cycle, at the peak current, occurs at $\emptyset = 0$, regardless of the ratio of $(V_{m_{L-L}}/V_{\rm DC})$. The corresponding maximum duty cycle is given by (42), and will be used in design which emulates the worst possible case

$$D_{\max \rm conv2} = \frac{V_{\rm DC} + (\sqrt{3}/2)V_{m_{L-L}}}{2V_{\rm DC} + (\sqrt{3}/2)V_{m_{L-L}}}. \tag{42}$$

1) Input Inductor Selection: Considering that the peak-to-peak ripple current through the input inductor is set to 10% of the maximum value of the converter input current. The input inductor ripple current can be expressed as

$$\Delta i_{L1\max} = 10\% \text{ of input current peak} = 0.1 I_m \frac{D_{\max}}{1 - D_{\max}} \tag{43}$$

Also, from the dc–dc converter basics, the ripple current can be expressed as

$$\Delta i_{\rm Lmax} = \frac{V_{\rm DC} D_{\max}}{L f_{sw}} \tag{44}$$

where f_{sw} is the switching frequency, while L is the inductance value. Equating (43) and (44), the input inductance L_1 is estimated as in (45)

$$L_1 = \frac{V_{\rm DC}(1 - D_{\max})}{0.1 I_m f_{sw}}. \tag{45}$$

2) Output Inductor Selection: For the output inductor, the peak-to-peak ripple current is recommended to be 30% of the maximum value of the converter output current [51]. Following the same steps used in the selection of the input inductor, L_2 could be selected according to the following equation:

$$L_2 = \frac{V_{\rm DC} D_{\max}}{0.3 I_m f_{sw}} \tag{46}$$

B. Capacitances Selection

1) Coupling Capacitor Selection: Based on the desired voltage ripples, the capacitance can be selected as follows:

$$C_1 = \frac{I_m D_{\max}}{\Delta V f_{sw}} \tag{47}$$

The ripple voltage across the coupling capacitance ΔV is recommended as 5% of the dc input voltage ($V_{\rm DC}$).

2) Output Capacitor Selection: The design equation (47) is typically used for the selection of the output capacitor. The only change is that the ripple voltage across the output capacitor

TABLE I
PARAMETERS OF FSTP SEPIC INVERTER

Inductors	$L_{1B} = 6.77$ mH, $L_{2B} = 2.26$ mH
	$L_{1C} = 7$ mH, $L_{2C} = 2.36$ mH
Capacitors	$C_{1B} = 10.6\ \mu$F, $C_{2B} = 2.8\ \mu$F
	$C_{1C} = 10.3\ \mu$F, $C_{2C} = 2.8\ \mu$F
DISMC coefficients	$K_1 = 2$, $K_2 = 10$, $K_3 = 1$, $K_4 = 100$

ΔV_o is recommended to be 10% of the peak voltage applied on the output of the SEPIC, which is equal to $V_{\rm DC} + V_{m_{L-L}}$. The output capacitor is selected according to (48)

$$C_2 = \frac{I_m D_{\max}}{\Delta V_o f_{sw}}. \tag{48}$$

C. Ratings of Switching Devices

For the proposed inverter topology, the voltage stresses of all switching devices for each SEPIC are equal to the sum of the input voltage and maximum output voltage as follows:

$$V_{\rm Dmax} = V_{\rm SWmax} = V_{\rm DC} + V_{m_{L-L}} \tag{49}$$

where V_D and $V_{\rm SW}$ are the voltage across the diode and the switch, respectively. Also, the maximum stresses I_{Dmax} and $I_{\rm SWmax}$ of the diodes and switches could be deduced from Fig. 6 as follows:

$$I_{\rm Dmax} = I_{\rm SWmax} = i_{L1} + i_{L2} \tag{50}$$

D. Design Example

In this section, the previously deduced equations are used to select the appropriate values of the components used in the proposed SEPIC inverter.

The design specifications of the proposed FSTP SEPIC inverter are as follows:

1) input voltage: 200 VDC;
2) peak output line voltage: 100 $\sqrt{3}$ VAC;
3) output frequency: 50 Hz;
4) switching frequency: 25 kHz;
5) rated current: $I_m = 4$A (Load: 25 Ω series with 1 mH).

From (38), $D_{\max conv1} = 0.65$, while from (39), $D_{\max conv2} = 0.63$. The parameters of both SEPIC converters for the above mentioned specifications are summarized in Table I.

V. SIMULATION AND EXPERIMENTAL RESULTS

The proposed FSTP SEPIC inverter has been designed, simulated, and tested to validate its overall performance. The simulations have been done using MATLAB/SIMULINK to validate the analytical results, and to prove the robustness of the recommended DISM control strategy when applied on the proposed inverter topology via different simulation studies. The output phase voltage of the inverter was set to a peak value of 100-V ac, while the input voltage was kept constant at 200-V dc. The parameters of the proposed FSTP SEPIC inverter for simulation are as summarized in the last section.

A. Simulation

The performance of the proposed FSTP SEPIC inverter under the DISM control strategy has been investigated during both normal and step-changed operating conditions. The corresponding simulation results are shown in Figs. 10 and 11. In particular, Fig. 10 shows the performance of the inverter during normal operating conditions, where the output capacitor voltage and the coupling capacitor voltage of both SEPIC converters are shown in Fig. 10(a) and (b), respectively. Fig. 10(a) shows that the output voltages of both SEPIC converters have sinusoidal waveforms shifted by 120° with a dc bias that is exactly equal to the input dc voltage. Fig. 10(b) shows that the average value of the coupling capacitor voltage for both SEPIC converters is equal to the value of the input dc voltage. The current of both input and output inductors for each SEPIC converter is shown in Fig. 10(c) and (d), respectively. Fig. 10(c) shows that the simulated waveforms of the input inductor currents for both SEPIC converters are consistent with those obtained by equation (7) and shown previously in Fig. 5(a). Fig. 10 (d) shows that the output inductor current has the same waveform of the corresponding load current with superimposed switching ripples. The duty cycle of both SEPIC converters is shown in Fig. 10(e), where they are varying between approximately 0.12 and 0.65. It should be noted that the waveform of the duty cycle of the SEPIC converter is similar to that obtained from the buck-boost converter at the same values of input and output voltages. This is due to the fact that both SEPIC and buck-boost converters have the same magnitude of the input/output relationship.

The input current of the dc supply is shown in Fig. 10(f), where it is a unidirectional current oscillating around 3 A, which is the correct dc value obtained from equation (10). This oscillation is due to the ripples imposed on the input inductor current of both SEPIC, and ripples of phase-A current.

The three-phase output voltages and load currents of the inverter are shown in Fig. 10(g) and (h), respectively, where the output voltages are well regulated without any filtering requirements.

Fig. 11 shows the performance of the inverter during step-changed operating conditions, where Fig. 11(a) exhibits the performance of the inverter under a step change in the load reference voltage from 50 to 100% with doubled frequency, which simulates voltage/frequency control of a three-phase induction motor. Fig. 11(b) shows the performance of the inverter when the load current is changed from 50 to 100%, where the load current has been doubled significantly but the output voltage is almost immediately compensated confirming the robustness of the DISMC.

B. Experiment

In order to validate the effective performance of the proposed FSTP SEPIC inverter and confirm the simulation results, an experimental system is built in laboratory with the parameters and components ratings summarized in Tables II and III, respectively. The PWM control signals are generated by a high performance DSP TMS320F28335 from Texas Instruments. The experimental results are shown in Figs. 12, 13, 14, and 15.

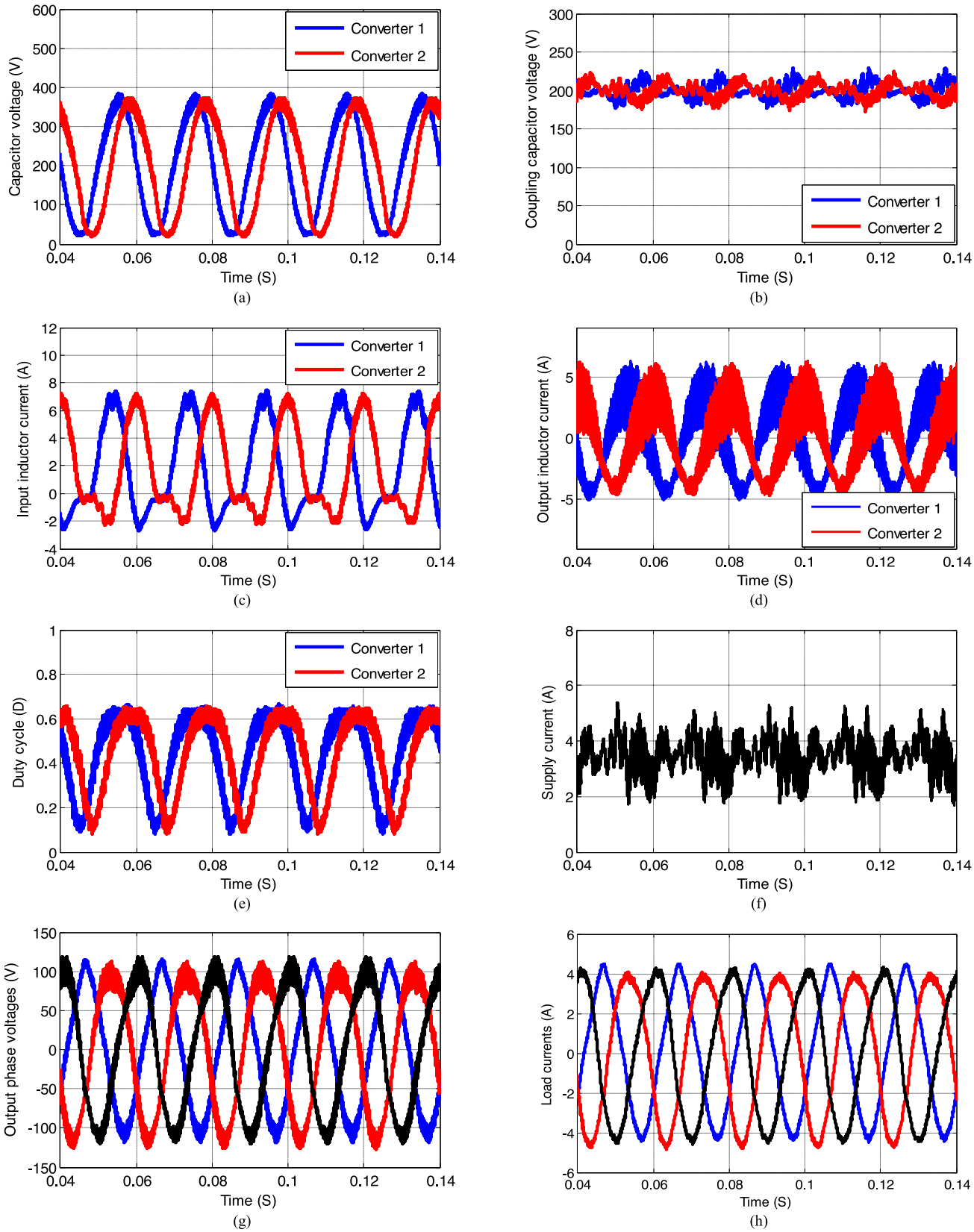


Fig. 10. Performance of the FSTP SEPIC inverter under normal operating conditions. (a) Output capacitor voltage of both SEPIC converters. (b) Coupling capacitor voltage of both SEPIC converters. (c) Input inductor current of both SEPIC converters. (d) Output inductor current of both SEPIC converters. (e) Duty cycle of both SEPIC converters. (f) Dc supply current. (g) Three-phase output phase voltages. (h) Three-phase load currents.

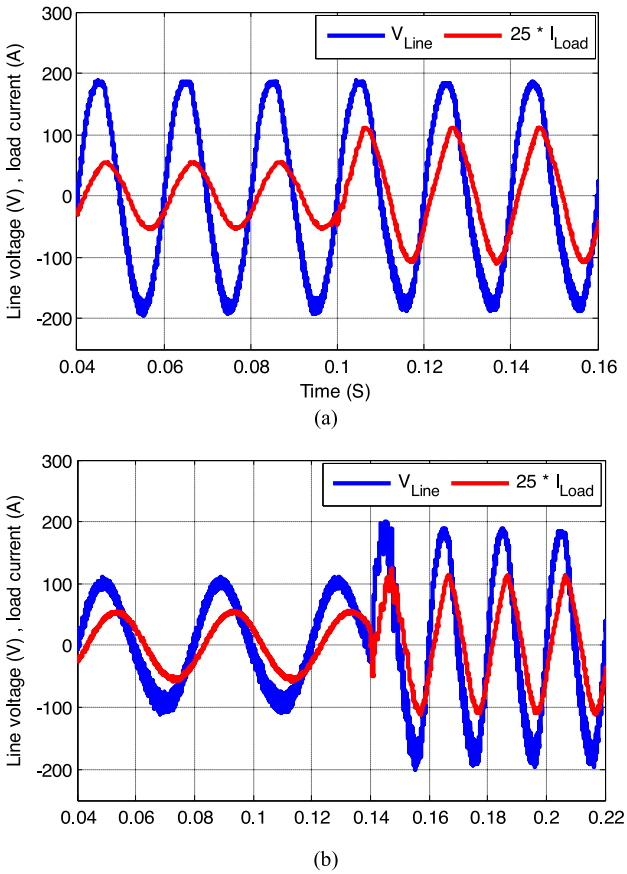


Fig. 11. Dynamic performance of the FSTP SEPIC inverter. (a) Load voltage and load current for a step change of reference load voltage from 50 to 100% with doubled frequency. (b) Load voltage and load current for a load step change from 50 to 100%.

TABLE II
SPECIFICATIONS OF THE FSTP SEPIC INVERTER FOR EXPERIMENTAL SETUP

Input dc voltage		200 V
Output ac voltage		3-phase 50 Hz, $V_{m\,L-L} = 100\sqrt{3}$ V
Switching frequency		20 kHz
Inductors		$L_{1B} = 6.7$ mH, $L_{2B} = 1$ mH
		$L_{1C} = 6.7$ mH, $L_{2C} = 1$ mH
Capacitors		$C_{1B} = 15\ \mu$F, $C_{2B} = 1.5\ \mu$F
		$C_{1C} = 15\ \mu$F, $C_{2C} = 1.5\ \mu$F
Load	Load 1	100 Ω
	Load 2	220 V, 1.5 HP, 50 Hz, 2840 RPM, three-phase induction motor

Figs. 12 and 13 show the performance of the SEPIC inverter when feeding a resistive load, while Figs. 14 and 15 show the performance of the inverter when feeding a three-phase induction motor.

Fig. 12(a) shows the dc input voltage, and the output capacitor voltage for each SEPIC dc–dc converter. The three voltage signals in Fig. 12 (a) are considered the voltage of each load-phase with respect to the supply common point. The output of the two SEPIC converters are sinusoidally modulated with 120° phase shift between them, with a deliberate dc bias exactly equals the voltage of the dc input source. Fig. 12(b) shows the voltage

TABLE III
RATINGS OF COMPONENTS FOR EXPERIMENTAL SETUP

Switching devices	Rated voltage > 574 V	Rated current	Load 1: > 4 A Load 2: > 13 A
Coupling capacitors	Rated voltage > 200 V		
Output capacitors	Rated voltage > 374 V		

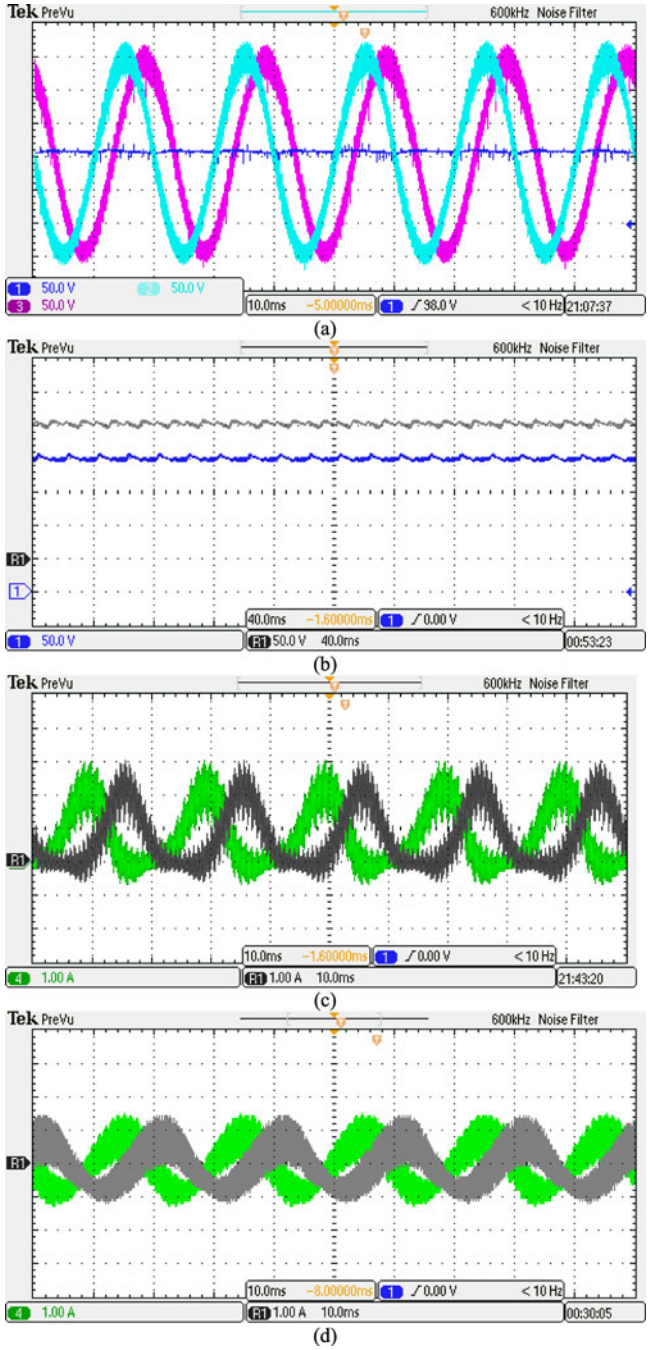


Fig. 12. (a) Voltage of each load phase with respect to the supply common point. (b) Voltage across coupling capacitor of each SEPIC converter. (c) Input inductor current for each SEPIC converter. (d) Output inductor current for each SEPIC converter (Voltage/div: 50 V/div, current/div: 1 A/div).

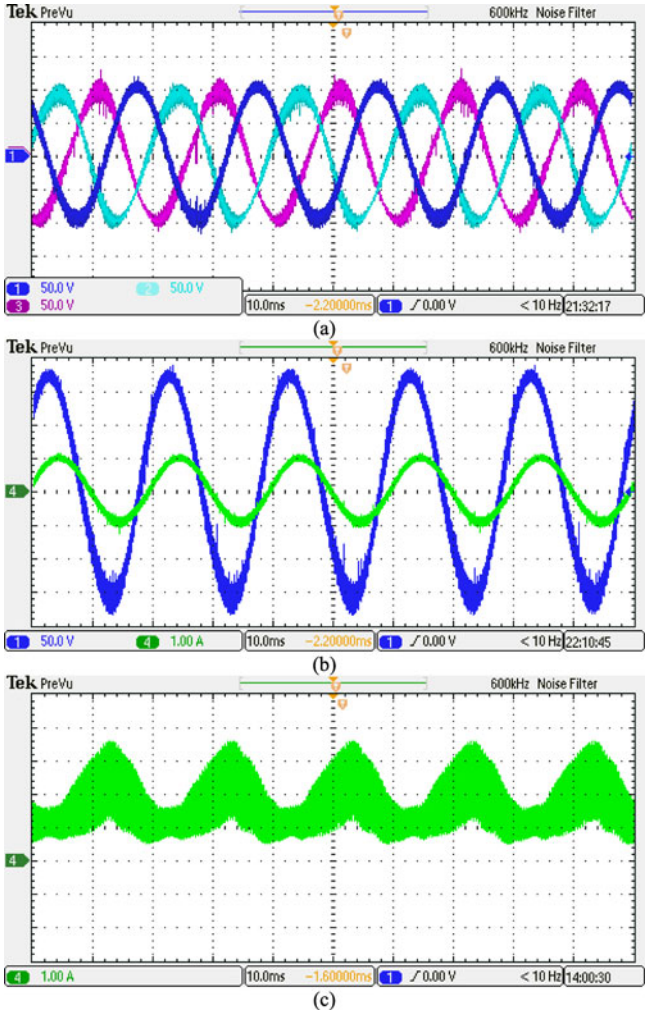


Fig. 13. (a) Three-phase output voltages of the SEPIC inverter. (b) Line voltage and load current for one phase of the SEPIC inverter. (c) Dc supply current (Voltage/div: 50 V/div, current/div: 1 A/div).

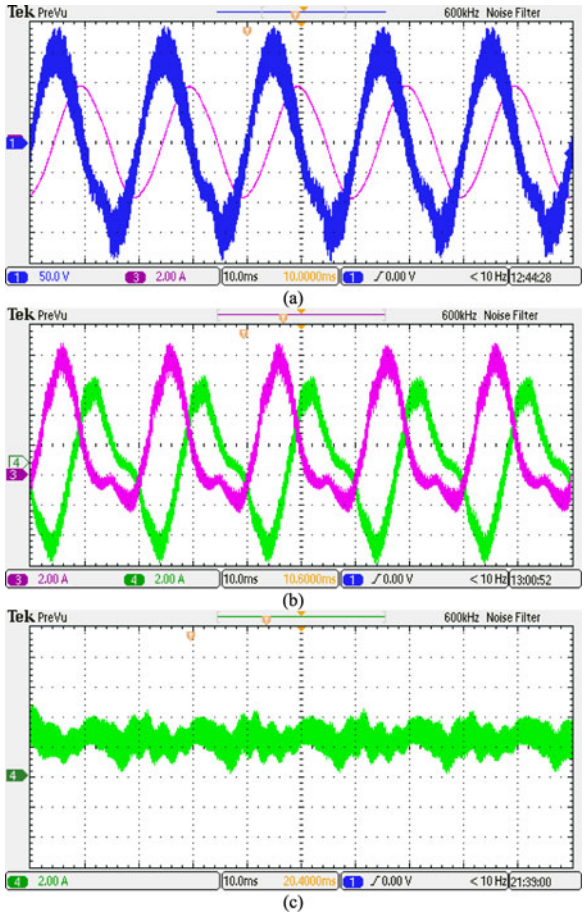


Fig. 14. Performance of the proposed FSTP SEPIC inverter when feeding a three-phase induction motor. (a) Line voltage and motor current. (b) Input inductor current for each SEPIC converter. (c) Supply input current (Voltage/div: 50 V/div, current/div: 2 A/div).

across the coupling capacitor of both SEPIC, where they have an average value equal to the input dc voltage. Fig. 12 (c) shows the input inductor current for each SEPIC dc–dc converter, where their waveforms are relatively consistent with both analytical and simulation results obtained before. Fig. 12(d) shows the output inductor currents for both converters, where they have almost the same waveform as their correspondent output load current. Load voltage and current are shown in Fig. 13, where the three-phase output voltages are shown in Fig. 13(a), while Fig. 13(b) shows the line voltage and the load current for one phase of the SEPIC inverter. Again, the output voltages have pure sinusoidal waveforms without a need to an output filter, which confirms the advantages of the proposed inverter topology. It can be noted that a small unbalance exists in the three-phase output voltages due to the asymmetry in the inverter topology. The voltage unbalance was found to be 1.9%. Fig. 13(c) shows that the dc supply current is unidirectional and does not fall to zero.

Fig. 14 shows the performance of the SEPIC inverter when feeding a three-phase induction motor driven at a constant speed, where Fig. 14(a) shows one of the output line voltages and the corresponding current. The voltage unbalance in the three-phase output voltages for this case was found to be 2.96%. Fig. 14(b) shows the input inductor currents of both SEPIC converters, where they have different waveforms, and are consistent with the results presented in Fig. 5(b). Fig. 14(c) shows the input current drawn from the dc supply.

Fig. 15 shows the output line voltage and the motor current during a step change in the operating speed through V/f control, where the reference line voltage and the stator frequency are changed from 50 to 100% as shown in Fig. 15(a), while the motor current is immediately compensated as shown in Fig. 15(b).

VI. Assessment of the Proposed FSTP SEPIC Inverter Compared to Conventional Three-Phase Topologies

A detailed comparison between different three-phase inverter topologies refereed in this paper (conventional SSTP VSI, conventional FSTP VSI, and the proposed FSTP SEPIC inverter) has been conducted to assess their feasibility in a general form, and in a numerical form at the same power level and the same output voltage. The assessment is summarized in Tables IV and V.

TABLE IV
GENERAL COMPARISON BETWEEN THREE-PHASE INVERTER TOPOLOGIES

	Conventional SSTP VSI	Conventional FSTP VSI	FSTP SEPIC-based inverter
Number of power switches, gate drive circuits, and snubber circuits	6 for each item	4 for each item	4 for each item
% Utilization factor of dc bus	50%	28.86%	57.74%
Minimum required dc link	$\frac{2}{\sqrt{3}}V_{\mathrm{m\,L-L}}$	$2V_{\mathrm{m\,L-L}}$	$V_{\mathrm{m\,L-L}}$
Stress on switches	V_{DC}	V_{DC}	$2V_{\mathrm{DC}} + V_{\mathrm{m\,L-L}}$
Switch peak current	I_{m}	I_{m}	$\mathrm{i_{L1}} + \mathrm{i_{L2}}$
Dead band insertion	Mandate	Mandate	Not necessary
Passive elements required	1 dc-link capacitor	2 dc-link split capacitors	2 Input inductors 2 Coupling capacitors 2 Output inductors 2 Output capacitors
Stress of required passive elements	V_{DC}	$\frac{V_{\mathrm{DC}}}{2}$ for each capacitor	I_{m} for output inductor V_{DC} for coupling capacitor $V_{\mathrm{DC}} + V_{\mathrm{m\,L-L}}$ for output capacitor
Output filtering requirements	(*LC* filter) 3 inductors + 3 capacitors	(*LC* filter) 3 inductors + 3 capacitors	No filter required
Stress of filter components	I_{m} for filtering inductor $V_{\mathrm{m\,phase}}$ for filtering capacitor	I_{m} for filtering inductor $V_{\mathrm{m\,phase}}$ for filtering capacitor	N/A

TABLE V
NUMERICAL COMPARISON FOR 2 KVA/120 $V_{\mathrm{RMS-PHASE}}$ 50-HZ THREE-PHASE INVERTERS ($\mathrm{f_{sw}} = 10$ KHZ, $\Delta \mathrm{i_{Lmax}} = 30\%$, AND $\Delta \mathrm{V_{Cmax}} = 10\%$)

	Conventional SSTP VSI	Conventional FSTP VSI	FSTP SEPIC-based inverter
Minimum required dc link	340 V	588 V	294 V (It may be increased to 310 V to avoid zero duty cycle)
Stress on switches	340 V	588 V	914 V
Switch current peak	7.85 A	7.85 A	26 A
Passive elements required	$C = 100\ \mu$F (peak voltage = 340 V)	$C_1 = C_2 = 100\ \mu$F (peak voltage = 294 V)	$L_1 = 7$ mH (peak current = 16A) $L_2 = 4.5$ mH (peak current = 10A) $C_1 = 33.5\ \mu$F (peak voltage = 310 V) $C_2 = 8.5\ \mu$F (peak voltage = 604 V)
Output filtering requirements	$L_f = 500\ \mu$H (peak current = 7.85 A) $C_f = 50\ \mu$F (peak voltage = 170 V)	$L_f = 500\ \mu$H (peak current = 7.85 A) $C_f = 50\ \mu$F (peak voltage = 170 V)	N/A
Theoretical efficiency	96.79%	97.63%	95.13%

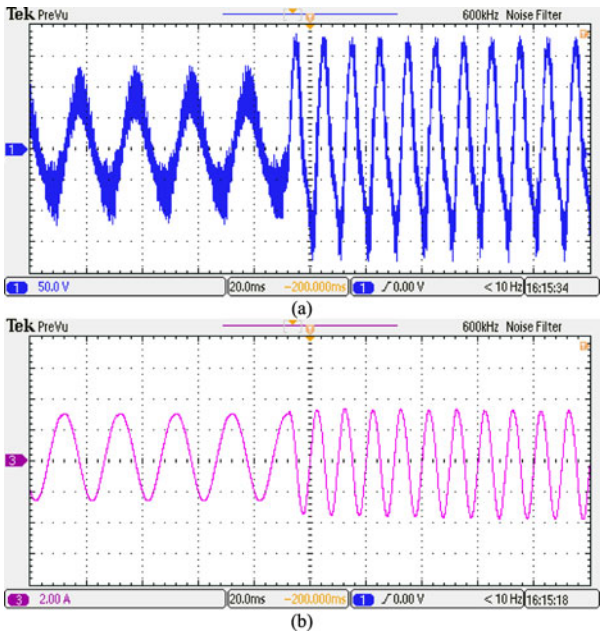


Fig. 15. Performance of SEPIC inverter during V/f speed control of a three-phase induction motor. (a) Line voltage. (b) Motor current (Voltage/div: 50 V/div, current/div: 2 A/div).

From this assessment, it is concluded that the proposed FSTP SEPIC inverter has shortcomings compared to both conventional SSTP VSI and FSTP VSI in terms of transistors rating, passive-elements rating and size, and efficiency. However it has several benefits that are not found in the other referred topologies, where it has a better voltage utilization factor of the input dc supply, which makes it more suitable for renewable energy sources with low output voltage such as photovoltaic and fuel cells. Also, the proposed FSTP SEPIC inverter generates a naturally filtered three-phase output voltages, and does not require a dead-band between the same-leg transistors which reduces the output waveform distortion and gain nonlinearity.

Compared to conventional SSTP VSI, the proposed FSTP SEPIC inverter has a reduced number of switches, PWM firing circuits, and snubber circuits, which contributes to the size reduction and increases the power density per volume.

Compared to conventional FSTP VSI, the proposed FSTP SEPIC inverter does not suffer from the problems of voltage fluctuation across the dc link split-capacitors, as the third phase load current is directly drawn from the dc source without circulation in any passive component.

VII. Conclusion

A dc–ac FSTP SEPIC-based inverter is proposed in this paper. The proposed inverter improves the utilization of the dc bus by a factor of two compared to the conventional FSTP voltage source inverter. Also, it can produce three-phase output voltages that are pure sinusoidal waves without a need for an output filter. Unlike conventional FSTP inverter, the proposed inverter does not suffer from the problems of voltage fluctuation across the dc link split-capacitors, as the third phase load current is directly drawn from the dc source without circulation in any passive component. An SMC with fixed switching frequency was designed and applied to the proposed SEPIC inverter with two different sliding surfaces called integral sliding-mode and double integral sliding-mode (DISMC). It was found that compared to ISMC, the DISMC can eliminate the steady-state error of the state variables by adding double-integral term of these errors in the sliding surface. Simulation and experimental results verified the performance of the proposed inverter with the recommended control strategy.

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