Nested Multilevel Topologies

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***Abstract*—This paper proposes multilevel topologies based on the concept of nested arrangement. Such topologies are called nested multilevel converters, since the central point of the legs are connected at the same point, with the external legs involving the internal ones. Nested configurations present advantages as compared to the equivalent NPC topologies in terms of reduced number of diodes and consequently higher efficiency. In addition to proposing a new family of power electronics converters, this paper presents an optimized pulse width modulation strategy that allows synthesizing voltage waveforms with higher quality, a losses comparison with the NPC topology, and a general comparison with other topologies proposed in the technical literature. Simulated and experimental results are presented to validate the theoretical expectations.**

***Index Terms*—DC-AC power converters, inverters, power electronics, pulse width modulation converters, static converters.**

I. Introduction

MULTILEVEL converters were first conceived for high-voltage and high-power applications. The neutral-point-clamped (NPC) inverter was first proposed in [1]. Since then, many configurations have been proposed [2]–[4] to establish the highly desirable characteristics for high-power applications, such as reduced waveform distortion and low blocking voltage by switching devices [5]. Besides the NPC, other principal configurations are flying capacitor, cascade, and modular multilevel converters [6]–[12].

More recently, the multilevel converters have found acceptance in low-power applications (e.g., in photovoltaic systems [13]–[15]), since it is possible to generate high-quality voltage waveforms with power semiconductor switches operating at a frequency near the fundamental [16]. Also, the number of the input dc-sources, in this application, is not longer restricted [17]. Even considering just one dc voltage source available, it is possible to employ multilevel converters with different dc-link sources requirement, as done in [18].

This paper investigates multilevel topologies based on the concept of nested arrangement. Such topologies are called nested multilevel converters because the central point of the legs are connected at the same point, with the external leg involving the internal one, as observed in Fig. 1. Fig. 1(a)–(c) shows the

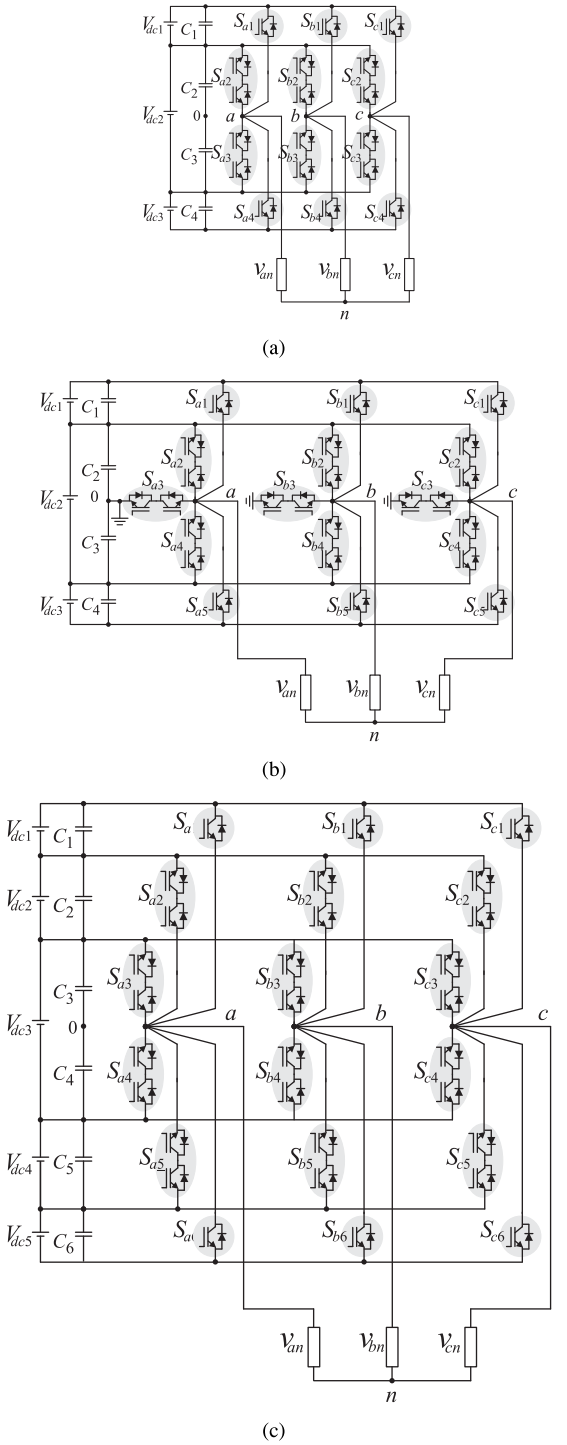

Fig. 1. Nested multilevel configurations with (a) four level, (b) five level, and (c) six level.

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TABLE I
POLE VOLTAGES AS A FUNCTION OF THE STATES OF THE SWITCHES

S_{x1}	S_{x2}	S_{x3}	S_{x4}	v_{x0}
1	0	0	0	$V_{dc1}+V_{dc2}/2$
0	1	0	0	$V_{dc2}/2$
0	0	1	0	$-V_{dc2}/2$
0	0	0	1	$-V_{dc1}-V_{dc2}/2$

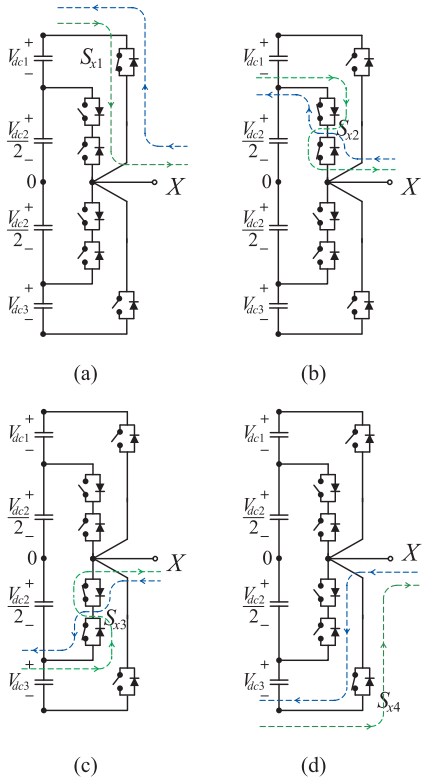

Fig. 2. Current flow through the switches of a leg on the nested configuration.

nested multilevel converter for four-, five-, and six-level output voltage, respectively. An auxiliary resonant pole applied to the three-level nested cell has been considered in [19] and [20]. Although the authors in [19] and [20] employ the term nested topology, the circuits are different from the topologies presented in Fig. 1. The five-level converter presented in Fig. 1(b) was proposed by [21]. The main contribution of this paper is to furnish a formal presentation of the nested multilevel configuration from four level to n-level. When compared to NPC topologies, the studied configurations can be considered as an interesting option for applications that demand a number of levels higher than or equal to four, since as far as the number of levels increase higher is the reduction on the number of diodes employed. Simulated and experimental results are presented to validate the theoretical expectations.

II. CONVERTER DESCRIPTION

Each converter's leg in Fig. 1(a) is constituted of two controlled switches (S_{x1} and S_{x4}) and two bidirectional controlled switches (S_{x2} and S_{x3}) with $x = a, b, c$. Table I shows the

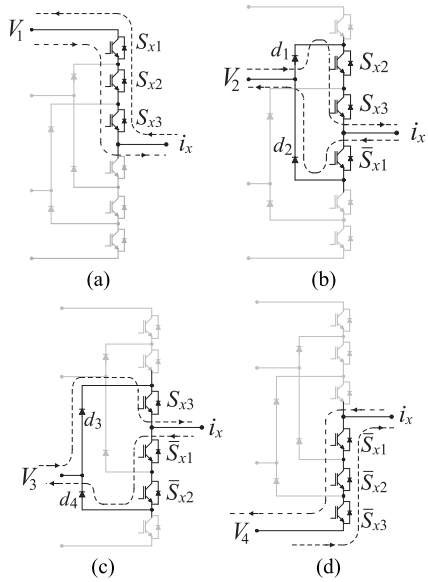

Fig. 3. Current flow through the switches of a leg on the four-level NPC topology.

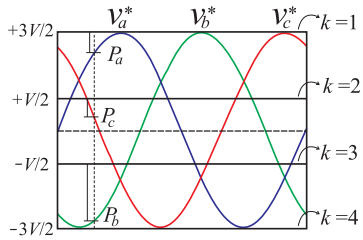

Fig. 4. DC levels of the four-level inverter and the three-phase references voltages.

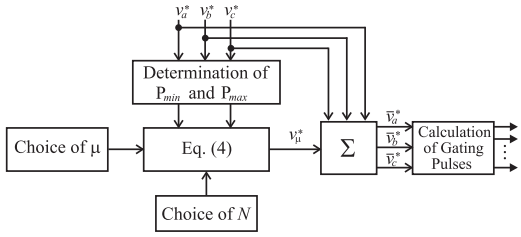

Fig. 5. Block diagram for the proposed hybrid PWM strategy.

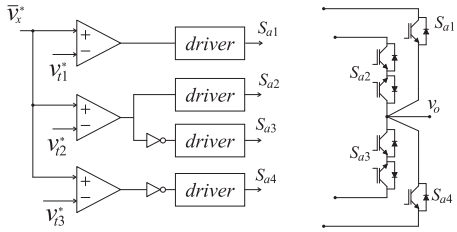

Fig. 6. PWM approach for the nested configuration.

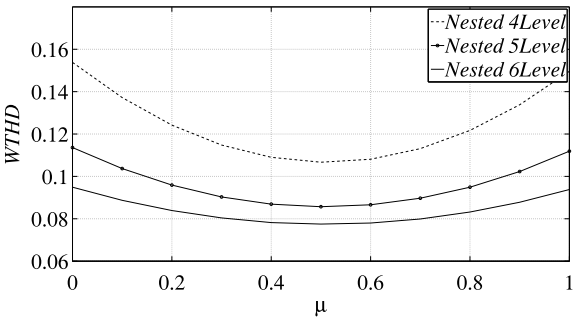

Fig. 7. WTHD of the load voltage as a function of μ.

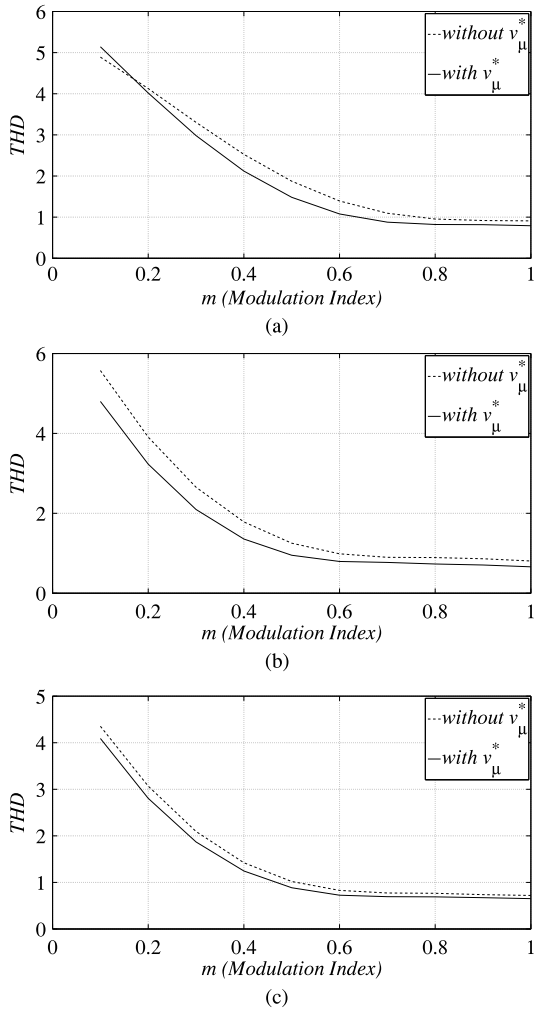

Fig. 8. THD of the current as a function of the modulation index for configuration with (a) four levels, (b) five levels, and (c) six levels.

output pole voltage v_{x0} as a function of switching states for the four-level topology. Each switch is connected per time, in order to avoid a short circuit through the leg. To guarantee a symmetrical output voltage, the input dc voltages are selected as $V_{\rm dc1} = V_{\rm dc2} = V_{\rm dc3} = V_{\rm dc}$, which means that $V_{C1} = V_{C4} = V_{\rm dc}$ and $V_{C2} = V_{C3} = V_{\rm dc}/2$.

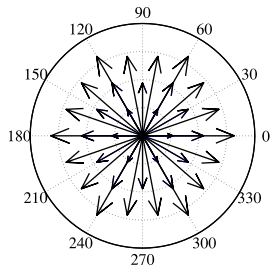

Fig. 9. Space vector dq plane.

TABLE II
COMPONENT SPECIFICATION FOR THE FOUR-LEVEL NESTED TOPOLOGY

	S_{x1}	S_{x2}	S_{x3}	S_{x4}
Blocking voltage in p.u.	1	2/3	2/3	1
Rated current in p.u.	1	1	1	1

TABLE III
COMPONENT SPECIFICATION FOR THE FOUR-LEVEL NESTED TOPOLOGY

	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}
Blocking voltage	1	3/4	1/2	3/4	1
Rated current	1	1	1	1	1

Fig. 2(a)–(d) shows the current flow (for positive and negative currents) when the switches S_{x1}, S_{x2}, S_{x3}, and S_{x4} are turned ON, respectively. The bidirectional controlled switches (S_{x2}, S_{x3}) have been employed in the inner leg, while the switches (S_{x1}–S_{x4}) have been used in the outer leg. If the positions of the switches S_{x1}–S_{x4} and S_{x2}, S_{x3} are changed, a short circuit will appear on the leg when the outer leg's switches are turned ON.

Fig. 3 shows the current path for a four-level leg of a NPC topology. Note that for generation of the highest voltage level [see Fig. 3(a)], the positive current (i_o) flows through three power switches, i.e., S_{x1}, S_{x2}, and S_{x3}, while the negative current flows through three diodes. Even with different power switches employed for both topologies (nested and NPC), the comparison between Figs. 2(a) and 3(a) shows that the conduction losses will be different as presented in Section V. For the generation of all other levels, the conduction losses of the nested topology will be lower than that one for the NPC configuration.

III. PULSE WIDTH MODULATION (PWM) STRATEGY

A. Hybrid PWM Strategy

The control of the nested configurations have been implemented by using the hybrid PWM strategy, which is described in this section. For hybrid PWM implementation, the references voltages v_a^*, v_b^*, and v_c^* are initially defined and must be modified to guarantee the same advantages of the space vector PWM

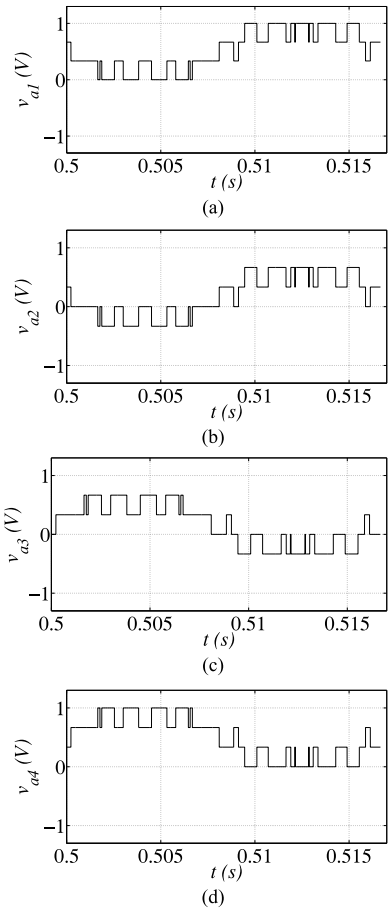

Fig. 10. Voltages across the power switches for the leg a.

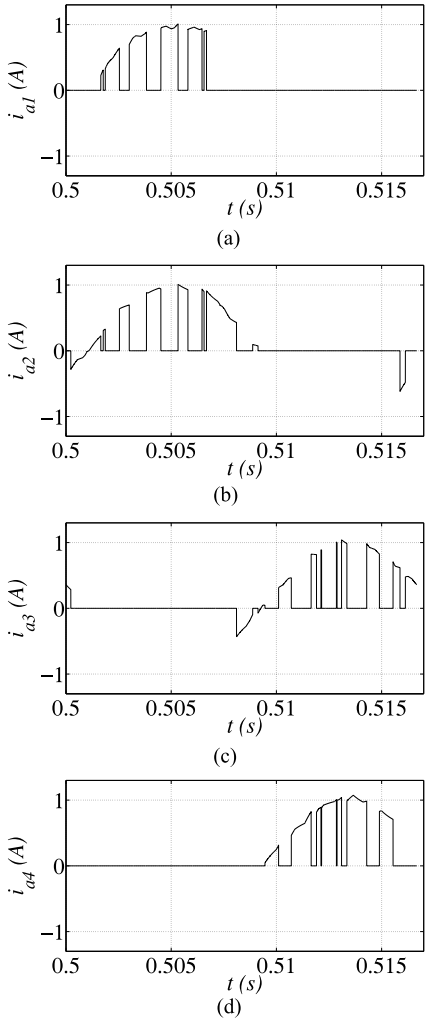

Fig. 11. Current flowing through the power switches for the leg a.

with the ease of implementation of scalar PWM. Then, the modified reference voltages $\overline{v}_a^*$, $\overline{v}_b^*$, and $\overline{v}_c^*$ can be defined from the three-phase sinusoidal references voltages v_a^*, v_b^*, and v_c^* as follows:

$$\overline{v}_a^* = v_a^* + v_\mu^* \tag{1}$$

$$\overline{v}_b^* = v_b^* + v_\mu^* \tag{2}$$

$$\overline{v}_c^* = v_c^* + v_\mu^* \tag{3}$$

where v_μ^* is a zero-sequence component.

Equations (1)–(3) cannot be solved unless v_μ^* is obtained. The voltage v_μ^* can be calculated taking into account the general apportioning factor μ that is

$$v_\mu^* = \mu P_{\min} - (1-\mu)\left(\frac{E}{N-1} - P_{\max}\right) \tag{4}$$

where $P_{\max} = \max P$, $P_{\min} = \min P$, $P = \{P_a, P_b, P_c\}$, N (in this case $N = 4$) is the number of levels of the inverter, and E is the total dc-link voltage. The parameters P_a, P_b, and P_c indicate the differences between the levels and the corresponding sinusoidal reference voltages at a certain modulation instant, as shown in Fig. 4 for the four-level topology.

P_a, P_b, and P_c can be determined considering that each level of the four-level inverter is represented by a horizontal axis that limits the graphics region of the sinusoidal references v_a^*, v_b^*, and v_c^*. The values of theses levels are given by

$$\text{Axis}(k) = \left(\frac{1}{2} - \frac{k-1}{N-1}\right) E \tag{5}$$

with $k = 1, \ldots, 4$ which are shown in Fig. 4.

Since the axis values have been determined, it turns out that

$$\text{if}(\text{Axis}(k)) > v_x^* > \text{Axis}(k+1), \text{then}, \; p_x = \text{Axis}(k) - v_x^*. \tag{6}$$

TABLE IV
LOSSES FOR THE CONVENTIONAL FOUR-LEVEL NPC TOPOLOGY

	$f_s = 720\,\text{Hz}$			$f_s = 5\,\text{KHz}$		
Case:	1	2	3	1	2	3
Conduction losses (in W):	5.38	5.15	5.37	5.34	5.12	5.34
Switching losses (in W):	0.26	0.5	1.02	1.87	3.7	7.52
Total losses (in W):	5.64	5.65	6.39	7.21	8.82	12.86

TABLE V
LOSSES FOR THE FOUR-LEVEL NESTED TOPOLOGY

	$f_s = 720\,\mathrm{Hz}$		$f_s = 5\,\mathrm{KHz}$			
Case:	1	2	3	1	2	3
Conduction losses (in W):	2.58	2.41	2.5	2.6	2.43	2.51
Switching losses (in W):	0.26	0.5	1.07	1.87	3.69	7.5
Total losses (in W):	2.84	2.91	3.57	4.47	6.12	10.01

TABLE VI
LOSSES FOR THE CONVENTIONAL FOUR-LEVEL NPC TOPOLOGY OPERATING UNDER RATED CONDITIONS 1200 V/50 A

	$f_s = 720\,\mathrm{Hz}$	$f_s = 5\,\mathrm{KHz}$
Conduction losses (in W)	270.54	270.51
Switching losses (in W)	27.64	197.82
Total losses (in W)	298.18	468.33

TABLE VII
LOSSES FOR THE NESTED FOUR-LEVEL TOPOLOGY OPERATING UNDER RATED CONDITIONS 1200 V/50 A

	$f_s = 720\,\mathrm{Hz}$	$f_s = 5\,\mathrm{KHz}$
Conduction losses (in W)	136.76	136.75
Switching losses (in W)	27.65	197.73
Total losses (in W)	164.41	334.48

TABLE VIII
COMPARISON AMONG THE FOUR-LEVEL POWER CONVERTERS

Controlled Power Switches	Extra Diodes	Irregular Losses Distribution	Flying Capacitor	Control Complexity	
Fig. 1(a)	6	0	yes	0	low
Fig. 3	6	4	yes	0	low
Fig. 1 4(a)	6	4	yes	0	low
Fig. 1 4(b)	12	0	no	0	high
Fig. 1 4(c)	12	0	no	3	high
Fig. 1 4(d)	6	0	yes	2	low

The time intervals T_1, T_2, and T_3 and the signals command of the inverter switches T_a, T_b, and T_c are determined by using

$$T_j = \frac{P_x}{\frac{E}{N-1}} T_s \text{ and } T_x = T_s - T_j \tag{7}$$

with $j = 1, 2, 3$ and $x = a, b, c$.

Fig. 5 shows the block diagram for the proposed hybrid PWM strategy. In fact, the experimental implementation of the nested topology was done by using the schematic presented in Fig. 5. In this case, the gating signals were obtained by programming the timers of the DSP TMS320F28335.

Alternatively, the switching gating signals can be defined by using analog implementation as presented in Fig. 6. In this case, it is employed a level-shift approach for the carrier signals. Note that the logic employed in Fig. 6 allows the generation of the gating signals as presented in Table I.

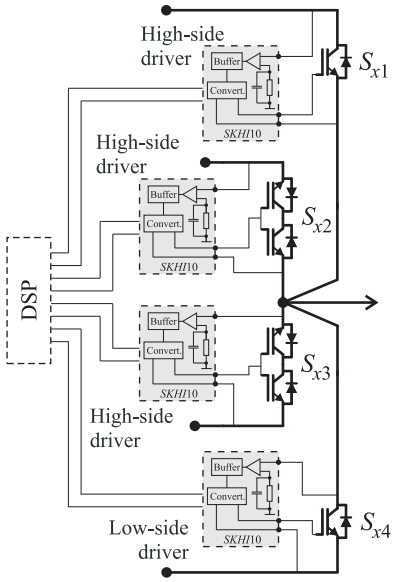

Fig. 12. Drive circuitry for the nested leg with three high-side and one low-side drivers.

Fig. 7 shows the influence of μ on the quality of the waveform generated by the nested topology with four, five, and six levels. The best solution in terms of weighted total harmonic distortion (WTHD) is $\mu = 0.5$, due to the symmetry of the pulsed voltage generated. On the other hand, choosing $\mu = 0$ or $\mu = 1$ guarantee better efficiency for the converter. Fig. 8(a)–(c) presents the total harmonic distortion (THD) of the load current versus the modulation index for the configuration with four, five, and six levels, respectively. Such figures compare the PWM implemented with and without the parameter v_μ^*. Note that the same PWM strategy can be extended for the configurations with higher number of levels just changing N in (4).

B. Space Vector Modulation (Four-Level Configuration)

By using the conservative three-phase to two-phase transformation, it can be shown that the voltages in quadrature v_d and v_q in the stationary reference frame can be expressed as a function of the desired load voltages v_{an}, v_{bn}, and v_{cn} as follows:

$$\begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{-\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{8}$$

where

$$v_{an} = v_{a0} - v_{n0} \tag{9}$$

$$v_{bn} = v_{b0} - v_{n0} \tag{10}$$

$$v_{cn} = v_{c0} - v_{n0} \tag{11}$$

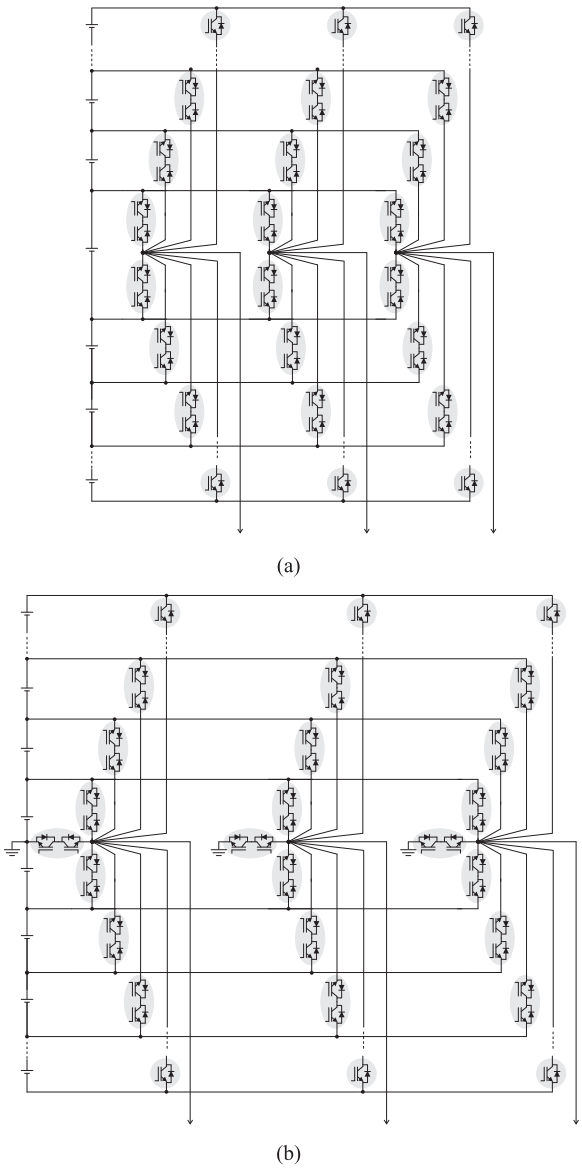

Fig. 13. Generalization of the nested configurations with (a) even and (b) odd number of levels.

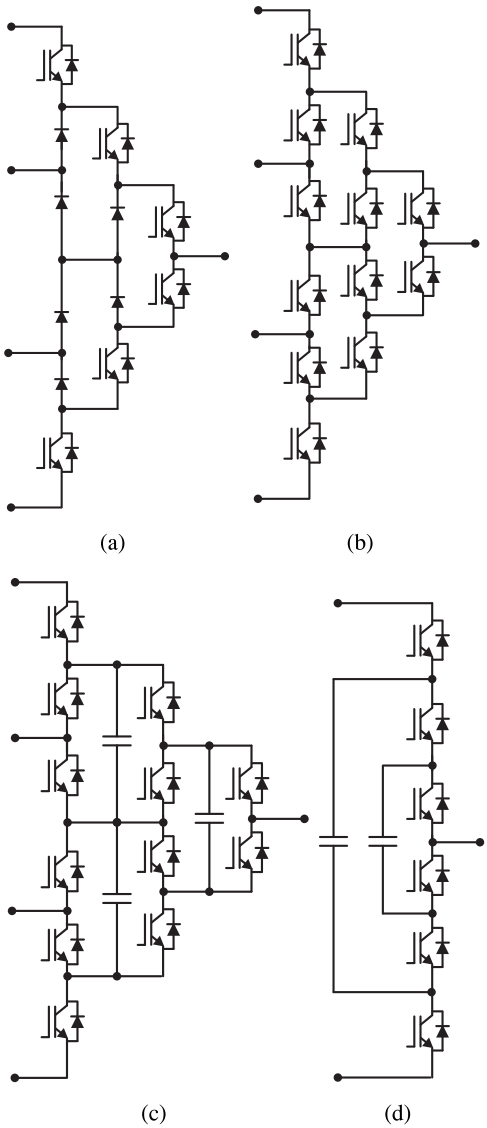

Fig. 14. Topologies proposed in the technical literature. (a) Diode clamping multilevel inverter proposed by [24]. (b) Active NPC converter studied in [25]. (c) Four-level inverter proposed by [26]. (d) Flying capacitor topology.

with

$$\begin{aligned} v_{a0} = {} & S_{a1}\overline{S}_{a2}\overline{S}_{a3}\overline{S}_{a4}(V_1) + \overline{S}_{a1}S_{a2}\overline{S}_{a3}\overline{S}_{a4}(V_2) \\ & + \overline{S}_{a1}\overline{S}_{a2}S_{a3}\overline{S}_{a4}(V_3) + \overline{S}_{a1}\overline{S}_{a2}\overline{S}_{a3}S_{a4}(V_4) \quad (12) \\ v_{b0} = {} & S_{b1}\overline{S}_{b2}\overline{S}_{b3}\overline{S}_{b4}(V_1) + \overline{S}_{b1}S_{b2}\overline{S}_{b3}\overline{S}_{b4}(V_2) \\ & + \overline{S}_{b1}\overline{S}_{b2}S_{b3}\overline{S}_{b4}(V_3) + \overline{S}_{b1}\overline{S}_{b2}\overline{S}_{b3}S_{b4}(V_4) \quad (13) \\ v_{c0} = {} & S_{c1}\overline{S}_{c2}\overline{S}_{c3}\overline{S}_{c4}(V_1) + \overline{S}_{c1}S_{c2}\overline{S}_{c3}\overline{S}_{c4}(V_2) \\ & + \overline{S}_{c1}\overline{S}_{c2}S_{c3}\overline{S}_{c4}(V_3) + \overline{S}_{c1}\overline{S}_{c2}\overline{S}_{c3}S_{c4}(V_4) \quad (14) \end{aligned}$$

and $V_1 = V_{\mathrm{dc1}} + \frac{V_{\mathrm{dc2}}}{2}$, $V_2 = \frac{V_{\mathrm{dc2}}}{2}$, $V_3 = -\frac{V_{\mathrm{dc2}}}{2}$, and $V_4 = -V_{\mathrm{dc3}} - \frac{V_{\mathrm{dc2}}}{2}$; S_{xj} are the state of the switches ($j = 1, 2, 3, 4$) with the complementary ones represented by $\overline{S}_{xj} = 1 - S_{xj}$, and $v_{n0} = \frac{1}{3}(v_{an} + v_{bn} + v_{cn})$.

There are 64 possible combinations for the state of the switches, which originate four null voltage vectors and 60 active voltage vectors spatially displaced as presented in Fig. 9. Note from this figure that there are 36 nonredundant vectors.

Since the space vector modulation involves vectorial equating volt-second integrals between a desired reference voltage vector and the output vectors, two adjacent vectors can be chosen to synthesize the desirable voltage as described in [22].

IV. Guideline for Component Selection and Drive Circuitry

The guideline for the semiconductor component selection is obtained through the selection of the blocking voltage, current rating, and switching frequency of all power switches employed in the nested configurations.

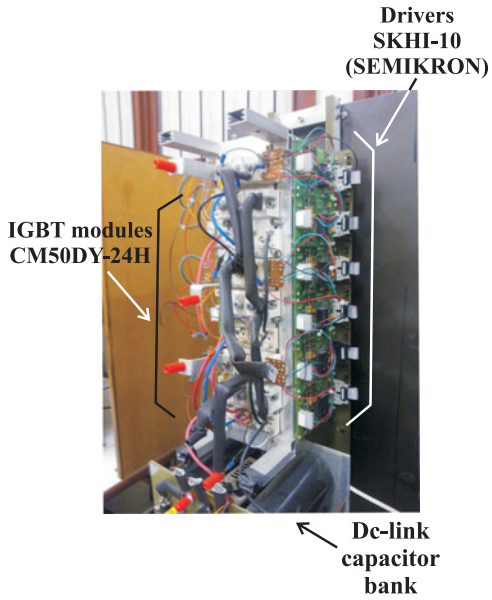

Fig. 15. Photo of the experimental setup.

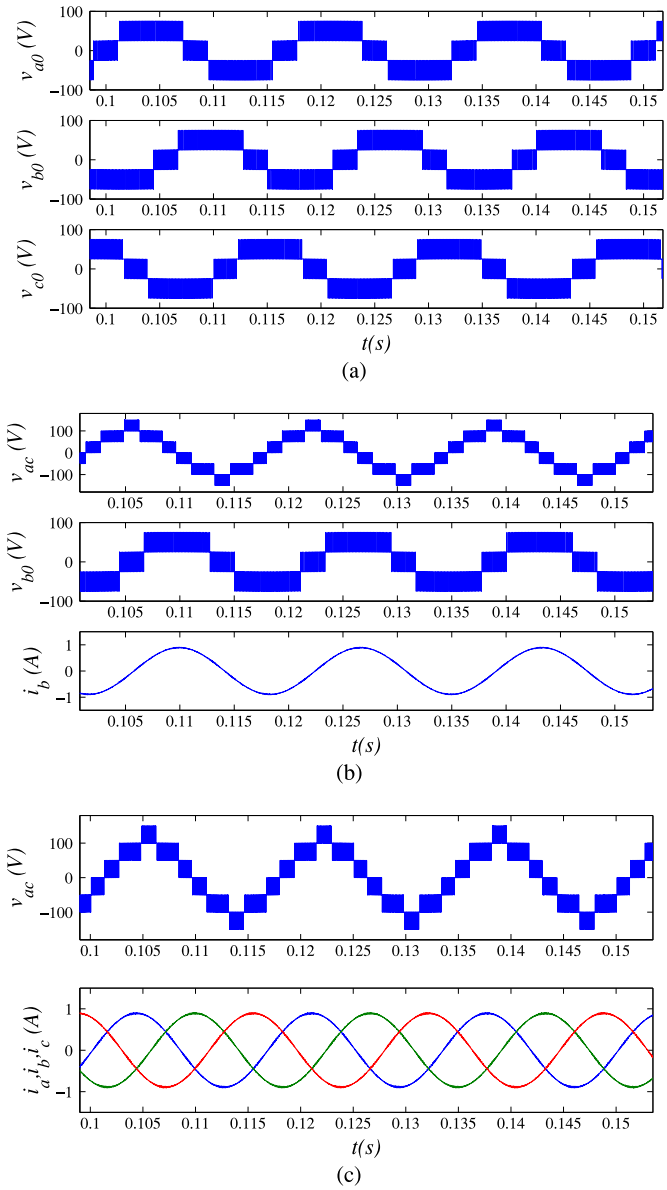

Fig. 16. Simulated results of the nested configuration with four levels. (a) Pole voltages. (b) From top to bottom: output line voltage, pole voltage, and phase current. (c) From top to bottom: output line voltage and current of the three-phase load.

Tables II and III show the blocking voltage and current ratings for the switches employed in the nested topologies with four and five levels, respectively. The load voltage and load current have been considered in p.u.(per unit), with both peak load voltage and peak load current given by 1 p.u. All power switches operate at the switching frequency, which is equal to 720 Hz.

Note that although the nested topologies reduce the number of diodes as compared to the conventional NPC topology, it presents irregular voltage stress among the power switches. Fig. 10 shows the voltages across the switches confirming the results in Table II. On the other hand, Fig. 11 shows that the currents are the same for all switches. These results were obtained assuming both load voltage and load current equal to 1 p.u. Note that the blocking voltage for the switches S_{a1} and S_{a4} are higher than that ones for the switches S_{a2} and S_{a3}. Such a characteristic of this topology actually favors the use of wide bandgap devices with high breakdown voltage, (e.g., SiC and GaN) for the switches placed at the positions of the switches S_{a1} and S_{a4}. While the switches S_{a2} and S_{a3} can employ conventional semiconductor devices.

As far as the connection of the power devices to the ground-referenced point goes, power switches employed in converters can use either a low-side switch drive or high-side switch drive. Since it is floating, the challenges faced by the high-side devices (*N*-channel) are higher than that one for the low-side devices. This is especially true because of the required voltage translation to the supply and because generally it is more difficult to turn OFF a floating switch. By comparing the nested configuration with the NPC topology with four levels [see Figs. 1(a) and 3], there are three high-side switch drives S_{x1}, S_{x2}, and S_{a3} per leg for the nested topology, while the NPC topology requires five.

V. Losses Comparison

The four-level nested configuration depicted in Fig. 1(a) has been compared to the conventional four-level NPC topology. Such a comparison was in terms of the losses for different conditions of loads, dc-link voltages and switching frequency.

The loss estimation is obtained through regression model, which has been achieved by experimental tests, as presented by [23]. The power switch used in the experimental tests was IGBT module CM50DY-24H (POWEREX) driven by SKHI-10 (SEMIKRON). That switch losses model includes: 1) IGBT and diode conduction losses and 2) switching losses (IGBT turn-on losses, IGTB turn-off losses and diode turn-off energy).

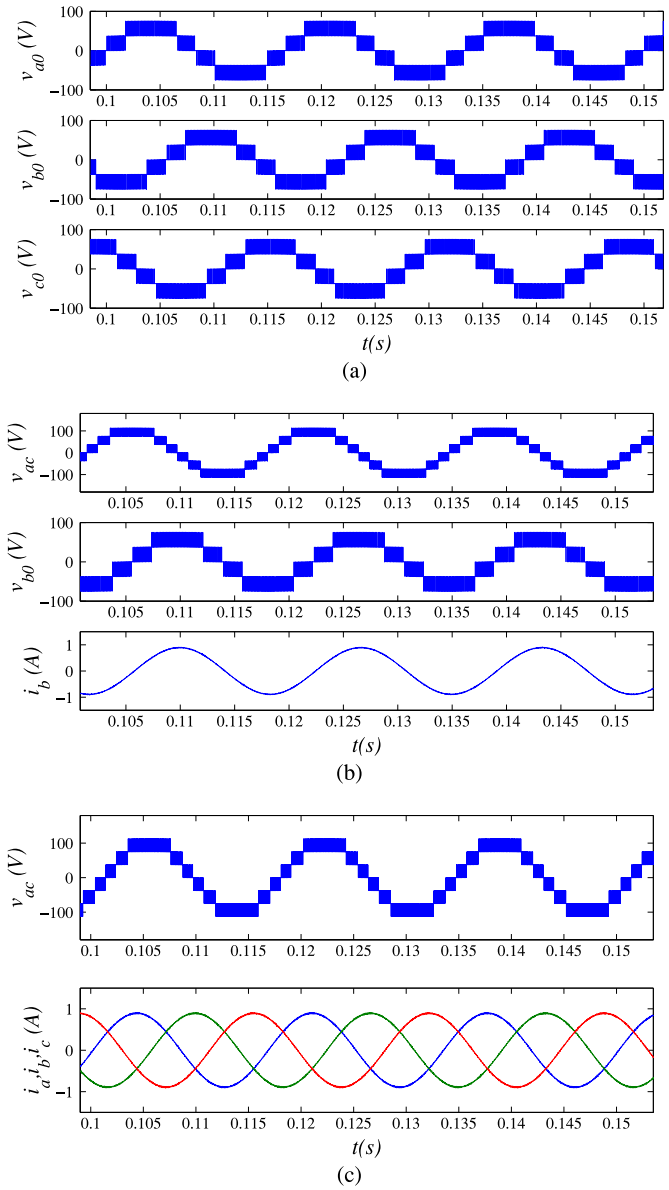

Fig. 17. Simulated results of the nested configuration with five levels. (a) Pole voltages. (b) From top to bottom: output line voltage, pole voltage, and phase current. (c) From top to bottom: output line voltage and current of the three-phase load.

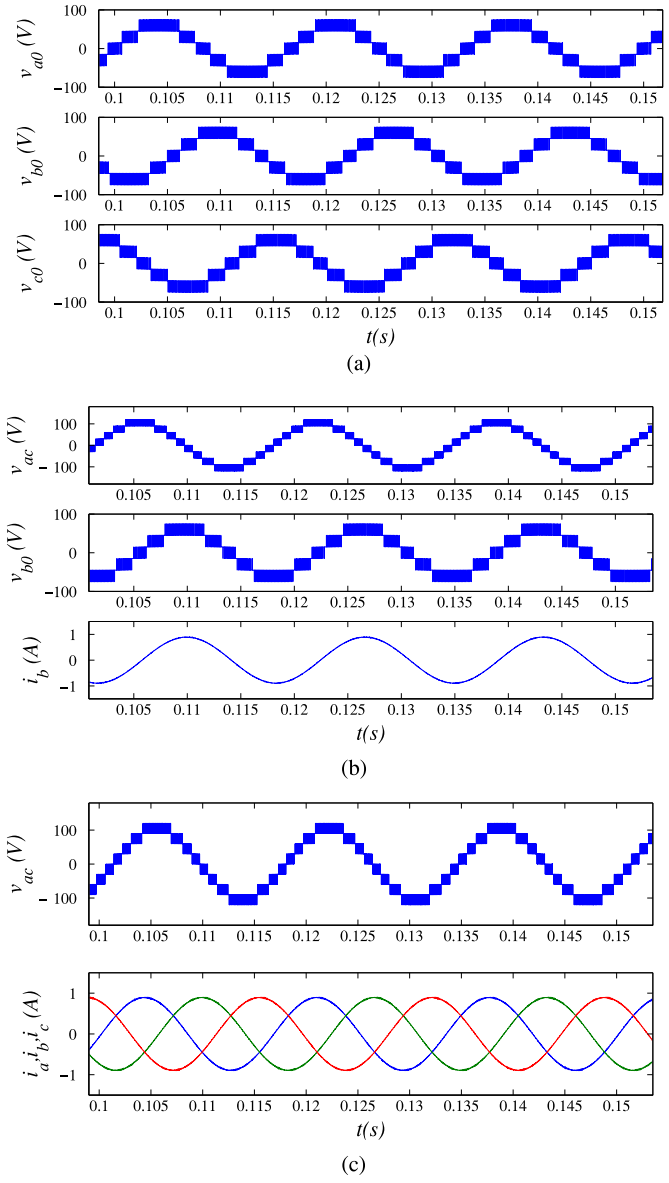

Fig. 18. Simulated results of the nested configuration with six levels. (a) Pole voltages. (b) From top to bottom: output line voltage, pole voltage, and phase current. (c) From top to bottom: output line voltage and current of the three-phase load.

Tables IV and V present the conduction, switching, and total losses for three different cases (see below) and considering two switching frequencies ($f_s = 720$ Hz and $f_s = 5K$Hz):

1) *Case 1 (dc-link voltage):* 150 V, $R = 65\ \Omega$ and $L = 7$ mH;
2) *Case 2 (dc-link voltage):* 300 V, $R = 142\ \Omega$ and $L = 15.3$ mH;
3) *Case 3 (dc-link voltage)*: 600 V, $R = 142\ \Omega$ and $L = 15.3$ mH.

Tables VI and VII present the losses for the four-level NPC and nested topologies with the switches operating under rated conditions (1200 V/50 A). Note that in all cases, the nested configuration presents advantages, especially due to conduction losses reduction obtained due to elimination of the diodes.

VI. Generalization and Comparison Among Topologies

The concept of nested topologies can be generalized for higher number of levels by using the same principle as presented in Fig. 1, i.e., the external leg involving the internal one.

Fig. 13 depicts the generalization of the nested configurations, with Fig. 13(a) showing the generalization for an even number of levels, and Fig. 13(b) showing the generalization for an odd number of levels.

Table VIII shows a comparison of the nested configuration (see Fig. 1) and other topologies proposed in the technical literature, e.g., NCP converter (see Fig. 3) and other circuits able to generate the same number of levels, as in Fig. 14. The figures of merit considered in the comparison of Table VIII are 1) num-

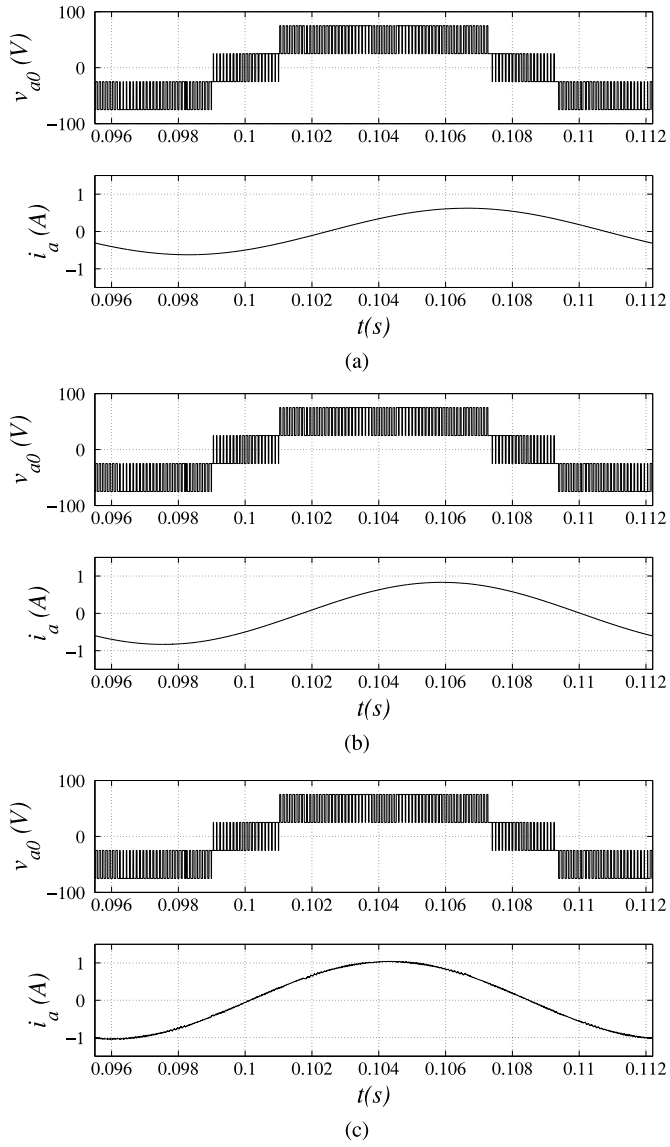

Fig. 19. Simulated results of the four-level nested configuration with power factor equal to (a) 0.6, (a) 0.8, and (a) 1.0.

ber of controlled power switches, 2) number of extra diodes, 3) losses distributions among the power switches, 4) the need for flying capacitors, and 5) the complexity of the control and PWM strategies.

VII. Simulated and Experimental Results

The nested multilevel configurations were validated through simulation and experimental results. The proof-of-concept setup was built with IGBTs from SEMIKRON controlled by DSP TMS320F28335 as presented in the Fig. 15. The drivers, power switches, and dc-link capacitors are highlighted in this photo. This testbed setup has been employed to obtain the outcomes of the four-level and five-level converters. The DSP is placed behind the rack.

The three-phase RL load was connected to the output converter with the following parameters $R = 65\,\Omega$ and $L = 7\mathrm{mH}$. Three dc sources with 50 V, each have been also employed

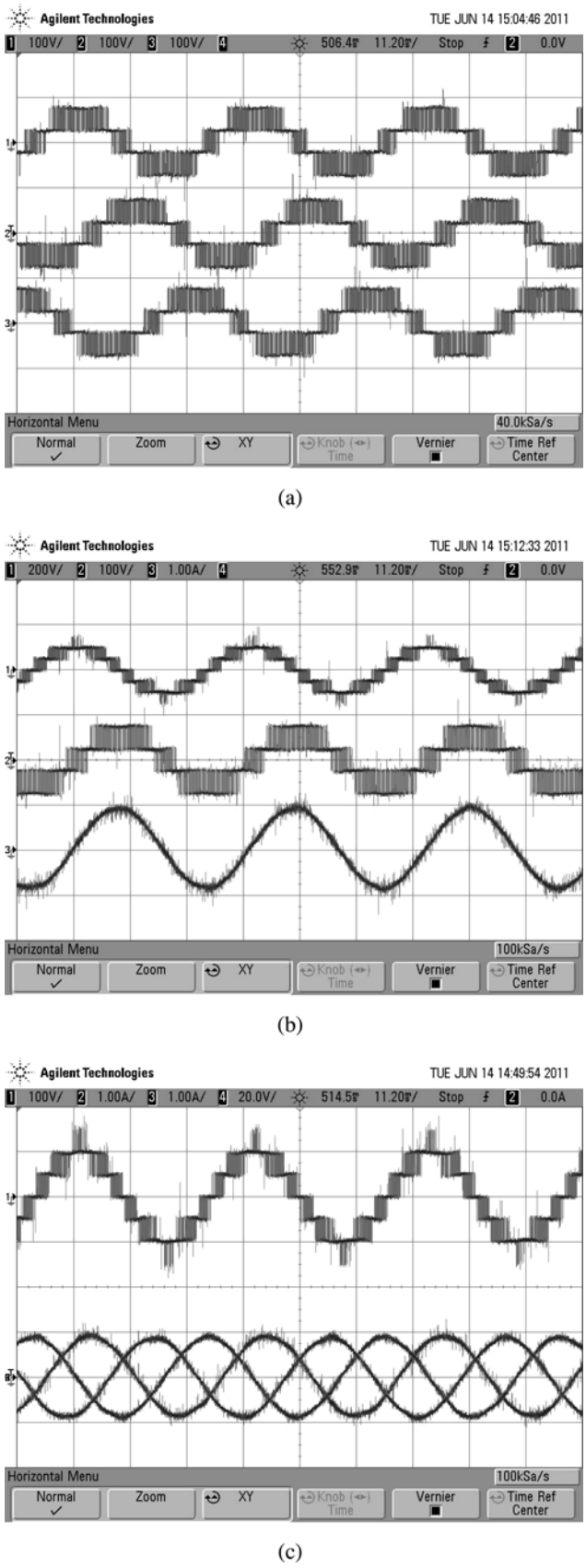

Fig. 20. Experimental results of the nested configuration with four levels. (a) Pole voltages. (b) From top to bottom: output line voltage, pole voltage, and phase current. (c) From top to bottom: output line voltage and current of the three-phase load.

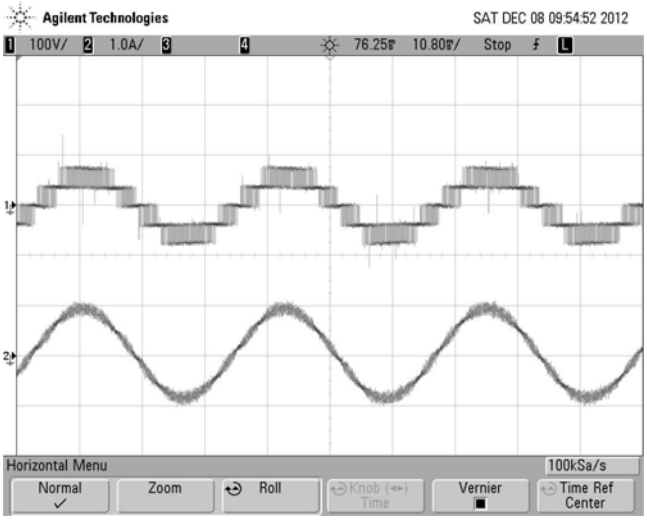

Fig. 21. Experimental results for the five-level nested configuration: (top) pole voltage and (bottom) load current.

with the dc-link capacitors equal to $C = 2200\ \mu$F. For comparison purposes, these are the same conditions as employed in the simulation results.

Fig. 16 shows simulated results for the nested configuration with four levels. The waveforms presented in this figure are 1) pole voltages; 2) from top to bottom: output line voltage, pole voltage, and phase current; and 3) from top to bottom: output line voltage and currents of the three-phase load. The same set of waveforms are shown in Figs. 17 and 18 for five and six levels, respectively. Fig. 19 shows additional simulated results for the four-level nested topology with three different power factors.

Fig. 20 shows the experimental results for the nested configuration with four levels under the same conditions as in Fig. 16. Comparing Figs. 16 and 20 it is evident that both simulated and experimental results match to each other. Fig. 21 shows experimental results for the five-level configuration presenting its pole voltage and output current.

VIII. Conclusion

This paper has proposed a family of multilevel converters based on the concept of nested arrangement. The main advantage of the nested configurations compared to the equivalent NPC topologies are in terms of reduced number of diodes employed and higher efficiency. It has been demonstrated that the conduction losses of the proposed nested topologies are lower than the equivalent NPC converter. Also, the generalized hybrid PWM strategy allows voltages generation with high quality for the converters with number of levels equal or higher than four.

Although dealing with irregular blocking voltage distribution among the semiconductor devices, the nested topologies favor the use of wide bandgap devices, such as SiC. In terms of the drivers employed for the nested topology, the four-level circuit requires three high-side drivers and one low-side driver, which is better than the other converters. A generalization of the nested circuit for an odd or even number of levels has been considered in this paper as well.

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