Interleaved Boost-Integrated *LLC* Resonant Converter With Fixed-Frequency PWM Control for Renewable Energy Generation Applications

Xiaofeng Sun, *Member, IEEE*, Yanfeng Shen, Yune Zhu, and Xiaoqiang Guo, *Member, IEEE*

***Abstract*—This paper proposes a current-fed *LLC* resonant converter that is able to achieve high efficiency over a wide input voltage range. It is derived by integrating a two-phase interleaved boost circuit and a full-bridge *LLC* circuit together by virtue of sharing the same full-bridge switching unit. Compared with conventional full-bridge *LLC* converter, the gain characteristic is improved in terms of both gain range and optimal operation area, fixed-frequency pulsewidth-modulated (PWM) control is employed to achieve output voltage regulation, and the input current ripple is minimized as well. The voltage across the turned-off primary-side switch can be always clamped by the bus voltage, reducing the switch voltage stress. Besides, its other distinct features, such as single-stage configuration, and soft switching for all switches also contribute to high power conversion efficiency. The operation principles are presented, and then the main characteristics regarding gain, input current ripple, and zero-voltage switching (ZVS) considering the nonlinear output capacitance of MOSFET are investigated and compared with conventional solutions. Also, the design procedure for some key parameters is presented, and two kinds of interleaved boost integrated resonant converter topologies are generalized. Finally, experimental results of a converter prototype with 120–240 V input and 24 V/25 A output verify all considerations.**

***Index Terms*—Current-fed converter, fixed-frequency PWM control, *LLC* resonant converter, wide voltage gain range.**

I. Introduction

RENEWABLE energy generation (REG) has been recognized as one of the most effective solutions to the increasingly serious energy crisis and environment pollution [1], [2]. The output voltages of renewable energy sources, such as photovoltaic, fuel cell, and etc., however, usually vary over a wide range with climate, weather, and operation conditions. On the other hand, small current ripple and high power conversion efficiency are usually required by REG systems for long-term, reliable, and efficient operation [3]–[6]. Therefore, to interface renewable energy sources, it is quite necessary to develop a dc/dc converter, which can cope with a wide input voltage range while maintaining low input current ripple and high power conversion efficiency.

Manuscript received April 20, 2014; revised August 11, 2014; accepted September 9, 2014. Date of publication September 16, 2014; date of current version March 5, 2015. This work was supported by the National Natural Science Foundation of China under Award 51077112. Recommended for publication by Associate Editor T. Shimizu.

The authors are with the Key Lab of Power Electronics for Energy Conservation and Motor Drive of Hebei Province, Department of Electrical Engineering, Yanshan University, Qinhuangdao 066004, China (e-mail: sxf@ysu.edu.cn; yanfeng.shen@hotmail.com; zhu607201@163.com; gxq@ysu.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2358453

Among various dc/dc converters, *LLC* resonant converter has been attracting more and more attention for its inherent merits, like soft switching, low EMI, high efficiency, and high power density [7]–[26]. Generally, for the traditional pulse frequency modulation (PFM) controlled half-/full-bridge *LLC* resonant converter, the characteristic impedance Z_r of the resonant tank has to be decreased or the operating frequency range has to be extended in order to obtain a wide dc voltage gain range (no less than twice) [14]–[16]. This may incur some undesirable problems, such as increased transformer size, wide switching frequency variations, and high conduction losses. Therefore, conventional *LLC* resonant converter is not suitable for wide input voltage range applications [17], [18], [27].

Many solutions associated with topology and control strategy have been proposed to extend the gain range of *LLC* resonant converter [18]–[24]. In [19], taking account of the MOSFETs' drain sources parasitic capacitances and the transformer leakage inductances, an *LLC*-*LC* resonant converter is introduced and the components' optimal values are derived for wide output voltage range. Liang *et al*. [20] propose a hybrid-bridge dual-mode *LLC* resonant converter, in which two operation modes—half-bridge mode and full-bridge mode—can be utilized to obtain a wide gain range with an improved switching strategy. A new *LLC* configuration is proposed in [21], and the gain range is extended by controlling the auxiliary switch and changing the magnetizing inductor based on the input voltage. Also, a three-level *LLC* resonant converter, consisting of two half-bridge *LLC* circuits in series, is proposed in [22] for an input range of 400–600 V. However, these solutions are implemented with PFM control and the frequency range is relatively large, which complicates the design and optimization of magnetic components.

To achieve a wide gain range with fixed-frequency control, Jin and Ruan [18] propose a hybrid full-bridge three-level *LLC* resonant converter and [23] presents a new type of *LLC* resonant converter by adding a controllable auxiliary winding. However, many power switches are employed in these schemes, resulting in increased cost and size. Besides, the added auxiliary switches in [23] operate with hard switching at high frequency, thus the switching loss is also a barrier for the performance improvement.

On the other hand, for these voltage-fed topologies [7]–[24], considerably bulky electrolytic capacitor is generally required to suppress the large input current ripple, resulting in large size, high cost, and shortened lifetime of REG systems [28]. By contrast, current-fed converters [6], [28]–[34] employed in REG applications not only aid in the reduction of input current ripple but also reduce the filter and transformer size [6],

[28]. However, it is well known that the conventional current-fed converters, such as current-fed full-bridge, half-bridge, and push–pull converters, suffer from high voltage spike across the switches at their turn-off [29]. Han *et al*. [30] and Jang *et al*. [31] propose two active clamping zero-voltage switching (ZVS) PWM current-fed half-bridge converters, in which the voltage surge across the turned-off switch can be absorbed and ZVS of power switches can be achieved within a certain operating range. In order to further reduce the input current ripple, component size, and voltage/current rating of switches/diodes, Rathore [32] proposes and designs an interleaved soft-switched active-clamped L–L type current-fed half-bridge converter. In [28], [33], and [34], a novel secondary modulation technique is proposed and applied to bidirectional current-fed half-bridge, full-bridge, and push–pull isolated converters. Thus, the voltage across the current-fed primary-side devices can be clamped naturally and the switch turn-off voltage spike can be well eliminated without any additional circuit. However, this modulation strategy does not hold for unidirectional current-fed converters.

To achieve wide gain range while maintaining low input current ripple, a cascaded two-stage *LLC* resonant converter consisting of a hard-switched current-fed boost converter and a half-bridge *LLC* converter is adopted in [25] for fuel cell application. The unregulated fixed-frequency-controlled *LLC* resonant converter is fed by the boost converter, thus the voltage gain is extended and the input current ripple is minimized as well. Similarly, in [26] an interleaved boost circuit and a full-bridge *LLC* circuit are cascaded to form a two-stage converter for plug-in electric vehicle charger. In these cascade converter topologies, however, since the boost stage operates in hard switching manner, both the switching losses and the reverse recovery losses are high, which decreases the overall converter efficiency.

In this paper, a novel two-phase interleaved boost integrated *LLC* (IBI-LLC) resonant converter is proposed for wide input voltage range. By integrating the two-phase interleaved boost converter with the full-bridge *LLC* converter, the regulated gain range is extended and the input current ripple is reduced as well. ZVS turn-ON and zero-current switching (ZCS) turn-OFF can be achieved, respectively, for primary switches and secondary rectifier diodes, which significantly minimize the switching losses and the reverse recovery losses. Besides, fixed-frequency PWM control is adopted, and the switching frequency f_s is constantly equal to the resonant frequency f_r, which benefits the optimization of magnetic components and passive filters with respect to volume and losses. Furthermore, owing to the fixed-frequency PWM control, the magnetizing inductor and boost inductors have little impact on the gain characteristics, and thus can be designed as large as possible to reduce the conduction losses under the condition that ZVS is achieved. The proposed IBI-LLC resonant converter is a preferable candidate for REG systems.

II. Operation Principle

The proposed IBI-LLC resonant converter is an integration of a two-phase interleaved boost converter and a full-bridge *LLC* resonant converter, as shown in Fig. 1. Switches pairs S_1, S_2, and S_3, S_4 form the left leg and the right leg, respectively. Inductor

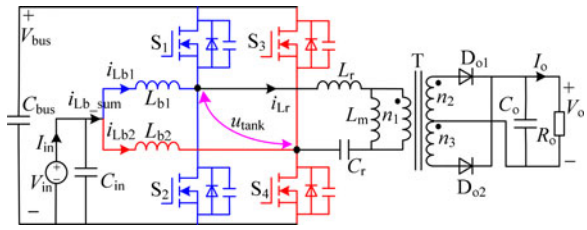


Fig. 1. Proposed IBI-LLC resonant converter.

L_{b1} is connected to the midpoint of the left leg to compose the first boost converter, and inductor L_{b2} is connected to the midpoint of the right leg to form the second boost converter. The two boost converters operate with interleaving and are phase-shifted with 180°. On the other hand, together with the *LLC* resonant tank (including the resonant inductor L_r, magnetizing inductor L_m, and resonant capacitor C_r), high-frequency transformer *T*, and the rectifier diodes D_{o1}, D_{o2}, the two legs further form a full-bridge *LLC* resonant converter. The two-phase interleaved boost converter and the full-bridge *LLC* resonant converter share the same switches S_1–S_4, leading to reduced number of power switches. For the proposed IBI-LLC resonant converter with an integrated single-stage structure, the input voltage $V_{\rm in}$ is boosted to the bus voltage $V_{\rm bus}$, which feeds the full-bridge resonant *LLC* converter simultaneously. The transformer turns ratio $n = n_1 : n_2 = n_1 : n_3$.

Fixed-frequency PWM control is adopted for the IBI-LLC resonant converter and the switching frequency f_s is equal to the *LC* resonant frequency f_r. The modulation strategy is shown in Fig. 2, where the upper switch and the lower switch of each leg operate complementarily with a dead time $t_{\rm dead}$. S_1 and S_3 have the same duty cycle *D* but are phase-shifted with 180°. And S_2 and S_4 have the same duty cycle 1–*D* but are 180° out of phase. With this modulation, the input resonant tank voltage $u_{\rm tank}$ features a three-level ac square wave with duty cycle *D* (if $D \le 0.5$) or $1 - D$ (if $D > 0.5$) and magnitude $V_{\rm bus}$. By changing the duty cycle *D* of S_1 and S_3, both the magnitude and duty cycle of $u_{\rm tank}$ can be modified. Thus, the fundamental component of $u_{\rm tank}$ can be controlled to achieve a wide gain range over full-load range.

The currents of the two integrated boost inductors L_{b1} and L_{b2} are denoted as $i_{L_{\rm b1}}$ and $i_{L_{\rm b2}}$, respectively, and the sum of the two inductor currents is represented by $i_{L_{\rm bsum}}$. Obviously, the average current of $i_{L_{\rm bsum}}$ is equal to the input current $I_{\rm in}$. Assume that the two boost inductors have the same value $i_{L_{\rm b1,2}}$ and current sharing between L_{b1} and L_{b2} is achieved. Thus, the two integrated boost inductors L_{b1} and L_{b2} share the same average current value $I_{\rm in}/2$ and current ripple value $\Delta i_{L_{\rm b1,2}}$. The current ripple of $i_{L_{\rm bsum}}$ is denoted as $\Delta i_{L_{\rm bsum}}$.

The gate driving signals and principal steady-state operation waveforms of the fixed-frequency PWM-controlled converter in the case of $D \le 0.5$ is depicted in Fig. 2(a). Referring to the timing diagrams, there are ten switching modes during a complete switching cycle T_s. [t_0, t_5] are the five switching modes during half a switching cycle and the corresponding equivalent circuits are shown in Fig. 3.

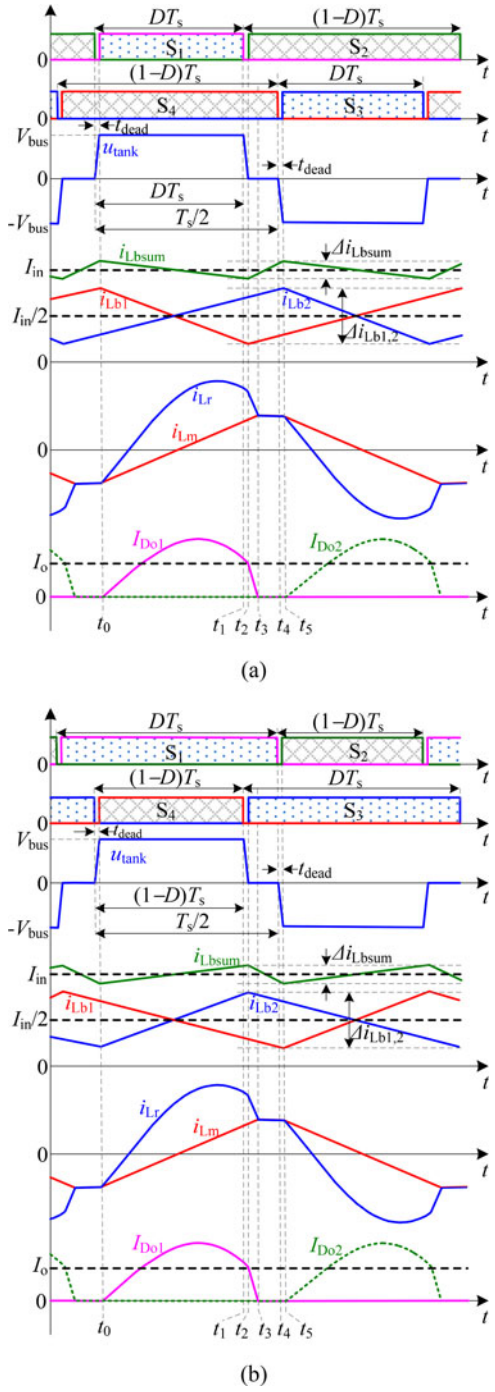


Fig. 2. Key operation waveforms of the proposed IBI-LLC resonant converter for (a) $D \le 0.5$ and (b) $D > 0.5$.

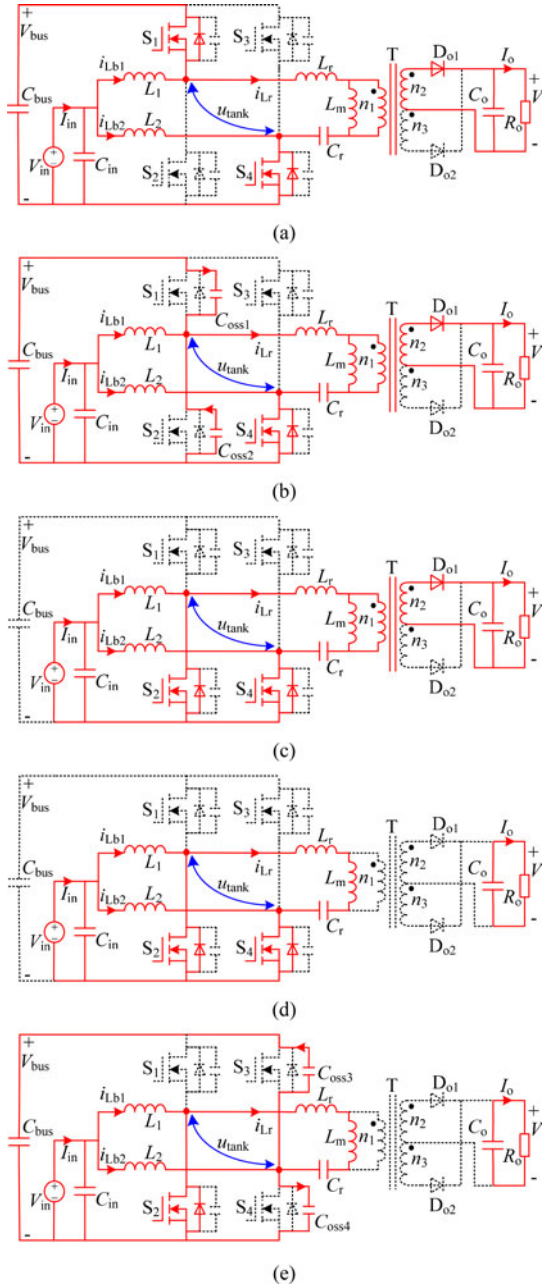


Fig. 3. Operation modes of the IBI-LLC resonant converter with fixed-frequency PWM control. (a) Stage 1 $[t_0, t_1]$. (b) Stage 2 $[t_1, t_2]$. (c) Stage 3 $[t_2, t_3]$. (d) Stage 4 $[t_3, t_4]$. (e) Stage 5 $[t_4, t_5]$.

Stage 1 [t_0, t_1] [see Fig. 3(a)]: S_4 has been conducting before this stage and S_1 is turned on at t_0. During this time interval, the resonant tank voltage $u_{\rm tank}$ equals the bus voltage $V_{\rm bus}$, and the magnetizing inductor voltage V_{L_m} is clamped to the output voltage. The primary resonant current i_{L_r} is sinusoidal with an amplitude I_{Lr_p} due to the resonance between L_r and C_r, and current i_{L_r} is greater than the magnetizing current i_{L_m}, which is increasing linearly. The current flowing through diode D_{o1} is proportional to the difference between ni_{L_r} and ni_{L_m}. At the same time, due to the simultaneous on-state of S_1 and S_4, L_{b1} and L_{b2} are being, respectively, discharged and charged, and the two turned-off switches S_2 and S_3 are being clamped by the bus voltage $V_{\rm bus}$. The further equivalent circuit of the resonant tank in this stage is shown in Fig. 4(a). Currents i_{L_r}, i_{L_m}, and the voltage across the resonant capacitor u_{C_r} can be expressed as

$$\begin{cases} i_{L_r}(t) = i_{L_r}(t_0)\cos(\omega_r(t-t_0)) \\ \qquad + ((V_{\rm in} - nV_o - u_{C_r}(t_0))/Z_r)\sin(\omega_r(t-t_0)) \\ i_{L_m}(t) = i_{L_r}(t_0) + nV_o(t-t_0)/L_m \\ u_{C_r}(t) = (V_{\rm in} - nV_o) - (V_{\rm in} - nV_o - u_{C_r}(t_0)) \\ \qquad \cdot \cos(\omega_r(t-t_0)) + i_{L_r}(t_0)Z_r\sin(\omega_r(t-t_0)) \end{cases} \quad (1)$$

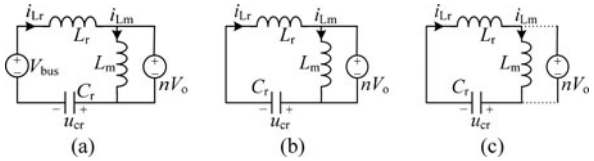


Fig. 4. Equivalent circuits of the resonant tank taking no account of the dead time. (a) $[t_0, t_1]$. (b) $[t_2, t_3]$. (c) $[t_3, t_4]$.

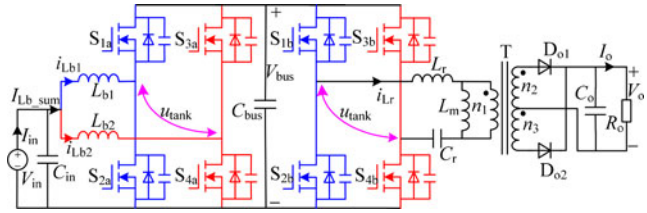


Fig. 5. Equivalent circuit of the IBI-LLC resonant converter.

where V_o is the output voltage, the angular frequency $\omega_r = 2\pi f_r$, and the characteristic impedance $Z_r = \sqrt{L_r/C_r}$.

Stage 2 [t_1, t_2] [see Fig. 3(b)]: At the moment of t_1, S_1 is turned off while S_4 and D_{o1} keep on conducting. During this dead-time interval, the output capacitors of S_1 and S_2, i.e., $C_{\rm oss1}$ and $C_{\rm oss2}$, begin to be, respectively, charged and discharged by virtue of resonant current i_{L_r} and boost current $i_{L_{\rm b1}}$. When the voltage across $C_{\rm oss2}$ decreases to zero and that across $C_{\rm oss1}$ increases to the bus voltage $V_{\rm bus}$, the antiparallel body diode of S_2 starts conducting. Thus, the turned-off switch S_1 begins to be clamped by the bus voltage $V_{\rm bus}$, and ZVS turn-ON of S_2 can be achieved subsequently.

Stage 3 [t_2, t_3] [see Fig. 3(c)]: At the time instant t_2, S_2 turns on under ZVS, and S_4 and D_{o1} are still in on-state. The magnetizing voltage V_{L_m} is still clamped to the output voltage and the magnetizing current i_{L_m} keeps on linearly increasing. However, the energy transferred to the secondary side is only provided by the resonant tank because the input resonant tank voltage equals zero. As a result, the resonant current i_{L_r} decreases rapidly in this stage. In addition, both L_{b1} and L_{b2} are being charged, and the two turned-off switches S_1 and S_3 are being clamped by the bus voltage, owing to the on-state of S_2 and S_4. The further equivalent circuit of the resonant tank is shown in Fig. 4(b). The currents i_{L_r}, i_{L_m} and the voltage u_{C_r} in this stage can be described as

$$\begin{cases} i_{L_r}(t) = i_{L_r}(t_2)\cos(\omega_r(t-t_2)) \\ \qquad\quad -((nV_o + u_{C_r}(t_2))/Z_r)\sin(\omega_r(t-t_2)) \\ i_{L_m}(t) = i_{L_r}(t_2) + nV_o(t-t_2)/L_m \\ u_{C_r}(t) = -nV_o + (nV_o + u_{C_r}(t_2)) \\ \qquad\quad \cdot \cos\omega_r(t-t_2) + i_{L_r}(t_2)Z_r \sin\omega_r(t-t_2). \end{cases} \tag{2}$$

Stage 4 [t_3, t_4] [see Fig. 3(d)]: With the decrease of resonant inductor current and the increase of magnetizing current, they equal to each other at the time instant t_3 and the rectifier diode D_{o1} is turned off with ZCS. Thus, both the reverse recovery and the voltage spike across D_{o1} can be avoided. During this time interval, instead of being clamped to the output voltage, the magnetizing inductor L_m begins to resonate together with L_r and C_r, and the resonant angular frequency $\omega_m = \omega_r/\sqrt{m+1}$, where m denotes the inductor ratio, i.e., $m = L_m/L_r$. Since S_2 and S_4 keep conducting in this stage, boost inductors L_{b1} and L_{b2} are still being charged, and S_1 and S_3 are still being clamped by the bus voltage $V_{\rm bus}$. The secondary side, however, is disconnected from the primary side, and the latter no longer supply energy to the former. The further equivalent circuit of the resonant tank is shown in Fig. 4(c). The currents i_{L_r} and i_{L_m} and the voltage u_{C_r} can be obtained by

$$\begin{cases} i_{L_r}(t) = i_{L_r}(t_3)\cos(\omega_m(t-t_3)) \\ \qquad\quad -(u_{C_r}(t_3)/(Z_r\sqrt{1+m}))\sin(\omega_m(t-t_3)) \\ i_{Lm}(t) = i_{Lr}(t) \\ u_{C_r}(t) = u_{C_r}(t_3)\cos(\omega_m(t-t_3)) \\ \qquad\quad + i_{L_r}(t_3)Z_r\sqrt{1+m}\sin(\omega_m(t-t_3)). \end{cases} \tag{3}$$

Stage 5 [t_4, t_5] [see Fig. 3(e)]: At the moment of t_4, S_4 is turned off while S_2 keeps on conducting. During this dead-time interval, the resonant current i_{L_r} equals to the magnetizing current i_{L_m}, and the secondary diodes are in off state. The output (parasitic) capacitors of S_3 and S_4, i.e., $C_{\rm oss3}$ and $C_{\rm oss4}$ begin to, respectively, being discharged and charged with the combination of resonant current i_{L_r} (equals to the magnetizing current i_{L_m}) and the current $i_{L_{\rm b2}}$ flowing through L_{b2}. When the voltage across $C_{\rm oss3}$ declines to zero, the antiparallel body diode of S_3 starts conducting and ZVS turn-ON for switch S_3 can be achieved subsequently. And the turned-off switch S_4 begins to be clamped by the bus voltage $V_{\rm bus}$.

The operation principles for the next half switching cycle and the operation processes for the case $D > 0.5$ are similar with the aforementioned analysis and, therefore, are omitted in this paper.

III. Characteristic Analysis and Comparison

The equivalent circuit from the input to the bus is a two-phase interleaved boost converter and that from the bus to the load is a full-bridge *LLC* resonant converter. Therefore, the resulting equivalent circuit of the proposed current-fed IBI-LLC resonant converter is a cascaded circuit, where the two-phase interleaved boost converter and the full-bridge *LLC* converter are linked by the bus capacitor $C_{\rm bus}$, as shown in Fig. 5. Instead of two power conversion stages in the cascaded circuit, the power delivered from the input to the load will be processed only once in the proposed single-stage IBI-LLC converter topology, which means higher power conversion efficiency can be achieved.

A. Gain Characteristic

The gain of the boost circuit does not interact with that of the full-bridge *LLC* circuit; therefore, analyzing the two integrated circuits regarding gain characteristics separately is a simple and effective way to derive the overall gain characteristics of the IBI-LLC resonant converter.

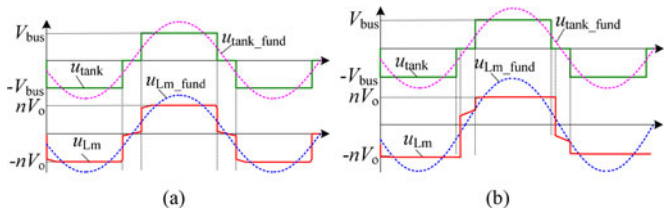


Fig. 6. Voltage waveforms of the resonant tank and the magnetizing inductor at (a) no load and (b) heavy load.

By imposing the volt-second balance rule on the boost inductor, the gain of the boost converter can be obtained

$$M_{\mathrm{Boost}} = \frac{V_{\mathrm{bus}}}{V_{\mathrm{in}}} = \frac{1}{D}. \tag{4}$$

As described in Section II, the two switching legs S_1, S_2, and S_3, S_4 are connected in parallel with the bus capacitor C_{bus}, the two switches of each switching leg operate in complementary manner, and all switches can achieve ZVS-ON. Thus, the voltage across a turned-off switch can be always clamped by the bus voltage V_{bus} owing to the on-state of the opposite switch in the same leg. According to (4), we can obtain the clamp voltage of primary-side turned-off switches with

$$V_{\mathrm{off\_clamp}} = V_{\mathrm{bus}} = \frac{V_{\mathrm{in}}}{D}. \tag{5}$$

Define the gain of the full-bridge *LLC* converter as $M_{LLC} = nV_o/V_{\mathrm{bus}}$ and then the gain of the IBI-LLC resonant converter can be calculated with

$$G = \frac{nV_o}{V_{\mathrm{in}}} = M_{LLC} M_{\mathrm{Boost}} = \frac{M_{LLC}}{D}. \tag{6}$$

1) First Harmonic Approximation: The fundamental components of magnetizing inductor voltage u_{L_m} and input resonant tank voltage u_{tank} are denoted as $u_{L_{m\_\mathrm{fund}}}$ and $u_{\mathrm{tank\_fund}}$, respectively. As analyzed previously, the input resonant tank voltage u_{tank} is a three-level ac rectangular waveform with duty cycle D or $1-D$. Therefore, the magnitude of $u_{\mathrm{tank\_fund}}$ is

$$V_{\mathrm{tank\_fund}} = \frac{4}{\pi} V_{\mathrm{bus}} \cos((0.5-D)\pi). \tag{7}$$

As shown in Fig. 6(a), when the converter operates at no load, the waveform of the magnetizing inductor voltage u_{L_m} has almost the same shape and duty cycle with the input resonant tank voltage u_{tank}, and therefore, it is easy to derive the magnitude of the fundamental component $u_{L_{m\_\mathrm{fund}}}$ by

$$V_{L_{m\_\mathrm{fund}}} = \frac{4}{\pi} nV_{\mathrm{o}} \cos((0.5-D)\pi). \tag{8}$$

Then, the dc voltage gain of the full-bridge *LLC* stage is

$$M_{LLC} = \frac{nV_o}{V_{\mathrm{bus}}} = \frac{V_{L_{m\_\mathrm{fund}}}}{V_{\mathrm{tank\_fund}}} = M_{\mathrm{ac}} \tag{9}$$

where M_{ac} is the ac gain of the full-bridge *LLC* stage. According to first harmonic approximation (FHA), the ac gain M_{ac} equals 1 when the switching frequency f_s is equal to the resonant frequency f_r [24]. As a result, the analytic dc voltage gain expression of the IBI-LLC resonant converter operating at no load can be obtained by

$$G = M_{LLC} M_{\mathrm{Boost}} = \frac{1}{D}. \tag{10}$$

For design convenience, (10) can be regarded as the no-load gain formula to facilitate the parameter design.

As the load become heavy, the waveform of u_{L_m} will distort a lot [see Fig. 6(b)], and thus, it is pretty difficult to obtain its fundamental component. As a result, FHA fails to accurately predict the gain characteristics of the IBI-LLC resonant converter at heavy load, and time-domain analysis must be conducted.

2) Time-Domain Analysis: The waveforms of resonant capacitor voltage u_{C_r}, resonant inductor current i_{L_r}, and magnetizing inductor current i_{L_m} all having half-wave symmetry, have the property

$$\begin{cases} i_{L_r}(t_0) = -i_{L_r}(t_5) \\ i_{L_r}(t_3) = i_{L_m}(t_3) \\ u_{C_r}(t_0) = -u_{C_r}(t_5). \end{cases} \tag{11}$$

Meanwhile, the average rectified output current is equal to the output current, i.e.

$$I_{\mathrm{rec}} = \frac{n}{t_5 - t_0} \int_{t_0}^{t_5} (i_{L_r}(t) - i_{L_m}(t))dt = \frac{V_o}{R_o}. \tag{12}$$

Define the quality factor by

$$Q = \frac{Z_r}{n^2 R_o}. \tag{13}$$

Ignoring the dead time, solve the equation group (1)–(3), (6), and (11)–(13) numerically, and the curves of dc voltage gain *G* versus duty cycle *D* for different quality factor *Q* or inductor ratio *m* can be obtained, as shown in Fig. 7. To verify the accuracy of the numerical calculation, the simulation results with the same parameters are depicted in Fig. 7(a) as well. As one can see, the numerical calculation results show a good agreement with the simulation results. Also, the no-load gain expression (10) is plotted in Fig. 7(a), and it coincides on the whole with simulation and numerical calculation results, only small error remains.

We can see from Fig. 7 that dc gain *G* decreases with respect to the increase of duty cycle *D*. Meanwhile, as the quality factor *Q* increases, gain *G* will get smaller. However, the inductor ratio *m* has little influence on the gain characteristics, as illustrated in Fig. 7(b), which is quite different from the conventional *LLC* resonant converter.

3) Comparative Analysis: Based on FHA, the dc gain of conventional PFM-controlled full-bridge *LLC* resonant converter can be obtained

$$G_{\mathrm{con}} = \frac{1}{\sqrt{[(f_n - 1/f_n)Q\pi^2/8]^2 + [(1-1/f_n^2)/m+1]^2}} \tag{14}$$

where the normalized switching frequency $f_n = f_s/f_r$.

According to (14), the gain curves of conventional PFM-controlled full-bridge *LLC* converter are plotted for different quality factor *Q* and inductor ratio *m*, as shown in Fig. 8. It is clear that the peak gain is strongly affected by both *Q* and *m*. In practical design, the full-load quality factor Q_{full} must be

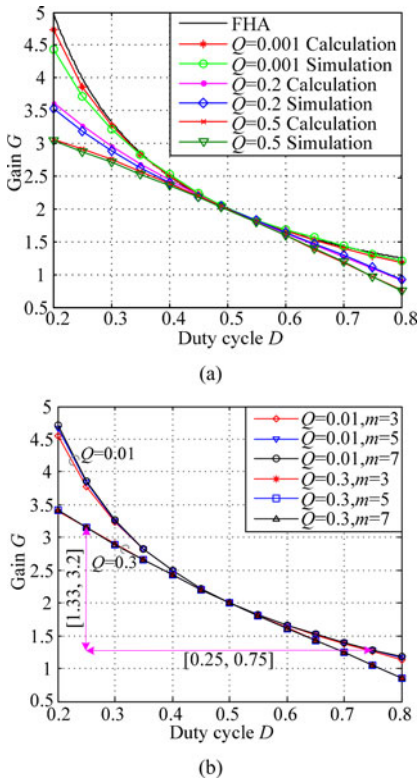


Fig. 7. Curves of dc voltage gain G versus duty cycle D: (a) calculated and simulated results with different quality factor Q; (b) calculated results with different inductor ratio m.

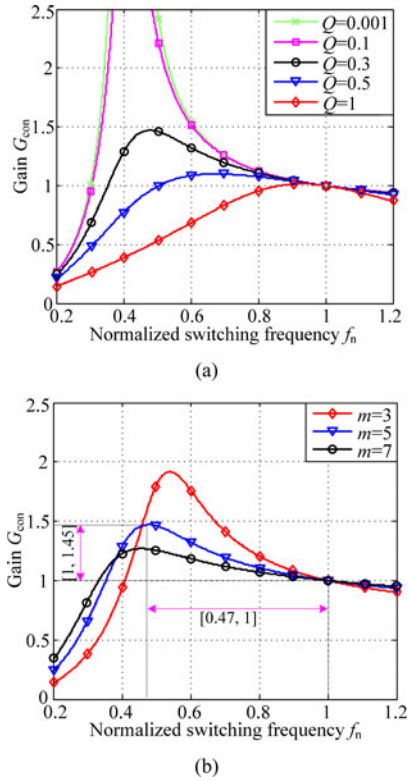


Fig. 8. Gain curves for conventional PFM-controlled full-bridge *LLC* converter with different (a) quality factors and (b) inductor ratios.

small enough to obtain a wide gain range over full-load variations. Small Q means small characteristic impedance Z_r. Thus, the resonant inductor L_r must be very small to keep the preset resonant frequency f_r unchanged. In order to minimize the circulating current and conduction loss, the magnetizing inductor L_m should increase, which indicates that the inductor ratio m will become larger as well. It can be obviously observed from Fig. 8(b) that the peak gain, however, will significantly decrease with the increased m. Then the required gain range may not be covered. Besides, the required switching frequency variations will have to be extended as well, which incurs some undesirable problems, such as increased transformer and inductor size, over large switching frequency variations. Therefore, the traditional *LLC* resonant converter is not suitable for wide input voltage range applications [17]–[18], [27]. By contrast, the gain characteristics of the proposed IBI-LLC resonant converter features fixed-frequency control, which is favorable for the design and optimization of magnetic elements and EMI filters. And from Fig. 7(b), we conclude that the gain is independent of inductor ratio m, which means the resonant inductor L_r and magnetizing inductor L_m can be, respectively, selected smaller and larger to obtain a wider gain range while maintaining low circulating current.

In addition, the gain curves of the proposed IBI-LLC and the conventional PFM-controlled full-bridge *LLC* with the same quality factor $Q = 0.3$ and inductor ratio $m = 5$ are depicted in Figs. 7(b) and 8(b), respectively. Within the duty cycle range [0.25, 0.75], a wide gain range [1.33, 3.2] (over twice) is achieved for the proposed IBI-LLC converter. However, the gain range of the conventional PFM-controlled *LLC* is [1, 1.45] within a wide normalized switching frequency range [0.46, 1]. As analyzed earlier, the proposed IBI-LLC resonant converter allows a smaller full-load quality factor while maintaining low power losses. Therefore, much wider gain range can be obtained for the proposed IBI-LLC converter in practice.

B. Input Current Ripple

As the proposed IBI-LLC converter features continuous current conduction, the input current ripple can be significantly reduced in comparison with voltage-fed converters [28]–[34]. And, due to the cancelation effect of each inductor current, the input current ripple can be further minimized. Thus, the inductor size can be reduced and the current root-mean-square (rms) stress on the input capacitor and bus capacitor can be alleviated, which is beneficial for power density improvement and reliability enhancement [35].

The current ripple of a single boost inductor current $i_{L_{b1,2}}$ is

$$\Delta i_{L_{b1,2}} = \frac{V_{in}(1-D)}{f_s L_{b1,2}}. \tag{15}$$

In comparison with $\Delta i_{L_{b1,2}}$, the current ripple of the sum of two boost inductor currents is significantly reduced with the two-phase interleaving operation of the integrated two boost circuits. Define the current ripple ratio of $\Delta i_{L_{bsum}}$ to $\Delta i_{L_{b1,2}}$ as λ, and (16) can illustrate how much the current ripple is

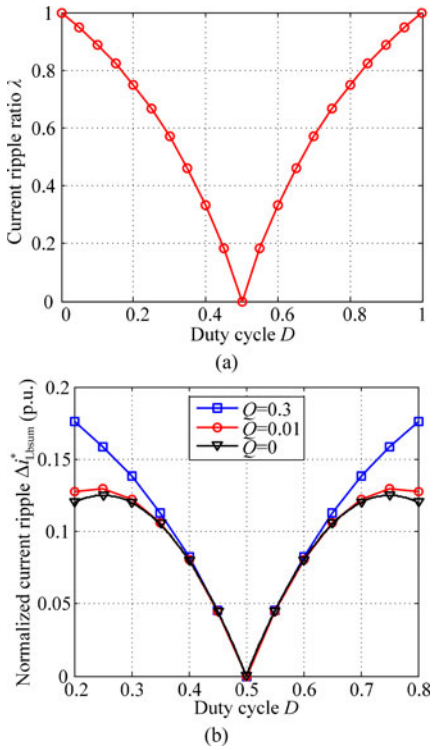


Fig. 9. Curves of (a) current ripple ratio λ versus duty cycle D and (b) normalized current ripple versus duty cycle D with different quality factors for the proposed IBI-LLC resonant converter.

minimized with two-phase interleaving

$$\lambda = \frac{\Delta i_{L_{bsum}}}{\Delta i_{L_{b1,2}}} = \begin{cases} \dfrac{1-2D}{1-D}, & D \le 0.5 \\ \dfrac{2D-1}{D}, & D > 0.5. \end{cases} \tag{16}$$

Fig. 9(a) depicts the curve of current ripple ratio λ versus duty cycle D for the proposed IBI-LLC resonant converter. As can be seen, the current ripple ratio λ decreases with respect to the convergence of duty cycle D to 0.5, which means that the effect of two-phase interleaving on reducing current ripple is more obvious. Particularly, when the duty cycle D is 0.5, a ripple-free input current can be achieved.

Substituting (15) into (16), we obtain the normalized current ripple of the sum of the two boost inductor currents $\Delta i^*_{L_{\rm bsum}}$

$$\Delta i^*_{L_{\rm bsum}} = \frac{\Delta i_{L_{\rm bsum}}}{nV_o/f_s L_{b1,2}} = \begin{cases} \dfrac{1-2D}{G}, & D \le 0.5 \\ \dfrac{(1-D)(2D-1)}{DG}, & D > 0.5. \end{cases} \tag{17}$$

Based on (17) and the numerically calculated gain G, the curves of normalized current ripple $\Delta i^*_{L_{\rm bsum}}$ versus duty cycle D for different quality factors can be plotted, as shown in Fig. 9(b). It reveals that the input current ripple is affected by both duty cycle D and quality factor Q (load). As duty cycle D converges to 0.5, the input current ripple will become smaller. Besides, when the load decreases, the input current ripple will get smaller as well. But this trend will go weak with the convergence of D to 0.5, due to the fact that the gain becomes more independent of load when D is closer to 0.5.

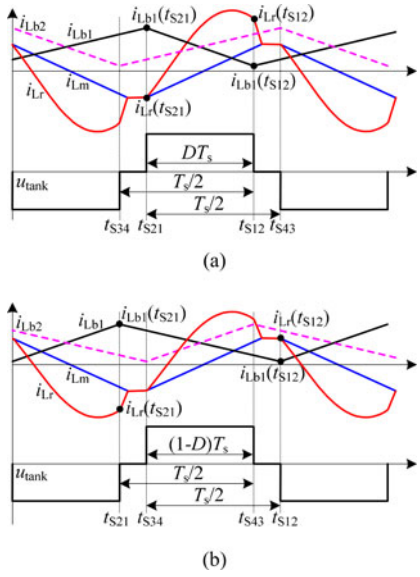


Fig. 10. Current comparison at four switching instants for (a) $D \le 0.5$ and (b) $D > 0.5$.

In practical applications, the increase of input current ripple requires a larger input capacitor to meet the strict current ripple requirements of renewable energy sources. Therefore, the input capacitor should be designed according to the worst input current ripple condition, where the maximum or minimum duty cycle is reached. In addition, to minimize the input current ripple of the IBI-LLC converter, the duty cycle D should be limited to a relatively small range around 0.5.

C. ZVS Analysis

The ZVS conditions of the proposed IBI-LLC resonant converter for $D < 0.5$ are different from those for $D > 0.5$. Therefore, they should be considered separately. Fig. 10 depicts the resonant tank voltage $u_{\rm tank}$, magnetizing inductor current i_{L_m}, and boost inductor currents $i_{L_{\rm b1}}$, $i_{L_{\rm b2}}$ for $D < 0.5$ and $D > 0.5$, taking no account of the dead time. Note that, being the boundary of the two considered cases, the case $D = 0.5$ can be included in either $D < 0.5$ or $D > 0.5$.

During a switching cycle, there are four switching commutation instants, namely $t_{S_{12}}$, $t_{S_{21}}$, $t_{S_{34}}$, $t_{S_{43}}$, which represent S_1 OFF to S_2 ON, S_2 OFF to S_1 ON, S_3 OFF to S_4 ON, and S_4 OFF to S_3 ON, respectively. Theoretically, to achieve ZVS in the four commutation instants, the currents should be satisfied with

$$i_{\rm ZVS}(t_{S_{21}}) = i_{L_r}(t_{S_{21}}) - i_{L_{\rm b1}}(t_{S_{21}}) < 0 \tag{18}$$

$$i_{\rm ZVS}(t_{S_{12}}) = i_{L_r}(t_{S_{12}}) - i_{L_{\rm b1}}(t_{S_{12}}) > 0 \tag{19}$$

$$i_{\rm ZVS}(t_{S_{34}}) = i_{L_r}(t_{S_{34}}) + i_{L_{\rm b2}}(t_{S_{34}}) < 0 \tag{20}$$

$$i_{\rm ZVS}(t_{S_{43}}) = i_{L_r}(t_{S_{43}}) + i_{L_{\rm b2}}(t_{S_{43}}) > 0. \tag{21}$$

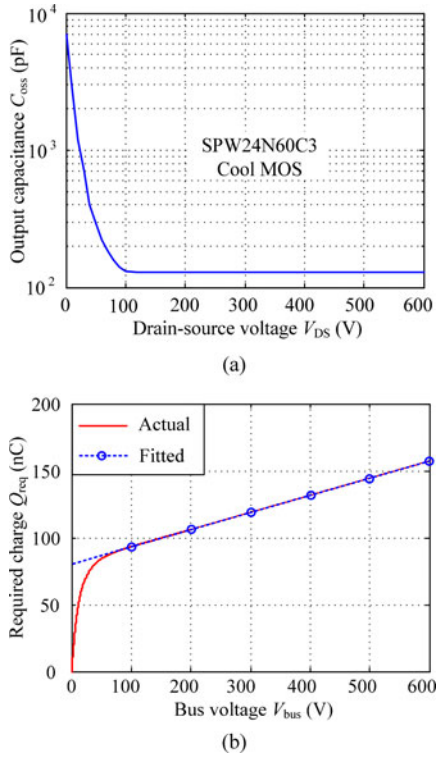


Fig. 11. Characteristics of (a) output capacitance $C_{\rm oss}$ versus drain–source voltage $V_{\rm DS}$ and (b) required charge $Q_{\rm req}$ versus bus voltage $V_{\rm bus}$, for power MOSFET SPWM24N60C3.

As the resonant current i_{L_r}, having half-wave symmetry, possesses the property $i_{L_r}(t) = -i_{L_r}(t + T_s/2)$, and the two interleaved boost inductor currents $i_{L_{b1}}$ and $i_{L_{b2}}$ satisfy $i_{L_{b1}}(t) = i_{L_{b2}}(t + T_s/2)$, (18)–(21) can be reduced to (18) and (19). As a result, only two switching commutation instants $t_{S_{12}}$ and $t_{S_{21}}$ remain, which represent the switching commutation instants of S_1 and S_2, as shown in Fig. 10. Obviously, $i_{L_r}(t_{S_{21}})$ is always less than 0 and $i_{L_{b1}}(t_{S_{21}})$ is always greater than 0. Thus, the ZVS current at $t_{S_{21}}$, i.e., $i_{\rm ZVS}(t_{S_{21}})$, is always less than 0. Accordingly, the final theoretical ZVS condition is (19).

In fact, when considering practical operation, enough charge must be charged or discharged to the output capacitor of MOSFET within the dead-time interval before the ZVS condition being created, as illustrated in Fig. 3. The required charge for a single MOSFET can be calculated by

$$Q_{\rm req} = \int_0^{V_{\rm bus}} C_{\rm oss}(V_{\rm ds})dV_{\rm ds} = \int_{V_{\rm bus}}^0 C_{\rm oss}(V_{\rm ds})dV_{\rm ds}. \quad (22)$$

The output capacitance $C_{\rm oss}$ is a nonlinear function of drain–source voltage $V_{\rm ds}$, especially for SuperJunction MOSFETs. Therefore, it is quite difficult to obtain the required charge $Q_{\rm req}$ directly. Drofenik *et al*. [36] propose a very effective numerical implementation method of nonlinear capacitance and applies it to the circuit simulator GeckoCIRCUITS [37], making it possible to obtain the accurate required charge $Q_{\rm req}$ for different bus voltage $V_{\rm bus}$ with the datasheet given by manufacturers.

Fig. 11(a) shows the curve of output capacitance $C_{\rm oss}$ versus drain–source voltage $V_{\rm DS}$ of SPW24N60C3, a CoolMOS of Infineon. The characteristic curve of required charge $Q_{\rm req}$ versus bus voltage $V_{\rm bus}$ can be obtained with circuit simulator GeckoCIRCUITS, as shown in Fig. 11(b). According to Fig. 11, when the bus voltage is greater than 100 V, the output capacitance will be nearly constant and the required charge $Q_{\rm req}$ will increase linearly with respect to the bus voltage $V_{\rm bus}$. With linear fit, the function of $Q_{\rm req}$ with respect to $V_{\rm bus}$ is found to be

$$Q_{\rm req} = 0.128V_{\rm bus} + 80.5({\rm nC}), V_{\rm bus} \in [100, 600]. \quad (23)$$

With (23), the required ZVS commutation charge for a single MOSFET can be easily and accurately obtained as long as $V_{\rm bus}$ is within 100–600 V.

Since the dead time is short and the commutation inductors are relatively large, it is justified to assume that the output capacitances are charged/discharged with constant current during the ZVS commutation time interval. The average commutation current during the dead-time interval can be calculated with

$$I_{\rm ZVS\_av} = \frac{2Q_{\rm req}(V_{\rm bus})}{t_{\rm dead}}. \quad (24)$$

The ZVS commutation currents are provided by the resonant tank together with the boost inductors, as illustrated with (18)–(21). Reducing the boost and magnetizing inductors leads to larger ZVS commutation currents during the dead-time interval, which is beneficial for the ZVS realization. However, conduction losses will increase correspondingly. Therefore, tradeoff must be made to achieve a better efficiency performance when designing the inductors.

D. Comparison

A comparison of four types of *LLC*-based converter topologies is illustrated in Table I.

As analyzed before, the main disadvantages of the voltage-fed full-bridge *LLC* converter are narrow gain range, large input current ripple, and over large frequency variations. On the other hand, it has been widely recognized that the conventional PFM-controlled *LLC* converter can achieve its optimal performance when the switching frequency f_s equals the resonant frequency f_r, where the circulating current is small and its gain is independent of load [24]. However, as the operating frequency diverges from the resonant frequency f_r, the amount of circulating energy increases. For a wide input voltage range, the efficiency curve of the conventional *LLC* converter may drop dramatically with respect to the significant decrease of the input voltage. As for the proposed IBI-LLC converter, its optimal operating condition occurs just at $D = 0.5$, where the circulating current is small, a ripple-free current ripple in the input can be achieved, and its gain is independent of load. This optimal operating point corresponds to the intermediate area of the whole allowed input voltage range. Therefore, its high efficiency and optimal operation performance can cover much wider input voltage range. Particularly, for the renewable energy sources, like photovoltaic and fuel cells, their maximum power points generally locate in the intermediate area of the allowed operating range, which matches the optimal operation area of the proposed IBI-LLC resonant converter pretty well.

TABLE I
COMPARISON OF FOUR TYPES OF *LLC*-BASED CONVERTER TOPOLOGIES

Topologies	Full-Bridge *LLC* Converter	Boost-Cascaded Half-Bridge *LLC* Converter [25]	Interleaved-Boost-Cascaded Full-Bridge *LLC* Converter [26]	Proposed IBI-LLC converter
Number of switches	4	3	6	4
Number of diodes (with center-tapped rectifier)	2	3	4	2
Number of inductors	1	2	3	3
Input current ripple	Large	Moderate	Small	Small
Input capacitor	Bulky	Moderate	Small	Small
Bus capacitor	—	Bulky	Small	Small
Soft switching	Primary switches: ZVS Secondary diodes: ZCS	Boost stage: hard-switching *LLC* stage: ZVS, ZCS	Boost stage: hard-switching *LLC* stage: ZVS, ZCS	Primary switches: ZVS secondary diodes: ZCS
Modulation	PFM	Boost stage: PWM *LLC* stage: unregulated	Boost stage: PWM *LLC* stage: PFM	PWM
Gain range	Narrow	Wide	Wide	Wide

Lee *et al*. [25] and Wang *et al*. [26], respectively, propose a boost-cascaded half-bridge *LLC* converter and a interleaved-boost-cascaded full-bridge *LLC* converter, where the gain range is extended and the input current ripple is minimized as well. The boost-cascaded half-bridge *LLC* converter features fewer components, but it has larger input current ripple, bulkier input and bus capacitors in comparison with the interleaved-boost-cascaded full-bridge *LLC* converter. Disadvantageously, in the two cascade converters [25], [26], the boost-stage switches and diodes operate with hard switching, leading to increased switching losses, degraded EMI, and decreased switching frequency (increased size). By contrast, the proposed IBI-LLC resonant converter has fewer components than the interleaved-boost-cascaded full-bridge *LLC* converter, and reduced input current ripple, and input and bus capacitors than the boost-cascaded half-bridge *LLC* converter. Most importantly, in the proposed IBI-LLC converter, all switches and diodes operate in soft switching manner and the energy from the input to the output is processed only once. Thus, fewer power losses, better EMI, and high power conversion efficiency can be achieved.

IV. PARAMETER DESIGN AND TOPOLOGY EXTENSION

As analyzed before, the gain characteristics of the IBI-LLC resonant converter are dominated by resonant inductor L_r and resonant capacitor C_r, while the ZVS conditions are mainly afffected by boost inductors L_{b1}, L_{b2} and magnetizing inductor L_m. Therefore, the selection of L_r and C_r should follow the gain range requirment and the designs of L_{b1}, L_{b2}, and L_m are ruled by the achievment of ZVS over the entire input voltage range and full-load range.

A. Resonant Parameters

As the duty cycle D deviates from 0.5, the reactive circulating current will increase, degrading the efficiency performance of the IBI-LLC resonant converter. Therefore, the duty cycle range is limited within $[D_{\min}, D_{\max}]$, where $D_{\min}$ and $D_{\max}$ represent the maximum duty cycle and the minimum duty cycle, respectively.

To meet the operation requirements for the given specifactions, the gain range should be satisfied from no load to full load within the duty cycle limit $[D_{\min}, D_{\max}]$. According to the gain characteristic curves shown in Fig. 12, the critical design points are the maximum duty cycle at no load and the minimum duty cycle at full load, which are represented with $A(D_{\max}, G_{\min})$ and $B(D_{\min}, G_{\max})$, respectivly.

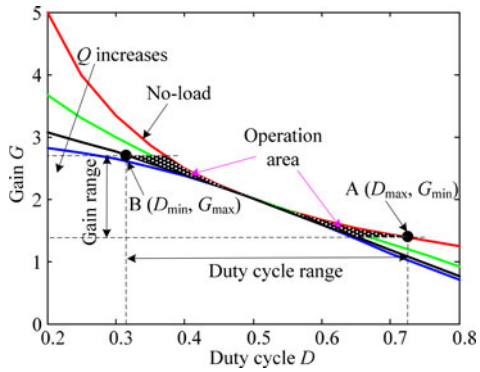


Fig. 12. Operation boundary and area for gain range requirement.

Based on the no-load gain expression (10), the gain at point A is

$$G_{\min} = \frac{1}{D_{\max}}. \tag{25}$$

Then the transformer turns ratio n can be obtained with

$$n = \frac{G_{\min} V_{\text{in\_max}}}{V_{\text{o}}} \tag{26}$$

where $V_{\text{in\_max}}$ is the maximum input voltage. The maximum gain $G_{\max}$ can be calculated with

$$G_{\max} = \frac{V_{\text{in\_max}} G_{\min}}{V_{\text{in\_min}}} \tag{27}$$

where $V_{\text{in\_min}}$ is the minimum input voltage. With the known points $A(D_{\max}, G_{\min})$ and $B(D_{\min}, G_{\max})$, the full-load quality factor Q_{full} can be derived with numerical calculation. Combing with the resonent frequency f_s, the critical resosnant parameters, i.e., the maximum resonant inductor $L_{r\_\max}$ and minimum resonant capacitor $C_{r\_\min}$ can be obatined.

In fact, as the characteristic impedance $Z_r = \sqrt{L_r/C_r}$ decreases, the operation area will become smaller, as shown in Fig. 12. Thus, the required duty cycle variations for both input

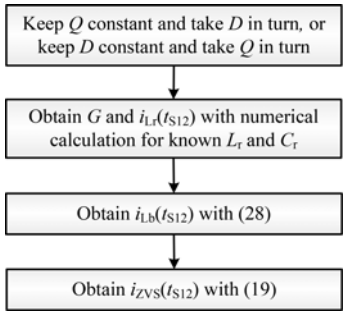


Fig. 13. Flowchart for deriving the ZVS commutation current $i_{\mathrm{ZVS}}(t_{S_{12}})$.

voltage and output load regulations will be narrowed and close to $D = 0.5$, which is beneficial for improving the efficiency and dynamic performances. Also, for the preset resonant frequency f_r, the product of L_r and C_r is constant. Thus, smaller Z_r means larger C_r and lower peak voltage stress across the resonant capacitor C_r, as demonstrated in (1)–(3). However, extremely small characteristic impedance Z_r will, in turn, result in overlarge output current in the short-circuit condition [16], [26]. Therefore, this tradeoff must be considered in practical design.

B. Magnetizing Inductor and Boost Inductors

To guarantee ZVS operation over the entire input voltage range and full-load range, it is necessary to find out the worst ZVS operating point, which could guide the design of the boost inductors L_{b1}, L_{b2}, and the magnetizing inductor L_m. As analyzed in Section III, the worst ZVS condition is at time instant $t_{S_{12}}$. Therefore, the worst ZVS operating point is the case where the ZVS commutation current $i_{\mathrm{ZVS}}(t_{S_{12}})$ has the minimum value. The flowchart of calculating the ZVS commutation current $i_{\mathrm{ZVS}}(t_{S_{12}})$ for different quality factor *Q* or duty cycle *D* is shown in Fig. 13.

Step 1: After finishing the selection of resonant parameters, the resonant current at $t_{S_{12}}$, i.e., $i_{L_r}(t_{S_{12}})$, can be derived with numerical calculation for different combinations of quality factor *Q* and duty cycle *D*.

Step 2: Based on the known *D*, *Q*, and derived gain *G*, the boost inductor current at time instant $t_{S_{12}}$ can be calculated with

$$i_{L_{b1}}(t_{S_{12}}) = \frac{GI_o}{2n} - \frac{(1-D)nV_o}{2Gkf_sL_r} \tag{28}$$

where *k* is the ratio of boost inductor to resonant inductor, i.e., $k = L_{b1}/L_r = L_{b2}/L_r$.

Step 3: The ZVS current at $t_{S_{12}}$, i.e., $i_{\mathrm{ZVS}}(t_{S_{12}})$, for different *Q* and duty cycle *D* can be derived with (19).

Fig. 14(a) depicts the curves of $i_{L_r}(t_{S_{12}})$ with respect to *D* at full load, and it shows that $i_{L_r}(t_{S_{12}})$ becomes smaller as duty cycle *D* increases. The curves of $i_{\mathrm{ZVS}}(t_{S_{12}})$ versus output current I_o for $D = 0.4$ and $D = 0.6$ are shown in Fig. 14(b) and (c), respectively. Obviously, $i_{\mathrm{ZVS}}(t_{S_{12}})$ decreases with respect to I_o and the trend hold for any combination of inductor ratios *m* and *k*. By comprehensively analyzing Fig. 14(a)–(c), one can conclude that the worst ZVS condition occurs when the converter operates at the maximum input voltage and full load.

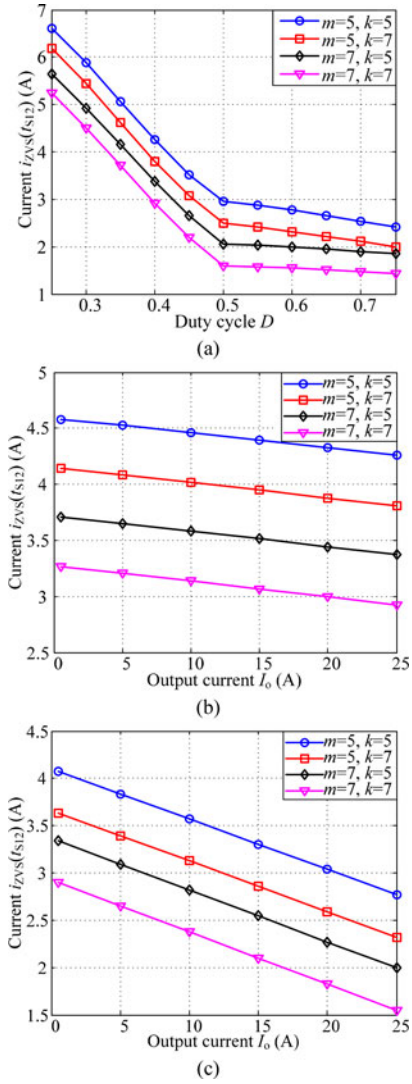


Fig. 14. Curves of ZVS current $i_{\mathrm{ZVS}}(t_{S_{12}})$ with respect to (a) duty cycle *D* at full load, (b) output current I_o for $D = 0.4$, and (c) output current I_o for $D = 0.6$.

Therefore, the boost inductors and the magnetizing inductor should be designed according to this worst operating point in order to maintain ZVS over the entire operation range.

C. Topology Extension

Based on the proposed IBI-LLC resonant converter, a family of interleaved boost integrated (IBI) resonant converter topologies can be generalized and derived, as shown in Fig. 15(a). Ports A, B, and C can be connected with dc source, capacitor, or load, and thus two-port dc–dc converters or three-port dc–dc converters can be formed. For the passive network D, it is justified to be placed with an *LC*, *LLC*, or *LCC* network, and thus, different types of resonant converters can be derived. Full-bridge rectifier, full-wave rectifier, current-doubler rectifier, or even active full-bridge and half-bridge may be inserted into E to derive unidirectional or bidirectional converters according to practical requirements.

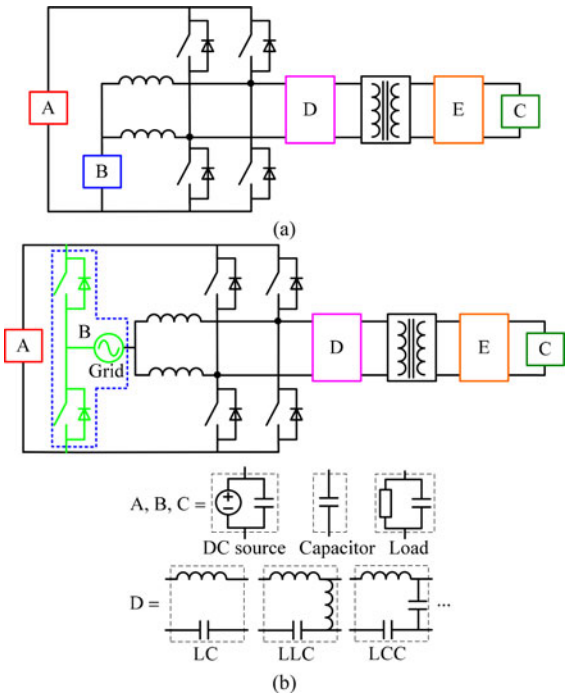


Fig. 15. Generalized topologies of two kinds of IBI resonant converters. (a) DC–DC converter; (b) grid-connected ac–dc converter.

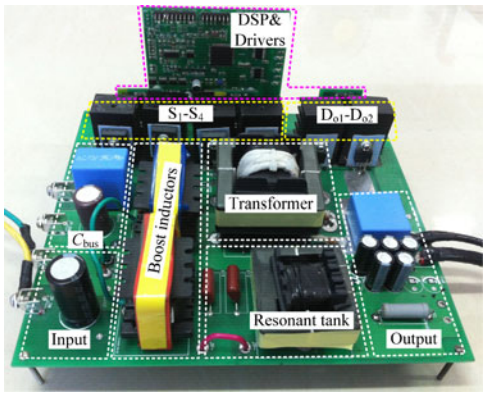


Fig. 16. Laboratory prototype.

By adding a half bridge operating at line frequency, a kind of grid-connected IBI resonant converter topologies for either two-port or three-port power conversion, and either unidirectional or bidirectional power flow can be derived, as shown in Fig. 15(b). It is noted that the two boost inductors can also be implemented with coupled inductors to minimize size and improve operation performance.

V. Experimental Results

A 600-W laboratory prototype, as shown in Fig. 16, has been built based on the design procedures presented in the paper. The specifications of the converter prototype are as follows: input voltage $V_{\rm in} = 120$–240 V, output voltage $V_o = 24$ V, rated output power $P_o = 600$ W, switching frequency $f_s = 100$ kHz, and *LC* serial resonant frequency $f_r = 100$ kHz. Details of the developed experimental converter prototype are listed in Table II. Gating signals for the devices are generated using a Texas Instruments TMS320F28016 DSP board. Two IR2110 are used to drive the primary-side MOSFETs and one IR2110 are used to drive the secondary-side synchronous rectification MOSFETs. A single output voltage closed loop is used to regulate the output voltage V_o regardless of wide input voltage range and full-load range.

TABLE II
Major Components' Parameters of the Experimental Prototype

Components	Parameters
Primary switches S_1–S_4	SPW24N60C3, 650 V, 24 A, $R_{\rm ds,on} = 0.16\Omega$
Secondary rectification switches D_{o1}–D_{o2}	IPP04CN10N, 100 V, 100 A, $R_{\rm ds,on} = 3.9$ mΩ
High-frequency transformer T	PC40EE55 ferrite core, primary turns $N_1 = 27$, secondary turns $N_2 = N_3 = 2$, magnetizing inductance $L_m = 370\ \mu$H, leakage inductance reflected to the primary side $L_k = 4.2\ \mu$H
Input boost inductors L_{b1}, L_{b2}	PC40EE50 ferrite core, turns $N = 29$, $L_{b1} = L_{b2} = 300\ \mu$H
External series inductor L_s	PC40EE50, ferrite core, turns $N = 10$, $L_s = 46.5\ \mu$H
Resonant inductance L_r	$L_r = L_k + L_s = 50.7\ \mu$H
Resonant capacitor C_r	2×100 nF in series, CBB capacitor, $C_r = 50$ nF
Input capacitor $C_{\rm in}$	$100\ \mu$F, 450 V electrolytic capacitor
Bus capacitor $C_{\rm bus}$	$47\ \mu$F, 450 V electrolytic capacitor 1 μF, high-frequency film capacitor
Output capacitor C_o	$5 \times 680\ \mu$F in parallel, 35 V, electrolytic capacitor 2.2 μF, high-frequency film capacitor

The steady-state operation waveforms at full load with different input voltages are shown in Fig. 17(a)–(c). As can be seen, over a wide input voltage range of 120–240 V, the proposed IBI-LLC resonant converter operates pretty well with the fixed-frequency PWM control. When $D \le 0.5$, the resonant tank voltage $u_{\rm tank}$ shares the same duty cycle D with the upper switches S_1 and S_3. But in the case of $D > 0.5$, the duty cycle of $u_{\rm tank}$ is equal to 1–D. This is in consistent with previous analysis. For the input voltage range of 120–240 V, the regulated duty cycle range of the converter at full load is 0.34–0.67, which is close to 0.5. Thus, the circulating current is small, leading to minimized conduction losses. Also, the ringing-free current and voltage waveforms significantly reduce the EMI in the circuit.

The two boost inductor currents $i_{L_{\rm b1}}$ and $i_{L_{\rm b2}}$ are almost even shared. In fact, the current distribution between two boost inductors depends on the parameters of inductors and semiconductors. Though the current ripple of a single phase boost inductor is relatively large, the ripple of the sum of two interleaved inductor currents is greatly reduced. For example, in Fig. 17(a), the ripple amplitude of $i_{L_{\rm b1,2}}$ is 2.65 A, while that of $i_{L_{\rm bsum}}$ is only 1.29 A, which matches well with (16). As for Fig. 17(b), the duty cycle $D = 0.5$, and an almost ripple-free input current is obtained. Therefore, it is a good candidate for REG systems, which usually require both wide input voltage range and low input current ripple.

As analyzed in Section III, for the fixed-frequency PWM-controlled IBI-LLC resonant converter, the ZVS operation performance of the right leg (S_3 and S_4) is the same with that of the left leg (S_1 and S_2), due to the symmetry of topology and

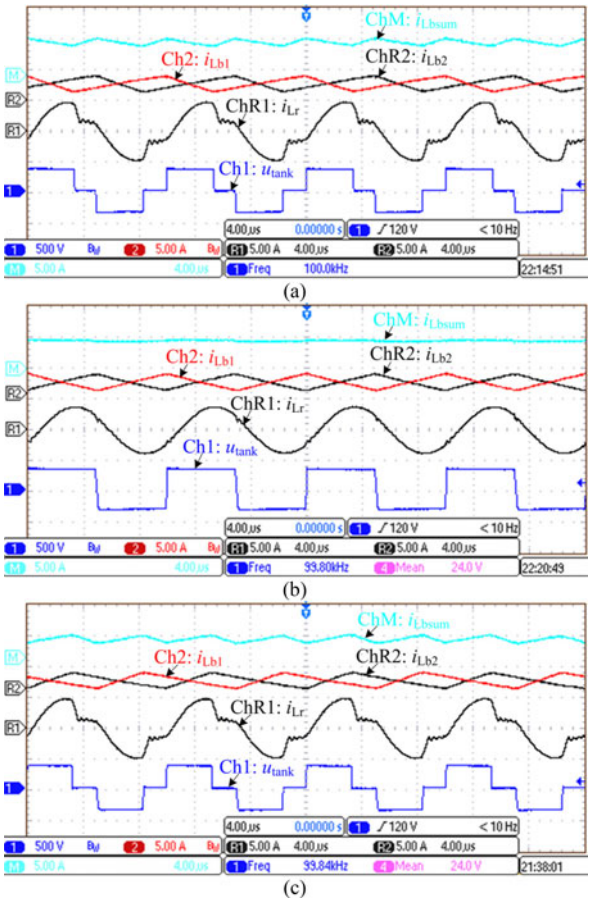


Fig. 17. Experimental steady-state voltage and current waveforms at full load for different input voltages: (a) $V_{\rm in} = 120$ V; (b) $V_{\rm in} = 162$ V; (c) $V_{\rm in} = 240$ V.

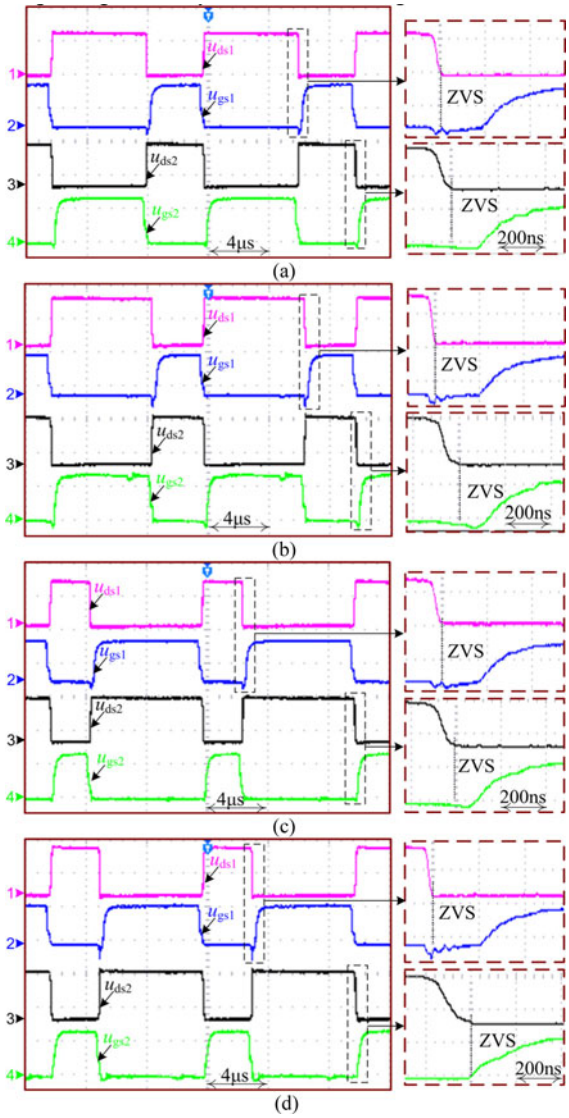


Fig. 18. ZVS-ON waveforms of S_1 and S_2 (Ch1: $u_{\rm ds1}$, 250 V/div; Ch2: $u_{\rm gs1}$, 10 V/div; Ch3: $u_{\rm ds2}$, 250 V/div; Ch4: $u_{\rm gs2}$, 10 V/div). (a) $V_{\rm in} = 120$ V, $P_o = 60$ W; (b) $V_{\rm in} = 120$ V, $P_o = 600$ W; (c) $V_{\rm in} = 240$ V, $P_o = 60$ W; (d) $V_{\rm in} = 240$ V, $P_o = 600$ W.

modulation. Therefore, only the ZVS waveforms of S_1 and S_2 are shown in this paper. Fig. 18(a) and (b) presents the drain–source voltage and gate driving signal waveforms of S_1 and S_2 with 120 V input at 10% load and full load. As can be seen, at both full load and very light load, drain–source voltages $V_{\rm ds1}$ and $V_{\rm ds2}$ decrease to 0 before the concerned gate signals $V_{\rm gs1}$ and $V_{\rm gs2}$ come, which means that ZVS turn-ON of S_1 and S_2 is achieved. The ZVS turn-ON waveforms with 240 V input at 10% load and full load are presented in Fig. 18(c) and (d), respectively. One can see that S_1 can achieve ZVS easily over the full-load range. As for S_2, its ZVS condition becomes harsher with respect to the increase of load. In Fig. 18(d), the gate driving signal $u_{\rm gs2}$ occurs just when the drain–source voltage $u_{\rm ds2}$ falls near to 0, which means that power switch S_2 operates in the critical ZVS-ON manner at this operating point, where the input voltage $V_{\rm in} = 240$ V, and the output power $P_o = 600$ W (full load). This coincides pretty well with the worst ZVS condition analysis conducted in Section IV. Thus, we can conclude that all primary power switches operate in ZVS manner over the full input voltage and output load ranges, resulting in significantly reduced switching losses and EMI.

On the other hand, we can also see from Fig. 18 that the voltage across the primary switches at turn off can be always clamped by the bus voltage $V_{\rm bus}$ ($V_{\rm bus} = V_{\rm in}/D$), regardless of input voltage and output load, Thus, voltage spike across MOSFETs is well eliminated and reliable operation can be ensured. This verifies the switch voltage stress analysis in Section III.

To verify the dynamic performance regarding load variations, Fig. 19(a) presents the dynamic responses of the fixed-frequency PWM-controlled IBI-LLC resonant converter with 200 V input as load steps up from 2.5 to 25 A, while Fig. 19(b) shows the corresponding step-down responses. As one can see, when a step load variation occurs, both the boost inductor currents and the resonant current response fast and the output voltage V_o can be tightly regulated to 24 V. The output voltage overshoot and undershoot are about 2 V, which is less than 10% $\times$24 V. At the same time, the two boost inductor currents $i_{L_{\rm b1}}$ and $i_{L_{\rm b2}}$ are always even shared both in steady states and in transients. Note that, the bus voltage $V_{\rm bus}$ will change about 20 V due to

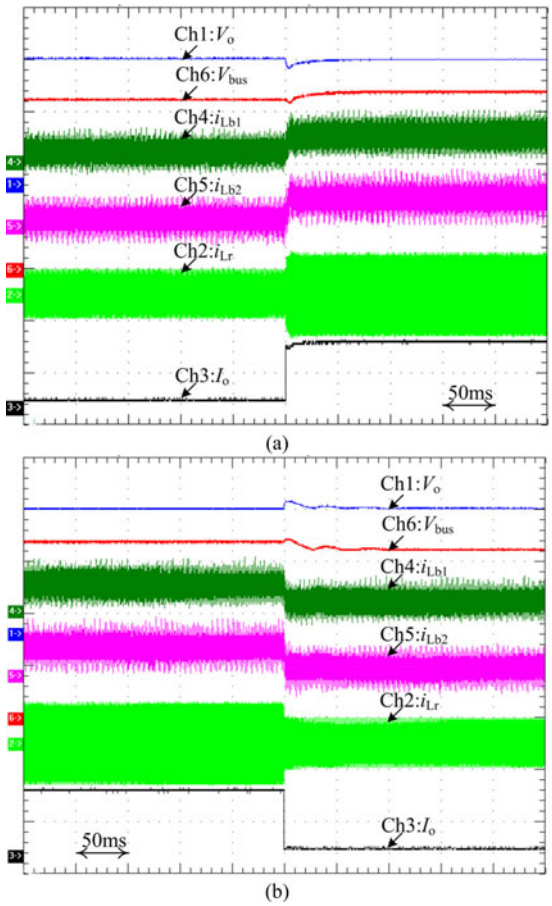


Fig. 19. Experimental results of the IBI-LLC resonant converter with closed-loop control in response to step changes in the load (Ch1: V_o, 10 V/div; Ch2: i_{L_r}, 5 A/div; Ch3: I_o, 20 A/div; Ch4: $i_{L_{b1}}$, 5 A/div; Ch5: $i_{L_{b2}}$, 5 A/div; Ch6: $V_{\rm bus}$, 100 V/div). (a) Step increase of load from 2.5 to 25 A. (b) Step decrease of load from 25 to 2.5 A.

the change of duty cycle *D*, which is used to regulate the output voltage for load variations.

Experimental full-load waveforms in response to a ramp increase of input voltage $V_{\rm in}$ from 130 to 230 V are presented in Fig. 20(a), and those responding to a ramp decrease of $V_{\rm in}$ from 230 to 130 V are shown in Fig. 20(b). As can be seen, the output voltage V_o can be regulated to 24 V quickly after the input voltage changes, and the overshoot and undershoot for both the output voltage V_o and the bus voltage $V_{\rm bus}$ are small. Thus, good dynamic performance with respect to input voltage variations is achieved for the IBI-LLC resonant converter with closed-loop control.

The calculated and experimental curves of duty cycle *D* versus input voltage $V_{\rm in}$ for full load and half load are plotted in Fig. 21(a). As can be seen, there is a slight difference between the theoretical and experimental results, which demonstrates the effectiveness of theoretical gain calculation. To make sure of reliable operation, the bus voltage should be limited within a reasonable range. Fig. 21(b) presents the measured and calculated curves of steady-state average bus voltage $V_{\rm bus}$ versus input voltage $V_{\rm in}$ at different loads. One can see that for the input voltage rang of 120–240 V, the bus voltage fluctuates

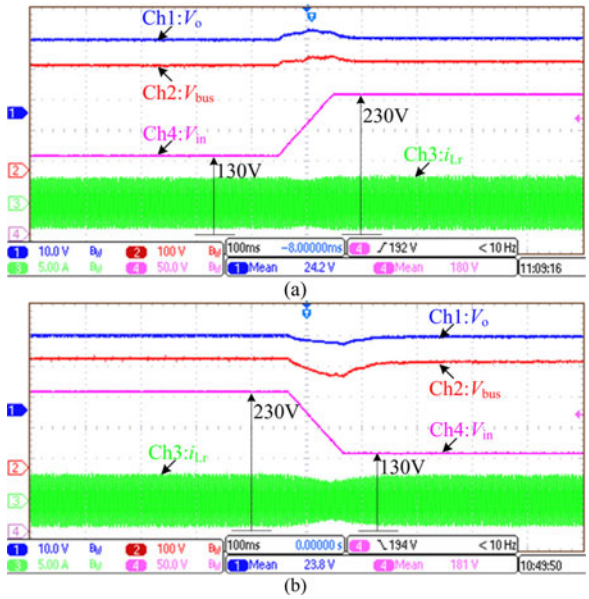


Fig. 20. Experimental results of the IBI-LLC resonant converter with closed-loop control in response to ramp changes in the input voltage $V_{\rm in}$. (a) Ramp increase of the input voltage $V_{\rm in}$ from 130 to 230 V. (b) Ramp decrease of the input voltage from 230 to 130 V.

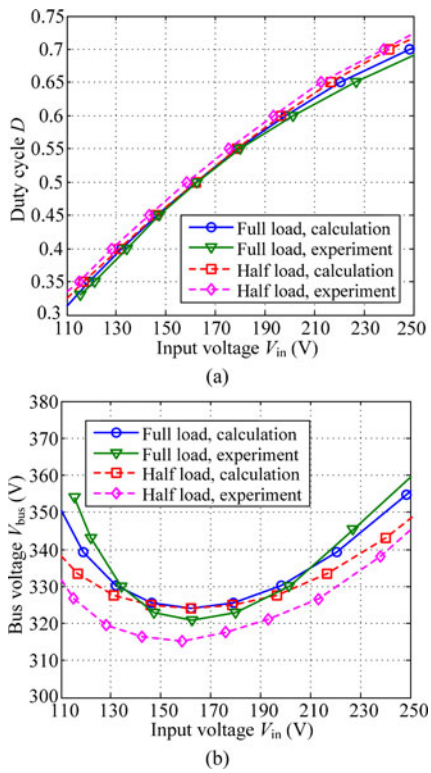


Fig. 21. Measured gain and bus voltage characteristics for different load conditions. (a) Curves of experimental and theoretical curves of duty cycle *D* versus input voltage $V_{\rm in}$. (b) Curves of bus voltage $V_{\rm bus}$ versus input voltage $V_{\rm in}$.

within a narrow range, from 315 to 355 V, which can guarantee the reliable operation of primary-side power switches (650 V MOSFET). In addition, we also notice that there is a slight voltage deviation between the theoretical and experimental results. It may be caused by the parasitic parameters (such as

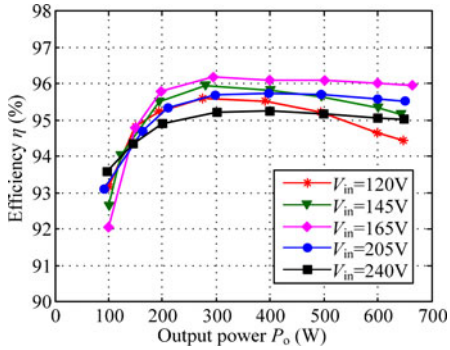


Fig. 22. Measured curves of efficiency η versus output power P_o for different input voltage conditions.

secondary-side parasitic inductance, parasitic capacitance of transformer windings, synchronous rectifier MOSFETs, etc.) and measurement error. However, the voltage deviation ($\leq$10 V) is relatively small in comparison with the bus voltage ($\geq$315 V) and therefore can be neglected to some extent.

Fig. 22 depicts the tested prototype efficiency curves with respect to output power for different input voltages. As can be seen, the IBI-LLC resonant converter operates with high efficiency over the whole input voltage range and wide load range.

VI. Conclusion

In this paper, a novel IBI-LLC resonant converter is proposed and explored. By incorporating a two-phase interleaved boost circuit into the full-bridge *LLC* resonant converter, the gain range is extended and the input current ripple is reduced as well. Fixed-frequency PWM control is adopted so as to simplify the design and optimization of magnetic elements and passive filters. Also, the magnetizing inductor and boost inductors have little impact on the gain curves, which is favorable for parameter design and efficiency improvement. The worst ZVS conditions occur when the IBI-LLC resonant converter operates with the maximum input voltage at full load. With proper design, all primary power switches operate with ZVS ON and all secondary rectifier diodes turn off under ZCS over full operating range, leading to reduced switching losses. Good dynamic performance regarding input voltage changes and load variations is achieved with closed-loop control. High power conversion efficiency is obtained for wide input voltage and load ranges. Therefore, the proposed IBI-LLC converter is a good candidate for interfacing with renewable energy sources. In addition, based on the proposed IBI-LLC resonant converter, two kinds of IBI resonant converter topologies are generalized and derived for REG applications.

References

[1] J. M. Carrasco, L. G. Franquelo, and J. T. Bialasiewicz, "Power electronic systems for the grid integration of renewable energy sources: A survey," *IEEE Trans. Power Electron.*, vol. 53, no. 4, pp. l002–1016, Aug. 2006.

[2] Y. Chuang, Y. Ke, H. Chuang, and Y. Wang, "A novel single-switch resonant power converter for renewable energy generation applications," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1322–1330, Mar./Apr. 2014.

[3] S. K. Majumder, R. K. Burra, and K. Acharya, "A ripple-mitigating and energy-efficient fuel cell power-conditioning system," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1437–1452, Jul. 2007.

[4] C. N. M. Ho, H. Breuninger, S. Patterson, G. Escobar, L. A. Serpa, and A. Coccia, "Practical design and implementation procedure of an interleaved boost converter using SiC diodes for PV applications," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2835–2845, Jun. 2012.

[5] P.-W. Lee, Y.-S. Lee, D. Cheng, and X. Liu, "Steady-state analysis of an interleaved boost converter with coupled inductors," *IEEE Trans. Ind. Electron.*, vol. 47, no. 4, pp. 787–795, Aug. 2000.

[6] U. R. Prasanna and A. K. Rathore, "Analysis, design, and experimental results of a novel soft-switching snubberless current-fed half-bridge frontend converter-based PV inverter," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3219–3230, Jul. 2013.

[7] Y. Gu, Z. Lu, L. Hang, Z. Qian, and G. Huang, "Three-level *LLC* series resonant DC/DC converter," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 781–789, Jul. 2005.

[8] W. Feng, F. C. Lee, and P. Mattavelli, "Simplified optimal trajectory control (SOTC) for *LLC* resonant converters," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2415–2426, May 2013.

[9] X. Fang, H. Hu, J. Shen, and I. Batarseh, "Efficiency-oriented optimal design of the *LLC* resonant converter based on peak gain placement," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2285–2296, May 2013.

[10] Z. Hu, Y. Qiu, Y.-F. Liu, and P. C. Sen, "A control strategy and design method for interleaved *LLC* converters operating at variable switching frequency," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4426–4437, Aug. 2014.

[11] D. Huang, S. Ji, and F. C. Lee, "*LLC* resonant converter with matrix transformer," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4339–4347, Aug. 2014.

[12] D. Wang and Y.-F. Liu, "A zero-crossing noise filter for driving synchronous rectifiers of *LLC* resonant converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1953–1965, Apr. 2014.

[13] W. Feng, F. C. Lee, and P. Mattavelli, "Optimal trajectory control of burst mode for LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 457–466, Jan. 2013.

[14] R. Beiranvand, B. Rashidian, M. R. Zolghadri, and S. M. H. Alavi, "Using *LLC* resonant converter for designing wide-range voltage source," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1746–1756, May 2011.

[15] R. Beiranvand, B. Rashidian, M. R. Zolghadri, and S. M. H. Alavi, "Optimizing the normalized dead-time and maximum switching frequency of a wide-adjustable-range *LLC* resonant converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 462–472, Feb. 2011.

[16] F. Musavi, M. Craciun, D. S. Gautam, W. Eberle, and W. G. Dunford, "An *LLC* resonant DC–DC converter for wide output voltage range battery charging applications," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5437–5445, Dec. 2013.

[17] K. H. Yi and G. W. Moon, "Novel two-phase interleaved *LLC* series-resonant converter using a phase of the resonant capacitor," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1815–1819, May 2009.

[18] K. Jin and X. Ruan, "Hybrid full-bridge three-level *LLC* resonant converter-a novel DC–DC converter suitable for fuel-cell power system," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1492–1503, Oct. 2006.

[19] R. Beiranvand, M. R. Zolghadri, B. Rashidian, and S. M. H. Alavi, "Optimizing the *LLC-LC* resonant converter topology for wide-output voltage and wide-output load applications," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3192–3204, Nov. 2011.

[20] Z. Liang, R. Guo, G. Wang, and A. Huang, "A new wide input range high efficiency photovoltaic inverter," in *Proc. IEEE Energy Convers. Congr. Expos.*, 2010, pp. 2937–2943.

[21] H. Hu, X. Fang, F. Chen, Z. J. Shen, and I. Batarseh, "A modified high-efficiency *LLC* converter with two transformers for wide input-voltage range applications," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1946–1960, Apr. 2013.

[22] I. O. Lee and G. W. Moon, "Analysis and design of a three-level *LLC* series resonant converter for high- and wide-input-voltage applications," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2966–2979, Jun. 2012.

[23] H. Y. Kwang, J. N. Young, and S. Phum, "*LLC* resonant converter with wide input voltage and load range at a fixed switching frequency," in *Proc. IEEE Power Eletron. Conf. Expo.*, 2012, pp. 1338–1342.

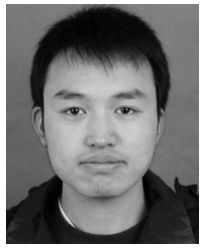
[24] X. Fang, H. Hu, Z. J. Shen, and I. Batarseh, "Operation mode analysis and peak gain approximation of the *LLC* resonant converter," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1985–1995, Apr. 2012.

[25] J.-Y. Lee, Y.-S. Jeong, and B.-M. Han, "An isolated DC/DC converter using high-frequency unregulated *LLC* resonant converter for fuel cell

applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2926–2934, Jul. 2011.
[26] H. Wang, S. Dusmez, and A. Khaligh, "Design and analysis of a full bridge *LLC* based PEV charger optimized for wide battery voltage range," *IEEE Trans. Veh. Technol.*, vol. 63, no. 4, pp. 1603–1613, Apr. 2014.
[27] T. LaBella, W. Yu, J.-S. Lai, M. Senesky, and D. Anderson, "A bidirectional-switch-based wide-input range high-efficiency isolated resonant converter for photovoltaic applications," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3473–3484, Jul. 2014.
[28] X. Pan and A. K. Rathore, "Current-fed soft-switching push–pull front-end converter-based bidirectional inverter for residential photovoltaic power system," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 6041–6051, Nov. 2014.
[29] W. Song and B. Lehman, "Current-fed dual-bridge DC–DC converter," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 461–469, Mar. 2007.
[30] S. K. Han, H. K. Yoon, G. W. Moon, M. J. Youn, Y. H. Kim, and K. H. Lee, "A new active clamping zero-voltage switching PWM current-fed half bridge converter," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1271–1279, Nov. 2005.
[31] S. J. Jang, C. Y. Won, B. K. Lee, and J. Hur, "Fuel cell generation system with a new active clamping current-fed half-bridge converter," *IEEE Trans. Energy Convers.*, vol. 22, no. 2, pp. 332–340, Jun. 2007.
[32] A. K. Rathore, "Interleaved soft-switched active-clamped L-L type current-fed half-bridge dc–dc converter," *Int. J. Hydrogen Energy*, vol. 34, no. 24, pp. 9802–9815, Dec. 2009.
[33] A. K. Rathore and U. R. Prasanna, "Analysis, design, and experimental results of novel snubberless bidirectional naturally clamped ZCS/ZVS current-fed half-bridge DC/DC converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4482–4491, Oct. 2013.
[34] X. Pan and A. K. Rathore, "Novel bidirectional snubberless naturally commutated soft-switching current-fed full-bridge isolated DC/DC converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2307–2315, May 2014.
[35] M. Pahlevaninezhad, P. Das, J. Drobnik, P. K. Jain, and A. Bakhshai, "A ZVS interleaved boost AC/DC converter used in plug-in electric vehicles," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3513–3529, Aug. 2012.
[36] U. Drofenik, A. Musing, and J. W. Kolar, "Voltage-dependent capacitors in power electronic multi-domain simulations," in *Proc. Int. Power Electron. Conf.*, Jun. 2010, pp. 643–650.
[37] Gecko-Simulations AG—GeckoCIRCUITS (2014). [Online]. Available: www.gecko-simulations.com

Xiaofeng Sun (M'13) received the B.S. degree in electrical engineering from Northeast Heavy Machinery Institute, Heilongjiang, China, in 1993, and the M.S. and Ph.D. degrees in power electronics from Yanshan University, Qinhuangdao, China, in 1999 and 2005, respectively.

From 2003 to 2007, he was an Associated Professor with the Department of Electrical Engineering, Yanshan University, where he has been a Professor since 2008 and currently the Director of Key Laboratory of Power Electronics for Energy Conservation and Motor Drive of Hebei Province. His current research interests include dc–dc converters, multiport converters, hybrid electric vehicles (HEVs), microgrids, and power quality control. He has authored or coauthored more than 70 transactions and conference papers. He is the holder of four granted patents of inventions.



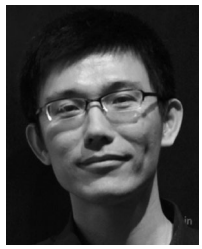
Yanfeng Shen received the B.S. degree in electrical engineering from Yanshan University, Qinhuangdao, China, in 2012, where he is currently working toward the M.S. degree in power electronics.

His current research interests include topology and control of dc–dc and dc–ac power converters for renewable energy systems. He has authored six technical papers in transactions or conferences and has four patents pending.

Mr. Shen was a recipient of the Graduate National Scholarship from the government of China in 2012.

Yune Zhu received the B.S. degree in measuring and control technology and instrumentations in 2010 from Yanshan University, Qinhuangdao, China, where she is currently working toward the M.S. degree in power electronics.

Her current research interests include topology and control of dc–dc power converters for renewable energy systems.



Xiaoqiang Guo (M'10) received the B.S. and the Ph.D. degrees in electrical engineering from the Yanshan University, Qinhuangdao, China, in 2003 and 2009, respectively.

He is currently an Associate Professor with Yanshan University, where he is involved in research associated with power electronics, industrial electronics, etc. He has authored or coauthored more than 50 technical papers, 10 of them published or to be published in IET Journals and IEEE Transactions, in addition to 9 patents. His current research interests include power electronics applications to distributed power generation systems and smartgrids.

Dr. Guo is a Member of the IEEE Power Electronics Society and the IEEE Industrial Electronics Society. He is an active Referee for the IEEE Transactions on Sustainable Energy, the IEEE Transactions on Industrial Electronics, and the IEEE Transactions on Power Electronics.