Effect of Nonlinearity of Parasitic Capacitance on Analysis and Design of Class E/F_3 Power Amplifier

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***Abstract*—In this paper, the analysis and comparison of a Class-E/F_3 power amplifier with nonlinear and linear shunt capacitance at 50% duty ratio are presented. An analytical analysis for nonlinear and linear shunt capacitance is presented, and its effects on the performance of the power amplifier are discussed. The different parameters, such as series reactance, peak switch voltage, and power output capability are compared for power amplifiers with linear and nonlinear shunt capacitance. Two design examples of the Class-E/F_3 power amplifiers with IRF530 MOSFETS and lumped elements at an operating frequency of 4 MHz are analyzed. The PSpice simulation and measurement for the power amplifier with nonlinear shunt capacitance have been done. The results agree with the analytical expressions that show the validity of the analytical expressions derived at zero-voltage switching and zero derivative voltage switching conditions.**

***Index Terms*—Nonlinear capacitance, power amplifier (PA), power output capability, switch current and voltage, switch mode.**

I. Introduction

In the modern wireless communication systems, the power amplifier (PA) with high efficiency and low harmonic is required. The Class-E PA is a type of the switching mode PA which can provide a very high efficiency with optimized load-network parameters [1]. Different configurations of the Class-E PA with nominal and subnominal conditions were studied in order to improve the PA performance including maximal operating frequency and output power capability [2]–[5]. In [4], by tuning the parallel *LC* resonator to the second harmonic, the peak switch voltage of $3V_{dd}$ instead of $3.6V_{dd}$ for nominal Class-E PAs has been obtained. However, deviations of the load-network parameters in a Class-E inverter, which is used as the primary coil driver in resonant inductive links, can cause permanent damage to the switch [5]. In this case, the exact analysis of the PAs considering the parasitic effect is very important. Recently, the effect of the MOSFET parasitic drain-to-source capacitance for achieving the Class-E zero-voltage switching (ZVS)/zero derivative voltage switching (ZDS) conditions was investigated in detail [6]–[10]. The high peak switch voltage makes a limitation of the Class-E PA with high output power. Therefore, two solutions have been used for reducing the peak switch voltage. These solutions require the insertion of additional circuit elements into the Class-E PA. The first solution, insertion of Zener diode and transformer with a diode, was described in [11] and [12]. The second solution consists of an additional harmonic control circuit. To control harmonic levels in the high-efficiency PA, the resonance networks consisting of a Class-F or an inverse Class-F configuration can be used with a Class-E PA [13]–[15]. The technique of using lumped or distributed circuit tuned to adjust the corresponding harmonics in the load network is usually used in conventional Class-F or inverse Class-F PAs. This technique can be applied to Class-E PAs, resulting in mixed mode Class-FE or Class-E/F. This method depicts a tradeoff between the Class-E and Class-F or inverse Class-F by reducing the peak output voltage and high output power capability. In [13], the Class-EF_2 and Class-E/F_3 with a peak factor greater than 2 and duty ratio of 50% or less than 50% is achieved. In [14], it was shown that the drain efficiency of more than 80% can be obtained in a Class-FE mode for duty cycles less than 50% with a voltage peak factor of 2. In [15], the Class-E/F PA was proposed based on a push/pull topology, operating in a similar manner as an inverse Class-F PA. This configuration results in reduction of the maximum drain voltage amplitude. The presence of a parallel resonant circuit in the Class-E/F_2 PA results in a high peak drain voltage in comparison with the Class-E mode [16]. To reach the high efficiency and good linearity, an inverse Class-F or Class-E mode can be used in advanced transmitter architectures such as Doherty, linear amplification using nonlinear components (LINC), or envelope elimination and restoration with digital pre distortion [17]–[20]. The operation of the Class-E/F_3 PA with the lumped elements and transmission lines has been investigated in [21]. An analysis of the Class-E/F PA at nonoptimum operation has been done in [22]. On the other hand, the operation of a Class-E/F_3 PA with linear shunt capacitance is different from the Class-E/F_3 PA with nonlinear parasitic capacitance. At high frequencies, the parasitic capacitance of the transistor becomes dominant. In fact, the switching device having a nonlinear output shunt capacitance generates higher peak switch voltage in comparison with the device with a linear shunt capacitance. In the notation of Class-E/F_n, "/F" means the inverse Class-F type resonator, and the subscript "*n*" means that low impedance is gained for the *n*th harmonic at the drain node. In practical designs for the specified output power and operation frequency range in various applications such as high-frequency electric process heating [23], dc–dc converters [24], and many power-electronics amplifiers [25], analysis of switched-mode PA with nonlinear effect of the shunt capacitance should be valuable.

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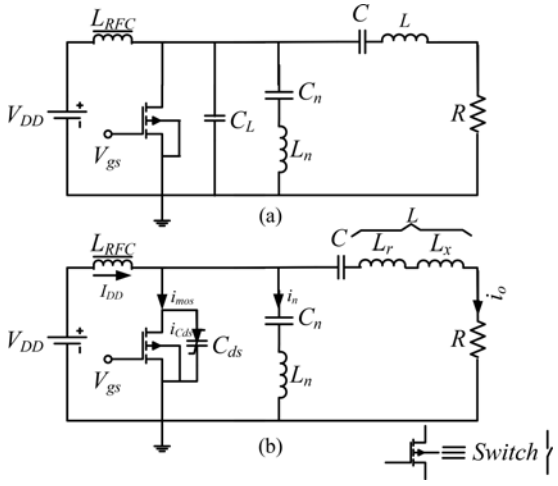

Fig. 1. Circuit of the Class-E/F$_n$ PA (a) with linear shunt capacitance, and (b) with nonlinear shunt capacitance which is studied in this paper.

II. Circuit Analysis

The basic circuit of a Class-E/F$_n$ PA is shown in Fig. 1. The basic Class-E/F$_3$ amplifier configuration consists of a single transistor with a shunt capacitor, a series resonant output filter at the fundamental frequency and a parallel series-resonant filter at the third harmonic. The nominal conditions in the Class E/F$_3$ PA are written as

$$v_s(\pi) = 0 \tag{1}$$

$$\frac{dv_s(\pi)}{d\theta} = 0. \tag{2}$$

The MOSFET drain-to-source parasitic capacitance has a nonlinear characteristic [6]–[10], which is expressed as

$$C_{\rm ds} = \frac{C_{j0}}{\sqrt{1+\dfrac{v_s}{V_{bi}}}} \tag{3}$$

where V_{bi} is the built-in potential, which changes from 0.5 to 0.9 V, v_s is the switch voltage, and C_{j0} is the capacitance at $v_s(0) = 0$. The driver circuit is a 4-MHz square-wave source with the amplitude of 6 V and offset of 0 V. The dc-feed inductance $L_{\rm RFC}$ is high enough so that the current through it is the dc-feed current I_{DD}. The resonant inductor L is divided into L_r and L_x. The resonant filter $L_r - C$ is resonant at the fundamental frequency and inductor L_x causes the phase shifts of ϕ_1. During the off state, the current through the MOSFET device is

$$\begin{aligned} i_{\rm mos}(\theta) =\ & I_{DD} - i_n(\theta) - i_o(\theta) = I_{DD} \\ & - I_n \sin(n\theta) - I_M \sin(\theta+\phi) = i_{\rm Cds}(\theta) \\ =\ & \frac{\omega C_{j0}}{\sqrt{1+\dfrac{v_s}{V_{bi}}}} \frac{dv_s}{d\theta} \end{aligned} \tag{4}$$

where $i_{\rm Cds}(\theta)$ is the current through the MOSFET parasitic capacitances, ϕ is the initial phase shift, I_M is the fundamental-frequency current amplitude, and I_n is the *n*th harmonic current amplitude. From (4) and $v_s(0) = 0$, we obtain

$$\int_0^{\theta} i_{\rm mos}(\theta')d\theta' = \omega \int_0^{v_s} \frac{C_{j0}}{\sqrt{1+\dfrac{v_s'}{V_{bi}}}} dv_s', \text{ for } 0 < \theta < \pi. \tag{5}$$

From (5), one can obtain

$$v_s(\theta) = V_{bi}[(h(\theta)+1)^2 - 1] \tag{6}$$

where

$$h(\theta) = \frac{I_{DD}\theta + \frac{I_n}{n}(\cos(n\theta) - 1) + I_M(\cos(\theta+\phi) - \cos(\phi))}{2\omega V_{bi} C_{jo}}. \tag{7}$$

Substituting $\theta = \pi$ and (1) into (6) results in

$$I_{DD}\pi + \frac{I_n}{n}(\cos(n\pi) - 1) - 2I_M \cos(\phi) = 0. \tag{8}$$

Then, substituting $\theta = \pi$ and (2) into (4) gives

$$I_{DD} + I_M \sin(\phi) = 0 \Rightarrow I_{DD} = -I_M \sin(\phi). \tag{9}$$

The relative amplitude of the *n*th harmonic component for any *n* can be obtained as [21]

$$I_n = \frac{4I_{DD}}{n\pi}. \tag{10}$$

By substituting (9) and (10) into (8), the initial phase angle ϕ can be calculated from

$$\tan\phi = \frac{2n^2\pi}{8 - n^2\pi^2}. \tag{11}$$

Note that the power loss in the Class-E PA due to finite switching time is small, and efficiency can drop to less than 1% when the maximum transition time is $\tau = 0.35$ (or 20°) [26]. For the square gate-to-source voltage, the power conversion efficiency is

$$\eta = \frac{P_o}{P_I} = \frac{RI_M^2}{2I_{DD}V_{DD}} = 1. \tag{12}$$

From (9) and (12), the amplitude of the output current I_M can be written as

$$I_M = \frac{-2V_{DD}\sin(\phi)}{R}. \tag{13}$$

A. Equivalent Linear and Nonlinear Shunt Capacitance

The average value of the switch voltage is equal to the dc-supply voltage V_{DD} which is written as

$$V_{DD} = \frac{1}{2\pi}\int_0^{2\pi} v_s(\theta)d\theta = \frac{V_{bi}}{2\pi}\int_0^{\pi} \left[\langle h(\theta)+1\rangle^2 - 1\right] d\theta. \tag{14}$$

By solving (14), one can obtain $R\omega C_{j0}$ as a function of V_{DD} according to

$$R\omega C_{j0} = \frac{27\pi}{(9\pi^2+4)(9\pi^2+16)V_{bi}} \times (12V_{bi} + \sqrt{144V_{bi}^2 + 128V_{DD}V_{bi} - 124\pi^2 V_{DD}V_{bi} + 15\pi^4 V_{DD}V_{bi}}). \tag{15}$$

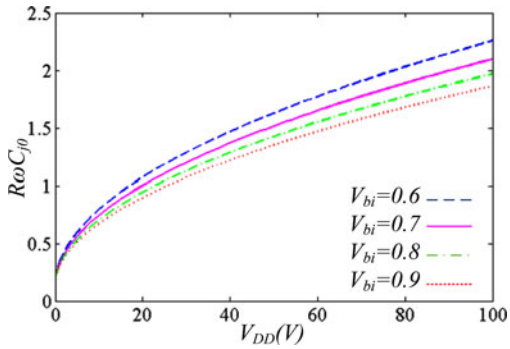

Fig. 2. Theoretical waveforms of switch voltage with linear capacitance v_{sL} (solid line) and nonlinear shunt capacitor v_s (dashed line).

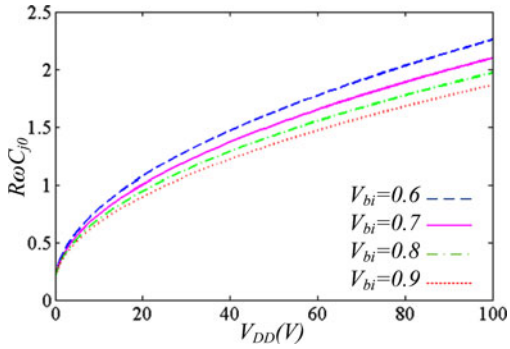

Fig. 3. Variation of $R\omega C_{j0}$ as a function of V_{DD}.

For the Class E/F$_3$ with linear shunt capacitance, the switch voltage can be written as

$$v_{sL}(\theta) = \frac{1}{\omega C_L} \times \left[I_{DD}\theta + \frac{I_n}{n}(\cos(n\theta) - 1) + I_M(\cos(\theta+\phi) - \cos(\phi)) \right] \tag{16}$$

whereas the linear shunt capacitance as [21]

$$C_L = \frac{648\pi}{(9\pi^2+4)(9\pi^2+16)R\omega}. \tag{17}$$

Fig. 2 shows the switch voltage waveforms of the Class-E/F$_3$ PA with linear (v_{sL}) and nonlinear (v_s) shunt capacitances. As seen from Fig. 3, the $R\omega C_{j0}$ increases with an increase in V_{DD} and decreases with an increase in V_{bi}. The value of $R\omega C_L$ is 0.209, and it is constant with increment of V_{DD}. The ratio of C_{j0}/C_L is calculated from (15) and (17). Fig. 4 shows the ratio of C_{j0}/C_L as a function of V_{DD}. This ratio increases from 1 to 11 as V_{DD} increases from 0 to 100 V and decreases with increasing voltage V_{bi}.

B. Comparison of Series Reactance for Class-E/F$_3$ PA With Linear and Nonlinear Shunt Capacitances

Fig. 5 shows the equivalent circuit of the Class-E/F$_3$ power amplifier at the fundamental frequency, where the voltage across

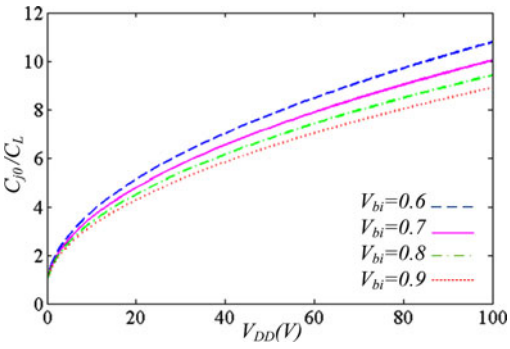

Fig. 4. Variation of C_{j0}/C_L as a function of V_{DD}.

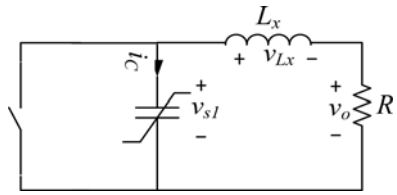

Fig. 5. Equivalent circuit of the Class E/F$_3$ PA at the fundamental frequency.

the reactance L_x is written as

$$v_{Lx} = \frac{\omega L_x V_M}{R}\cos(\theta+\phi) \quad \text{for} \quad 0 < \theta < 2\pi. \tag{18}$$

The voltage across the resonant circuit for $0 < \theta < 2\pi$ is

$$v_{s1}(\theta) = v_o(\theta) + v_{Lx}(\theta) = V_M \sin(\theta+\phi) + \frac{\omega L_x V_M}{R}\cos(\theta+\phi) = V_1 \sin(\theta+\phi_1) \tag{19}$$

where V_1 is the amplitude of v_{s1} written as

$$V_1 = V_M\sqrt{1+\left(\frac{\omega L_x}{R}\right)^2} \tag{20}$$

and ϕ_1 is the load phase angle obtained by

$$\phi_1 = \phi + \tan^{-1}\left(\frac{\omega L_x}{R}\right). \tag{21}$$

The output voltage of the resonant circuit v_{s1} has only the fundamental-frequency component of the switch voltage v_s. Therefore

$$\frac{1}{\pi}\int_0^{2\pi} v_s(\theta)\cos(\theta+\phi_1)d\theta = 0. \tag{22}$$

From (22), it follows that:

$$\tan\phi_1 = \frac{\int_0^{\pi} v_s(\theta)\cos(\theta)d\theta}{\int_0^{\pi} v_s(\theta)\sin(\theta)d\theta}. \tag{23}$$

The reactance *X* can be defined from (21) as

$$X = \omega L_x = R\tan(\phi_1 - \phi). \tag{24}$$

Fig. 6 shows the normalized reactance *X/R* as a function of V_{DD}, which increases from 0.96 to 0.974 as V_{DD} increases from

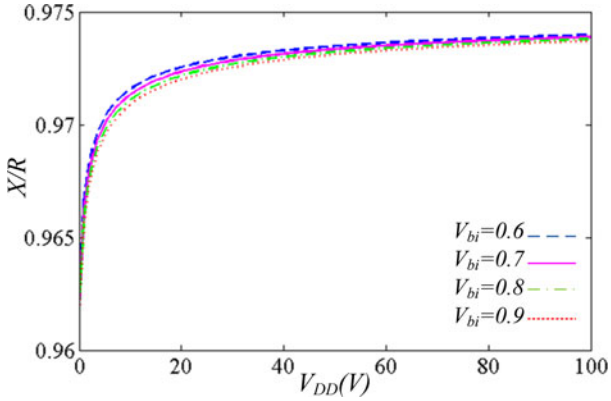

Fig. 6. Variation of *X/R* as a function of V_{DD}.

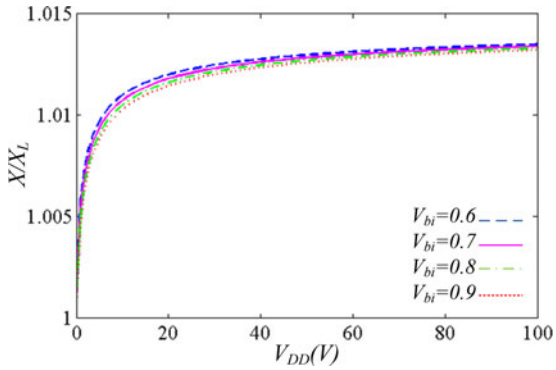

Fig. 7. Variation of X/X_L as a function of V_{DD}.

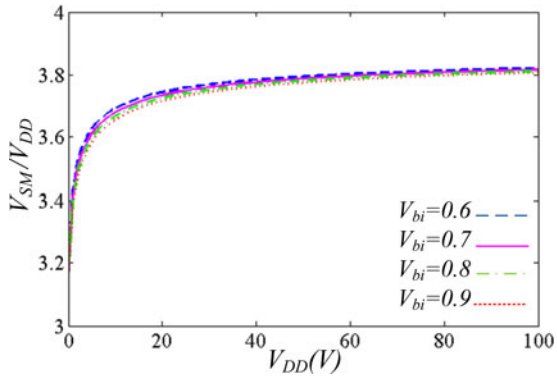

Fig. 8. Ratio of V_{SM}/V_{DD} as a function of V_{DD}.

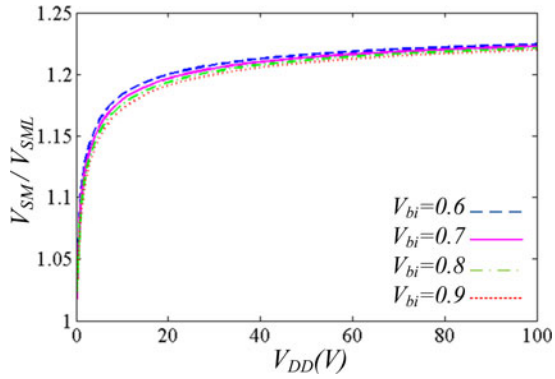

Fig. 9. Ratio of V_{SM}/V_{SML} as a function of V_{DD}.

0 to 100 V. The series reactance X_L in the Class-E/F$_3$ PA with a linear shunt capacitance is defined as [21]

$$\frac{X_L}{R} = \frac{(9\pi^2 - 20)(9\pi^2 - 32)}{1296\pi}. \tag{25}$$

Consequently, the ratio between the nonlinear and linear reactances can be written as

$$\frac{X}{X_L} = \frac{1296\pi}{(9\pi^2 - 20)(9\pi^2 - 32)} \tan(\phi - \phi_1). \tag{26}$$

Fig. 7 shows the ratio of the series reactances X/X_L as a function of V_{DD}. It can be seen that this ratio increases from 1 with increasing voltage and saturates at about 1.014.

C. Comparison of Peak Switch Voltage and Current for Class E/F$_3$ With Linear and Nonlinear Shunt Capacitances

The peak switch voltage appears in the range of $0 < \theta < \pi$. As a result

$$\frac{|V_{SM}|}{V_{DD}} = \frac{V_{bi}}{V_{DD}}[(h(\theta_{\max}) + 1)^2 - 1]. \tag{27}$$

For the peak voltage value, the derivative value of the switch voltage is zero. Hence, from (4), it can be obtained for $n = 3$ that

$$I_{DD} - I_3 \sin(3\theta_{\max}) - I_M \sin(\theta_{\max} + \phi) = 0. \tag{28}$$

The value of $\theta_{\max}$ at peak value of the switch voltage cannot be obtained analytically. However, from (28), it can numerically be calculated as $\theta_{\max} = 0.5\,\pi$. Fig. 8 shows the ratio of V_{SM}/V_{DD} versus V_{DD} for the PA with linear and nonlinear shunt capacitances. With a nonlinear capacitance, this ratio increases from 3 to about 3.8 as V_{DD} increases and decreases with increasing V_{bi}. The ratio of V_{SML}/V_{DD} with a linear capacitance is constant and equal to 3.142. Fig. 9 shows the ratio of V_{SM}/V_{SML} as a function of V_{DD}, where this ratio increases with increasing voltage V_{DD} and saturates at about 1.23. The peak value of the switch current appears during the on-state. According to numerical calculations, it is confirmed that the value of θ which satisfies this condition is approximately $\theta = 1.79\,\pi$. Consequently

$$\frac{I_{SM}}{I_{DD}} = 1 - \frac{I_3}{I_{DD}} \sin(3\theta) - \frac{I_M}{I_{DD}} \sin(\theta + \phi). \tag{29}$$

From (29), it follows that the value of I_{SM}/I_{DD} is constant and equal to 3.056, which is similar to that of the PA with linear shunt capacitance.

The definition of the output power capability c_p is

$$c_p = \frac{V_{DD} I_{DD}}{|V_{SM}|\,|I_{SM}|} \tag{30}$$

where V_{SM} and I_{SM} are the peak values of the drain voltage and current of the MOSFET. Fig. 10 shows c_p versus V_{DD} where

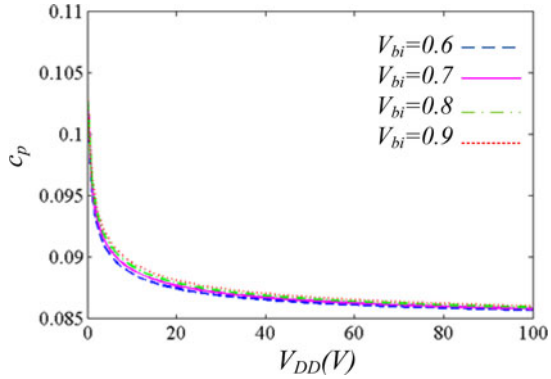

Fig. 10. c_p as a function of V_{DD} for fixed value of V_{bi}.

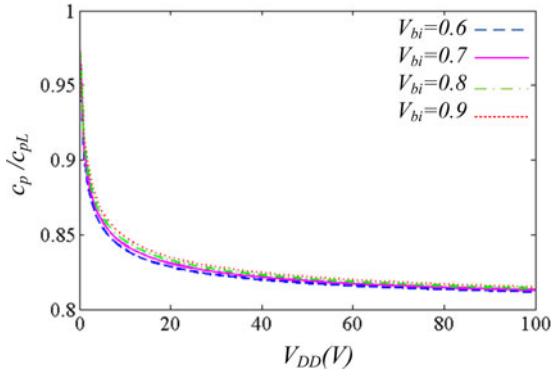

Fig. 11. c_p/c_{pL} as a function of V_{DD} for fixed value of V_{bi}.

the value of c_p decreases from 0.11 to 0.086 with increasing V_{DD}. On the other hand, c_{pL} is constant and is equal to 0.104 with linear shunt capacitance. Fig. 11 depicts the ratio of the output power capabilities c_p/c_{pL}. It can be seen that this ratio decreases from 1 to 0.82 as V_{DD} is increased from 0 to 100 V.

III. Power Conversion Efficiency

Generally, each reactive element which is used in the structure of the PA has parasitic resistance. As shown in Fig. 12, we consider the power losses in equivalent series resistance (ESR) of the dc-feed inductor r_{LRFC}, ESRs of the load network r_{LC}, parallel resonant filter r_{LCs}, and the switch on-resistance r_s. The power loss in r_{LRFC} is obtained as

$$P_{rL_{\mathrm{RFC}}} = \frac{1}{2\pi}\int_0^{2\pi} r_{\mathrm{LRFC}} I_{DD}^2 d\theta = r_{\mathrm{LRFC}} I_{DD}^2. \tag{31}$$

Similarly, the power loss in r_{LC} and r_{LCs} are

$$P_{r_{LC}} = \frac{1}{2\pi}\int_0^{2\pi} r_{LC} i_o^2 d\theta = \frac{r_{LC} I_M^2}{2} \tag{32}$$

$$P_{r_{LCs}} = \frac{1}{2\pi}\int_0^{2\pi} r_{LCs} i_n^2 d\theta = \frac{r_{LCs} I_n^2}{2}. \tag{33}$$

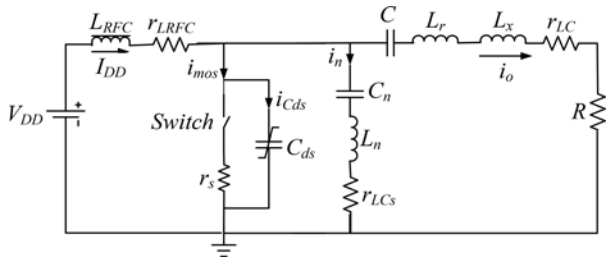

Fig. 12. Equivalent circuit of Class E/F$_3$ PA including ESRs.

The power loss P_{rs} in the switch on-resistance r_s is

$$\begin{aligned} P_{rs} &= \frac{1}{2\pi}\int_{\pi}^{2\pi} r_s i_s^2 d\theta \\ &= \frac{r_s}{2\pi}\left[\pi I_{DD}^2 + \frac{\pi}{2}(I_M^2 + I_3^2) + 6 I_M I_{DD}\cos(\phi) + 2 I_3 I_{DD}\right]. \end{aligned} \tag{34}$$

As a result, by using (10), (11), (13), and (31)–(34), the power conversion efficiency η is written as

$$\begin{aligned} \eta &= \frac{P_o}{P_o + P_{rLC} + P_{rLCs} + P_{rs}} \\ &= \left\{1 + \frac{r_s}{R}\left[\frac{1}{2} - \frac{9\sin(2\phi)}{2\pi} + \left(1 + \frac{32}{9\pi^2}\right)\sin^2(\phi)\right] \right. \\ &\quad \left. + \frac{16 r_{LCS}\sin^2(\phi)}{9\pi^2 R} + \frac{r_{LC}}{R} + \frac{2 r_{\mathrm{LRFC}}\sin^2(\phi)}{R}\right\}^{-1} \end{aligned} \tag{35}$$

IV. Design Example of Class-E/F$_3$ PA

A. Design Example With Nonlinear and Linear Shunt Capacitances

In this section, the design example of the Class-E/F$_3$ PA with nonlinear parasitic capacitances of the MOSFET is presented. Because the other elements are functions of R and the optimum load resistance R is affected by the nonlinearities, the nonlinearities of the shunt capacitances affect the values of all elements in the PA. When the supply voltage and the output power are given as design specifications, the analytical design equations indicate that the series-resonant-circuit elements L and C are independent of the nonlinearity of the shunt capacitances. The PA achieves ZVS/ZDS conditions if the designer uses the MOSFETs that have required output capacitances. The parameter of the nonlinear shunt capacitance is determined by the operating frequency, the load resistance, supply voltage, and built-in potential. This PA is implemented with the IRF530 MOSFET. From the breakdown voltage viewpoint, it is proved that the IRF530 MOSFET is a proper device. The design specifications for the PAs are $f = 4$ MHz, $V_{DD} = 25$ V, $P_{out} = 11.0$ W, $Q = 10$, and $D = 0.5$. From (11), we obtained $\phi = -0.61$ rad. Hence, the load resistance is equal to 36 Ω. From the definition of the loaded quality factor Q, the inductance L is written as

$$L = \frac{RQ}{\omega}. \tag{36}$$

TABLE I
DIFFERENT ELEMENT VALUES OF THE CLASS-E/F$_3$ PA

Parameters	Values of elements at $V_{DD} = 25$ V	
	Linear capacitance	Nonlinear capacitance
$C_{\rm ds}$ and C_L	$C_L = 77.88$ pF	$C_{\rm ds} = 64.63$ pF
X	35 Ω	34.56 Ω
V_{SM}	78.5 V	93 V
c_p	0.104	0.088

TABLE II
IDENTICAL ELEMENT VALUES OF THE CLASS-E/F$_3$ PA

Parameters	Values of elements at $V_{DD} = 25$ V	
	Linear capacitance	Nonlinear capacitance
ϕ	−0.61 rad	−0.61 rad
V_M	28.6 V	28.6 V
I_{DD}	0.456 A	0.456 A
P_o	11.0 W	11.0 W
I_M	0.795 A	0.795 A
I_{SM}	1.39 A	1.39 A

Then, from (36), it is calculated as $L = 14.33$ μH and, from (25) and (36), the inductance L_r is defined as

$$L_r = L - L_x = \frac{1}{\omega}[RQ - X)] \tag{37}$$

resulting in $L_r = 12.93$ μH. Similarly, the resonant capacitance is defined as

$$C = \frac{1}{\omega^2 L_r} = \frac{1}{\omega[RQ - X]} \tag{38}$$

that results in $C = 122.5$ pF. The series resonant circuit C_3–L_3 affects the shaping of the transistor current and voltage waveforms. For Class-E/F$_3$ PA, it is required zero impedance at the third harmonic. Therefore, the value of the C_3–L_3 branch is selected to obtain low impedance at the third harmonic. The initial values for the elements of the resonant circuit C_3–L_3 are as follows: $L_3 = 10$ μH and $C_3 = 17.56$ pF. The inductance of the RF choke is selected as $L_f = 100$ μH. The values of the elements for nominal conditions in Class-E/F$_3$ PA with linear and nonlinear shunt capacitances are shown in Table I and II.

B. Simulation and Test Results

To validate the analytical expressions and the design example in the previous sections, the circuit experiment and PSpice simulation are carried out. The MOSFET model used throughout this paper is obtained from the default package of PSpice, which is licensed by Cadence. A 4-MHz input square waveform with the amplitude of 6 V with offset of 0 V is generated by the function generator Stanford Research DS345. The power gain is calculated by

$$G = 10\log_{10}\left(\frac{P_o}{P_{\rm in}}\right) \tag{39}$$

TABLE III
VALUE OF THE ELEMENTS FOR THE NOMINAL CONDITIONS IN THE CLASS-E/F$_3$ PA

	Theoretical	Simulated	Measured
$R(\Omega)$	36	36	36
$L_{\rm RFC}$ (μH)	100	100	100
L (μH)	14.33	14.33	14.2
C (pF)	122.5	122.5	122
C_3 (pF)	17.56	17.16	17
L_3 (μH)	10	10	10.1
$r_{\rm LRFC}$ (Ω)	0.15	0.165	0.17
r_L (Ω)	2.45	2.42	2.5
r_{Ls} (Ω)	1.23	1.25	1.28
r_s (Ω)	0.16	0.16	0.16
V_{SM} (V)	93	82.3	82
I_{SM} (A)	1.39	1.38	1.38
V_o (V)	28.96	28.9	28.5
P_o (W)	11.0	10.7	10.5
$P_{\rm in}$ (mW)	–	–	30
Gain (dB)	–	–	25
η (%)	100	97.27	95.45
THD(%)	0.0	4.81	5.1

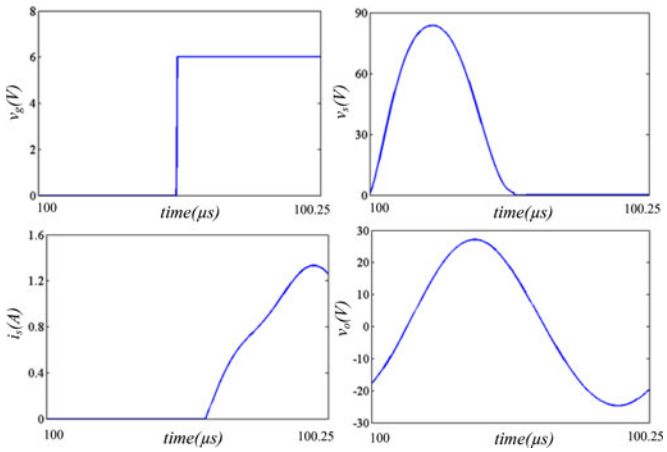

Fig. 13. Simulated waveforms of (a) gate–source voltage v_g, (b) switch voltage v_s, (c) switch current i_s, and (d) output voltage v_o of Class-E/F$_3$ PA.

where $P_{\rm in}$ and P_o are the input power and output power, respectively. The total harmonic distortion (THD) is calculated by

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_{\rm on}^2}}{V_{o1}} \tag{40}$$

where $V_{\rm on}$ is a root-mean-square value of the nth harmonic in the output voltage v_o. The measured value of THD for the circuit design example is given in Table III. The simulated waveforms of the Class-E/F$_3$ PA are shown in Fig. 13. The photograph and measured results of the fabricated amplifier are shown in Fig. 14. The waveform of the switch voltage validates that the ZVS and ZDS conditions of the proposed amplifier are achieved. The ESRs of the passive elements are measured by a HP-4284A, and the MOSFET on-resistance is obtained from PSpice model of the IRF530. These values were used for theoretical derivation of the power conversion efficiency and PSpice simulation. The

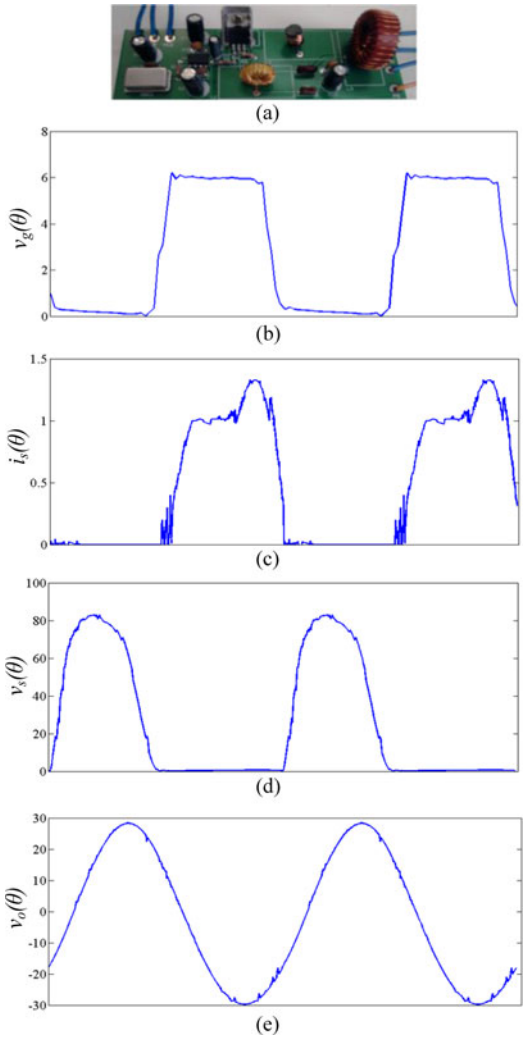

Fig. 14. (a) Photograph and measured (b) gate–source voltage v_g, (c) switch current i_s, (d) switch voltage v_s and (e) output voltage v_o of Class-E/F$_3$ PA.

power losses, output power, and power conversion efficiency are given in Table III. The waveform data of the output voltage v_o are obtained from the Textronix TDS3014B. For measurements of the voltage and power losses, a 34401A Digital Multimeter is used.

V. Conclusion

In this paper, an analysis of the Class-E/F$_3$ PA with nonlinear shunt capacitance is presented for the duty ratio of 0.5. The theoretical results were achieved using both analytical and numerical calculations. One design procedure is given for an example at operating frequency of 4 MHz. When the supply voltage and output power are specified, all parameters are independent of the nonlinearity of the shunt capacitances. The nonlinear shunt capacitance is determined through the operating frequency, the load resistance, dc-supply voltage, and built-in potential voltage. The different parameters, such as series reactance, peak switch voltage, and power output capability are compared for Class-E/F$_3$ PAs with linear and nonlinear shunt capacitance. The theoretical results were validated by PSpice simulation using a model of the real transistor and by experimental results. The calculated and measured results were in good agreement. In particular, the switch voltage waveform satisfied both conditions for optimum operation. It is shown analytically that the maximum switch voltage and output power capability have been affected by the nonlinearity of the shunt capacitance. On the other hand, the amplitude of the output voltage and output current is always proportional to the dc supply voltage and current with an identical proportion constant and is not affected by the nonlinearity of the shunt capacitance. Two design examples of the Class-E/F$_3$ PAs with IRF530 MOSFETs and lumped elements at operating frequency of 4 MHz are given. The experimental results show the validity of the analytical expressions derived at ZVS and ZDS conditions.

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