Bridgeless PFC-Modified SEPIC Rectifier With Extended Gain for Universal Input Voltage Applications

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***Abstract*—In this paper, a new single-phase ac–dc PFC bridgeless rectifier with multiplier stage to improve the efficiency at low input voltage and reduce the switch-voltage stress is introduced. The absence of an input rectifier bridge in the proposed rectifier and the presence of only two semiconductor switches in the current flowing path during each switching cycle result in less conduction losses and improved thermal management compared to the conventional full bridge topology. Lower switch voltage stress allows utilizing a MOSFET with lower $R_{\mathbf{DS\text{-}on}}$. The proposed topology is designed to operate in discontinuous conduction mode (DCM) to achieve almost a unity power factor and low total harmonic distortion (THD) of the input current. The DCM operation gives additional advantages such as zero-current turn-on in the power switches and simple control circuitry. The proposed topology is compared with modified full-bridge SEPIC rectifier in terms of efficiency, THD, and power factor. Detailed converter analysis, small signal model, and closed-loop analysis are presented. Experimental results for a 200 W/400 V_{dc} at universal line voltage range to evaluate the performance of the proposed bridgeless PFC rectifiers are detailed.**

***Index Terms*—Bridgeless rectifier, discontinuous current mode (DCM), power factor correction, SEPIC rectifier, total harmonics distortion (THD).**

I. Introduction

Power supplies with active power factor correction (PFC) techniques are becoming necessary for many types of electronic equipment to meet harmonic regulations and standards, such as the IEC 61000-3-2 [1]. PFC rectifiers have wide array of industrial applications such as telecommunication and biomedical industries.

Most power factor correction topologies so far implement a boost-type circuit configuration at its front end [2]–[9] because of its low cost and its high performance in terms of efficiency, power factor, and simplicity. However, for universal input voltage applications, the boost converter suffers from lower efficiency and higher total harmonic distortion at low input voltage. In addition, the boost converter has relatively high switch voltage stress which is equal to the output voltage. Also, the boost rectifier has some practical drawbacks, such that, input–output isolation cannot easily be implemented, the startup inrush current is high, and there is a lack of current limiting during overload conditions. Furthermore, it is well known that the boost converter operating in discontinuous current mode (DCM) can offer a number of advantages, such as inherent PFC function, very simple control, soft turn-on of the main switch, and reduced diode reversed-recovery losses. However, the DCM operation requires a high-quality boost inductor since it must switch extremely high peak ripple currents and voltages. As a result, a more robust input filter must be employed to suppress the high-frequency components of the pulsating input current, which increases the overall weight and cost of the rectifier. In addition, several PFC topologies based on flyback, buck-boost, and Cuk converters have been published [10]–[16]. However, these topologies have an inverting output.

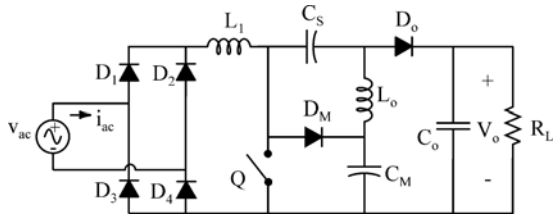

Fig. 1. Modified SEPIC rectifier [20].

On the other hand, SEPIC rectifier has several advantages such as: Step up and step down capabilities in addition to magnetic coupling that will lead to reduction in input current ripple [16]–[20]. In [20], a wide static gain SEPIC converter operating in continuous conduction mode (CCM) have been proposed to increase the static gain at low input voltage without extreme switch duty-cycle and with reduced switch voltage stress. This has been achieved by inserting a voltage multiplier cell ($\mathrm{D_M}$ and $\mathrm{C_M}$) in the conventional SEPIC converter as shown in Fig. 1. However, the proposed topology in [20] utilizes a full bridge at the input side resulting in higher conduction losses because the current path flows through at least two bridge diodes at any instant of time. In addition, the reported topology in [20] utilizes a snubber circuit to decrease switching losses.

In this paper, a new single-phase ac–dc PFC bridgeless rectifier with extended gain range operating in DCM is introduced. The DCM operation results in soft turn-on switching and

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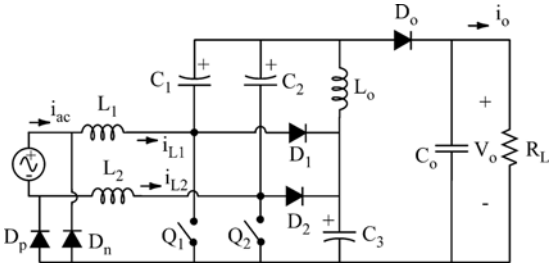

Fig. 2. Proposed bridgeless rectifier.

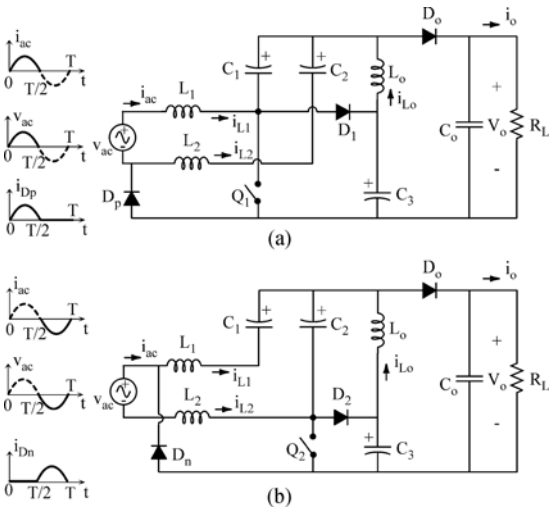

Fig. 3. Equivalent rectifier circuit. (a) During positive half-line period. (b) During negative half-line period.

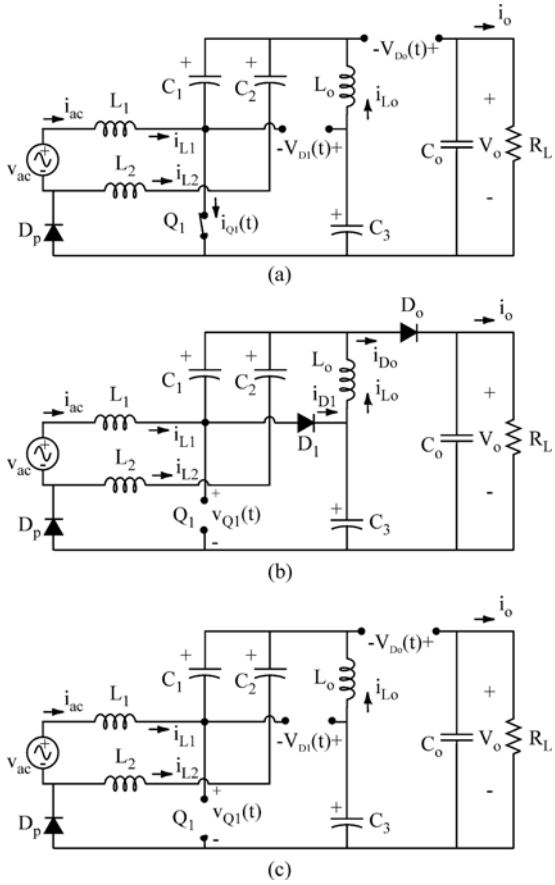

Fig. 4. Topological stages over one switching period T_s during positive half-line period for the propose converter of Fig. 2. (a) Switch ON topology. (b) Switch OFF topology. (c) DCM topology.

relatively low inrush current. The voltage gain can be extended without extreme duty cycle operation which makes the proposed topology suitable for universal line voltage applications. The proposed bridgeless rectifier with coupled magnetic configurations results in higher overall efficiency and higher power density.

II. Proposed Circuit

Fig. 2 shows the proposed bridgeless SEPIC PFC rectifier with voltage multiplier cell. The bridgeless configuration will reduce the conduction losses and the multiplier cell (D_1, C_3 and D_2, C_3) will increase the gain and reduce the switch voltage stress. Hence, the proposed topology enhances the overall efficiency. The proposed circuit consists of two symmetrical configurations. Each configuration will operate in a half-line cycle. By implementing two slow diodes D_p and D_n, the output ground is always connected to the terminals of ac mains directly over the whole ac line cycle. As a result, this stabilizes voltage potential of output ground and reduces common mode EMI generation. Furthermore, the three separate inductors can be magnetically coupled into a single magnetic core to attain an input current having very low current ripples. Consequently, the generated EMI noise level is greatly minimized as well as the requirement for the input filtering. The proposed converter utilizes two nonfloating switches (Q_1 and Q_2). Switch Q_1 is turned ON/OFF during the positive half-line cycle [see Fig. 3(a)] and the current flows back to the source through Diode D_p. During the negative half-line cycle, switch Q_2 is switched ON/OFF with the current flowing back through diode D_n as illustrated in Fig. 3(b). Moreover, the two power switches Q_1 and Q_2 can be driven by the same control signal, which significantly simplifies the control circuitry.

Despite the advantages of the proposed rectifier, the addition of the multiplier cell makes the characteristics of the proposed topology similar to the characteristics of the classical boost converter. In other words, the proposed topology has the same major practical drawbacks as the conventional boost converter, such that the dc output voltage is always higher than the peak input voltage, input–output isolation cannot be easily implemented, high startup inrush current, as well as a lack of current limiting during overload conditions.

III. Principle of Operation

Since the proposed circuit consists of two symmetrical configurations as illustrated in Fig. 3, the circuit is analyzed for the positive half line cycle configuration shown in Fig. 3(a). Assuming that the three inductors are operating in DCM, then the circuit operation during one switching period T_s in a positive half-line period can be divided into three distinct operating

modes, as shown in Fig. 4(a)–(c), and it can be described as follows.

A. First Stage

In this stage, switch Q_1 is turned-on by the control signal and both diodes D_1 and D_o are reversed biased as shown in Fig. 4(a). In this stage, the three-inductor currents increase linearly at a rate proportional to the input voltage v_{ac}

$$\frac{di_{Ln}}{dt} = \frac{v_{ac}}{L_n}, \quad n = 1, 2, o. \tag{1}$$

B. Second Stage

During this subinterval, switch Q_1 is turned-off and both diodes D_1 and D_o will conduct simultaneously providing a path for the three inductors' currents as shown in Fig. 4(b). In this stage, the three inductors' currents decrease linearly at a rate proportional to the capacitor C_1 voltage V_{C1}. This stage ends when the sum of the currents flowing in the inductors adds up to zero, hence diodes D_1 and D_o are reverse biased

$$\frac{di_{Ln}}{dt} = -\frac{v_{C1}}{L_n}, \quad n = 1, 2, o. \tag{2}$$

C. Third Stage

In this stage, switch Q_1 remains turned-off while both diodes D_1 and D_o are reverse biased as illustrated in Fig. 4(c). Diode D_p provides a path for i_{Lo}. The three inductors behave as current sources, which keeps the currents constant. Hence, the voltage across the three inductors is zero. This period ends when switch Q_1 is turned-on initiating the next turn-on of the switching cycle. Fig. 5 illustrates the theoretical DCM waveforms during one switching period T_s for the proposed rectifier.

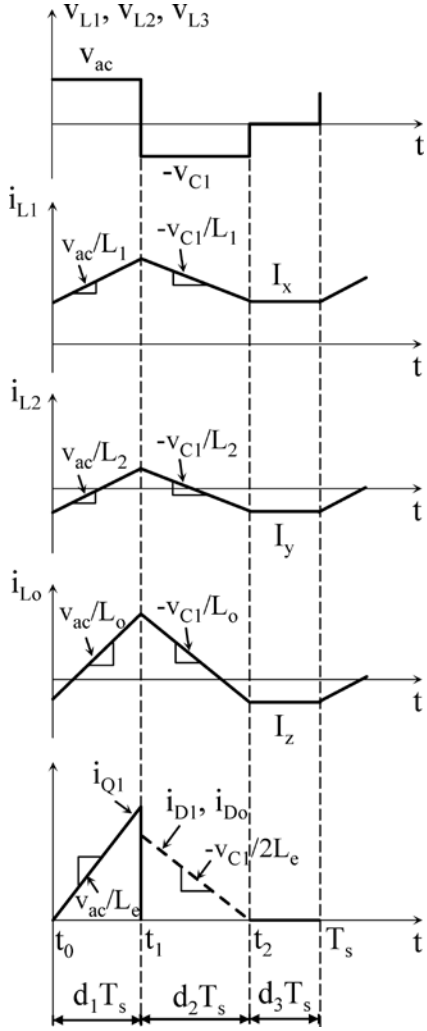

Fig. 5. Theoretical DCM waveforms during switching period for the proposed rectifier.

IV. Design Procedure and Simulation

In this section, the components of the proposed circuit will be designed and the operation of the circuit with the calculated values will be validated using simulation.

A. Voltage Conversion Ratio, M

Average diode current over half-line cycle is

$$I_{D_o} = \frac{1}{T_L/2}\int_0^{T_L/2} \bar{i}_{Do}\,dt \tag{3}$$

where T_L is the period of the line voltage and $\bar{i}_{Do}$ is the average output diode current over a switching cycle. Hence, the average current of diode D_o over half-line cycle can be presented by

$$I_{D_o} = \frac{d_1^2 T_s V_M}{\mathrm{T_L} L_e} \int_0^{T_L/2} \frac{\sin^2(\omega t)}{M - \sin(\omega t)}\,dt \tag{4}$$

where V_M is the peak input voltage, *M* is the conversion ratio (V_o/V_M), and L_e is the parallel combination of inductors L_1, L_2, and L_o. Note that the integral part in (4) can be simplifies as

$$\int_0^{T_L/2} \frac{\sin^2(\omega t)}{M - \sin(\omega t)}dt = \int_0^{T_L/2} \left(-\sin(\omega t) - M + \frac{M^2}{M - \sin(\omega t)}\right) dt. \tag{5}$$

Solving (5) and substituting into (4) and using the fact that (4) is equal to the average current through the load (V_o/R_L), the switch control cycle can be expressed as function of *M* as follows:

$$d_1 = \sqrt{\frac{KM}{\alpha}} \tag{6}$$

where α and *K* are expressed as

$$\alpha = -\frac{2}{\pi} - M + \frac{2M^2}{\pi\sqrt{M^2-1}}\left[\frac{\pi}{2} + \tan^{-1}\left(\frac{1}{\sqrt{M^2-1}}\right)\right] \tag{7}$$

$$K = \frac{2L_e}{T_s R_L}. \tag{8}$$

B. Input Current and Effective Input Resistance

Using the ideal waveforms of Fig. 5, the average output current over a switching cycle can be represented by

$$\overline{i_o} = \frac{1}{4}\frac{d_1^2 T_s v_{ac}^2}{L_e v_{C1}} \tag{9}$$

where

$$v_{C1} = \frac{V_o - v_{ac}}{2}. \tag{10}$$

Using instantaneous power balance principle and by assuming a lossless converter

$$v_{ac}\, i_{ac} = V_o \overline{i_o}. \tag{11}$$

The effective input resistance can be derived by substituting (9) and (10) into (11) and it is given by

$$R_{e\_\text{in}} = \frac{v_{ac}}{i_{ac}} = \frac{M - \sin(\omega t)}{M}\left(\frac{2L_e}{d_1^2 T_s}\right). \tag{12}$$

Examining (12) it can be easily seen that the resistance is nonlinear as it depends on v_{ac}. Equation (12) also shows that when *M* is large, line current becomes less distorted and almost sinusoidal. On the other hand, low values of *M* (i.e., as *M* approaches unity) causes distortion of the line current and increased harmonic content. Therefore, the DCM operation of the proposed converter is similar to the DCM operation of classical boost converter, where operation as a perfect PFC is not expected due to the presence of the third harmonic component in the input current. This is unlike "Buck-Boost family" converters (Buck-Boost, Flyback, Sepic, Cuk, and ZETA) which are considered as perfect PFC converters (i.e., unity power factor) if they are designed to operate in DCM with voltage-follower control. Therefore, the proposed rectifier shown in Fig. 2 is hybrid combinations of a Boost converter and a SEPIC, where operation as a perfect PFC is not expected. However, simple open-loop control scheme can be implemented for providing unity power factor at constant switching frequency [21].

C. Boundaries Between CCM and DCM

Referring to the diode D_o current waveform in Fig. 5, the DCM operation mode requires that the sum of the duty cycle and the normalized switch-off time length be less than one

$$d_2 < 1 - d_1. \tag{13}$$

The principle of inductor volt–second balance was applied on the three inductors L_1, L_2, and L_o and the duty cycle of the second stage d_2 can be expressed as

$$d_2 = \frac{2\sin(\omega t)}{M - \sin(\omega t)} d_1 \tag{14}$$

substituting (14) into (13) and using (10), the following condition for DCM is obtained:

$$K < K_{\text{crit}} = \left(\frac{M - \sin(\omega t)}{M + \sin(\omega t)}\right)^2 \left(\frac{\alpha}{M}\right) \tag{15}$$

where K_{crit} is the critical value of *K* operating at DCM that has a maximum and minimum values depending on the input line angle ωt.

D. Inductors Design

The inductor values are calculated using inductor current ripple equation shown below

$$\Delta i_{L1} = \frac{v_{ac}(t)}{2L_1} d_1 T_s. \tag{16}$$

The maximum inductor current ripple can be calculated from the peak input current

$$\Delta i_{L1-\text{Max}} = 10\% i_{ac\_\text{peak}}. \tag{17}$$

By substituting (17) into (16), the input inductances L_1 and L_2 can be calculated. The value of inductance L_o can be found from the following relation:

$$\frac{1}{L_e} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_o}. \tag{18}$$

E. Intermediate Capacitor Design

The energy transfer capacitors C_1 and C_2 are important elements in the proposed topology since their values greatly influence the quality of input line current. These capacitors are designed under the following constraints:

To present nearly constant voltage value during switching cycle and to follow the input voltage profile during line cycle. The resonant frequency between (L_1, C_1, L_o, and C_3) during DCM stage of the switching cycle shown in Fig. 4(c) must be much greater than the line frequency (f_L) to avoid input current oscillations at every line half cycle and lower than switching frequency (f_s) to assure constant voltage in a switching period

$$f_L < f_r < f_s \tag{19}$$

where

$$f_r = \frac{1}{2\pi\sqrt{(L_1 + L_o)(C_1 + C_3)}}. \tag{20}$$

Based on the conditions in (17) and (18), the value of $C_1 = C_2 = C_3 = 1.2\ \mu F$ is chosen for this particular design.

F. Output Capacitor C_o

The output capacitor must be large enough to minimize the output voltage ripple since the output voltage ripple frequency is twice the input line frequency [17]. The output filter capacitor (C_o) is determined as in bridgeless Sepic rectifier proposed in [18]. For an output voltage ripple equal to 2% of the output voltage, the output capacitance is expressed as

$$C_o = \frac{1}{\Delta v_{Co}}\left(\frac{d_1^2 T_s V_M^2}{4L_e V_{C1}}\left(\frac{T_L}{8} + \frac{T_L}{4\pi}\right) - \frac{V_o T_L}{4R_L}\right) \tag{21}$$

where

$$V_{C1} = \frac{V_o - V_M}{2}. \tag{22}$$

TABLE I
COMPONENTS USED IN THE PROPOSED RECTIFIER

Parameters	Value	Type
Inductor L_1 and L_2	2.2 mH	Toroid Inductor from Wilco, part no. DC4-2200, 4 A, $R_{\rm DC} = 0.419\ \Omega$
Inductor L_o	180 μH	Toroid Inductor from Wilco, part no. DC4-180, 11.4 A, $R_{\rm DC}$ M Ω
Capacitor C_1, C_2, and C_3	1.2 μF	Polypropylene, 1000 V
Capacitor C_o	1000 μF	Electrolytic, 450 V
Diodes D_p and D_n	–	SBR10U300CT Schottky, 600 V, 8 A, $V_f = 0.89$ V
Diodes D_1, D_2 and Do	–	BY329 Fast recovery, 1000 V, 8 A, $V_f = 1.5$ V
Switches Q_1 and Q_2	–	STW34NM60ND, 600 V, 29 A, ESR $= 0.011\ \Omega$

TABLE II
SEMICONDUCTORS VOLTAGE AND CURRENT STRESS

Component	Peak Voltage Stress	Peak Current Stress	RMS Current Stress
Q_1 and Q_2	$\frac{V_M+V_o}{2}$	$\frac{d_1 T_s}{L_e} V_M$	$\frac{V_M}{K R_L} \times \sqrt{\frac{d_1^3}{3}}$
D_1 and D_2	$\frac{V_M+V_o}{2}$	$\frac{d_1 T_s}{2 L_e} V_M$	$ID^*_{1,\rm rms}$
D_o	$\frac{V_M+V_o}{2}$	$\frac{d_1 T_s}{2 L_e} V_M$	$\sqrt{2} \times ID^*_{1,\rm rms}$
D_n and D_p	V_M	$\frac{2P_o}{V_M}$	$\frac{P_o}{V_M}$

*$ID_{1,\rm rms} = \frac{V_M}{K R_L}\sqrt{\frac{2d_1^3}{3}\left(\frac{M^3}{\pi\sqrt{M^2-1}}\left[\frac{\pi}{2}+\tan^{-1}\left(\frac{1}{\sqrt{M^2-1}}\right)\right]-\frac{1}{4}-\frac{M}{\pi}-\frac{M^2}{2}\right)}$.

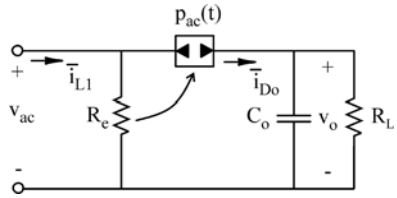

Fig. 6. Loss-free resistor model at steady state.

G. Design Procedure

A simplified design procedure is presented in this section to determine the component values of the proposed rectifier for the following power stage specifications.

1) input voltage: 120 V at 50 Hz;
2) output voltage: 400 V;
3) output power: 200 W;
4) switching frequency $f_s = 50$ kHz;
5) maximum input current ripple $\Delta i_{L1} = 10\%$ of fundamental input current;
6) output voltage ripple $\Delta v_o = 2\%$ of V_o.

From the aforementioned data and assuming that the efficiency is 100%, the values of the circuit components are calculated based on the following procedure:

1) find $K_{\rm crit}$ from (15);
2) find L_e from (8) for a given $K < K_{\rm crit}$ (e.g., $K = 0.85\ K_{\rm crit}$);
3) calculate duty cycle d_1 using (6);
4) find L_1 and L_2 from (16) and (17);
5) find L_o from (18);
6) find C_1, C_2, and C_3 from (20) for a given f_r (e.g., $f_r =$ 2 kHz);
7) find C_o from (21).

Based on the above procedure, the components for the above operating point are shown in Table I. Table I also shows types of diodes and switches types that have been utilized in the experimental prototype.

H. Semiconductor Devices Stresses

The expressions for the semiconductors devices voltage and current stresses for the proposed rectifier are given in Table II. Referring to Table II, it is clear that the power switch in the proposed topology is subjected to a lower voltage stress compared with the conventional boost and Sepic converters. Therefore, the proposed topology appears to be promising candidate for high-voltage gain PFC applications.

I. Large Signal Model

As mentioned previously, one of the advantages of designing the rectifier to operate in DCM is that the input current follows input voltage profile naturally. This means that the rectifier appears as an emulated resistor and the power factor is almost unity. The average switch voltage over a switching cycle can be expressed as

$$\langle v_{Q1}(t)\rangle_{Ts} = \langle v_{ac}(t)\rangle_{Ts}\,. \tag{23}$$

The average switch current over a switching cycle can be derived by integrating the switch current waveform depicted in Fig. 5

$$\langle i_{Q1}(t)\rangle_{Ts} = \frac{d_1^2 T_s}{2L_e}\,\langle v_{ac}(t)\rangle_{Ts}\,. \tag{24}$$

Dividing (23) by (24) gives

$$\frac{\langle v_{Q1}(t)\rangle_{Ts}}{\langle i_{Q1}(t)\rangle_{Ts}} = \frac{2L_e}{d_1^2 T_s} = R_e. \tag{25}$$

Equation (25) shows that the switch Q_1 emulates a resistor with resistance R_e. Following the same procedures, the average voltage and current of the output diode D_o over a switching cycle can be obtained and are given by

$$\langle v_{Do}(t)\rangle_{Ts} = \langle v_{C1}(t)\rangle_{Ts} \tag{26}$$

$$\langle i_{Do}(t)\rangle_{Ts} = \frac{d_1^2 T_s}{4L_e}\frac{\langle v_{ac}(t)\rangle_{Ts}^2}{\langle v_{C1}(t)\rangle_{Ts}}. \tag{27}$$

Then, by multiplying (26) and (27), the equivalent power out of the diode D_o can be expressed as

$$\langle v_{Do}(t)\rangle_{Ts}\,\langle i_{Do}(t)\rangle_{Ts} = \frac{\langle v_{ac}(t)\rangle_{Ts}^2}{2R_e} = \frac{\langle p_{ac}(t)\rangle_{Ts}}{2}. \tag{28}$$

According to (25) and (28), the switch network could be modeled by a loss-free resistor and a controlled power source as shown in Fig. 6. For sinusoidal input voltage, the instantaneous power delivered to the power source $P_{ac}(t)$ is

$$p_{ac}(t) = \frac{V_m^2}{2R_e}\sin^2(\omega t) = \frac{V_m^2}{2R_e}(1-\cos(2\omega t)). \tag{29}$$

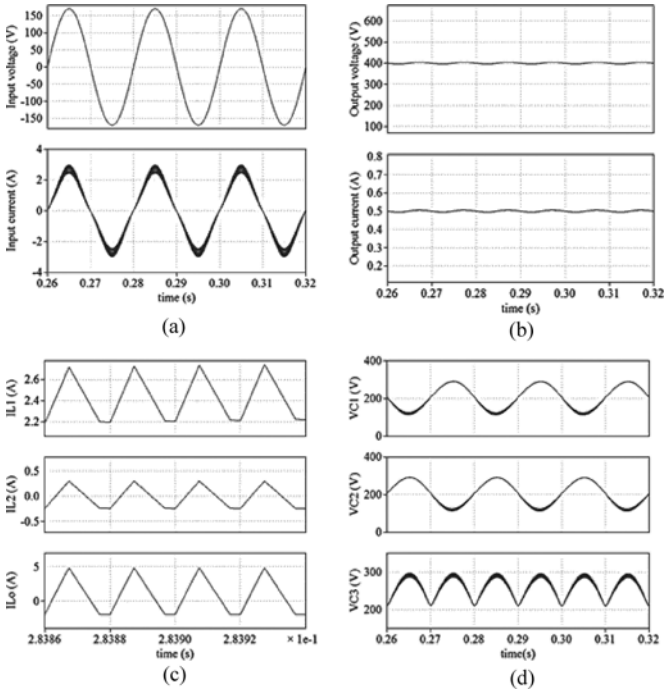

Fig. 7. Simulation results (a) Input current and voltage. (b) Output current and voltage. (c) Inductors L_1, L_2, and L_o switching currents. (d) Voltage across capacitors C_1, C_2, and C_3.

As a result, the voltage across the output capacitor C_o must have ripple at $2f_L$. For output voltage regulation, the feedback loop cannot attempt to remove the capacitor voltage ripple at the second harmonic of the line frequency. Removal of the second-harmonic voltage through feedback would cause significant distortion of the ac line current.

J. Simulation

The proposed rectifier of Fig. 2 has been simulated using the calculated components and power stage specification presented in the previous section. The simulated input voltage and current are in phase as it is shown in Fig. 7(a) which ensures power factor correction property of the proposed circuit. It is clear that the desired output voltage (400 V) is met as it is illustrated in Fig. 7(b). The DCM operation can be clearly noted by observing the switching current waveforms of the three inductors L_1, L_2, and L_o as shown in Fig. 7(c). Finally, the voltage across the intermediate capacitors C_1, C_2, and C_3 are shown in Fig. 7(d). Fig. 8(a) and (b) shows the input current and voltage for uncoupled and coupled inductors, respectively.

K. Static Gain

The converter static gain has been compared to the conventional boost and conventional Sepic [6] in DCM. The gain was calculated by assuming that all inductors in the three converters have the same inductance value of 100 μH and they are operating at the same switching frequency of 50 kHz and delivering 200-W load power at an output voltage of 400 V.

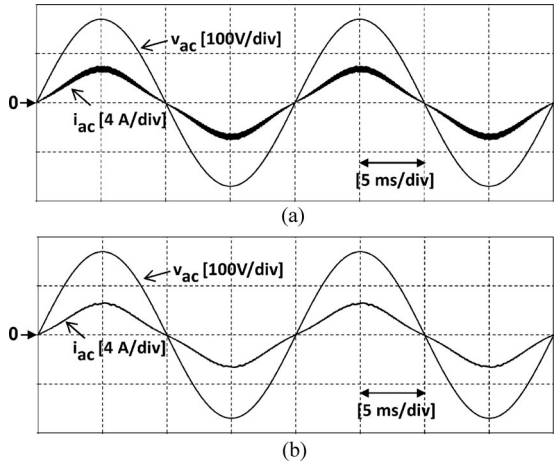

Fig. 8. Simulated input current and input voltage for the converter of Fig. 2(a). (a) Uncoupled inductors case. (b) Coupled inductors case.

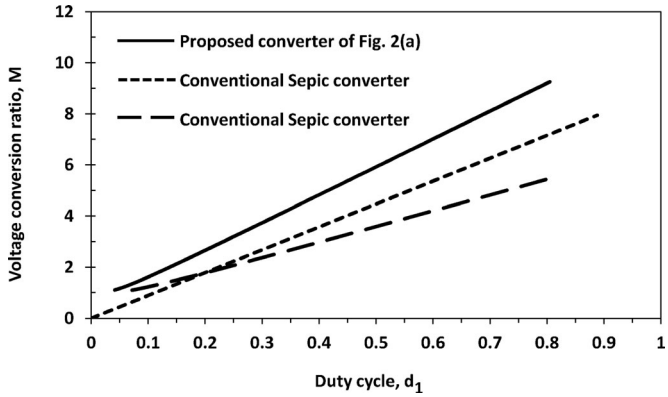

Fig. 9. Converter voltage gain in DCM as function of duty cycle for modified Sepic, conventional boost, and conventional Sepic converters.

Fig. 9 shows the DCM gain characteristic for each topology as function of duty cycle, d_1. Fig. 9 shows that for a given duty cycle d1, the proposed converter of Fig. 2(a) has higher voltage gain as compared to the conventional boost and conventional Sepic converters. This is true since the proposed converter has the lowest value of the dimensionless parameter *K* (i.e., lowest equivalent inductance value).

V. Feedback Control

It is required to have a transfer function with good approximation representing the dynamic behavior of the converter to design a feedback control for the proposed rectifier. However, Equations (4) and (6) are highly nonlinear equations and complex to use to develop small signal model of the converter. To simplify it, the integration term in (5) can be approximated using MATLAB curve fitting tool box as follows:

$$I_{D_O} = \frac{d_1^2 T_s V_M}{2L_e}\left(\frac{0.48}{M-0.92}\right). \tag{30}$$

Using power balance principle and assuming 100% efficiency, the average input current over a half-line cycle can be

represented by the following relation:

$$i_{ac} = \frac{d_1^2 T_s}{L_e} V_o \left(\frac{0.48}{M - 0.92} \right). \tag{31}$$

A. Small Signal Modeling

The equivalent circuit of the injected current "CIECA" was used to construct the system model [22]–[24]. To derive the small signal model, the equations of input current and output averaged over half-line cycle are required. Equations (6) and (7) were calculated in Section IV. These equations are linearized around a quiescent operating point as follows:

$$\begin{aligned} &v_{ac} = V_M + \hat{v}_{ac}, \quad v_o = V_o + \hat{v}_o, \quad d_1 = D + \hat{d}_1, \\ &i_o = I_o + \hat{i}_o, \quad i_{ac} = I_M + \hat{i}_{ac} \end{aligned} \tag{32}$$

where the *ac* variations are small in magnitude compared to the dc quiescent values

$$\hat{v}_{ac} \ll V_M, \ \hat{v}_o \ll V_o, \ \hat{d}_1 \ll D, \ \hat{i}_o \ll I_o, \ I_M \ll \hat{i}_{ac}. \tag{33}$$

The linearized input current can be expressed in a canonical form by using 3-D Taylor series expansion about the quiescent point (V_M, V_o and D) [25]

$$\hat{i}_{ac} = j_1 \hat{d}_1 + g_1 \hat{v}_o + \frac{1}{r_1} \hat{v}_{ac} \tag{34}$$

where the coefficients (j_1, g_1, r_1) can be calculated by

$$j_1 = \frac{2 d_1 T_s}{L_e} V_o V_M \left(\frac{0.48}{V_o - 0.92 V_M} \right) \tag{35}$$

$$g_1 = \frac{(V_o - 0.92 V_M) \left(\frac{0.48 d_1^2 T_s}{L_e} V_M \right) - \left(\frac{0.48 d_1^2 T_s}{L_e} V_M V_o \right)}{(V_o - 0.92 V_M)^2} \tag{36}$$

$$\frac{1}{r_1} = \frac{(V_o - 0.92 V_M) \left(\frac{0.48 d_1^2 T_s}{L_e} V_o \right) - \left(\frac{(0.44) d_1^2 T_s}{L_e} V_M V_o \right)}{(V_o - 0.92 V_M)^2}. \tag{37}$$

In addition, the linear result of the output current after perturbation is

$$\hat{i}_o = j_2 \hat{d}_1 + g_2 \hat{v}_{ac} + \frac{1}{r_2} \hat{v}_o \tag{38}$$

where the coefficients (j_2, g_2, r_2) are

$$j_2 = \frac{d_1 T_s}{L_e} V_M^2 \left(\frac{0.48}{V_o - 0.92 V_M} \right) \tag{39}$$

$$g_2 = \frac{(V_o - 0.92 V_M) \left(\frac{0.48 d_1^2 T_s V_M}{L_e} \right) + \left(\frac{(0.22) d_1^2 T_s V_M^2}{L_e} \right)}{(V_o - 0.92 V_M)^2} \tag{40}$$

$$\frac{1}{r_2} = \frac{0.48 d_1^2 T_s V_M^2}{2 L_e (V_o - 0.92 V_M)}. \tag{41}$$

Using the canonical form equations, the average small signal model can be constructed as depicted in Fig. 10. Using Fig. 10, output-to-control $G_{vd}(s)$, output-to-input $G_{vg}(s)$, and output impedance $Z_{\text{out}}(s)$ can be expressed as follows:

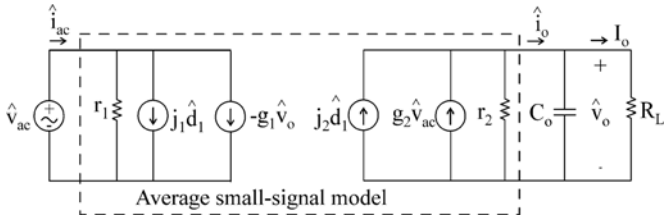

Fig. 10. Small-signal equivalent circuit for the proposed rectifier.

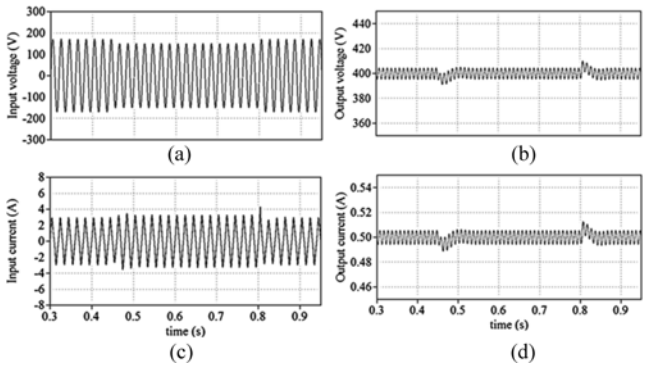

Fig. 11. Simulated closed-loop response under input voltage disturbances: (a) Input line voltage. (b) Output voltage. (c) Input current. (d) Load current.

$$G_{vd}(s) = \frac{j_2 (R_L // r_2)}{1 + s(C_o (R_L // r_2))} \tag{42}$$

$$G_{vg}(s) = \frac{g_2 (R_L // r_2)}{1 + s(C_o (R_L // r_2))} \tag{43}$$

$$Z_{\text{out}}(s) = \frac{r_2 // R_L}{1 + s C_o (r_2 // R_L)}. \tag{44}$$

It is clear that the three transfer functions are consisting of one stable pole with no right-half plane zeros or poles.

B. Controller Design

A lag compensator represented by (45) is adapted for this design. The crossover frequency is selected to be well below twice the line frequency, to avoid excessive second-harmonic injection from the output voltage into the input current

$$G_C(s) = 2 \left(1 + \frac{100}{s} \right). \tag{45}$$

C. Closed-Loop Simulation

Fig. 11 shows the simulated transient response of the input and output voltages and currents due to input voltage disturbances. In addition, the effect of load variation is considered. Fig. 12 presents the regulation of the output voltage under 50% load variations for the proposed rectifier with the lag compensator.

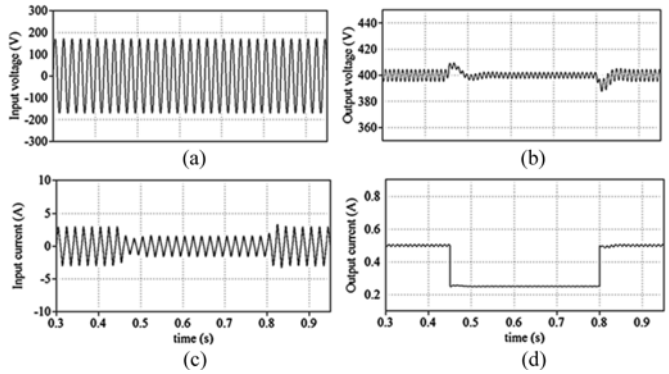

Fig. 12. Simulated closed-loop response when subjected to an output load change: (a) Input line voltage. (b) Output voltage. (c) Input current. (d) Load current.

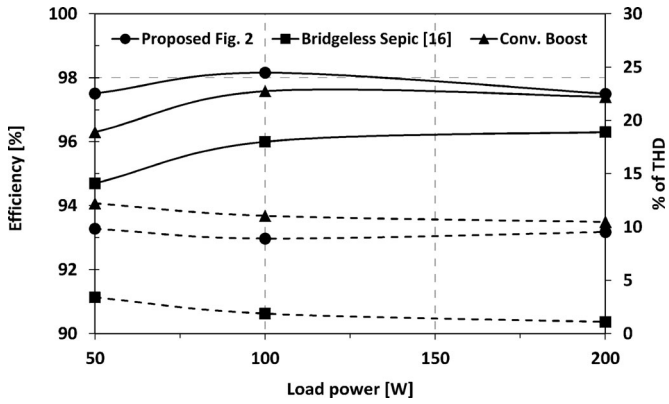

Fig. 13. Efficiency (solid line) and percent of THD (dashed line) as a function of load power at an input voltage of 120 $V_{\rm rms}$.

D. Comparison With the Full-Bridge Modified SEPIC Rectifier

A comparison between the proposed circuit shown in Fig. 2 and the modified full bridge SEPIC rectifier of Fig. 1 has been performed at a load of 200 W. In addition, the proposed topology has been compared to bridgeless Sepic and bridgeless boost converters. To ensure a fair comparison, both topologies are selected to operate at the same operating point of $K = 0.85\ K_{\rm crit}$, and output power of 200 W. Moreover, an equivalent series resistor (ESR) of 50 mΩ is placed in series with all inductors and capacitors.

Furthermore, Pspice actual semiconductor models have been used to simulate the switches. The THD variation and converter efficiency for the proposed topology, conventional bridgeless boost, and bridgeless Sepic converters were obtained and depicted in Fig. 13. As shown in Fig. 13, the conventional bridgeless Sepic converter has the lowest THD because it is a perfect PFC converter unlike the proposed modified Sepic and boost converters. Fig. 14 shows comparison in terms of power factor and THD between the full-bridge modified Sepic of [20] and the proposed topology while Fig. 15 compares both topologies in terms of efficiency. The following equation is used to calculate

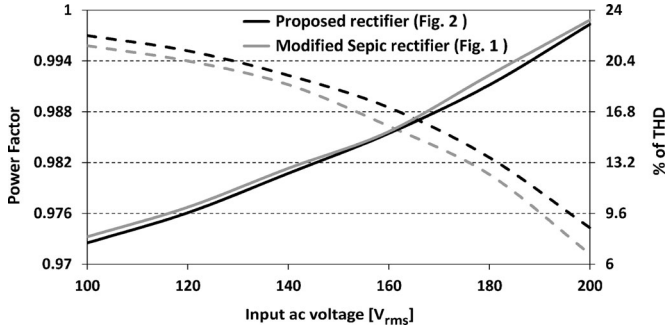

Fig. 14. Power factor (dashed line) and percent of THD (solid line) as a function of input ac voltage at $P_{\rm out} = 200$ W.

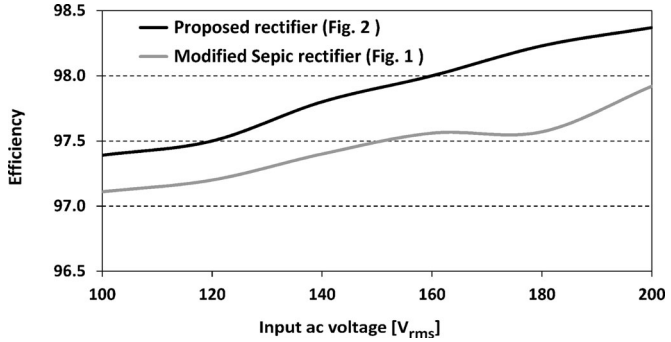

Fig. 15. Conversion efficiency as a function of input voltage at $P_{\rm out} = 200$ W.

TABLE III
COMPARISON AT 120 $V_{\rm rms}$ INPUT VOLTAGE, 400-V OUTPUT VOLTAGE AND 200 W AT CCM/DCM BOUNDARY CONDITION

Item	Proposed converter	Conventional Boost	Conventional Bridgeless Sepic [17]
Duty cycle at operating point	$d_1 = \frac{V_o - V_M}{V_o + V_M} = 0.4$	$d_1 = \frac{V_o - V_M}{V_o} = 0.57$	$d_1 = \frac{V_o}{V_o + V_M} = 0.7$
Minimum critical inductance for DCM operation ($L_{\rm crit}$)	$\left(\frac{M-1}{M+1}\right)^2 \frac{\alpha}{M} \frac{R_L T_S}{2}$ $= 190\mu$H	$\frac{M-1}{2M^3} \frac{R_L T_S}{2}$ $= 415\mu$H	$\frac{R_L T_S}{4(M+1)^2}$ $= 355\mu$H
Active switch voltage stress	$\frac{V_M + V_o}{2} = 285$ V	$V_o = 400$ V	$V_M + V_o = 570$ V

the power factor of the converter:

$$\mathrm{PF} = \frac{1}{\sqrt{1 + (\mathrm{THD})^2}}. \tag{46}$$

Table III presents the switch voltage stresses of the proposed topology, boost, and conventional Sepic converters. As shown in Table III, the modified Sepic converter has lower switch stress and lower inductance to guarantee DCM operation. In addition,

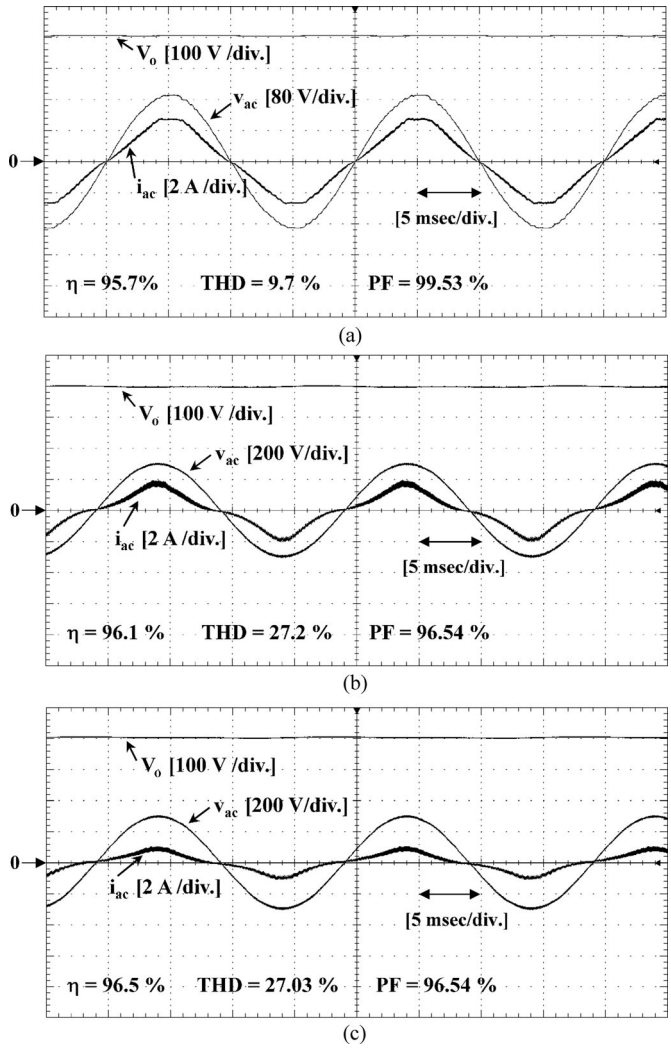

Fig. 16. Experimental result at 400 V output voltage. (a) $V_{\rm ac} = 120\ V_{\rm rms}$ and $P_{\rm out} = 200$ W. (b) $V_{\rm ac} = 220\ V_{\rm rms}$ and $P_{\rm out} = 200$ W. (c) $V_{\rm ac} = 220\ V_{\rm rms}$ and $P_{\rm out} = 100$ W.

Fig. 13 shows that the proposed topology has higher efficiency than the bridgeless boost and bridgeless Sepic, however, the bridgeless Sepic has lower THD.

It shall be noted that the measured efficiencies shown in Fig. 16 are less than the simulated ones. This can be attributed to imperfection in the simulated models of the components versus the ones used in the prototype.

VI. Experimental Results

A laboratory prototype has been constructed using the same component values shown in Table I to validate the theoretical analysis and simulation results. Fig. 16(a) and (b) presents the input line current, input voltage, and output voltage at an input voltage of 120 $V_{\rm rms}$ and 220 $V_{\rm rms}$ and a load power of 200 W, respectively. Fig. 16(c) presents line input current, input voltage, and load voltage at a load power of 100 W. It can be observed from Fig. 16 that the input line current is in phase with the input voltage. However, the THD at $220V_{\rm rms}$ is higher than that at

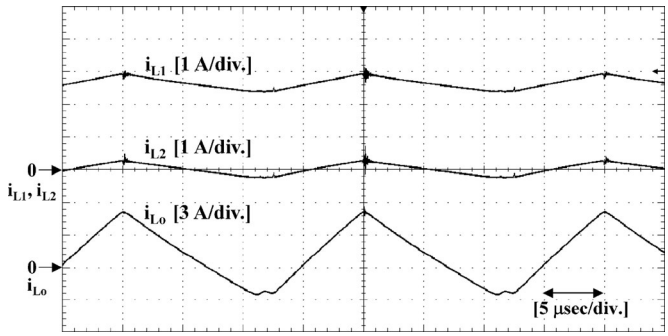

Fig. 17. Experimental results: Inductors L_1, L_2 and L_o switching level current. ($V_{\rm ac} = 120\ V_{\rm rms}$, $V_{\rm out} = 400$ V, and $P_{\rm out} = 200$ W).

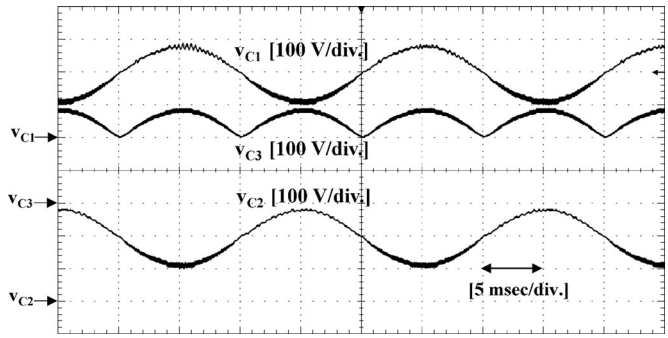

Fig. 18. Experimental results: Voltage across capacitors C_1, C_2, and C_3. ($V_{\rm ac} = 120\ V_{\rm rms}$, $V_{\rm out} = 400$ V, and $P_{\rm out} = 200$ W).

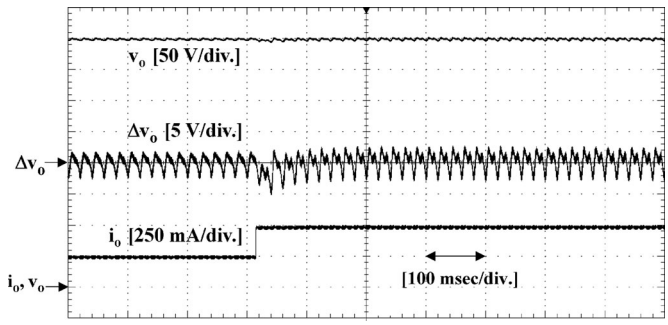

Fig. 19. Experimental results: Output voltage and output current response due to 50% load step up.

120 $V_{\rm rms}$ as predicted in (12). Fig. 17 shows the current waveform at switching level through the three inductors L_1, L_2, and L_3 which clearly verify the DCM operation. The intermediate capacitors C_1, C_2, and C_3 line voltages waveforms are shown in Fig. 18. It is clear that the experimental results are consistent with the simulation results depicted in the previous section. The designed lag compensator was implemented into the prototype to check its effect during disturbance existence. Fig. 19 represents the first test condition, the load is stepped up by 50% from 100 to 200 W, the output voltage, ripple voltage, and output current waveforms are depicted and it is clear that the output voltage is tightly regulated due to the lag compensator. In the second test condition, the load is stepped down by 50% from

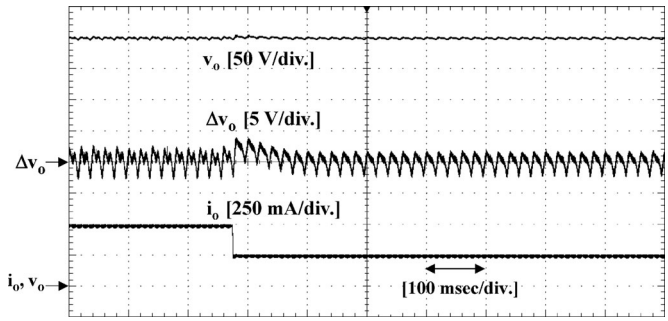

Fig. 20. Experimental results: Output voltage and output current response due to 50% load step down.

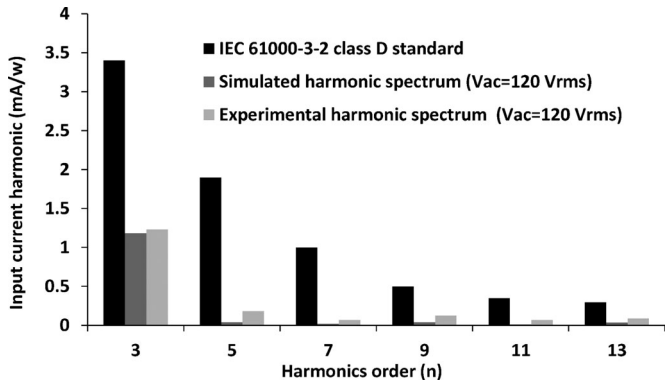

Fig. 21. Simulated and experimental harmonic spectrum for input line current of the proposed circuit compared to IEC 61000-3-2 class D standard at an input voltage of 120 $V_{\rm rms}$.

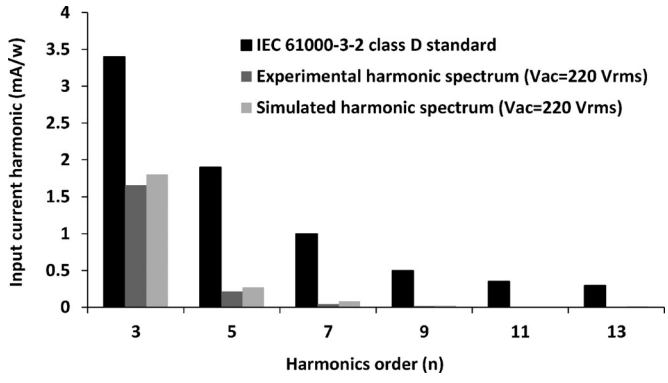

Fig. 22. Simulated and experimental harmonic spectrum for input line current of the proposed circuit compared to IEC 61000-3-2 class D standard at an input voltage of 220 $V_{\rm rms}$.

200 to 100 W and the response of the output voltage, ripple voltage, and output current is shown in Fig. 20. As a result, the disturbance caused by load variations can be rejected using lag compensator. Finally, the simulated and experimental harmonic spectrum in the input line current compared with IEC 61000-3-2 Class D standard at input voltages of 120 $V_{\rm rms}$ and 220 $V_{\rm rms}$ are shown in Figs. 21 and 22, respectively.

VII. Conclusion

A new topology based on modified SEPIC has been presented. The proposed topology has a higher efficiency than the full bridge topology. In addition, the proposed topology exhibits lower voltage stress over the whole input voltage range than the conventional Sepic and boost converters. Approximated large and small signal models have been presented. A simple closed-loop controller design based on the derived small-model has been presented and the capability of the controller at load transients and input disturbances has been presented. The two power switches in the proposed topology can be driven by the same control signal, which significantly simplifies the control circuitry. Simulation and experimental results have been presented to validate the operation of the proposed circuit at open-loop- and closed-loop conditions.

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