# An Online Modulation Strategy to Control the Matrix Converter Under Unbalanced Input Conditions

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***Abstract*—Due to absence of a dc-link energy storage element in the direct matrix converter (MC), any abnormality/disturbance in the input voltages is directly reflected on the output voltages. In this paper, a new modulation strategy to control the 3×3 MC under unbalanced input voltage conditions is proposed. The proposed strategy is based on modification of the space vector modulation strategy, which formulates and solves an optimization problem to determine the best switching states and their corresponding optimal duty cycles, such that the errors in the output voltages and the input currents under unbalanced input voltage conditions are minimized. The salient feature of the proposed strategy is its capability to extend the output operating range of the MC. The proposed strategy ensures that optimal performance of the MC over the entire operating range, including the case when the converter operates with an output voltage greater than the maximum attainable balanced output voltage under unbalanced input voltage conditions, is achieved. Performance of the proposed strategy is evaluated and validated based on time-domain simulation studies in the MATLAB/Simulink software environment and experimentation on a scaled-down laboratory prototype.**

***Index Terms*—Abnormal input voltages, matrix converter (MC), space vector modulation (SVM).**

## I. Introduction

THE absence of a dc-link energy storage makes the direct matrix converter (MC) more sensitive to any disturbance in the input voltages. Majority of modulation strategies developed for the MC are based on the assumption of balanced input voltages. Consequently, if the input voltages of the MC are subjected to any disturbance/imbalance, low-order harmonics are introduced in the output voltages and input currents of the converter. Furthermore, under unbalanced input voltage conditions, the maximum attainable balanced output voltages of the MC is reduced [1]–[3].

In the technical literature, a few methods have been proposed to mitigate the impacts of unbalanced input voltages on the performance of the MC [2]–[11]. The methods presented in [4]–[7] reduce the undesirable harmonics in the output voltages of the MC. The proposed methods in [1], [2], [8], [10], and [12] target improving the quality of the input currents, while generating balanced voltages at the output of the converter. In [5]–[7], the converter modulation strategy is modified to calculate the duty cycles of the switches based on instantaneous values of the input voltages. In [6], to mitigate the presence of undesired harmonics in the output voltages, the duty cycles of the switches are calculated based on the instantaneous values of the input voltages. In [5], the unbalanced input voltages are decomposed into the positive and negative sequence components, and the duty cycles of the switches are calculated such that the negative sequence component of the output voltages is enforced to be zero. In [4], the voltage gain of the MC is updated based on the fuzzy logic, and the duty cycles are calculated based on the Alesina–Venturini strategy. In [7], the gain of the MC is calculated based on the instantaneous values of the input voltages and the duty cycles of the switches are calculated using the indirect space vector modulation (SVM) strategy. In [9] and [3], a feed-forward method, based on the instantaneous measurement of the input voltages is proposed. In [1], [2], and [8] authors improve the quality of the input currents under unbalanced conditions. In [10], the modulation strategy proposed in [13] is modified to eliminate the undesirable harmonics in the input currents. This method introduces negative sequence components in the reference currents to improve the quality of the input currents. In [2], two approaches are proposed and analyzed to improve the quality of the input currents based on selection of the reference angle of the input currents. In the first approach, the input current vector is chosen to be in phase with the input voltage vector. In the second approach, the input current vector is calculated based on the positive and negative sequence components of the input voltages. Li *et al.* [8] propose three methods to select the phase angle of the input current: 1) In the first method, the phase angle is calculated based on the positive and negative sequence components of the input voltages, 2) in the second method, the input currents are chosen to be in phase with the input voltages, and 3) in the third method, the input currents are chosen to be in phase with the positive sequence of the input voltages. In all of the aforementioned methods, the maximum attainable voltage gain of the MC, which under ideal and balanced input voltage conditions is limited to 0.86, is further reduced [3], [11].

In this paper, a new modulation strategy is developed to optimizes the performance of the MC in terms of the output power quality under unbalanced input voltage conditions, when operating with a voltage gain less or greater than the maximum attainable one. The developed modulation strategy modifies the conventional direct SVM strategy to operate the MC under unbalanced input voltage conditions. The implementation of the proposed strategy involves calculation of optimal duty cycles of

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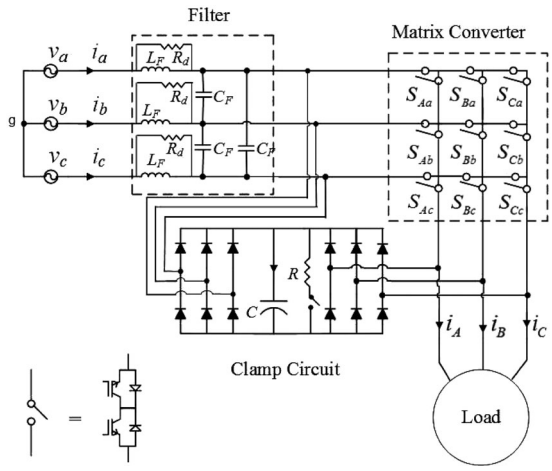


Fig. 1. Circuit diagram of the 3 × 3 MC.

the switching states to ensure that errors in the output voltages and the phase of the input currents are minimized. The duty cycles of the corresponding switching states are calculated based on formulating and solving an optimization problem. Performance of the proposed modulation strategy is evaluated based on time-domain simulation studies in the MATLAB/Simulink software environment and experimentation on a scaled-down laboratory prototype. The study results demonstrate capability of the proposed strategy to operate the MC under unbalanced input voltages, with improved output power quality.

The rest of this paper is organized as follows. Section II provides a brief overview of the conventional SVM strategy for the MC. Section III discusses the impacts of unbalanced input voltages on the operation of the MC. Section IV presents the proposed modulation strategy. Section V reports the study results and Section VI concludes the paper.

## II. Overview of the SVM Strategy for the MC

Fig. 1 shows a schematic diagram of a three-phase to three-phase MC in which the input and output voltages (currents) are $v_a, v_b, v_c (i_a, i_b, i_c)$ and $v_A, v_B, v_C (i_A, i_B, i_C)$, respectively. The converter circuit is comprised of nine bidirectional switches that allow connection of any of the output phases to each of the input phases. Since input terminals $a, b$, and $c$ are connected to voltage sources, they must not be short circuited through the MC switches. Similarly, since output terminals $A, B$, and $C$ are connected to current sources, they must not be open circuited at any instant. Based on the constraints, the MC has 27 permissible switching states. The SVM strategy is based on instantaneous space vector representation of the output line-to-line voltages and input currents generated by the 27 permissible switching states [14]. Out of 27 switching states, six of them are referred as the synchronous switching states. For these switching states, each output phase is connected to a different input phase. Eighteen of the switching states referred as the active switching states are shown in Fig. 2. For these switching states, two of the output phases are connected to the same input phase, and the third output phase is connected to a different input phase. Each

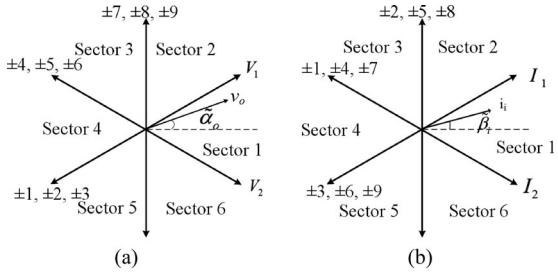


Fig. 2. Space vector representation of (a) output line-to-line voltages and (b) input currents of the MC.

of the eighteen active switching states is assigned a number between $\pm 1$ and $\pm 9$. The output voltage/input current vectors of a pair of active switching states with the same number and opposite signs have the same magnitude in opposite directions. The remaining three switching states are zero states. Based on the position of the reference output voltage and current vectors as shown in Fig. 2, the SVM strategy selects four active switching states that have vector components along the desired direction and a zero switching state to modulate the MC. Table I lists the active vectors that can be used for various voltage sector $(K_V)$ and current sector $(K_I)$ combinations.

The duty cycles of the selected switching vectors, i.e., $d_I, d_{II}, d_{III}$, and $d_{IV}$, as well as the zero vector $d_0$ for unity power factor at the input are [14]

$$d_I = \frac{2}{\sqrt{3}} q \cos\left(\tilde{\alpha_o} - \frac{\pi}{3}\right) \cos\left(\tilde{\beta_i} - \frac{\pi}{3}\right) \tag{1a}$$

$$d_{II} = \frac{2}{\sqrt{3}} q \cos\left(\tilde{\alpha_o} - \frac{\pi}{3}\right) \cos\left(\tilde{\beta_i} + \frac{\pi}{3}\right) \tag{1b}$$

$$d_{III} = \frac{2}{\sqrt{3}} q \cos\left(\tilde{\alpha_o} + \frac{\pi}{3}\right) \cos\left(\tilde{\beta_i} - \frac{\pi}{3}\right) \tag{1c}$$

$$d_{IV} = \frac{2}{\sqrt{3}} q \cos\left(\tilde{\alpha_o} + \frac{\pi}{3}\right) \cos\left(\tilde{\beta_i} + \frac{\pi}{3}\right) \tag{1d}$$

$$d_0 = 1 - d_I - d_{II} - d_{III} - d_{IV} \tag{1e}$$

where $\tilde{\alpha_o}$ $(\tilde{\beta_i})$, as shown in Fig. 2, represents the phase angle of output voltage (input current) vector with respect to the bisecting line of the sector and $q$ is the gain of the converter. Finally, the active and zero switching states are arranged and applied in a sequence that requires minimum number of commutations.

## III. Operation of the MC Under Unbalanced Input Voltage Conditions

In the technical literature, various modulation strategies have been proposed to synthesize the reference output voltage of the MC with unity power factor [15]–[17]. The proposed modulation strategies are developed based on the assumption of balanced voltages on the input side of the converter. Any imbalance, sag or spike in the input voltages significantly impacts the performance of the MC. The impacts of unbalanced input voltages on the output voltages, input currents, and maximum attainable voltage gain of the MC have been investigated in the literature [1], [3], [11], [18].

TABLE I
SWITCHING STATES FOR VARIOUS VOLTAGE AND CURRENT SECTOR COMBINATIONS

| $K_I$ | 1 | | | | 2 | | | | 3 | | | | 4 | | | | 5 | | | | 6 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $K_V$ | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | −3 | +1 | +6 | −4 | +9 | −7 | −3 | +1 | −6 | +4 | +9 | −7 | +3 | −1 | −6 | +4 | −9 | +7 | +3 | −1 | +6 | −4 | −9 | +7 |
| 2 | +2 | −3 | −5 | +6 | −8 | +9 | +2 | −3 | +5 | −6 | −8 | +9 | −2 | +3 | +5 | −6 | +8 | −9 | −2 | +3 | −5 | +6 | +8 | −9 |
| 3 | −1 | +2 | +4 | −5 | +7 | −8 | −1 | +2 | −4 | +5 | +7 | −8 | +1 | −2 | −4 | +5 | −7 | +8 | +1 | −2 | +4 | −5 | −7 | +8 |
| 4 | +3 | −1 | −6 | +4 | −9 | +7 | +3 | −1 | +6 | −4 | −9 | +7 | −3 | +1 | +6 | −4 | +9 | −7 | −3 | +1 | −6 | +4 | +9 | −7 |
| 5 | −2 | +3 | +5 | −6 | +8 | −9 | −2 | +3 | −5 | +6 | +8 | −9 | +2 | −3 | −5 | +6 | −8 | +9 | +2 | −3 | +5 | −6 | −8 | +9 |
| 6 | +1 | −2 | −4 | +5 | −7 | +8 | +1 | −2 | +4 | −5 | −7 | +8 | +1 | +2 | +4 | −5 | +7 | −8 | −1 | +2 | −4 | +5 | +7 | −8 |
| | I | II | III | IV | I | II | III | IV | I | II | III | IV | I | II | III | IV | I | II | III | IV | I | II | III | IV |

### A. Impact on the Output Voltages

Under balanced input voltage conditions, the input voltage vector has a constant magnitude and angular frequency while under unbalanced conditions, both magnitude and the angular frequency become time variant. In this case, the input voltage space vector can be represented as the summation of positive and negative sequence components by

$$\overline{\boldsymbol{v}}_{\boldsymbol{i}} = \overline{\boldsymbol{v}}_{\boldsymbol{ip}} + \overline{\boldsymbol{v}}^{*}_{\boldsymbol{in}} = \overline{\boldsymbol{V}}_{\boldsymbol{p}} e^{j\omega_i t} + \overline{\boldsymbol{V}}^{*}_{\boldsymbol{n}} e^{-j\omega_i t}$$
$$\overline{\boldsymbol{V}_{\boldsymbol{p}}} = V_P \angle \alpha_p, \overline{\boldsymbol{V}_{\boldsymbol{n}}} = V_N \angle \alpha_n. \quad (2)$$

The switching functions/strategies developed for balanced input voltages, when applied to unbalanced conditions, introduce harmonics in the output voltages due to the presence of the negative sequence components in the input voltages. The studies in [18] show that under unbalanced input voltage conditions, low-order harmonics of order of $(2\omega_i \pm \omega_o)$ appear in the output voltages, which lead to the distorted output voltages and, consequently, distorted output currents as well.

### B. Impact on the Input Currents

To maintain unity power factor at the input side of the MC, the reference input current vector is chosen in phase with the input current vector. Consequently, under unbalanced conditions, the angular frequency of the reference input current, which should be kept in phase with the input voltage vector, varies over time. The theoretical analysis in [2] shows that the input current vector under unbalanced conditions is represented as

$$\overline{\boldsymbol{i}}_i = \left(\frac{4}{3}\right) \frac{e^{-j\beta_i}}{2\cos\beta_i} \left[ \sum_{k=1,3,\ldots}^{\infty} \frac{p_o}{\overline{\boldsymbol{V}_{\boldsymbol{p}}}^{*}} \left( -\frac{\overline{\boldsymbol{V}_{\boldsymbol{n}}}}{\overline{\boldsymbol{V}_{\boldsymbol{p}}}^{*}} \right)^{\frac{k-1}{2}} e^{jk\omega_i t} \right] \quad (3)$$

where $p_o$ is the output power. Based on (3), under unbalanced conditions, the input current has low-order positive sequence harmonics whose magnitude decay by an unbalance factor of $\frac{|\overline{\boldsymbol{V}_{\boldsymbol{n}}}|}{|\overline{\boldsymbol{V}_{\boldsymbol{p}}}|}$.

### C. Impact on the Maximum Attainable Output Voltage

As investigated in [1], [3], and [11], under unbalanced input voltage conditions, the maximum attainable output voltage of the MC is reduced. In [1], it is shown that the maximum attainable balanced output voltages under unbalanced input voltage conditions is limited to

$$V_o \leq \frac{\sqrt{3}}{2}(V_P - V_N). \quad (4)$$

To ensure that, under unbalanced input voltage conditions, the output voltages of the MC do not contain low-order harmonics, the existing modulation strategies are modified to accommodate this goal [2]–[11]. However, little attention has been paid to evaluate and/or improve the performance of MC, when operating with an output voltage greater than $\frac{\sqrt{3}}{2}(V_P - V_N)$. In this paper, a new modulation strategy that aims at optimizing the performance of the MC under unbalanced input voltage conditions while operating, in particular, with a voltage gain larger than the maximum attainable gain is developed. Although synthesis of the desired output voltages with a voltage gain larger than the maximum attainable one is not achievable within all time instants, the developed strategy ensures optimal performance of the MC in terms of the output power quality. Optimal performance of the MC is achieved by formulating and solving an optimization problem, which determines the duty cycles of the switching states such that the error between the average voltages synthesized by the MC and their reference voltages is minimized.

## IV. THE PROPOSED MODULATION STRATEGY

The circuit configuration of the MC allows generating the load voltages with controllable magnitude and frequency, as well as maintaining the unity power factor at the input side. The objective of the developed modulation strategy is to synthesize the reference output voltage of the MC and to maintain unity power factor at the input. The developed modulation strategy is based on modification of the conventional direct SVM strategy to optimize the converter performance. In the proposed strategy, the corresponding duty cycles of the selected switching states are calculated by solving an optimization problem that 1) minimizes the error between the average voltages synthesized by the switching states and the reference voltages and 2) aligns the input current vector along the desired direction. The implementation of the developed SVM strategy within each sampling period $T_s$ includes the following steps:

1) determination of the direction of input current vector;
2) identification of the location of reference output voltage and input current vectors;

3) for a given voltage and current sector combination, determination of four switching vectors that have vector components in the desired directions;
4) determination of the duty cycles of selected switching states.

In the technical literature, various methods have been proposed to improve the quality of the input currents of the MC operating under unbalanced input voltage conditions [1], [2], [8], [10]. In [2], two approaches are proposed and analyzed to improve the quality of the input currents based on selection of the reference angle of the input currents. In the first approach, the input current vector is chosen to be in phase with the input voltage vector. In the second approach, the input current vector is calculated based on the positive and negative sequence components of the input voltages. The theoretical analysis in [2] shows that the second approach reduces the harmonic content of the input currents without appreciably increasing the rms value of the currents. The experimental results in [12] confirm the effectiveness of the second approach in reducing the harmonic content of the input currents. In this paper, the direction of the current vector is chosen based on the second approach proposed in [2], which ensures that the input currents only includes the positive and negative sequence components of fundamental frequency. The input current direction $\beta_i$ as shown in Fig. 2 is varied dynamically as follows:

$$\beta_i = \text{angle}\left(\overline{\boldsymbol{v}}_{\boldsymbol{ip}} - \overline{\boldsymbol{v}}_{\boldsymbol{in}}^{*}\right) = \text{angle}\left(\overline{\boldsymbol{V}}_{\boldsymbol{p}} e^{j\omega_i t} - \overline{\boldsymbol{V}}_{\boldsymbol{n}}^{*} e^{-j\omega_i t}\right). \quad (5)$$

The implementation procedure for the steps 2 and 3 is similar to the conventional SVM strategy as discussed in Section II. However, in step 4, the duty cycles of the switching states are calculated based on solving an optimization problem formulated as

$$\begin{aligned}
&\text{Minimize}\\
&[V_{1,\text{ref}} - (V_{1,I}\, d_I + V_{1,II}\, d_{II})]^2\\
&\quad + [V_{2,\text{ref}} - (V_{2,III}\, d_{III} + V_{2,IV}\, d_{IV})]^2\\
&\quad + [I_{2,\text{ref}} I_{1,I}\, d_I - I_{1,\text{ref}} I_{2,II}\, d_{II}]^2\\
&\quad + [I_{2,\text{ref}} I_{1,III}\, d_{III} - I_{1,\text{ref}} I_{2,IV}\, d_{IV})]^2\\
&\text{Subject to}\\
&d_I + d_{II} + d_{III} + d_{IV} \le 1, d_k \ge 0, d_k \le 1,\\
&\quad \text{for } k \in \{I, II, III, IV\} \qquad (6)
\end{aligned}$$

where $V_{1,\text{ref}}$ and $V_{2,\text{ref}}$ ($I_{1,\text{ref}}$ and $I_{2,\text{ref}}$) are the components of the output voltage (input current) reference vector along $V_1$ ($I_1$) and $V_2$ ($I_2$) as indicated in Fig. 3. $V_{1,I}$ ($V_{1,II}$, $V_{1,III}$, $V_{1,IV}$) and $V_{2,I}$ ($V_{2,II}$, $V_{2,III}$, $V_{2,IV}$) are the components of the output voltage vector along $V_1$ and $V_2$ for the switching vectors $V_I$ ($V_{II}$, $V_{III}$, $V_{IV}$). $I_{1,I}$ ($I_{1,II}$, $I_{1,III}$, $I_{1,IV}$) and $I_{2,I}$ ($I_{2,II}$, $I_{2,III}$, $I_{2,IV}$) are the components of the input current for the switching vectors $V_I$ ($V_{II}$, $V_{III}$, $V_{IV}$). The constraints of the optimization problem in (6) ensure that the duty cycles of the switching states belong to [0, 1] and their summation is less than or equal to 1.

Without loss of generality, both output voltage and input current reference vectors are assumed to be in Sector 1. As shown in Table I, the switching states $-3$, $+1$, $+6$, and $-4$ are used

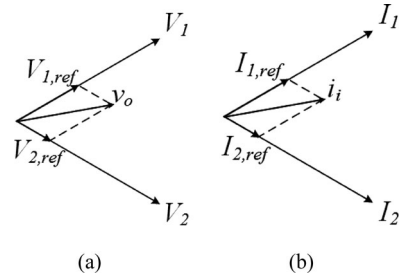


Fig. 3. Components of (a) the output voltage and (b) input current vectors of the MC along the sector boundaries.

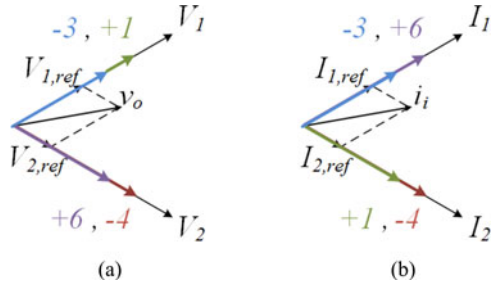


Fig. 4. Components of (a) the output voltage and (b) input current vectors of the selected switching states when $K_V = 1$ and $K_I = 1$.

to modulate the MC. The output voltage and input current vectors generated by these switching states are shown in Fig. 4. In Fig. 4, the boundaries of output voltage (input current) sector are represented by $V_1$ and $V_2$ ($I_1$ and $I_2$), respectively. The components of the reference output voltage (input current) vector along $V_1$ ($I_1$) and $V_2$ ($I_2$) are given as $V_{1,\text{ref}}$ and $V_{2,\text{ref}}$ ($I_{1,\text{ref}}$ and $I_{2,\text{ref}}$), respectively. As illustrated in Fig. 4(a), component of the output voltage vector generated by the switching states $-3$ and $+1$ along $V_2$ is zero, i.e., $V_{2,I}$ and $V_{2,II}$ are equal to zero. Furthermore, component of the output voltage vector generated by the switching states $+6$ and $-4$ along $V_1$ is also zero, i.e., $V_{1,III}$ and $V_{1,IV}$ are equal to zero. Similarly, component of the input current vector for the switching states $-3$ and $+6$ ($+1$ and $-4$) along $I_1$ ($I_2$) is zero. The duty cycles $d_I$ and $d_{II}$ of the switching states $-3$ and $+1$ are calculated such that the error between the component of reference voltage along $V_1$, i.e., $V_{1,\text{ref}}$ and voltage generated by the switching states $-3$ and $+1$ is minimized, while the input current vector is along the desired direction. The first term of (6) minimizes the error between the average voltages synthesized by the switching states $-3$ and $+1$ and the reference voltage $V_{1,\text{ref}}$. To ensure that the input current vectors generated by the switching states $-3$ and $+1$ are along the desired direction, the following conditions should be satisfied [14]:

$$\begin{aligned}
d_I I_{1,I} &= I_{1,\text{ref}}\\
d_{II} I_{2,II} &= I_{2,\text{ref}}. \qquad (7)
\end{aligned}$$

The third term of the optimization problem (6) ensures that the error between the input current vector and its reference vector is minimized. Similarly, the second term of the optimization problem (6) minimizes the error between the average voltages synthesized by the switching states $+6$ and $-4$ and the reference

voltage $V_{2,\mathrm{ref}}$. The fourth term of the optimization problem (6) ensures that error between the input current vector and its reference vector is minimized. By expanding the terms, the objective function of the optimization problem in (6) can be rewritten as

$$\begin{aligned}\text{Minimize}\ \ & f(d_I, d_{II}, d_{III}, d_{IV}) = K_1 d_I^2 + K_2 d_{II}^2 + K_1 d_{III}^2 \\ & + K_2 d_{IV}^2 + K_3 d_I d_{II} + K_3 d_{III} d_{IV} + K_{4a} d_I \\ & + K_{5a} d_{II} + K_{4b} d_{III} + K_{5b} d_{IV} + K_{6a} + K_{6b} \quad (8)\end{aligned}$$

where

$$K_1 = V_{1,I}^2 + I_{2,\mathrm{ref}}^2, K_2 = V_{1,II}^2 + I_{1,\mathrm{ref}}^2 \quad (9a)$$

$$K_3 = 2(V_{1,I} V_{1,II} - I_{1,\mathrm{ref}} I_{2,\mathrm{ref}}) \quad (9b)$$

$$K_{4a} = -2(V_{1,\mathrm{ref}} V_{1,I}), K_{5a} = -2(V_{1,\mathrm{ref}} V_{1,II}) \quad (9c)$$

$$K_{6a} = V_{1,\mathrm{ref}}^2 \quad (9d)$$

$$K_{4b} = -2(V_{2,\mathrm{ref}} V_{2,I}), K_{5b} = -2(V_{2,\mathrm{ref}} V_{2,II}) \quad (9e)$$

$$K_{6b} = V_{2,\mathrm{ref}}^2. \quad (9f)$$

The optimization problem of (6) is a nonlinear optimization problem with inequality constraints. The solution to (6) can be obtained by calculation of the values that satisfies the Karush–Kuhn–Tucker (KKT) conditions, which are first-order necessary conditions [19]. The constraint space of the optimization problem can be divided into 31 regions in which the solution lies within one of those regions. However, this approach is complicated and may not be implementable in real time as the calculation burden is significantly high. To resolve this issue and for the sake of simplicity, a simplified method that can be implemented in real time is developed to solve the optimization problem of (6). The developed simplified method, which essentially solves the optimization problem of (6) with reduced computational effort, decomposes of the optimization problem in (6) into two sub-optimization problems expressed by

$$\begin{aligned}&\text{Minimize}\ [V_{1,\mathrm{ref}} - (V_{1,I} d_I + V_{1,II} d_{II})]^2 \\ &+ [I_{2,\mathrm{ref}} I_{1,I} d_I - I_{1,\mathrm{ref}} I_{2,II} d_{II}]^2 \quad (10)\\ &\text{Subject to} \\ &d_I + d_{II} \le a_1,\ \ d_k \ge 0,\ \ d_k \le 1, \quad \text{for } k \in \{I, II\}\end{aligned}$$

and

$$\begin{aligned}&\text{Minimize}\ [V_{2,\mathrm{ref}} - (V_{2,III} d_{III} + V_{2,IV} d_{IV})]^2 \\ &+ [I_{2,\mathrm{ref}} I_{\alpha,III} d_{III} - I_{1,\mathrm{ref}} I_{2,IV} d_{IV})]^2 \quad (11)\\ &\text{Subject to} \\ &d_{III} + d_{IV} \le a_2,\ \ d_k \ge 0,\ \ d_k \le 1, \quad \text{for } k \in \{III, IV\}.\end{aligned}$$

The objective functions of the optimization problems in (10) and (11) are convex and their solutions can be obtained by calculating the values that satisfy the KKT conditions [19]. The constraint $d_I + d_{II} + d_{III} + d_{IV} \le 1$ of the optimization problem in (6) couples the sub-optimization problems in (10) and (11). This constraint, i.e., $d_I + d_{II} + d_{III} + d_{IV} \le 1$, is split into two constraints, i.e., $d_I + d_{II} \le a_1$ and $d_{III} + d_{IV} \le a_2$. The summation of the constants $a_1$ and $a_2$ is equal to one. If either of $a_1$ or $a_2$ is fixed, then, the two sub-optimization problems can be solved separately. However, since neither $a_1$ nor $a_2$ is fixed, the following approach is followed to solve the optimization problems:

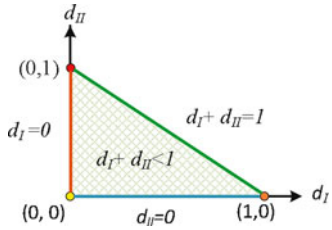


Fig. 5. Constraint space of the optimization problem of (10).

1) solve the optimization problem of (10) to find $d_I$ and $d_{II}$ with $a_1 = 1$;
2) solve the optimization problem of (11) to find $d_{III}$ and $d_{IV}$ with $a_2 = 1$;
3) verify if the constraint $d_I + d_{II} + d_{III} + d_{IV} \le 1$ is satisfied. If the constraint is not satisfied, recalculate the duty cycles based on the formulae given in Table III.

The optimization problems of (10) and (11) are similar. Therefore, to avoid repetition, only the solution to problem (10) is discussed. By expanding the terms of the objective function, the optimization problem in (10) can be rewritten as

$$\begin{aligned}&\text{Minimize}\ f(d_1, d_2) = K_1 d_1^2 + K_2 d_2^2 + K_3 d_1 d_2 + K_{4a} d_1 \\ &+ K_{5a} d_2 + K_{6a} \quad (12)\\ &\text{Subject to} \\ &d_I + d_{II} \le a_1,\ \ d_k \ge 0,\ \ d_k \le 1, \quad \text{for } k \in \{I, II\}\end{aligned}$$

where

$$K_1 = V_{1,I}^2 + I_{2,\mathrm{ref}}^2,\ \ K_2 = V_{1,II}^2 + I_{1,\mathrm{ref}}^2 \quad (13a)$$

$$K_3 = 2(V_{1,I} V_{1,II} - I_{1,\mathrm{ref}} I_{2,\mathrm{ref}}),\ \ K_{4a} = -2(V_{1,\mathrm{ref}} V_{1,I}) \quad (13b)$$

$$K_{5a} = -2(V_{1,\mathrm{ref}} V_{1,II}),\ \ K_{6a} = V_{1,\mathrm{ref}}^2. \quad (13c)$$

The constraint space of the optimization problem represented in Fig. 5, can be divided into seven regions listed in Table II. The solution to the problem is in a specific region if the corresponding inequalities of each condition are satisfied in that region. The optimal solution to the optimization problem in each region can be obtained by equations listed in the corresponding solution column of Table II. To calculate the corresponding duty cycles, the coefficients of the objective function should be found using (13). Subsequently, the conditions for region 1 listed in Table II are evaluated, and if satisfied, the duty cycles are calculated using the corresponding formulae. Otherwise, the algorithm proceeds to evaluate the conditions in region 2 to find the optimal values of the duty cycles $d_I$ and $d_{II}$. $d_{III}$ and $d_{IV}$ are calculated by a similar procedure as well. Subsequently, if the constraint $d_I + d_{II} + d_{III} + d_{IV} \le 1$ is satisfied, the obtained values are the optimal solution. If the constraint

TABLE II
SOLUTIONS TO THE OPTIMIZATION PROBLEM IN VARIOUS REGIONS

| Region | Constraints | Condition | Solution |
|---|---|---|---|
| 1 | $d_I = 1, d_{II} = 0$ | $K_3 + K_{5a} - 2K_1 - K_{4a} > 0, 2K_1 + K_{4a} < 0$ | $d_I = 1, d_{II} = 0$ |
| 2 | $d_I = 0, d_{II} = 1$ | $2K_2 + K_{5a} < 0, -2K_2 - K_{5a} + K_3 + K_{4a} < 0$ | $d_I = 0, d_{II} = 1$ |
| 3 | $d_I + d_{II} = 1$ | $-(K_{4a} + K_3) - \frac{K_{5a}+2K_2-K_{4a}-K_3}{2K_1+2K_2-2K_3} > 0$ | $d_I = \frac{K_{5a}+2K_2-K_{4a}-K_3}{2(K_1+K_2-K_3)}, d_{II} = 1 - d_I$ |
| 4 | $d_I = 0, d_{II} = 0$ | $K_{4a} > 0, K_{5a} > 0$ | $d_I = 0, d_{II} = 0$ |
| 5 | $d_{II} = 0$ | $-K_3K_{4a} + 2K_1K_{5a} > 0$ | $d_{II} = 0, d_I = \frac{-K_{4a}}{2K_1}$ |
| 6 | $d_I = 0$ | $-K_3K_{5a} + 2K_2K_{4a} > 0$ | $d_I = 0, d_{II} = \frac{-K_{5a}}{2K_2}$ |
| 7 | $d_I + d_{II} < 1$ | $d_I, d_{II} \in [0, 1]$ | $d_I = \frac{K_3K_{5a}-2K_{4a}K_2}{K_3^2-4K_1K_2}, d_{II} = \frac{2K_1K_3-K_{4a}K_3}{K_3^2-4K_1K_2}$ |

TABLE III
RECALCULATION OF THE DUTY CYCLES

| | Recalculated duty cycles |
|---|---|
| $d_I, d_{II}, d_{III}, d_{IV} \in (0, 1)$ | $d_{I,r} = d_I + \frac{\Delta d c_2}{2(c_1+c_2)}, d_{II,r} = d_{II} + \frac{\Delta d c_1}{2(c_1+c_2)}, d_{III,r} = d_{III} + \frac{\Delta d c_2}{2(c_1+c_2)}, d_{IV,r} = d_{IV} + \frac{\Delta d c_1}{2(c_1+c_2)}$ |
| $d_I = 0$ | $d_{II,r} = d_{II} + \Delta d \frac{c_3}{c_3+2K_2(c_1+c_2)}, d_{III,r} = d_{III} + \Delta d \frac{2K_2c_1}{c_3+2K_2(c_1+c_2)}, d_{IV,r} = 1 - d_{II,r} - d_{III,r}$ |
| $d_{II} = 0$ | $d_{I,r} = d_I + \Delta d \frac{c_3}{c_3+2K_2(c_1+c_2)}, d_{III,r} = d_{III} + \Delta d \frac{2K_1c_1}{c_3+2K_1(c_1+c_2)}, d_{IV,r} = 1 - d_{I,r} - d_{III,r}$ |
| $d_{III} = 0$ | $d_{IV,r} = d_{IV} + \Delta d \frac{c_3}{c_3+2K_2(c_1+c_2)}, d_{I,r} = d_I + \Delta d \frac{2K_1c_1}{c_3+2K_1(c_1+c_2)}, d_{II,r} = 1 - d_{IV,r} - d_{I,r}$ |
| $d_{IV} = 0$ | $d_{III,r} = d_{III} + \Delta d \frac{c_3}{c_3+2K_2(c_1+c_2)}, d_{I,r} = d_I + \Delta d \frac{2K_1c_1}{c_3+2K_1(c_1+c_2)}, d_{II,r} = 1 - d_{III,r} - d_{I,r}$ |
| $d_I = 0, d_{III} = 0$ | $d_{II,r} = d_{II} + \frac{\Delta d}{2}, d_{IV,r} = 1 - d_{II,r}$ |
| $d_{II} = 0, d_{IV} = 0$ | $d_{I,r} = d_I + \frac{\Delta d}{2}, d_{III,r} = 1 - d_{I,r}$ |
| $d_I = 0, d_{IV} = 0$ | $d_{II,r} = d_{II} + \frac{\Delta d K_1}{K_1+K_2}, d_{III,r} = 1 - d_{II,r}$ |
| $d_{II} = 0, d_{III} = 0$ | $d_{IV,r} = d_{IV} + \frac{\Delta d K_1}{K_1+K_2}, d_{I,r} = 1 - d_{IV,r}$ |

is not satisfied, the duty cycles are recalculated based on the formulae given in Table III. The formulae that can be used to recalculate the duty cycles are based on the values obtained in steps 1 and 2. The values of coefficients $c_1$, $c_2$, and $c_3$ are defined as $c_1 = K_3 - 2K_1, c_2 = K_3 - 2K_2, c_3 = 4K_1K_2 - K_3^2$, $\Delta d = 1 - (d_I + d_{II} + d_{III} + d_{IV})$. The coefficients $K_1$, $K_2$, and $K_3$ are defined in (13). The detailed mathematical solution to the optimization problem is provided in the Appendix.

## V. PERFORMANCE EVALUATION

This section presents a set of simulation and experimental results to evaluate the performance and effectiveness of the proposed modulation strategy under unbalanced input voltage conditions. The simulation studies are conducted in the MATLAB/Simulink software environment. The bidirectional switches of the prototype MC are realized using the back-to-back IGBTs with antiparallel diodes in the common-collector configuration. The experimental studies are performed using a 2-kVA scaled-down prototype. The bidirectional switches of the MC are realized by back-to-back connection of IRG7PH35UD1 IGBT modules in the common collector configuration. A four-step commutation strategy based on the current sign measurement is employed to commutate the bidirectional switches. The control is implemented using the National Instruments cRIO controller system. The block diagram of the control implemented in the cRIO system is shown in Fig. 6. The parameters of the study system and the prototype including the input filter, input supply, and load are listed in Table IV. The laboratory prototype of the MC is shown in Fig. 7. The proposed modulation strategy is implemented with the switching frequency of 10 kHz, corresponding to the switching period of 100 $\mu$s. The performance of the MC operating with the proposed strategy under unbalanced input voltage conditions with a reference

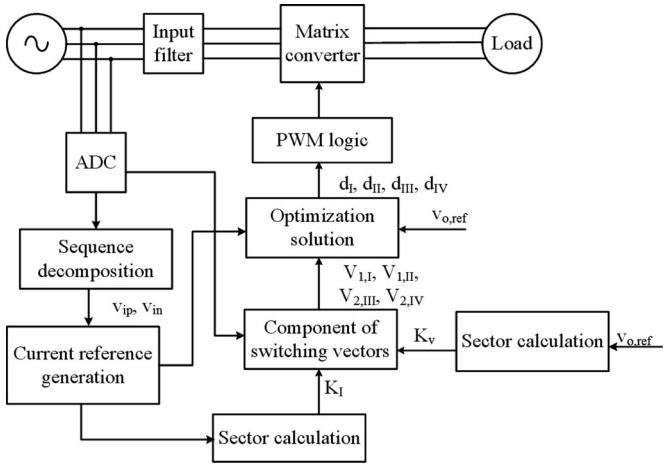


Fig. 6. Implementation block diagram of the proposed strategy.

TABLE IV
PARAMETERS OF THE STUDY SYSTEM

| Parameter | Value | Parameter | Value | Parameter | Value |
|---|---|---|---|---|---|
| $V_{\text{in}}$ | 100 V | $L_f$ | 2 mH | $C$ | 100 $\mu$F |
| $f_{\text{in}}$ | 60 Hz | $C_f$ | 4.7 $\mu$F | $R_L$ | 25 $\Omega$ |
| $f_{\text{sw}}$ | 10 kHz | $R_d$ | 33 $\Omega$ | $L_L$ | 40 mH |

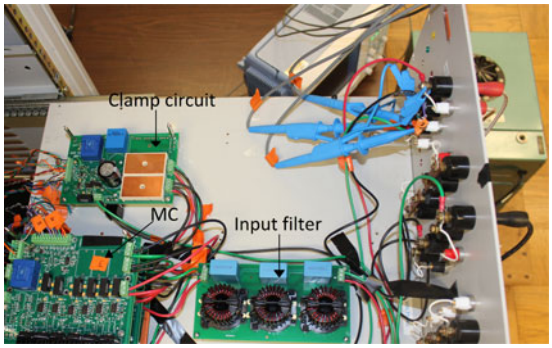


Fig. 7. Experimental setup.

output voltage less and greater than the maximum attainable output voltage is evaluated. As given in (5), the input current direction $\beta_i$ is varied dynamically for the SVM and the proposed strategies. The coefficients defined in (9) are calculated using per unit values of voltage and current. The magnitudes of the reference output voltage and the current are chosen as the base values.

### A. Simulation Results

Simulation studies are conducted in the MATLAB/Simulink environment for the MC, when subjected to 20% unbalanced input voltages by injecting a negative sequence set of voltages, i.e., $V_N = 20\angle 0°$ in addition to the positive-sequence voltages, i.e., $V_P = 100\angle 0°$. Performance of the proposed modulation strategy is evaluated for the following operating conditions. 1) An output voltage magnitude and frequency of 50 V and 60 Hz, respectively and 2) an output voltage magnitude and frequency of 86 V and 60 Hz, respectively. The input current reference angle is generated based on the method described in Section IV.

The simulated waveforms of the MC of Fig. 1 under the operating condition 1) are shown in Fig. 8. The three-phase unbalanced input voltages and the angle of the input current reference are shown in Figs. 8(a) and (b), respectively. The three-phase load and input currents are shown in Figs. 8(c) and (d), respectively. The value of the objective function defined in (10) is provided in Fig. 8(e). As shown in Fig. 8, for a reference output voltage of 50 V, the duty cycles of the switches can be calculated such that the MC operates at the desired reference voltage and current reference angle. Therefore, the value of the objective function defined in (10) remains zero.

The simulated waveforms of the MC system of Fig. 1 under the operating condition 2) are shown in Fig. 10. The three-phase load and input currents are shown in Figs. 10(c) and (d),

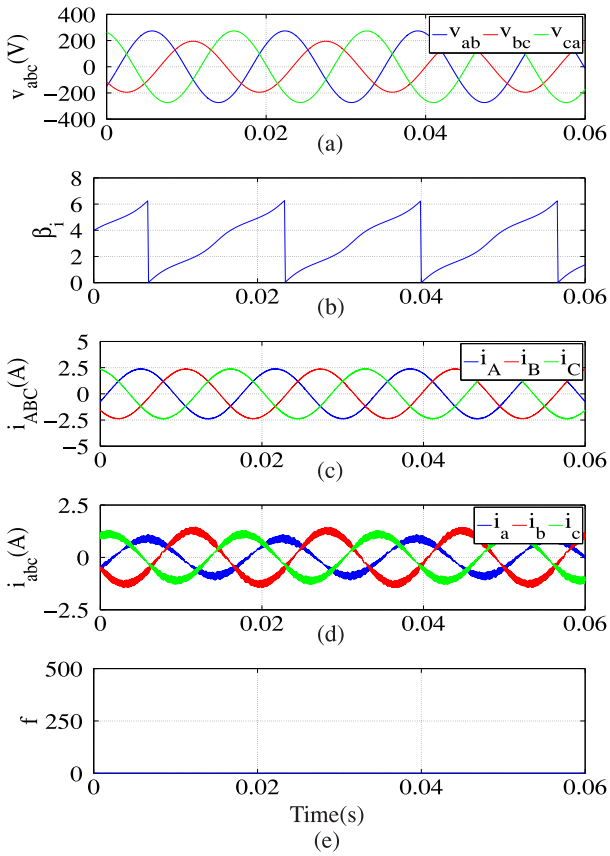


Fig. 8. Simulation waveforms of the MC operating with the proposed modulation strategy under unbalanced input voltage conditions when $V_o = 50$ V and $f_o = 60$ Hz: (a) input voltages, (b) angle of the reference input current, (c) three-phase load currents, (d) three-phase input currents, and (e) Value of the objective function defined in (10).

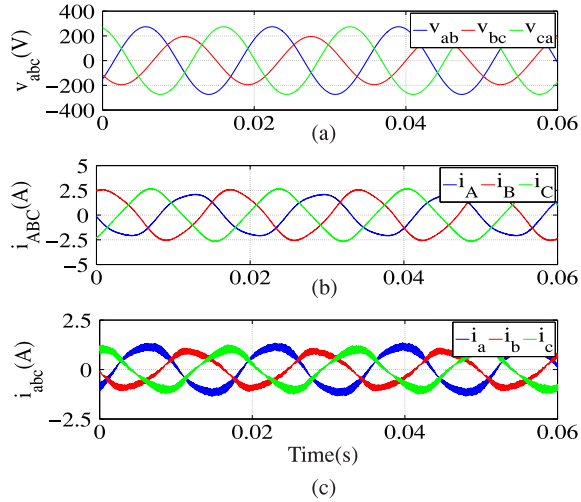


Fig. 9. Simulation waveforms of the MC operating with the SVM strategy under unbalanced input voltage conditions when $V_o = 50$ V and $f_o = 60$ Hz: (a) input voltages, (b) three-phase load currents, and (c) three-phase input currents.

respectively. The value of the objective function defined in (10) is provided in Figs. 10(e). Based on the Fig. 10, for a reference output voltage of 86 V, the value of the objective function defined in (10) is nonzero at some instants, indicating that it is not

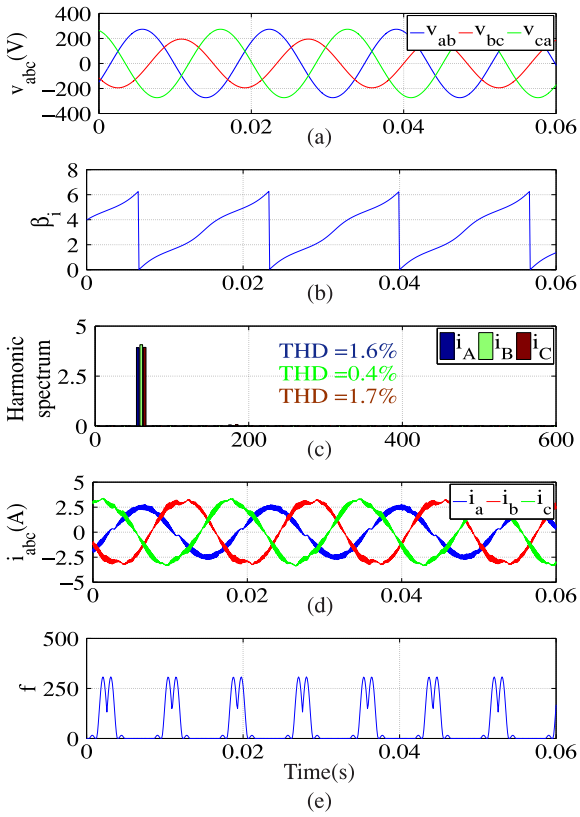


Fig. 10. Simulation waveforms of the MC operating with the proposed modulation strategy under unbalanced input voltage conditions when $V_o = 86$ V and $f_o = 60$ Hz: (a) input voltages, (b) angle of the reference input current, (c) Three-phase load currents, (d) three-phase input currents, and (e) value of the objective function defined in (10).

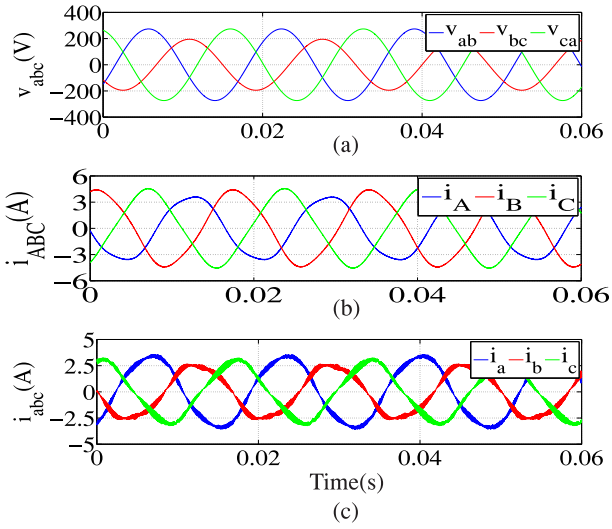


Fig. 11. Simulation waveforms of the MC operating with the SVM strategy under unbalanced input voltage conditions when $V_o = 86$ V and $f_o = 60$ Hz: (a) input voltages, (b) three-phase load currents, and (c) three-phase input currents.

possible to generate the desired reference output voltage and input current angle. However, the proposed modulation strategy ensures that optimum performance of MC is achieved by finding the duty cycles that minimize the error.

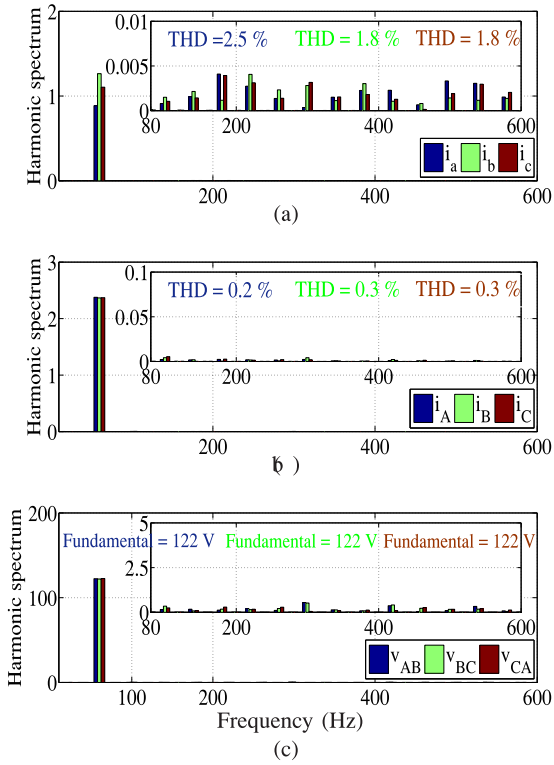


Fig. 12. Simulated harmonic spectra of the MC waveforms operating with the proposed modulation strategy when $V_o$=50 V and $f_o = 60$ Hz: (a) three-phase input currents, (b) three-phase load currents, and (c) three-phase line-to-line output voltages.

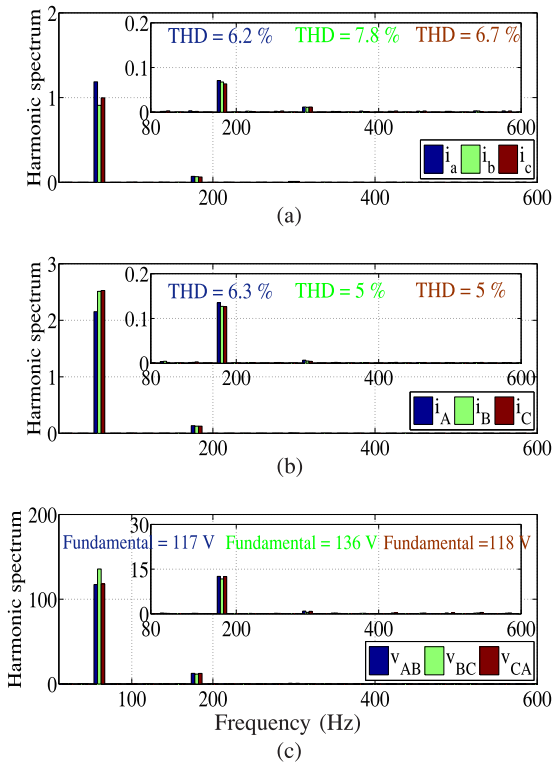


Fig. 13. Simulated harmonic spectra of the MC waveforms operating with the SVM strategy when $V_o$=50 V and $f_o = 60$ Hz: (a) three-phase input currents, (b) three-phase load currents, and (c) three-phase line-to-line output voltages.

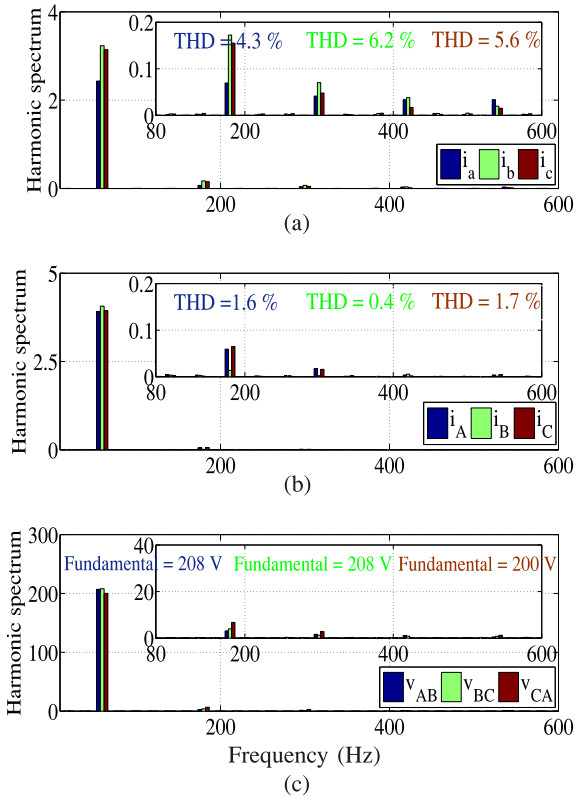


Fig. 14. Simulated harmonic spectra of the MC waveforms operating with the proposed modulation strategy when $V_o = 86$ V and $f_o = 60$ Hz: (a) three-phase input currents, (b) three-phase load currents, and (c) three-phase line-to-line output voltages.

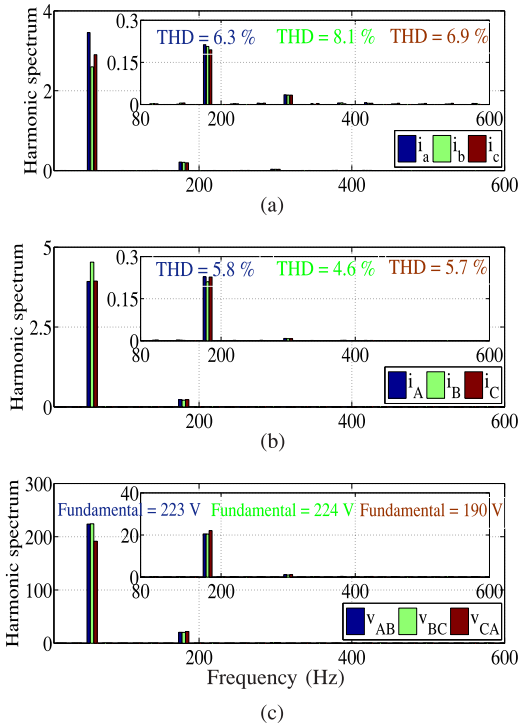


Fig. 15. Simulated harmonic spectra of the MC waveforms operating with the SVM strategy when $V_o$=86 V and $f_o = 60$ Hz with SVM modulation strategy: (a) three-phase input currents, (b) three-phase load currents, and (c) three-phase line-to-line output voltages.

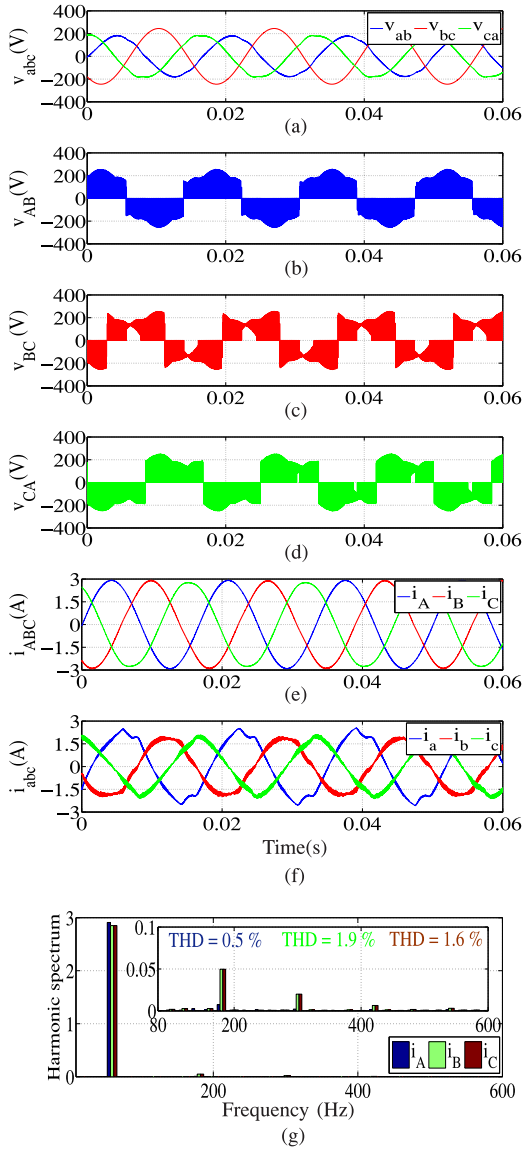


Fig. 16. Simulation waveforms of the MC operating with the proposed modulation strategy under 15% imbalance in the input voltages when $V_o = 64$ V and $f_o = 60$ Hz, (a) input voltages, (b)–(d) three-phase line-to-line output voltages, (e) three-phase load currents, (f) Three-phase input currents, and (g) harmonic spectrum of load currents.

To highlight the superiority of the proposed strategy over the SVM strategy in terms of improving the output current waveforms, the corresponding MC waveforms operating with the SVM strategy with an output voltage magnitude of 86 and 50 V for $f_o = 60$ Hz are shown in Figs. 9 and 11, respectively.

The harmonic spectrum of the converter input and output currents and their corresponding THDs when operating with the proposed modulation strategy and the SVM strategy for the reference output voltages of 50 and 86 V, i.e., equivalent to the line-to-line voltages of 122 and 210 V, are given in Figs. 12–15, respectively. As shown in Figs. 12 and 14, by using the proposed modulation strategy, the THDs of the input and output currents are considerably reduced. The simulation studies also confirm the capability of MC operating under unbalanced input

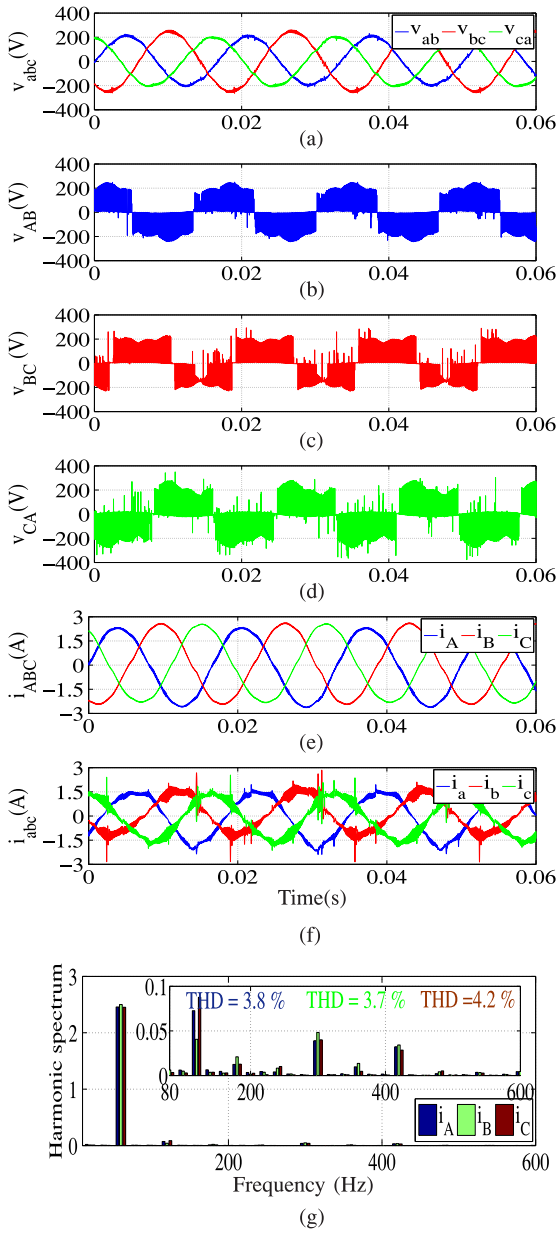


Fig. 17. Experimental waveforms of the MC operating with the proposed modulation strategy under 15% imbalance in the input voltages when $V_o = 64$ V and $f_o = 60$ Hz: (a) input voltages, (b)–(d) three-phase line-to-line output voltages, (e) three-phase load currents, (f) three-phase input currents, and (g) harmonic spectrum of load currents.

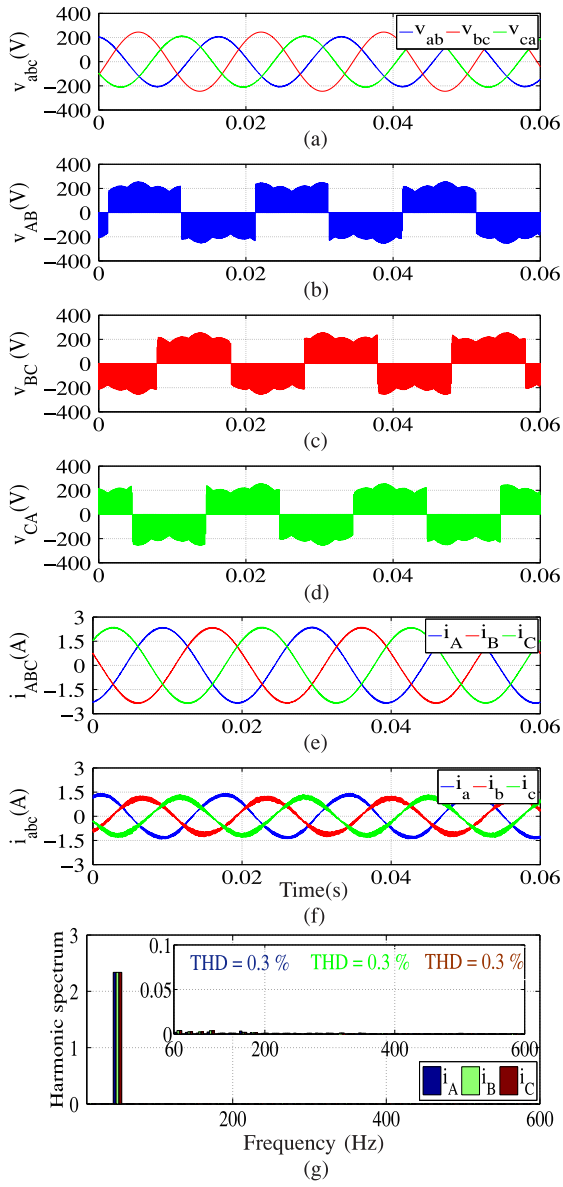


Fig. 18. Simulation waveforms of the MC operating with the proposed modulation strategy under 9.5% imbalance in the input voltages when $V_o = 50$ V and $f_o = 50$ Hz: (a) input voltages, (b)–(d) three-phase line-to-line output voltages, (e) three-phase load currents, (f) three-phase input currents, and (g) harmonic spectrum of load currents.

voltage conditions, even with a reference voltage greater than the maximum attainable one.

### B. Experimental Studies

The simulation and experimental results of the MC system of Fig. 1 operating with the proposed modulation strategy under 15% imbalance in the input voltages when $V_o = 64$ V and $f_o = 60$ Hz are shown in Figs. 16 and 17, respectively. For this case, the set of three-phase input voltages can be represented with $V_P = 88.5$ V and $V_N = 13$ V. As shown in Figs. 16(e) and 17(e), despite the presence of 15% imbalance in the input voltages, the proposed strategy modulates the converter by minimizing the error between the output voltages and their reference values, while maintaining the desired input current reference angle.

The simulation and experimental results of the MC system of Fig. 1 operating with the proposed modulation strategy under 9.5% imbalance in the input voltages when $V_o = 50$ V and $f_o = 50$ Hz are shown in Figs. 18 and 19, respectively. For this case, the set of three-phase input voltages can be represented with $V_P = 94$ V and $V_N = 9$ V. As shown in Fig. 19, the proposed strategy modulates the converter by minimizing the error between the reference and the output voltages of the converter, while maintaining the desired input current reference angle. The results of Figs. 18 and 19 confirm the capability of the proposed

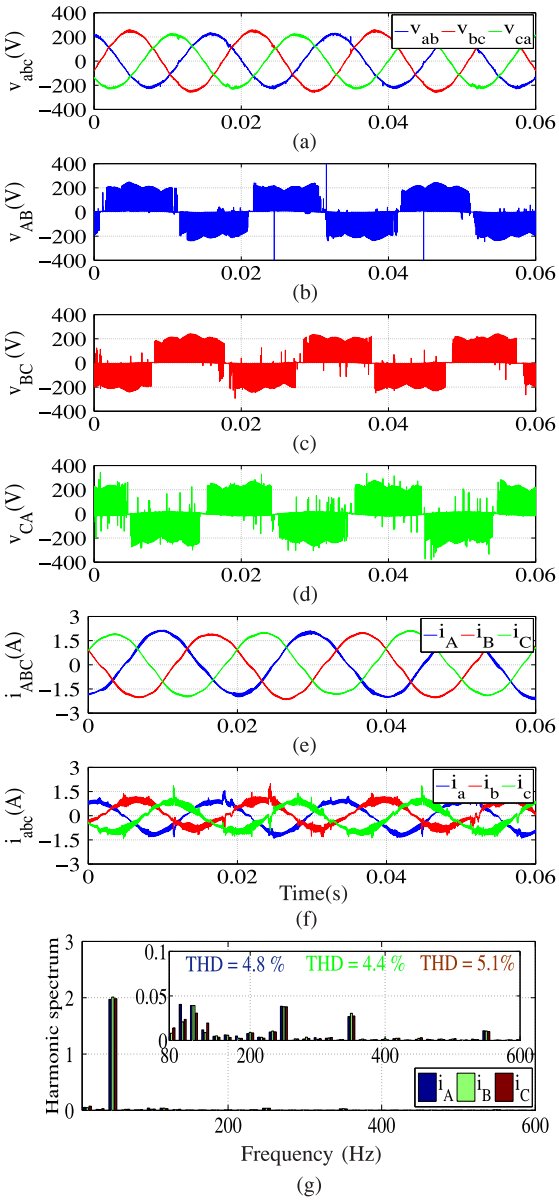


Fig. 19. Experimental waveforms of the MC operating with the proposed modulation strategy under 9.5% imbalance in the input voltages when $V_o = 50$ V and $f_o = 50$ Hz: (a) input voltages, (b)–(d) three-phase line-to-line output voltages, (e) three-phase load currents, (f) three-phase input currents, and (g) harmonic spectrum of load currents.

strategy to operate the MC under various unbalanced input voltage conditions.

## VI. Conclusion

In this paper, a new modulation strategy for the MC operating under unbalanced input voltage conditions is presented. The proposed strategy ensures that optimal performance of the MC over the entire operation range, including the case when the converter operates with an output voltage greater than maximum attainable balanced output voltage under unbalanced input voltage conditions, is achieved. The modulation strategy, which is based on modification of the conventional SVM strategy, determines the duty cycles of switching states by formulating and solving an optimization problem that minimizes the error between the reference and the measured output voltages. Based on the KKT conditions, the solution to the optimization problem is found. The capability of the proposed modulation strategy is investigated based on time-domain simulation studies, in the MATLAB/Simulink environment and experimental studies. The studies conclude that the proposed strategy ensures optimal performance of the MC is achieved over the entire operating range under unbalanced input voltage conditions.

## Appendix

### A. Solution to a Nonlinear Optimization Problem With Inequality Constraints

The optimization problem in (10) is a standard nonlinear optimization with inequality constraints. The potential candidates for optimizing (10) can be found by solving the first-order KKT conditions [19]. To verify, if the obtained point is a local minimizer, the second-order conditions need to be evaluated. However, if it is proved that the function $f(\boldsymbol{d})$ is convex, the point obtained by the first-order conditions is the global minimizer over the feasible region [19].

*1) First-Order Conditions (The KKT Conditions):* The KKT conditions for the optimization problem of (10) are given by

a)

$$\boldsymbol{\mu} = \begin{bmatrix} \mu_1 & \mu_2 & \mu_3 & \mu_4 & \mu_5 \end{bmatrix}^T \geq \mathbf{0}$$

b)

$$\begin{bmatrix} 2K_1 d_I + K_3 d_{II} + K_{4a} \\ K_3 d_I + 2K_2 d_{II} + K_{5a} \end{bmatrix} + \mu_1 \begin{bmatrix} 1 \\ 1 \end{bmatrix} + \mu_2 \begin{bmatrix} -1 \\ 0 \end{bmatrix} + \mu_3 \begin{bmatrix} 0 \\ -1 \end{bmatrix} + \mu_4 \begin{bmatrix} 1 \\ 0 \end{bmatrix} + \mu_5 \begin{bmatrix} 0 \\ 1 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix},$$

c)

$$\mu_1(d_I + d_{II} - 1) = 0, \quad \mu_2 d_I = 0, \quad \mu_3 d_{II} = 0$$
$$\mu_4(d_I - 1) = 0, \quad \mu_5(d_{II} - 1) = 0$$

d)

$$d_I + d_{II} \leq 1$$

where $\mu_1$, $\mu_2$, $\mu_3$, $\mu_4$, and $\mu_5$ are the KKT multipliers. The coefficients $K_1$, $K_2$, $K_3$, $K_{4a}$, and $K_{5a}$ are defined in (9). The KKT conditions for problem (10) have seven variables, two equations, and five inequality conditions. The solution space or the feasible space of the problem can be divided into seven different possible regions. The constraints that need to be satisfied by the solution in each region can be derived by solving the KKT conditions. In this section, the constraints for region 1 are derived. A similar procedure can be used to derive constraints in the other regions.

*Region 1:* $d_I = 1$ and $d_{II} = 0$

For this solution, the inequality constraints $d_I + d_{II} \leq 1$, $d_{II} \leq 0$, and $d_I \leq 1$ are active constraints, while $d_I \leq 0$ and $d_{II} \leq 1$ are nonactive constraints. To satisfy the third KKT

condition, the following conditions must be true:

$$\mu_2 = 0, \quad \mu_5 = 0, \quad \mu_1, \mu_3, \mu_4 > 0. \tag{14}$$

Substituting for $\mu_2 = 0$, $\mu_5 = 0$, $d_I = 1$, and $d_{II} = 0$ in the second KKT condition, the associated equations are written as

$$2K_1 + K_{4a} + \mu_1 + \mu_4 = 0 \tag{15a}$$

$$K_3 + K_{5a} + \mu_1 - \mu_3 = 0. \tag{15b}$$

Based on (15) and for $\mu_1$, $\mu_3$, $\mu_4 > 0$, the following two conditions need to be satisfied:

$$K_3 + K_{5a} - 2K_1 - K_{4a} > 0, \tag{16a}$$

$$(K_3 + K_{5a}) < (K_3 + K_{5a} - 2K_1 - K_{4a}). \tag{16b}$$

Based on the aforementioned discussion, it can be concluded that if the constraints in (16) are satisfied, then $d_I = 1$ and $d_{II} = 0$ is a candidate for the minimizer.

*2) Global Minimum for the Optimization Function:* The KKT condition is only a necessary condition and not a sufficient condition. However, if the function $f(\boldsymbol{d})$ is a convex function, the point obtained by the first-order condition is a global optimum. To prove that function $f(\boldsymbol{d})$ is a convex function, it should be proved that the Hessian of the function $f$ is positive semidefinite. The Hessian of $f$ is

$$\boldsymbol{F}(\boldsymbol{d}) = \begin{bmatrix} 2K_1 & K_3 \\ K_3 & 2K_2 \end{bmatrix}. \tag{17}$$

Since the Hessian matrix $\boldsymbol{F}(\boldsymbol{d})$ is symmetric, Sylvester's criterion can be used to determine the positive definiteness of the matrix [19].

*Sylvester's Criterion:* A quadratic form $\boldsymbol{x^T Q x}$, $\boldsymbol{Q = Q^T}$ is positive definite, if and only if, the leading principal minors of $Q$ are positive.

The leading principal minors of the matrix $\boldsymbol{F}(\boldsymbol{d})$ are

$$\Delta_1 = \ 2K_1 = 2(V_{1,I}^2 + I_{2,\mathrm{ref}}^2) \tag{18}$$

$$\Delta_2 = \ \det \boldsymbol{F}(\boldsymbol{d}) = 4(V_{1,I} I_{1,\mathrm{ref}} + V_{1,II} I_{2,\mathrm{ref}})^2. \tag{19}$$

The selected vector $V_I$ to modulate the converter is nonzero. Hence, $V_{1,I}^2 + I_{2,\mathrm{ref}}^2$ is nonzero and always positive. Therefore, the leading principal minor $\Delta_1$ is always positive. Based on (19), it can be concluded that $\Delta_2$ is a nonnegative number. For any given voltage current sector combination, $V_{1,I}$ and $V_{1,II}$ are positive. Furthermore, $I_{1,\mathrm{ref}}$ and $I_{2,\mathrm{ref}}$ are nonnegative numbers and, within each switching cycle, their values are not simultaneously zero, leading to $\Delta_2$ to be always positive. Therefore, $f(\boldsymbol{d})$ is a positive definite on $\mathbb{R}^2$ and, hence, it can be concluded that the feasible point found by the first-order necessary condition is a strict global minimizer.

### B. Sub-optimization Problems

In this section, the equivalence of the solution to the optimization problem of (6) to solve the suboptimization problems of (10) and (11) is discussed. The solution to the sub-optimization problems can be classified into two cases: 1) $d_I + d_{II} + d_{III} + d_{IV} \leq 1$ and 2) $d_I + d_{II} + d_{III} + d_{IV} > 1$, which will be individually discussed in the followings.

*1) The KKT Conditions:* The KKT conditions for the optimization problem of (6) are given by

a)

$$\boldsymbol{\mu} = [\,\mu_1 \quad \mu_2 \quad \mu_3 \quad \mu_4 \quad \mu_5 \quad \mu_6 \quad \mu_7 \quad \mu_8 \quad \mu_9\,]^T \geq \mathbf{0}$$

b)

$$\begin{bmatrix} 2K_1 d_I + K_3 d_{II} + K_{4a} \\ K_3 d_I + 2K_2 d_{II} + K_{5a} \\ 2K_1 d_{III} + K_3 d_{IV} + K_{4b} \\ K_3 d_{III} + 2K_2 d_{IV} + K_{5b} \end{bmatrix} + \mu_1 \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} + \mu_2 \begin{bmatrix} -1 \\ 0 \\ 0 \\ 0 \end{bmatrix} + \mu_3 \begin{bmatrix} 0 \\ -1 \\ 0 \\ 0 \end{bmatrix} + \mu_4 \begin{bmatrix} 0 \\ 0 \\ -1 \\ 0 \end{bmatrix} + \mu_5 \begin{bmatrix} 0 \\ 0 \\ 0 \\ -1 \end{bmatrix} + \mu_6 \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} + \mu_7 \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \end{bmatrix} + \mu_8 \begin{bmatrix} 0 \\ 0 \\ 1 \\ 0 \end{bmatrix} + \mu_9 \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

c)

$$\mu_1(d_I + d_{II} + d_{III} + d_{IV} - 1) = 0,$$
$$\mu_2 d_I = 0, \quad \mu_3 d_{II} = 0, \quad \mu_4 d_{III} = 0, \quad \mu_5 d_{IV} = 0,$$
$$\mu_6(d_I - 1) = 0, \quad \mu_7(d_{II} - 1) = 0,$$
$$\mu_8(d_{III} - 1) = 0, \quad \mu_9(d_{IV} - 1) = 0,$$

d)

$$d_I + d_{II} + d_{III} + d_{IV} \leq 1,$$
$$-d_I \leq 0, \quad -d_{II} \leq 0, \quad -d_{III} \leq 0, \quad -d_{IV} \leq 0,$$
$$d_I \leq 1, d_{II} \leq 1, \quad d_{III} \leq 1, \quad d_{IV} \leq 1.$$

The KKT conditions for the sub-optimization problem of (10) are given by

a)

$$\boldsymbol{\mu} = [\,\mu_{1a} \quad \mu_2 \quad \mu_3 \quad \mu_4 \quad \mu_5 \quad ]^T \geq \mathbf{0}$$

b)

$$\begin{bmatrix} 2K_1 d_I + K_3 d_{II} + K_{4a} \\ K_3 d_I + 2K_2 d_{II} + K_{5a} \end{bmatrix} + \mu_{1a} \begin{bmatrix} 1 \\ 1 \end{bmatrix} + \mu_2 \begin{bmatrix} -1 \\ 0 \end{bmatrix} + \mu_3 \begin{bmatrix} 0 \\ -1 \end{bmatrix} + \mu_4 \begin{bmatrix} 1 \\ 0 \end{bmatrix} + \mu_5 \begin{bmatrix} 0 \\ 1 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

c)

$$\mu_{1a}(d_I + d_{II} - 1) = 0,$$
$$\mu_2 d_I = 0,\ \ \mu_3 d_{II} = 0,\ \ \mu_4(d_I - 1) = 0,$$
$$\mu_5(d_{II} - 1) = 0$$

d)

$$d_I + d_{II} \le 1,\ \ -d_I \le 0,\ \ -d_{II} \le 0,\ \ d_I \le 1,\ \ d_{II} \le 1.$$

Similarly, the KKT conditions for the suboptimization problem of (11) are given by

a)

$$\boldsymbol{\mu} = \begin{bmatrix} \mu_{1b} & \mu_2 & \mu_3 & \mu_4 & \mu_5 \end{bmatrix}^T \ge \mathbf{0}$$

b)

$$\begin{bmatrix} 2K_1 d_{III} + K_3 d_{IV} + K_{4b} \\ K_3 d_{III} + 2K_2 d_{IV} + K_{5b} \end{bmatrix} + \mu_{1b} \begin{bmatrix} 1 \\ 1 \end{bmatrix} + \mu_6 \begin{bmatrix} -1 \\ 0 \end{bmatrix} + \mu_7 \begin{bmatrix} 0 \\ -1 \end{bmatrix} + \mu_8 \begin{bmatrix} 1 \\ 0 \end{bmatrix} + \mu_9 \begin{bmatrix} 0 \\ 1 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

c)

$$\mu_{1b}(d_{III} + d_{IV} - 1) = 0,$$
$$\mu_6 d_{III} = 0,\ \ \mu_7 d_{IV} = 0,$$
$$\mu_8(d_{III} - 1) = 0,\ \ \mu_9(d_{IV} - 1) = 0$$

d)

$$d_{III} + d_{IV} \le 1, -d_{III} \le 0,\ \ -d_{IV} \le 0,\ \ d_{III} \le 1,$$
$$d_{IV} \le 1.$$

The coefficients $K_1$, $K_2$, $K_3$, $K_{4a}$, $K_{5a}$, $K_{4b}$, and $K_{5b}$ are defined in (9).

*2) Solution for Case 1 ($d_I + d_{II} + d_{III} + d_{IV} \le 1$):* Considering the solution space of (6), when $d_I + d_{II} + d_{III} + d_{IV} < 1$ and $d_I, d_{II}, d_{III}, d_{IV} \in (0, 1)$, all the constraints of (6) become inactive. Hence

$$\boldsymbol{\mu} = \begin{bmatrix} \mu_1 & \mu_2 & \mu_3 & \mu_4 & \mu_5 & \mu_6 & \mu_7 & \mu_8 & \mu_9 \end{bmatrix}^T = \mathbf{0^T}. \tag{20}$$

The solution can be obtained by solving the following set of equations:

$$\begin{bmatrix} 2K_1 d_I + K_3 d_{II} + K_{4a} \\ K_3 d_I + 2K_2 d_{II} + K_{5a} \\ 2K_1 d_{III} + K_3 d_{IV} + K_{4b} \\ K_3 d_{III} + 2K_2 d_{IV} + K_{5b} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{21}$$
$$d_I + d_{II} + d_{III} + d_{IV} \le 1$$
$$-d_I \le 0,\ \ -d_{II} \le 0,\ \ -d_{III} \le 0,\ \ -d_{IV} \le 0$$
$$d_I \le 1,\ \ d_{II} \le 1,\ \ d_{III} \le 1,\ \ d_{IV} \le 1. \tag{22}$$

Now, consider the solutions to the optimization problems of (10) and (11) in $d_I + d_{II} < 1$ and $d_{III} + d_{IV} < 1$, respectively. Since all the constraints of optimization problems (10) and (11) are inactive, the solution can be obtained by solving:

$$\begin{bmatrix} 2K_1 d_I + K_3 d_{II} + K_{4a} \\ K_3 d_I + 2K_2 d_{II} + K_{5a} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}, \tag{23}$$
$$d_I + d_{II} \le 1,\ \ -d_I \le 0,\ \ -d_{II} \le 0,\ \ d_I \le 1,\ \ d_{II} \le 1. \tag{24}$$
$$\begin{bmatrix} 2K_1 d_{III} + K_3 d_{IV} + K_{4b} \\ K_3 d_{III} + 2K_2 d_{IV} + K_{5b} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}, \tag{25}$$
$$d_{III} + d_{IV} \le 1,\ \ -d_{III} \le 0,\ \ -d_{IV} \le 0,\ \ d_{III} \le 1,\ \ d_{IV} \le 1. \tag{26}$$

As shown in (21), (10), and (11), solving (21) is equivalent to solving (23) and (25). Therefore, the solution to the optimization problem in (6) when $d_I + d_{II} + d_{III} + d_{IV} < 1$ and $d_I$, $d_{II}$, $d_{III}, d_{IV} \in (0, 1)$ is equivalent to the solution to the optimization problems in (10) and (11) when $d_I + d_{II} < 1$ and $d_{III} + d_{IV} < 1$, respectively. Following a similar procedure, the equivalence of solutions for other regions when $d_I + d_{II} + d_{III} + d_{IV} \le 1$ can be proved.

*3) Solution for Case ($d_I + d_{II} + d_{III} + d_{IV} > 1$):* Since the objective functions in (10) and (11) when $d_I + d_{II} + d_{III} + d_{IV} > 1$, $d_{II} = 0$, $d_{IV} = 0$, and $d_I + d_{III} > 1$ are strictly convex, the solution is assumed to lie on $d_I + d_{III} = 1$. Consequently, by solving (6) with $d_{II} = 0$, $d_{IV} = 0$, and $d_I + d_{III} = 1$, the solution is obtained as

$$d_I = \frac{K_{4b} - K_{4a} + 2K_1}{4K_1},\ \ d_{III} = 1 - d_I. \tag{27}$$

Following a similar procedure, the solutions for the remaining combinations when $d_I + d_{II} + d_{III} + d_{IV} > 1$ can be obtained.

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