An Adaptive ZVS Full-Bridge DC–DC Converter With Reduced Conduction Losses and Frequency Variation Range

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***Abstract*—This paper presents a description and analysis of a full-bridge converter with a novel passive and robust auxiliary circuit for zero-voltage-switching (ZVS) operation. A generalized time-domain state-space analysis is provided to describe the steady-state behavior of the auxiliary circuit. Complete comparison between the well-known single-inductor auxiliary circuit, and the proposed one is presented. For a similar peak current in the auxiliary branch, needed for ZVS, a minimum of 20% reduction in rms current is achieved to decrease the conduction losses in the power switches and in the auxiliary circuit. Also, 65% reduction in switching frequency variation is obtained. This narrower frequency range reduces the need for very high-frequency operation and the associated gate driver losses as well as the difficulty of electromagnetic interference (EMI) filter design. All the theoretical results are experimentally verified.**

***Index Terms*—DC–DC converter, full-bridge converter, passive auxiliary circuit, reduced frequency variation, zero-voltage switching (ZVS).**

NOMENCLATURE

$L_{\rm S1}$	Series inductor in proposed auxiliary.
$L_{\rm P1}$	Parallel inductor in proposed auxiliary.
$C_{\rm P1}$	Capacitor in proposed auxiliary.
$L_{\rm aux1}$	Inductor in single-inductor auxiliary (leading leg).
$L_{\rm aux2}$	Inductor in single-inductor auxiliary (lagging leg).
C_{a1}, C_{a2}	Splitting capacitor.
T	Switching period.
f_s	Switching frequency.
$\omega_{\rm SW}$	Switching angular frequency.
ω_0	Resonant frequency.
r	Ratio of $\omega_{\rm SW}$ and ω_0.
$V_{\rm dc}$	Input dc voltage.
$I_{L_{\rm S1}\_0}$	Peak current in $L_{\rm S1}$, at $t=0$.
$I_{L_{\rm P1}\_0}$	Peak current in $L_{\rm P1}$, at $t=0$.
$V_{C_{\rm P1}\_\max}$	Peak voltage across $C_{\rm P1}$.
$V_{C_{\rm P1}\_0}$	Voltage across $C_{\rm P1}$, at $t=0$.
$I_{\rm base}$	Absolute value of $I_{L_{\rm S1}0}$ at $\omega_{\rm SW}=\omega_0/2$.
$I_{L_{\rm S1}\_H_k}$	kth harmonic of current in $L_{\rm S1}$.
$I_{L_{\rm aux1}\_\rm peak}$	Peak current in $L_{\rm aux1}$.
N	Transformer turns ratio.
$L_{\rm leak}$	Transformer leakage inductance (primary).
L_M	Transformer magnetizing inductance (primary).
$L_{\rm out}$	Output filter inductor.
$C_{\rm out}$	Output filter capacitor.
$S_{\rm 1U}, S_{\rm 1L}, S_{\rm 2U}, S_{\rm 2L}$	Switches.
$P_{\rm out\_nom}$	Nominal output power.
$V_{\rm out\_nom}$	Nominal output voltage.
ESR	Equivalent series resistance.
ESL	Equivalent series inductance.

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I. INTRODUCTION

FULL-BRIDGE converter is the widely accepted topology for medium to high power range. It has many advantages such as full voltage swing on the ac lines (from positive to negative of dc-link voltage), switch voltage stress not more than dc voltage, equal utilization of all the switches, optimal use of a smaller transformer by using flux in both directions, and possibility of high-power-density designs.

Soft-switching of the full-bridge converter switches must be guaranteed for reliable high-frequency operation. In a full-bridge converter with phase-shift modulation, it is possible to take advantage of the parasitic leakage inductance of the power transformer to gain ZVS property. In the case of heavy loads, the current leaving the midpoint of a switch leg is inductive, i.e., lags the voltage waveform, which brings the desirable ZVS operation. However, relying on transformer leakage inductance limits the choice for turns ratio of the transformer and cannot ensure ZVS for the entire operating points, especially at light-load situations. Details of the transition behavior are reported in [1], [2]. In the light-load conditions and/or high input voltages, the current becomes very low and ZVS is usually lost.

Various methods have been suggested to extend the soft-switching property of full-bridge converters. In [3] and [4], the solution is based on modifying the transformer and adding passive components on the load side. The approaches in [5] and [6] are by adding passive auxiliary circuits to the output filtering stage. In [7] and [8], a secondary-side switch is used.

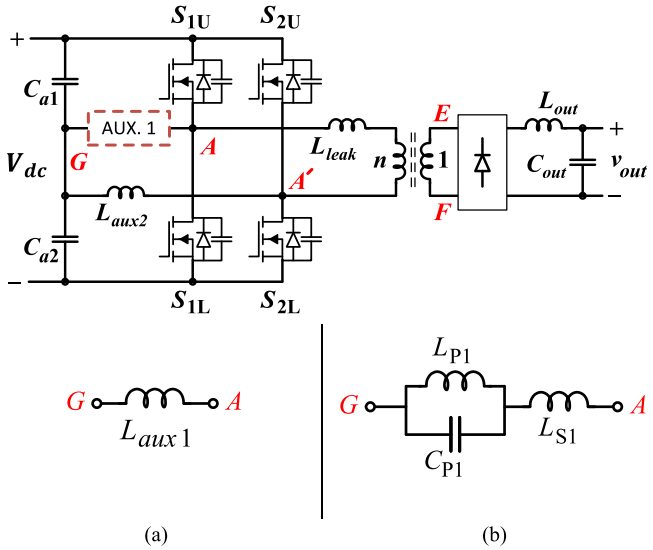

Fig. 1. Full-bridge converter with (a) the single-inductor [19] and (b) the proposed auxiliary circuits for leading leg. In both topologies, the single-inductor auxiliary is used for lagging leg.

There are also solutions based on modifications on primary side. In [9] and [10], the bridge is connected to the transformer through a coupled inductor that must be sized to pass the entire current. The auxiliary transformer in [11] handles the primary current and is clamped to dc bus using two fast diodes. The primary of main transformer in [12] is also clamped and connected to the bridge via coupled inductors. The solution in [13] uses two power transformers. In [14], several passive components are added in between the bridge and the transformer to gain-soft switching. In [15], ZVS is obtained without passing the entire current through the auxiliary circuit. There are also methods using active auxiliary circuits on primary side, for example, with one additional switch [16] or two [17], [18].

A low-cost and robust passive auxiliary circuit with a single inductor is suggested in [2] and later in [19] and [20], with the auxiliary circuit shown inside dashed lines Fig. 1. Based on this auxiliary circuit, an adaptive control method is suggested in [1], effective in maintaining ZVS operation of both the switch legs. Due to phase-shift modulation scheme of the main converter, each leg has 50% duty cycles; therefore, the current waveforms in the auxiliary inductors have nearly triangular shapes. The splitting capacitors guarantee zero dc current in steady-state operation. The peak value of the auxiliary current is determined by the input voltage and the switching frequency, which the latter is controlled by their suggested adaptive control method.

The duration of time between turn-off of one switch in a leg and turn-on of the other switch in the same leg is commonly named as deadtime. A nonzero deadtime is needed to ensure the safe operation without a shoot though between the positive and negative lines of the dc bus, which is specifically designed to have low impedance for the optimal operation. On the other hand, a long deadtime is not favorable and increases the losses. Thus, the deadtime is usually a small portion of the switching cycle. In a single-inductor auxiliary circuit, such as in Fig. 1,

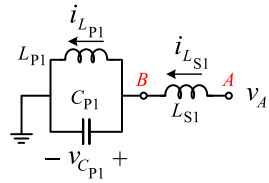

Fig. 2. Major voltage and currents for leading leg auxiliary circuit.

the auxiliary current reaches its peak value just before the deadtime. During the deadtime, the auxiliary current ensures that the process of charging and discharging the snubber capacitors happens completely and the next switch turns on under ZVS condition. After the deadtime, the auxiliary current has no function and only adds to the losses. Therefore, having the needed peak current with the least rms current is desirable.

The present papers introduces a novel auxiliary circuit that: 1) provides the same peak current value during the deadtime but has considerable lower rms value; 2) has a sharper frequency dependence behavior that reduces the needed frequency variation range for the adaptive control in [1]; and 3) the auxiliary inductors elements have half the value of comparable single-inductor auxiliary and, therefore, have smaller footprint, fewer number of turns, and less proximity-effect, lower equivalent series resistance (ESR) and, therefore, lower conduction losses. The details of events during the deadtime are provided in [1] and [2] and not repeated here. The focus of the paper is mostly on the auxiliary circuits and their application in a typical full-bridge dc–dc converter.

This paper is organized as follows: In Section II, the proposed auxiliary circuit is explained and its steady state operation analysis is presented. In Section III, the comparison between the proposed and single-inductor auxiliaries is provided. Section IV discusses the criterion to select the lowest practical rms current in the auxiliary branch toward a higher efficiency. Section V shows the experimental results for the auxiliary circuits, and Section VI deals with the process of implementing the proposed auxiliary circuit in a dc-dc converter.

II. Proposed Auxiliary Circuit

Single-inductor and the proposed auxiliary circuits for the leading leg are shown in Fig. 1(a) and (b), respectively. $L_{\rm aux1}$ in Fig. 1(a) is replaced with $L_{\rm S1}$ in series with $L_{\rm P1}||C_{\rm P1}$ in Fig. 1(b). The major voltage and currents of the proposed auxiliary circuit are defined in Fig. 2.

A. Assumptions

The following assumptions are considered for the analysis:

1) the converter is in steady-state operation with phase-shift modulation;
2) all passive components are ideal with ESR of zero;
3) C_{a1} and C_{a2} are equal and large, so their midpoint (node G) has half of the dc source voltage, thus, the voltage of switch leg ac nodes (v_A and $v_{A'}$) are equal to $V_{\rm dc}/2$ ($-V_{\rm dc}/2$) when switch or diode of $S_{\rm 1U}$ or $S_{\rm 2U}$ ($S_{\rm 1L}$ or $S_{\rm 2L}$) conduct;

4) the duty cycles of v_A and $v_{A'}$ are 50%;
5) $L_{\rm S1}$ and $L_{\rm P1}$ are similar, equal to L. Value of $C_{\rm P1}$ is C.

B. Steady-State Operation

The state variables are $i_{L_{\rm S1}}$, $i_{L_{\rm P1}}$, and $v_{C_{\rm P1}}$. The midpoint of the splitting capacitor branch (node *G* in Fig. 1) is selected as the ground level. Following the notations of Fig. 2

$$\begin{cases} i_{L_{\rm S1}} = i_{L_{\rm P1}} + i_{C_{\rm P1}} \\ v_{C_{\rm P1}} = v_{L_{\rm P1}} \\ v_A = v_{L_{\rm S1}} + v_{C_{\rm P1}} \end{cases} \text{or} \quad \begin{cases} \dfrac{di_{L_{\rm S1}}}{dt} = -\dfrac{1}{L}v_{C_{\rm P1}} + \dfrac{1}{L}v_A \\ \dfrac{di_{L_{\rm P1}}}{dt} = \dfrac{1}{L}v_{C_{\rm P1}} \\ \dfrac{dv_{C_{\rm P1}}}{dt} = \dfrac{1}{C}i_{L_{\rm S1}} - \dfrac{1}{C}i_{L_{\rm P1}} \end{cases} \tag{1}$$

The rising edge of v_A happens at $t = 0$, and it goes to $V_{\rm dc}/2$ where the initial values of the state variable are $I_{L_{\rm S1}0}$, $I_{L_{\rm P1}0}$, and $V_{C_{\rm P1}0}$. Introducing ω_0 as $\omega_0 \triangleq 1/\sqrt{LC/2}$, the state equations for $0 \le t \le T/2$ become

$$\begin{bmatrix} i_{L_{\rm S1}}(t) \\ i_{L_{\rm P1}}(t) \\ v_{C_{\rm P1}}(t) \end{bmatrix} = \begin{bmatrix} \dfrac{1+\cos\omega_0 t}{2} & \dfrac{1-\cos\omega_0 t}{2} & -\dfrac{\sin\omega_0 t}{L\omega_0} \\ \dfrac{1-\cos\omega_0 t}{2} & \dfrac{1+\cos\omega_0 t}{2} & \dfrac{\sin\omega_0 t}{L\omega_0} \\ \frac{1}{C\omega_0}\sin\omega_0 t & -\frac{1}{C\omega_0}\sin\omega_0 t & \cos\omega_0 t \end{bmatrix} \times \begin{bmatrix} I_{L_{\rm S1}\_0} \\ I_{L_{\rm P1}\_0} \\ V_{C_{\rm P1}\_0} \end{bmatrix} + \begin{bmatrix} \omega_0 t + \sin\omega_0 t \\ \omega_0 t - \sin\omega_0 t \\ L\omega_0(1-\cos\omega_0 t) \end{bmatrix} \frac{V_{\rm dc}}{4L\omega_0} \tag{2}$$

for $0 \le t \le T/2$, where T is the period of the switching cycle. At steady-state operation, the state variables have zero dc values and at $t = T/2$ all of them reach to the negative of their initial values. Thus

$$\begin{bmatrix} i_{L_{\rm S1}}(t = T/2) \\ i_{L_{\rm P1}}(t = T/2) \\ v_{C_{\rm P1}}(t = T/2) \end{bmatrix} = -\begin{bmatrix} i_{L_{\rm S1}}(t = 0) \\ i_{L_{\rm P1}}(t = 0) \\ v_{C_{\rm P1}}(t = 0) \end{bmatrix} = -\begin{bmatrix} I_{L_{\rm S1}\_0} \\ I_{L_{\rm P1}\_0} \\ V_{C_{\rm P1}\_0} \end{bmatrix} \tag{3}$$

From (2) and (3), we have

$$\begin{bmatrix} \dfrac{3+\cos(\pi/r)}{2} & \dfrac{1-\cos(\pi/r)}{2} & -\dfrac{\sin(\pi/r)}{L\omega_0} \\ \dfrac{1-\cos(\pi/r)}{2} & \dfrac{3+\cos(\pi/r)}{2} & \dfrac{\sin(\pi/r)}{L\omega_0} \\ \dfrac{1}{C\omega_0}\sin(\pi/r) & -\dfrac{1}{C\omega_0}\sin(\pi/r) & 1+\cos(\pi/r) \end{bmatrix} \begin{bmatrix} I_{L_{\rm S1}\_0} \\ I_{L_{\rm P1}\_0} \\ V_{C_{\rm P1}\_0} \end{bmatrix} = -\begin{bmatrix} \pi/r + \sin(\pi/r) \\ (\pi/r) - \sin(\pi/r) \\ L\omega_0(1-\cos(\pi/r)) \end{bmatrix} \frac{V_{\rm dc}}{4L\omega_0} \tag{4}$$

where $r \triangleq 2\pi/\omega_0 T = \omega_{\rm SW}/\omega_0$. The condition for (4) to have unique answers is

$$r \ne \frac{1}{2n-1}, \qquad \forall n \in N \tag{5}$$

The inequality in (5) means that $\omega_{\rm SW}$ must be selected such that neither itself nor any of its odd harmonics are close to ω_0. To emphasize it further, we examine the net impedance seen from node A to the ground in Fig. 2

$$Z(\omega) = j\omega L\left[\frac{2-LC\omega^2}{1-LC\omega^2}\right] = j2\omega L\left[\frac{1-\omega^2/\omega_0^2}{1-\omega^2/(\omega_0/\sqrt{2})^2}\right] \tag{6}$$

Equation (6) reveals that the forbidden r values in (5) belong to the situations in which $\omega_{\rm SW}$ or one of its odd harmonics is a zero of $Z(\omega)$.

Once the condition of (5) is met, (4) determines $I_{L_{\rm S1}\_0}$, $I_{L_{\rm P1}\_0}$, and $V_{C_{\rm P1}\_0}$ uniquely as

$$I_{L_{\rm S1}\_0} = -\frac{1}{\pi}\left[\frac{\pi}{2r} + \tan\left(\frac{\pi}{2r}\right)\right] I_{\rm base} = -\frac{1}{\pi}(y + \tan y) I_{\rm base} \tag{7}$$

$$I_{L_{\rm P1}\_0} = -\frac{1}{\pi}\left[\frac{\pi}{2r} - \tan\left(\frac{\pi}{2r}\right)\right] I_{\rm base} = -\frac{1}{\pi}(y - \tan y) I_{\rm base} \tag{8}$$

$$V_{C_{\rm P1}\_0} = 0 \tag{9}$$

where

$$I_{\rm base} \triangleq \frac{\pi}{4}\frac{V_{\rm dc}}{L\omega_0} \tag{10}$$

$$y \triangleq \frac{\pi}{2r} \tag{11}$$

$I_{\rm base}$ is the absolute value of $I_{L_{\rm S1}\_0}$ and $I_{L_{\rm P1}\_0}$ when $r = 0.5$. The time-domain state variables for $0 \le t \le T/2$ are given as

$$i_{L_{\rm S1}}(t) = \frac{1}{\pi}\left[y\left(\frac{4t}{T} - 1\right) + \sec y \cdot \sin\left(y\left(\frac{4t}{T} - 1\right)\right)\right] I_{\rm base} \tag{12}$$

$$i_{L_{\rm P1}}(t) = \frac{1}{\pi}\left[y\left(\frac{4t}{T} - 1\right) - \sec y \cdot \sin\left(y\left(\frac{4t}{T} - 1\right)\right)\right] I_{\rm base} \tag{13}$$

$$v_{C_{\rm P1}}(t) = \frac{1}{4}\left[1 - \sec y \cdot \cos\left(y\left(\frac{4t}{T} - 1\right)\right)\right] V_{\rm dc} \tag{14}$$

The other half period is obtainable by symmetry. It is straightforward to check that

$$i_{L_{\rm S1}}\left(t = \frac{T}{4}\right) = i_{L_{\rm P1}}\left(t = \frac{T}{4}\right) = 0$$

and peak capacitor voltage happens at $t = T/4$ as

$$V_{C_{\rm P1}\_\max} = v_{C_{\rm P1}}\left(t = \frac{T}{4}\right) = (1 - \sec y)\frac{1}{4}V_{\rm dc} \tag{15}$$

The typical waveforms of v_A, $i_{L_{\rm S1}}$, $i_{L_{\rm P1}}$, and $v_{C_{\rm P1}}$ are illustrated in Fig. 3 for $r \sim 0.5$. The dashed lines indicate the current waveform of the single-inductor auxiliary circuit of Fig. 1 (a).

Fig. 4 shows $i_{L_{\rm S1}}(t)/I_{\rm base}$ versus time for $r = 0.4$, 0.5, and 0.625. The horizontal axis is selected as t/T to reveal the behavior regardless of difference in the switching frequencies (various r values). The left (right) vertical axis indicates the normalized current (voltage). At higher r the peak value of i_{L_1} (i.e., $|I_{L_{\rm S1}\_0}|$)

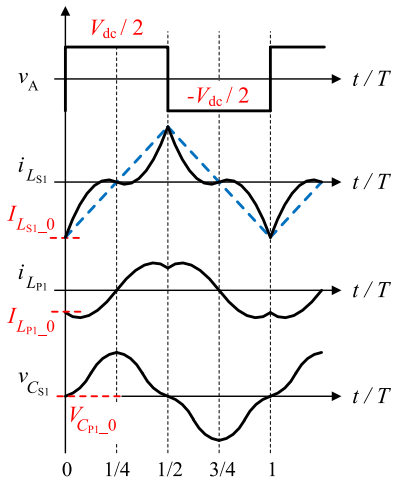

Fig. 3. Auxiliary circuit major voltage and current waveforms.

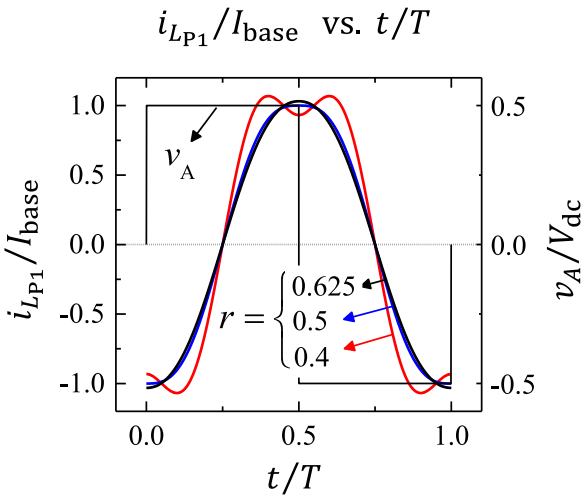

Fig. 5. $i_{L_{P1}}(t)/I_{\text{base}}$ versus time for $r = 0.4, 0.5, 0.625$.

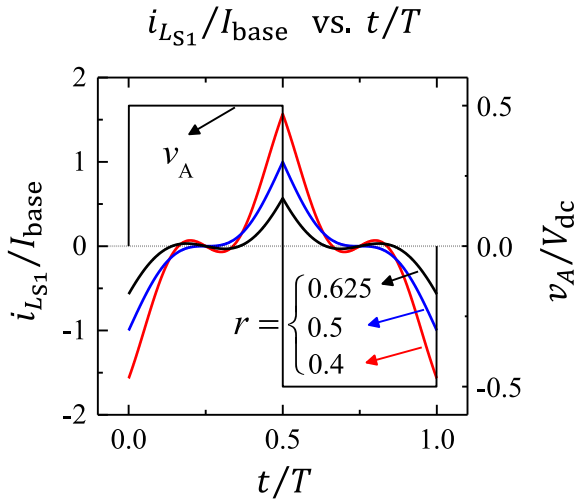

Fig. 4. $i_{L_{S1}}(t)/I_{\text{base}}$ versus time for $r = 0.4, 0.5, 0.625$.

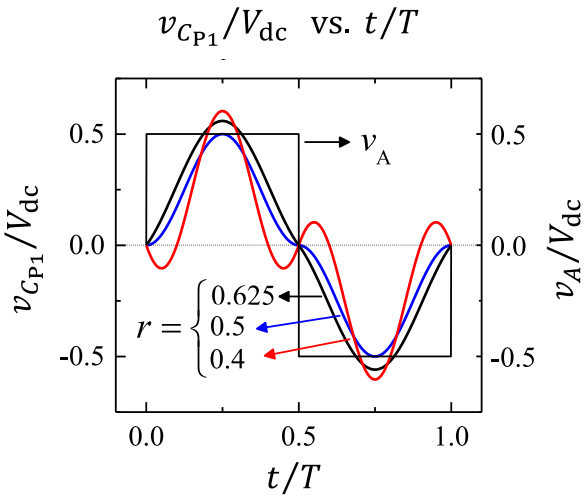

Fig. 6. $v_{C_{P1}}(t)/V_{\text{dc}}$ versus time for $r = 0.4, 0.5, 0.625$.

becomes smaller. For any r, the current zero-crossing moments are at $t/T = 1/4$ and $3/4$.

Fig. 5 illustrates $i_{L_{P1}}(t)/I_{\text{base}}$ for the same r values as in Fig. 4. The peak of $i_{L_{P1}}$ is close to I_{base}. Behavior of $v_{C_{P1}}(t)/V_{\text{dc}}$ is shown in Fig. 6. As predicted in (15), $V_{C_{P1}\_\max}$ happens at $t/T = 1/4$ and its lowest value ($V_{\text{dc}}/4$) belongs to $r = 0.5$. The capacitor voltage is smaller than V_{dc} and a high-voltage capacitor is not required.

The frequency behavior of $I_{L_{S1}\_0}/I_{\text{base}}$, $I_{L_{P1}\_0}/I_{\text{base}}$, and $V_{C_{P1}\_\max}/V_{\text{dc}}$ versus is shown in Fig. 7 for $1/3 < r < 1$. The asymptotic growth of $I_{L_{S1}\_0}$ and $I_{L_{P1}\_0}$ near $r = 1/3$ and 1 is expected because at $r \to 1$ ($r \to 1/3$) the impedance Z of the auxiliary branch given in (6) becomes very small for the main (third) harmonics of ω_{SW} or equivalently $n = 1$ ($n = 3$) in (5). The smallest $V_{C_{P1}\_\max}$ of $V_{\text{dc}}/4$ happens at $r = 1/2$.

To obtain ZVS in the leading leg of the converter, the net value of the current leaving node A at $t = 0$ must be negative; therefore, $I_{L_{S1}\_0}$ must be certainly negative. This means that operation under $\omega_{\text{SW}} < 0.7742\omega_0$ is required.

III. Comparison With Single-Inductor Auxiliary

To have a basis for comparing auxiliary circuits of Fig. 1 (a) and (b), it is necessary to select the component values such that they have a similar peak current at the same V_{dc} and at a specific frequency. The selected matching frequency here is $\omega_{\text{SW}} = \omega_0/2$ ($r = 0.5$). This is the frequency at which $V_{C_{P1}\_\max}$ is minimum and $|I_{L_{S1}\_0}| = |I_{L_{P1}\_0}| = I_{\text{base}}$. In order to have the same peak current for single-inductor auxiliary

$$\frac{V_{\text{dc}}}{2} \times \frac{T}{2} = L_{\text{aux1}} \times 2I_{\text{base}} \Rightarrow L_{\text{aux1}} = \frac{TV_{\text{dc}}}{8I_{\text{base}}} = 2L \quad (16)$$

Equation (16) means that L_{aux1} must be exactly $2L$ to fulfill the requirement of equal peak currents at $r = 0.5$. Thus, the inductors for the proposed auxiliary are smaller in inductance and physical size, which means more flexibility in PCB design, higher surface per volume ratio (for a better heat exchange), and possibility of using off-the-shelf components.

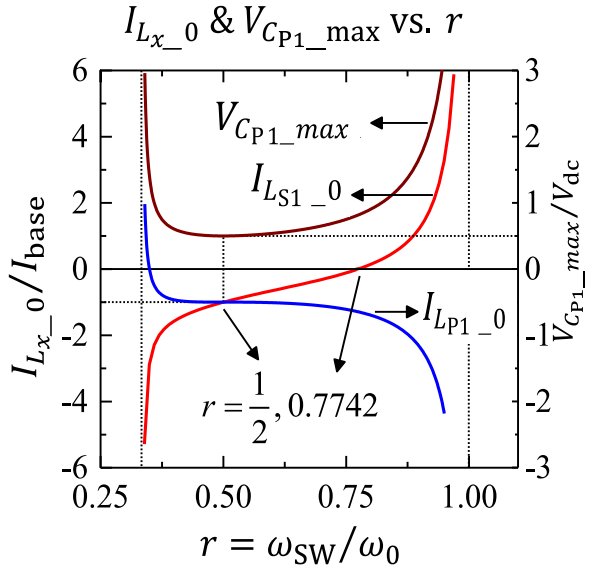

Fig. 7. Variation of $I_{Lx\_0}/I_{\text{base}}(x=S_1,P_1)$ and $V_{C\text{P}1\_\max}/V_{\text{dc}}$ with $1/3<r<1$.

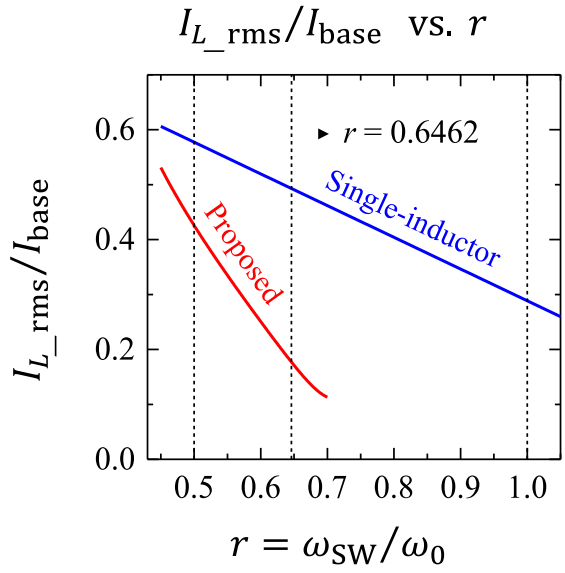

Fig. 9. Variation of $I_{L\_\text{rms}}/I_{\text{base}}$ versus r for proposed and single-inductor auxiliary circuits.

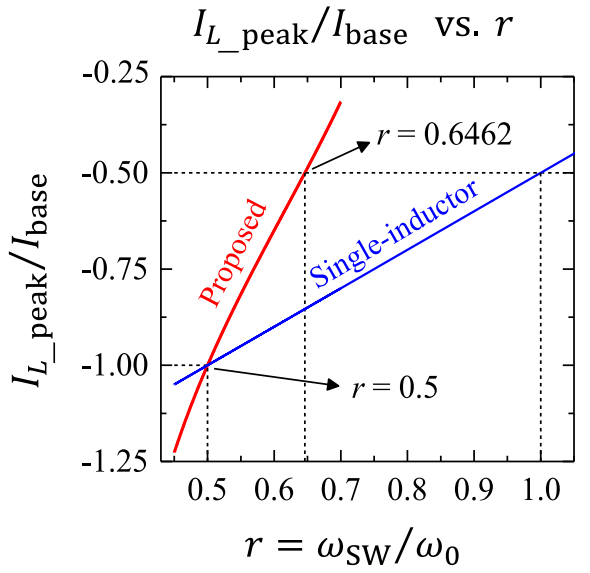

Fig. 8. Variation of $I_{L\_\text{peak}}/I_{\text{base}}$ versus r for proposed and single-inductor auxiliary circuits.

The variation of $I_{L_{\text{aux1}}\_\text{peak}}$ versus frequency (in the single-inductor auxiliary) has the form of

$$I_{L_{\text{aux1}}\_\text{peak}}=-\frac{\omega_0/2}{\omega_{\text{SW}}}I_{\text{base}}=-\frac{1}{2r}I_{\text{base}} \tag{17}$$

Hereafter, the terms I_{L_peak} and I_{L_rms} are used to refer to the peak and rms currents of auxiliary circuits, respectively, i.e., $I_{L\_\text{peak}}=I_{L_{\text{S1}}\_0}$ for the proposed auxiliary from (7) and $I_{L\_\text{peak}}=I_{L_{\text{aux1}}\_\text{peak}}$ from (17) for the single-inductor one. Fig. 8 illustrates $I_{L\_\text{peak}}/I_{\text{base}}$ versus frequency for both the auxiliary circuits. At $r=0.5$, both circuits have similar I_{L_peak} equal to $-I_{\text{base}}$ due to (16). Fig. 8 shows that for the single-inductor auxiliary to vary from $I_{L\_\text{peak}}=-I_{\text{base}}$ to $I_{L\_\text{peak}}=-0.5I_{\text{base}}$, the switching frequency must be doubled, i.e., r needs to reach 1. The proposed auxiliary, however, has a sharper frequency dependence and I_{L_peak} varies from $-I_{\text{base}}$ to $-0.5I_{\text{base}}$ when r is increased from 0.5 to only about 0.6462; therefore, a 65% reduction in frequency range is achieved compared to the single-inductor auxiliary case. Therefore, adjusting the peak auxiliary current is possible with within a narrower frequency range and less restrictions on gate driver and electromagnetic interference (EMI) filter design. Fig. 8 also shows that for the proposed auxiliary variation of I_{L_peak} by frequency is almost linear for $0.5<r<0.6462$. This aspect simplifies the design of frequency control loop significantly.

For the single-inductor auxiliary with a triangular current the rms current $I_{L_{\text{aux1}}\_\text{rms}}$ is

$$I_{L_{\text{aux1}}\_\text{rms}}=\frac{1}{\sqrt{3}}\left|I_{L_{\text{aux1}}\_\text{peak}}\right|=\frac{1}{2\sqrt{3}r}I_{\text{base}} \tag{18}$$

And the rms currents of the proposed auxiliary are

$$I_{L_{\text{S1}}\_\text{rms}}=-\frac{g\left(y\right)}{\pi\cos y}I_{\text{base}} \tag{19}$$

$$I_{L_{\text{P1}}\_\text{rms}}=-\frac{h\left(y\right)}{\pi\cos y}I_{\text{base}} \tag{20}$$

$$g\left(y\right)=\sqrt{\frac{1}{6y}\left[2y\left(y^2-6\right)\cos^2 y+9\sin y\cos y+3y\right]} \tag{21}$$

$$h\left(y\right)=\sqrt{\frac{1}{6y}\left[2y\left(y^2+6\right)\cos^2 y-15\sin y\cos y+3y\right]} \tag{22}$$

Fig. 9 illustrates the variation of rms currents versus frequency for the same inductors as in Fig. 8. The proposed auxiliary has smaller I_{L_rms} values for all values of r.

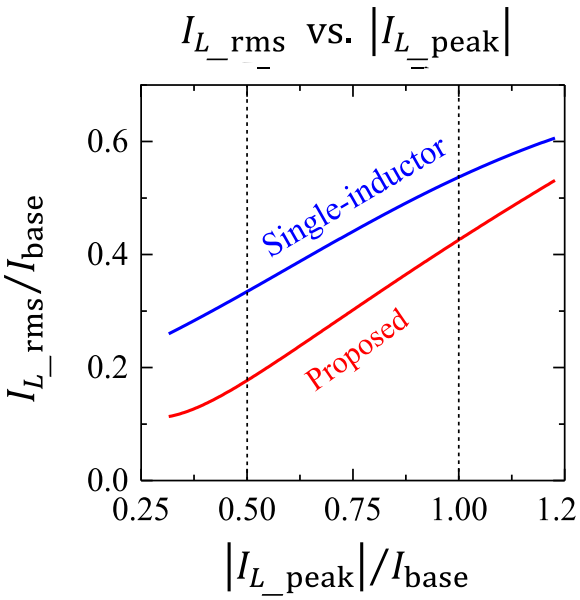

Fig. 10. Variation of I_{L_rms}/I_{base} versus I_{L_peak}/I_{base} for proposed and single-inductor auxiliary circuits.

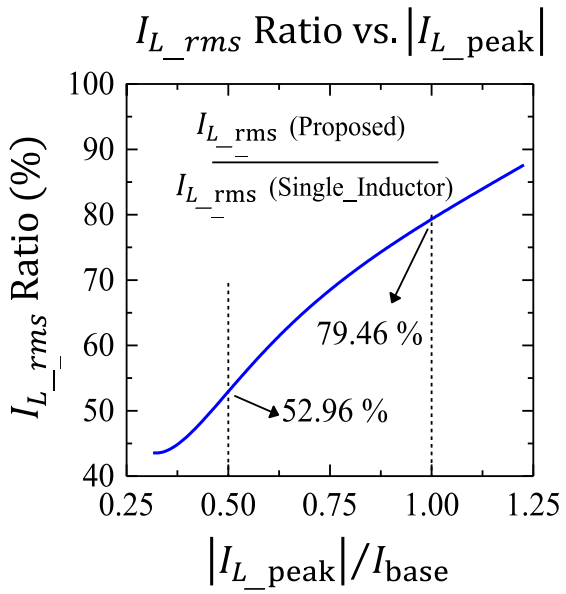

Fig. 11. Ratio of I_{L_rms}/I_{base} versus I_{L_peak}/I_{base} for proposed and single-inductor auxiliary circuits.

For a better comparison, in Fig. 10, the different frequency dependences are eliminated and I_{L_rms} values are depicted for similar I_{L_peak} values for both the auxiliaries. For any I_{L_peak} value the proposed auxiliary has a lower I_{L_rms}. This reduces the losses in the switches as well as in the auxiliary circuit itself.

Fig. 11 provides a better visualization of the achieved reduction in I_{L_rms}. I_{L_rms}(proposed) is equal to 52.96% (79.46%) of I_{L_rms}(single_inductor) when $I_{L\_peak} = 0.5I_{base}$ ($I_{L\_peak} = I_{base}$) for both of them. Therefore, a minimum of 20% reduction in rms current is obtained. Lower I_{L_rms} at the same I_{L_peak} means the same ZVS operation with reduced conduction losses in switches, passive elements, and printed circuit board.

The reason of the reduced I_{L_rms} (with the same I_{L_peak}) can be better shown by considering the harmonic content of the current waveforms. v_A is a square waveform and can be expressed as

$$v_A(t) = \frac{4}{\pi} \times \frac{V_{dc}}{2} \sum_{n=1,3,5,\cdots}^{\infty} \frac{1}{n} \sin(n\omega_{SW} t) \tag{23}$$

$V_{A\_H_n}$ is the amplitude of nth harmonic of $v_A(t)$ as

$$V_{A\_H_n} = \frac{2V_{dc}}{\pi n}, \qquad n = 1, 3, 5, \ldots. \tag{24}$$

For the single-inductor auxiliary

$$I_{L_{aux1}\_H_n} = \frac{V_{A\_H_n}}{L_{aux1} n\omega_{SW}} = \frac{1}{L_{aux1} n\omega_{SW}} \times \frac{2V_{dc}}{\pi n} \tag{25}$$

Using (25) and (10) with $L_{aux1} = 2L$ and $\omega_{SW} = r\omega_0$

$$I_{L_{aux1}\_H_n} = \frac{1}{r} \left(\frac{2}{n\pi}\right)^2 \times I_{base} \tag{26}$$

For the proposed auxiliary, from (6)

$$Z(n\omega_{SW}) = j2n\omega_{SW} L \left[\frac{1 - (n\omega_{SW})^2/\omega_0^2}{1 - (n\omega_{SW})^2/(\omega_0/\sqrt{2})^2}\right]$$

or

$$Z(n\omega_{SW}) = j2n\omega_{SW} L \left[\frac{1 - r^2 n^2}{1 - 2r^2 n^2}\right] \tag{27}$$

$$I_{L_1\_H_n} = \frac{V_{A\_H_n}}{|Z(n\omega_{SW})|} = \frac{1}{2n\omega_{SW} L} \left[\frac{1 - 2r^2 n^2}{1 - r^2 n^2}\right] \times \frac{2V_{dc}}{\pi n}$$

or

$$I_{L_1\_H_n} = \frac{1}{r} \left(\frac{2}{n\pi}\right)^2 \left[\frac{1 - 2r^2 n^2}{1 - r^2 n^2}\right] \times I_{base} \tag{28}$$

Fig. 12 illustrates the variation of harmonic amplitudes versus I_{L_peak}/I_{base} for both the proposed and single-inductor auxiliary circuits. For the proposed circuit, the main harmonic is smaller than that of the single-inductor one, but all the other harmonics are higher. The combination of harmonics results in the same peak but lower rms values.

IV. Frequency Ratio for Lower RMS Current

In the previous section we selected $r = 0.5$ as r_{min} (to get the largest peak current) and the adaptive controller in [1] was in charge to increase r adaptively to reduce the peak current as needed. Fig. 8 shows that the peak current dropped to half at $r = 0.6462$. The choice of $r_{min} = 0.5$ for the maximum peak current was arbitrary. In this section, we study the effect of other choices of r_{min} on the rms current toward having a lower rms current while having the same peak current for ZVS.

Similar to (18) for the single-inductor auxiliary, it is helpful to know I_{L_rms} as a function of I_{L_peak} for the proposed auxiliary

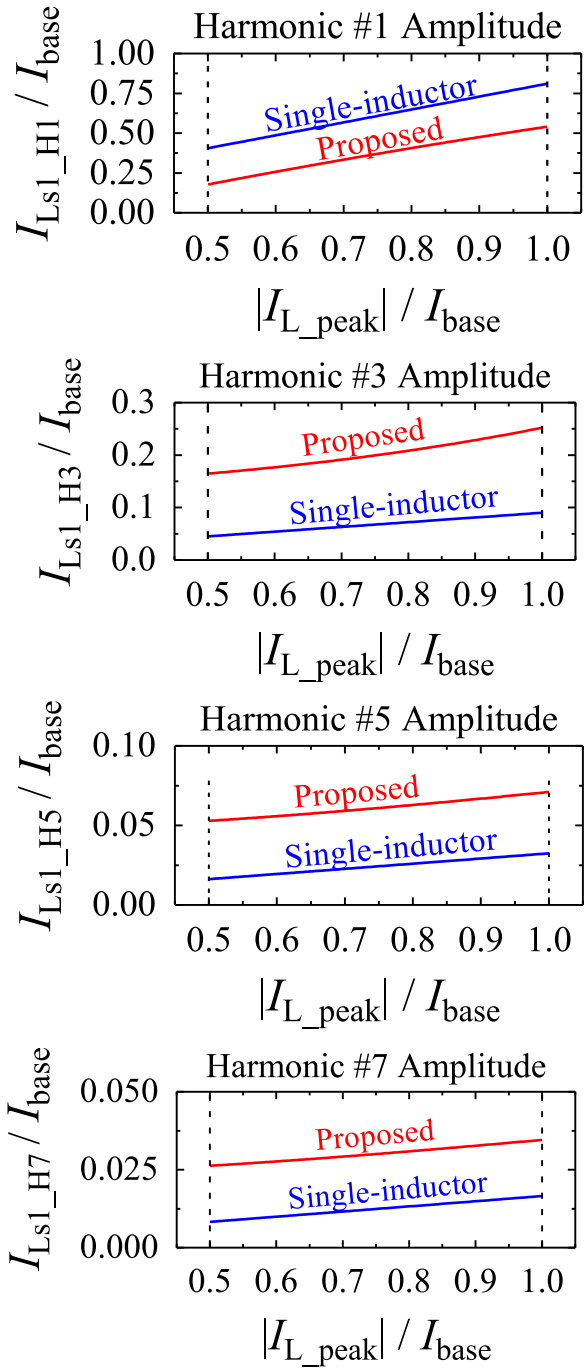

Fig. 12. Variation of harmonic amplitudes versus I_{L_peak}/I_{base} for proposed and single-inductor auxiliary circuits.

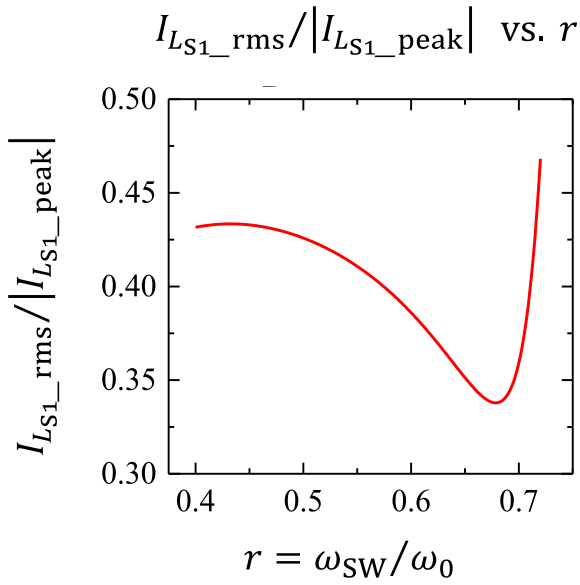

Fig. 13. Ratio of $I_{L_{S1}\_rms}/I_{L\_peak}$ versus r.

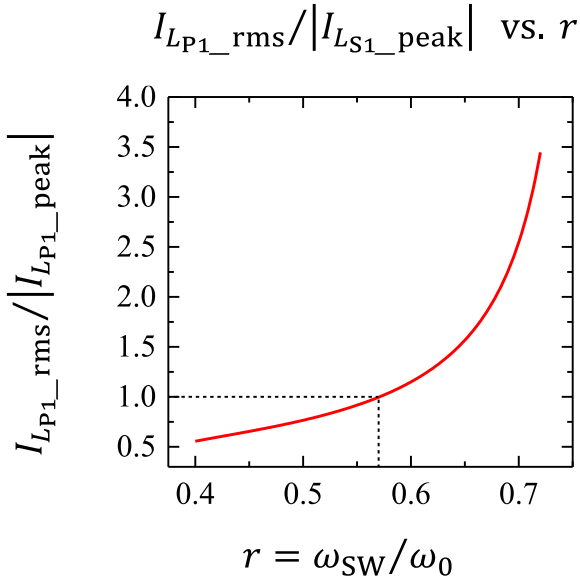

Fig. 14. Ratio of $I_{L_{P1}\_rms}/I_{L\_peak}$ versus r.

circuit. By calculating I_{base} from (10) and substituting into (19), we get

$$I_{L_{S1}\_rms} = -\frac{g(y)}{y\cos y + \sin y}\left|I_{L_{S1}\_peak}\right| \quad (29)$$

$$I_{L_{P1}\_rms} = -\frac{h(y)}{y\cos y + \sin y}\left|I_{L_{S1}\_peak}\right| \quad (30)$$

with $g(y)$ and $h(y)$ from (21) and (22), respectively. Equation (29) allows to select r_{min} based on rms currents. Fig. 13 shows the variations of $I_{L_{S1}\_rms}/\left|I_{L_{S1}\_peak}\right|$ versus r. For a fixed number for $\left|I_{L_{S1}\_peak}\right|$, the value of $I_{L_{S1}\_rms}$ gets smaller at r values greater than 0.44 and the decreasing trend continues to about $r = 0.68$. Thus, it is advantageous to select r_{min} of higher than 0.5 to get less rms current for the same peak value. It is necessary to monitor the values of $I_{L_{P1}\_rms}$ as well. Fig. 14 depicts that for $r > 0.57$, the ratio of $I_{L_{P1}\_rms}/\left|I_{L_{S1}\_peak}\right|$ exceeds one and grows rapidly. Therefore, it is better to choose a r_{min} between 0.5 and 0.57.

V. Auxiliary Experimental Results

Experimental verification of the merits of the proposed auxiliary is provided in this section. The examined auxiliary

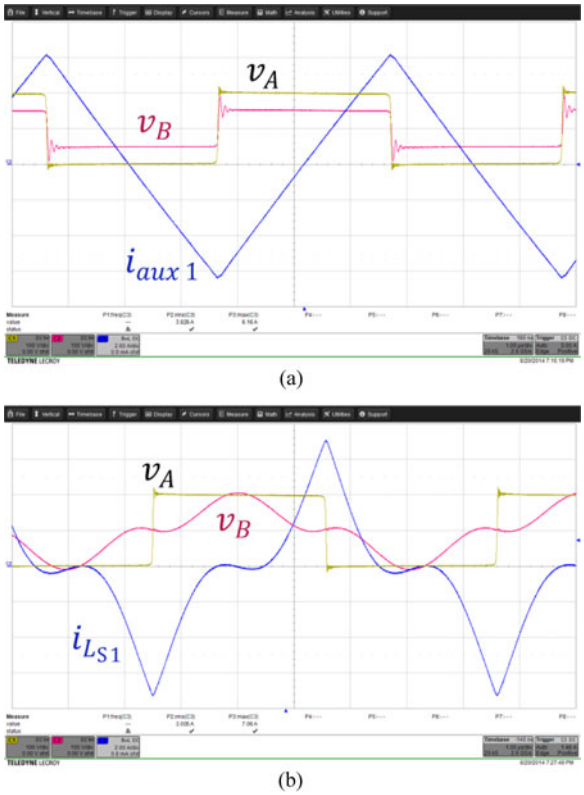

Fig. 15. Experimental waveforms at $r = 0.42$: (a) single-inductor auxiliary and (b) proposed auxiliary (100 V/div and 2 A/div).

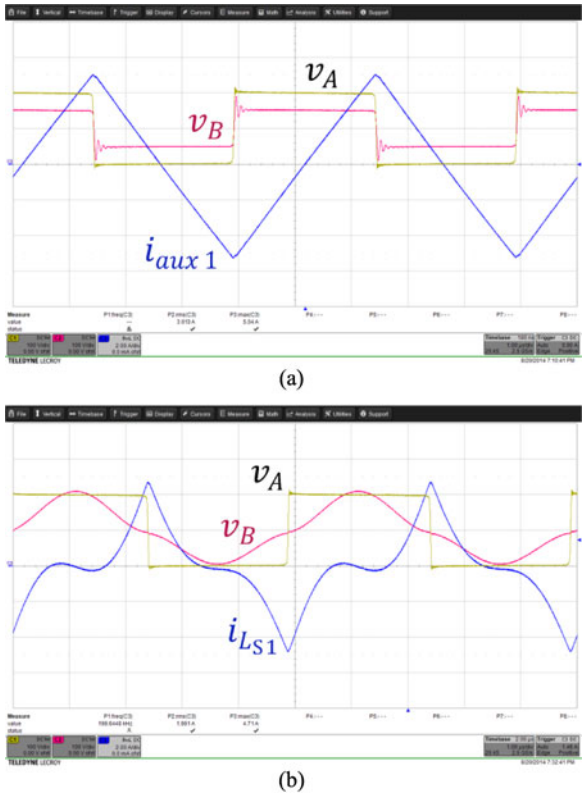

Fig. 16. Experimental waveforms at $= 0.51$: (a) single-inductor auxiliary and (b) proposed auxiliary (100 V/div and 2 A/div).

circuit included $L_{S1} = L_{P1} = 11\,\mu$H, $C_{P1} = 30$ nF, and $C_{a1} = C_{a2} = 10\,\mu$F. The switching frequency range was from 167 to 227 kHz. V_{dc} was selected to be 200 in all the experiments. Because of the linearity of the auxiliary components, the currents are linear to the voltage so testing at one voltage level was sufficient. This means that the auxiliary inductors were being used in their linear operating regions and not close to saturation.

Using the component values, ω_0 was 2.462 Mrad/s, or 392 kHz. I_{base} was 5.8 A. Three frequency ratios of $r = 0.42$, 0.51, and 0.58 were examined, i.e., 167, 200, and 227 kHz. Because in the case of the single-inductor auxiliary, the inductance is twice as large as in the case of the proposed auxiliary, the tests were done by disconnecting C_{P1} from node *B* defined in Fig. 2 to have the single-inductor auxiliary circuit. Figs. 15–17 illustrate the experimental waveforms for $r = 0.42$, 0.51, and 0.58, respectively. Note that v_A and v_B were measured to the negative line of dc input (and not to node *G*). The peak and rms values are given in Table I and Fig. 18.

In Fig. 15, $r = 0.42$ and the peak current in the proposed auxiliary is greater than of that of single inductor. On the other hand, in Fig. 17, $r = 0.58$ and the proposed inductor has a lower peak current. Also Fig. 18 shows that the proposed inductor provides a lower rms current for all peak currents examined, in agreement with the analytical predictions.

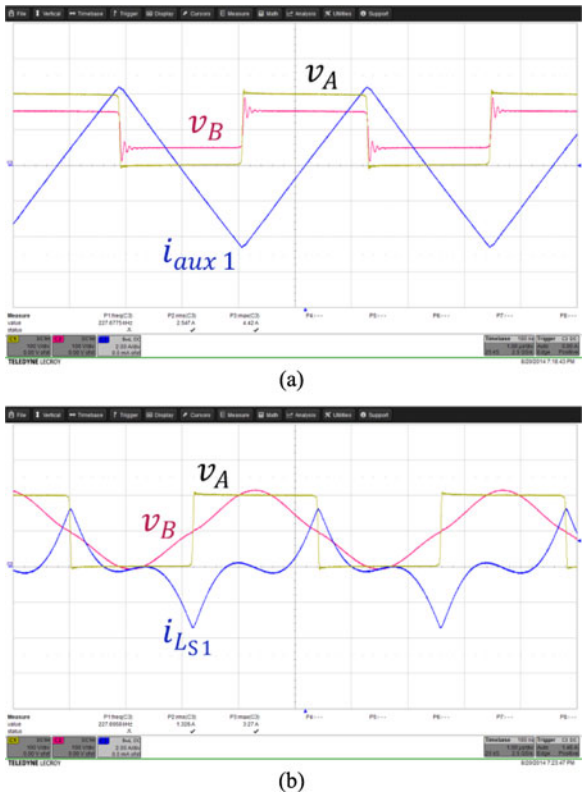

Fig. 17. Experimental waveforms at $= 0.58$: (a) single-inductor auxiliary and (b) proposed auxiliary (100 V/div and 2 A/div).

TABLE I
EXPERIMENTAL CURRENTS

	Single Inductor		Proposed	
	Peak (A)	rms (A)	Peak (A)	rms (A)
0.42	6.16	3.826	7.06	3.005
0.51	5.04	3.013	4.71	1.995
0.58	4.42	2.547	3.27	1.326

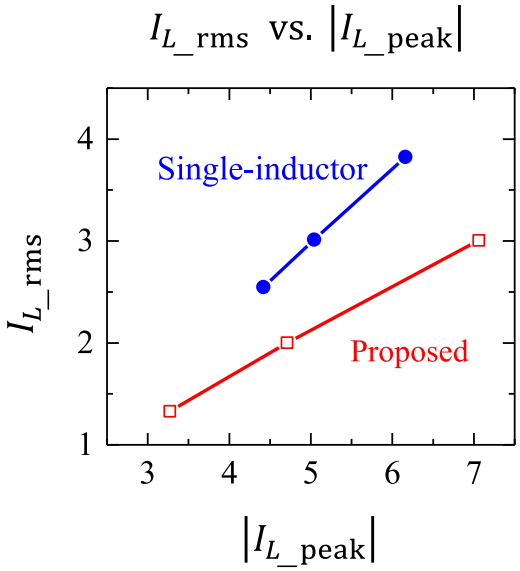

Fig. 18. Experimental currents.

TABLE II
CONVERTER SPECIFICATIONS

Symbol	Parameter	Value
$P_{\text{out\_nom}}$	Nominal output power	750 W
V_{dc}	Input voltage	200–300 V
$V_{\text{out\_nom}}$	Nominal output voltage	57.6 V
f_s	Switching frequency	200 kHz

VI. DESIGN EXAMPLE AND EFFICIENCY MEASUREMENTS

In this section, the steps to design the proposed auxiliary for the converter in Fig. 1 are given. A 750-W prototype was implemented to verify the performance of the auxiliary circuit within a dc–dc converter. The converter specifications are shown in Table II. The load consists of 24 lead-acid battery cells which can reach to 2.4 V/cell in boost charge mode, i.e., $V_{\text{out\_nom}}$ of 57.6 V.

In principle, it is possible to design the converter such that the energy in the transformer leakage inductor L_{leak} in Fig. 1, provides ZVS for heavy-load operating points [21]. In practice, however, this choice results in a large value for L_{leak} and some unwanted consequences: the duty cycle of v_{EF} will be considerably less than $v_{AA'}$, and this difference is load dependent. To compensate for this loss of duty cycle, the transformer turns ratio must be reduced, which increases the current in the switches

TABLE III
CONVERTER COMPONENT VALUES

Symbol	Parameter	Value
N	Transformer turns ratio	2.5:1
L_{leak}	Transformer leakage inductance (primary)	$<$500 nH
L_M	Transformer magnetizing inductance (primary)	$>$5 mH
L_{out}	Output filter inductor	5 μH
C_{out}	Output filter capacitor	100 μF
S_{1U}, S_{1L}, S_{2U}, S_{2L}	Switches	APT84F50B2

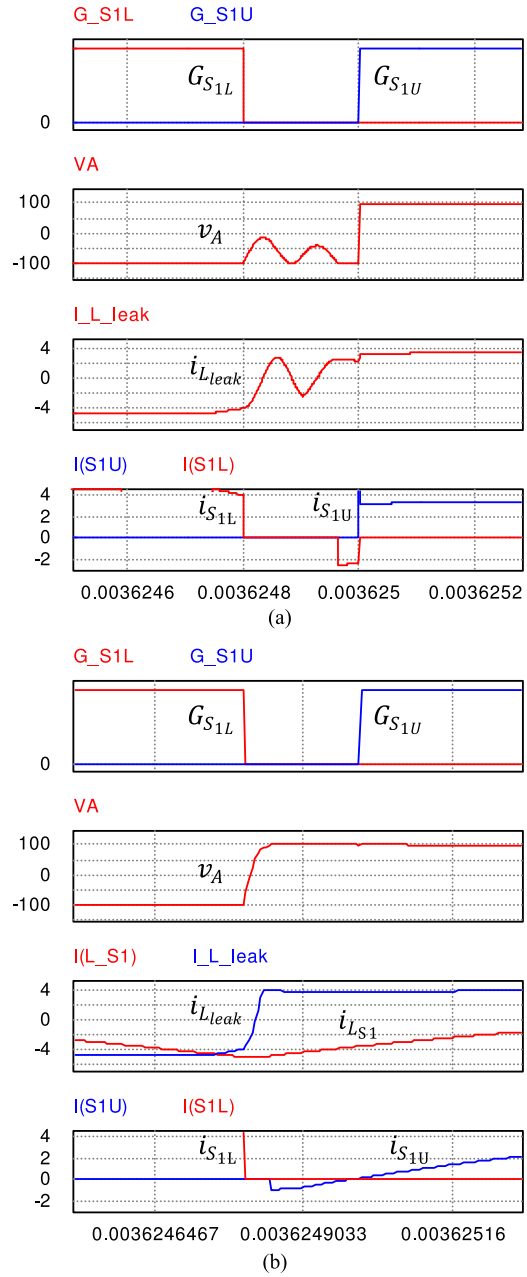

Fig. 19. Waveform of leading leg during deadtime at full load and $V_{\text{dc}} =$ 200 V: (a) without auxiliary circuit and (b) with auxiliary circuit.

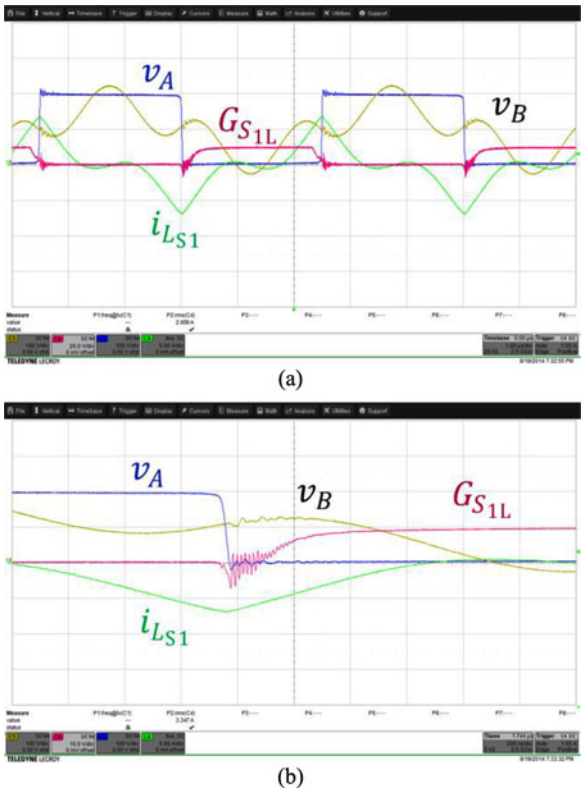

Fig. 20. ZVS turn-on of S_{1L}, with proposed auxiliary circuits for V_{dc} of 200 V and 10% load. v_A, v_B, and $v_{G_{S_{1L}}}$ are measures to the negative line of dc input. Falling of v_A (the voltage across S_{1L}) happens before rising edge of $G_{S_{1L}}$ so S_{1L} turns on under ZVS. No voltage spikes are observed (100 V/div for v_A and v_B, 10 V/div for and $v_{G_{S_{1L}}}$, and 2 A/div for $i_{L_{S1}}$).

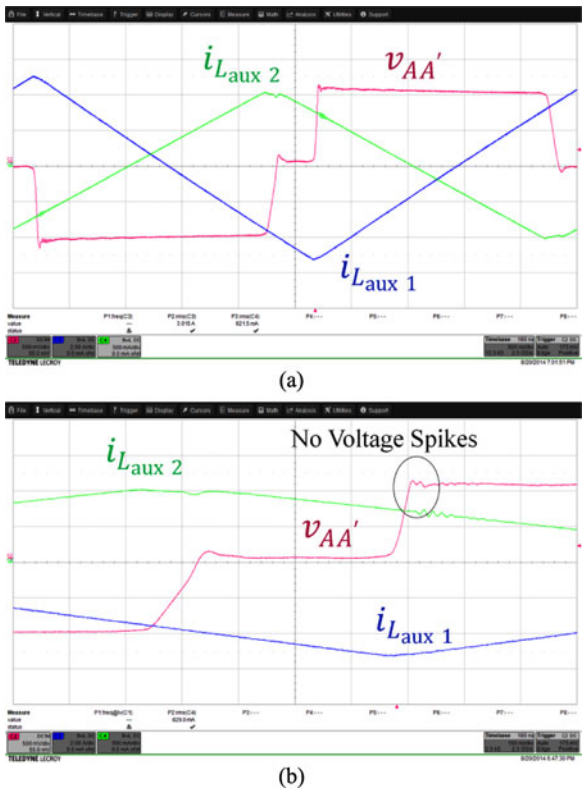

Fig. 21. ZVS turn-on of S_{1U}, with single-inductor auxiliary circuit for V_{dc} of 200 V and 10% load. S_{1U} turns on under ZVS. No voltage spikes are observed (100 V/div for $v_{AA'}$, 2 A/div for $i_{L_{aux1}}$, and 500 mA/div for $i_{L_{aux2}}$).

and decreases the efficiency. On the other hand, having a transformer with a small L_{leak} minimizes the load-dependent duty cycle difference between v_{EF} and $v_{AA'}$. Thus, in ideal case, V_{out} becomes a function of V_{dc} and phase shift, with a reduced dependence on the load level (when the converter operates in continuous current mode). The selected values for the converter are listed in Table III. The deadtime was 200 ns and the switches were APT84F50B2 with R_{ds}(on) of 100 mΩ in warm state and effective drain–source capacitors of 0.845 nF. MOSFET drivers were IR2181.

For the lagging leg, S_{2U} and S_{2L}, the single inductor auxiliary L_{aux2} is 100 μH, to provide enough current to charge/discharge the drain–source capacitors of S_{2U} and S_{2L} during the deadtime in no-load situations. With existence of a load higher than 10% the lagging leg always operates under ZVS turn-on. In the entire experiment L_{aux2} was kept connected. For the leading leg, S_{1U} and S_{1L}, the situation is different. Fig. 19 depicts the simulated waveform of leading leg during deadtime at full load and $V_{dc} = 200$ V without any auxiliary circuit (using PSIM software ver. 9.3). v_A is measured to node G in Fig. 1. Due to the low value of L_{leak}, even at full-load situation, the energy in L_{leak} is not enough to change the polarity of S_{1U} and S_{1L} drain–source capacitors during the deadtime and v_A does not reach to 100 V before the rising moment of $G_{S_{1U}}$. Thus, S_{1U} has a hard switching turn-on. This is shown clearly in Fig. 19(a).

In presence of the auxiliary circuit, Fig. 19(b), v_A continues to rise monotonically to 100 V after turning off of S_{1L}. At the same time, $i_{L_{leak}}$ becomes positive. To keep v_A at 100 V level (needed for ZVS turn-on of S_{1U}), there must be a current path to provide $i_{L_{leak}}$ and this is the auxiliary circuit. In other words, in addition to the current needed for changing the polarity of S_{1U} and S_{1L} drain–source capacitors, the auxiliary circuit should provide $i_{L_{leak}}$ during the deadtime. Thus, the auxiliary circuit must be sized for the largest $i_{L_{leak}}$, which happens at the lowest V_{dc}, highest V_{out}, and highest load current. In the converter under consideration, these values were 200 V, 57.6 V, and 12.76 A, respectively. The largest $i_{L_{leak}}$ during deadtime was 3.68 A, and considering the 1.69 A needed to charge/discharge two effective drain–source capacitors of 0.845 nF, the peak current of the auxiliary branch must be larger than 5.37 A. Thus, L and C were selected as 11 μH and 15 μF.

The effectiveness of the proposed auxiliary to maintain the ZVS trun on for the leading leg switch S_{1L} is evident in Fig. 20(a) and the magnified one in Fig. 20(b) for V_{dc} of 200 V and 10% load. Note that v_A, v_B, and $v_{G_{S_{1L}}}$ are measured to the negative line of dc input. Falling of v_A (the voltage across S_{1L} due to measuring to the negative dc line) happens before rising edge of $G_{S_{1L}}$. This means that S_{1L} turns on under ZVS. No voltage spikes are observed. The same ZVS situation is in place for switch S_{1U} (not shown).

The bridge voltage $v_{AA'}$ and the auxiliary currents for leading and lagging legs are shown in Figs. 21 and 22, under the same

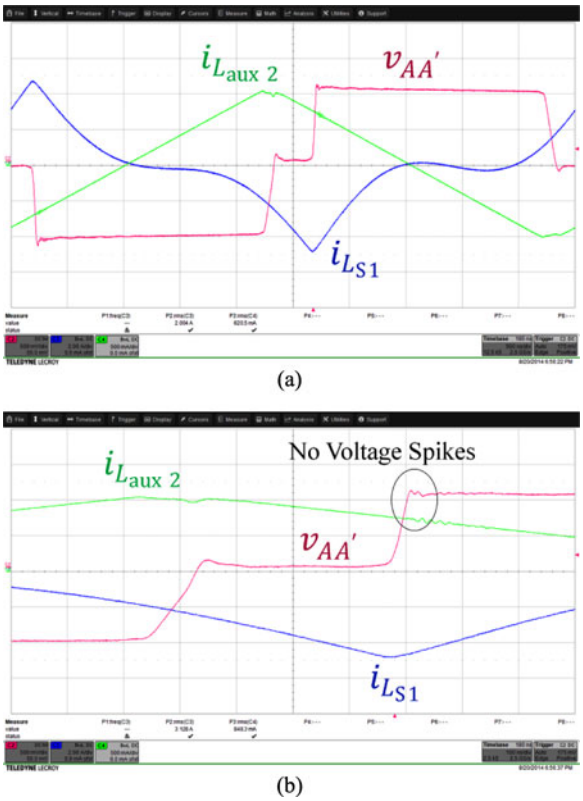

Fig. 22. ZVS turn-on of S_{1U}, with proposed auxiliary circuit for V_{dc} of 200 V and 10% load. S_{1U} turns on under ZVS. No voltage spikes are observed (100 V/div for $v_{AA'}$, 2 A/div for $i_{L_{aux1}}$, and 500 mA/div for $i_{L_{aux2}}$).

conditions as in Fig. 20 for the single-inductor and the proposed auxiliaries. The voltage measurements were done with a differential probe. The smoothness of rising edge and absence of voltage spikes in $v_{AA'}$ reveal the effectiveness of both types of auxiliaries in maintaining ZVS turn-on for switch S_{1U}. This proves that there is no difference in functionality of the single-inductor and the proposed auxiliaries as far as ZVS is concerned. And the proposed auxiliary did the same function with a lower rms current.

The impact of the auxiliary circuit choices for the leading leg on the efficiency of the prototype converter is depicted in Fig. 23, for V_{dc} of 200 and 300 V. The general trends for both the dc voltages levels were similar: without any auxiliary circuit, the efficiency was measures for various load levels as the baseline.

The single inductor was capable of reducing the switching losses more than the additional conduction losses introduced in the circuit so the efficiency increased for all the load levels. The proposed auxiliary enhanced the efficiency more effectively for the lower load levels compared with the heavy-load situations. At 80% and above, the conduction losses were dominant and the difference between two types of the auxiliaries became negligible.

Although the proposed auxiliary is capable of providing the same functionality with lower rms current and sharper frequency dependence, there are some consequences such as a slightly higher component count, and the need to design the auxiliary inductors well below the saturation level of their cores.

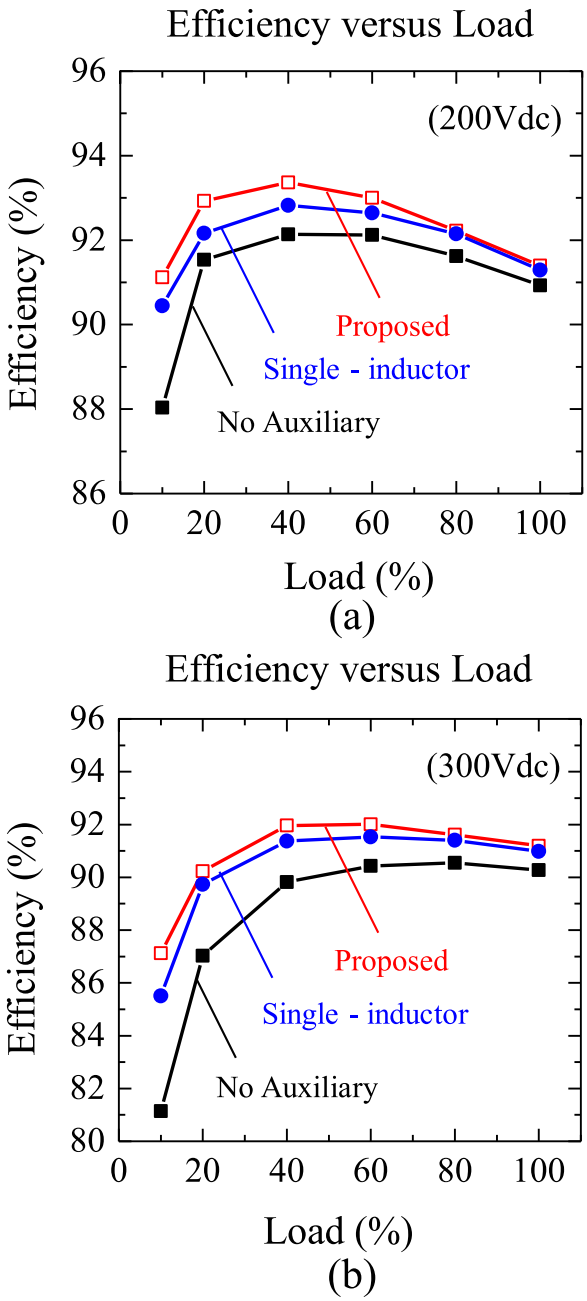

Fig. 23. Efficiency curves in absence of auxiliary circuit, with single-inductor and proposed auxiliary circuits (for leading leg) for V_{dc} of 200 V (left) and 300 V (right).

Also the design requires low ESR and ESL capacitors for dc bus and the splitting branches, due to the higher harmonic content in the auxiliary current as shown in Fig. 12.

VII. Conclusion

A simple passive auxiliary circuit is proposed to obtain ZVS operation of switches for the entire operational conditions of the phase-shift full-bridge converter. The details of auxiliary circuit are described. Experimental results confirm the effectiveness of

the proposed circuit in providing the peak current with lower rms value with no significant increscent in the conduction loss.

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