Letters

A Rapid Switch Bridge Selection Method for Fully Integrated DC–DC Buck Converters

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***Abstract*—This letter presents a method for optimum selection of synchronous buck converter switch bridge topology and devices in the CMOS technology of choice. The comparative method targets maximum power efficiency, and it assumes an application where the dc–dc converter is on the same IC as the load with a known constant operating point. As its principal idea, the method circumvents the need for exhaustive comparative simulation work to cover the vast design space of available MOS device and cascode/noncascode topology combinations. Instead, the method narrows the space by using a set of basic parameters to approximate the best combination. The result, thus, provides sharp focus for subsequent detailed design and topology-dependent optimization. The method is illustrated by comparing its results to simulations of synchronous 3.3–1.65-V buck converters in 45 and 65-nm CMOS with core, I/O, and high-voltage devices.**

***Index Terms*—Buck converter, cascode, circuit optimization, CMOS, monolithic integration.**

I. Introduction

COMPLETE dc–dc converter integration for system-on-chip (SoC) solutions is a growing research trend. The main attraction lies in the reduced system size that is required for deriving SoC voltage domains from an external battery. The *LC*-based synchronous buck downconverters are one of the major architectures, with switching frequencies (f_{SW}) in tens or hundreds of megahertz being proposed in order to integrate the output *LC* filter in Fig. 1 [1]. However, low core device breakdown voltages in nanoscale CMOS often prevent the use of single switches for commonly used battery voltages (V_{IN}), such as 3.6–3.7 V for Li-ion applications. Various cascode topologies and/or high-voltage (HV) devices, when available, have thus been proposed as a solution [2], [3].

Despite such solutions, the goal of maximizing the power efficiency η is met with a very large design space, once specifications on V_{IN}, output voltage V_{OUT}, and the range of load current I_L are known. This space consists of the variety of cascode/noncascode switch bridge topologies and available MOS switch devices in a given CMOS technology. One may undertake time-consuming comparative design work and simulations. However, it would be significantly more effective to first narrow down the design space with a predesign benchmark method. Its results can then provide sharp focus for the actual detailed design process and topology-dependent optimization strategy.

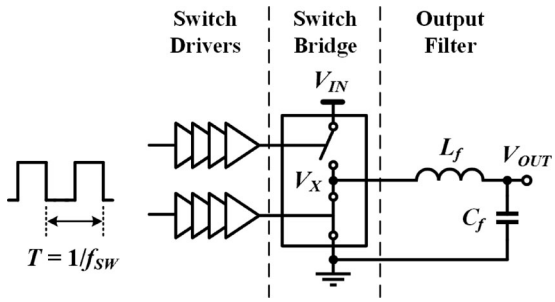

Fig. 1. Simplified schematic of a generic synchronous buck converter.

This letter proposes a method for selecting the buck converter switch bridge topology and device type combination that maximizes η in the CMOS technology of choice. It is chiefly intended for cases where the load is on the same chip and requires a constant supply voltage and I_L. Section II discusses the design space and presents a method for rapid comparison of available topology/device combinations. Section III confirms the method through simulation of three example topologies with different MOS devices in 45 and 65-nm CMOS. Conclusions are presented in Section IV.

II. Systematic Topology/Device Comparison

A. Design Space Considerations

The design space for fully integrated buck converters consists of 1) *m* available switch device types and 2) *n* possible switch bridge topologies. With regards to devices, typical nanoscale (22–90 nm) CMOS technologies offer high-performance core transistors for supply voltages around 0.9–1.2 V, in many threshold voltage (V_{th}) variations also within one technology. They also offer thick-oxide I/O devices (1.8/2.5/3.3 V), and some include specialized HV devices for supplies of 5 V or above that are of special interest for dc–dc converters [4]. All device types differ from each other in parasitic characteristics, which is especially important for fully integrated high-f_{SW} conversion.

With regards to topologies, the intended battery voltage V_{IN} is an important factor. Specifically, device breakdown voltages

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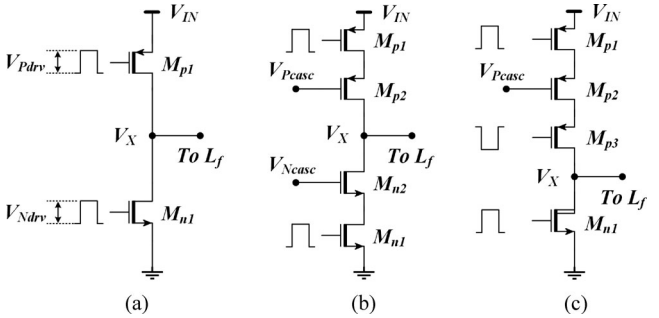

Fig. 2. Example buck converter switch bridges: (a) symmetric 1×1, (b) symmetric 2×2, and (c) asymmetric 3×1.

$V_{\mathrm{break},i}$ play the most significant role. The basic synchronous buck converter topology with one NMOS and one PMOS device in Fig. 2(a) is sufficient when $V_{\mathrm{IN}} \leq V_{\mathrm{break},i}$. For example, 1.8-to-0.9-V conversion can be done by using single 1.8-V I/O or 5-V HV devices. Device cascoding such as in Fig. 2(b) and (c) enables higher values for V_{IN}, such that $V_{\mathrm{IN,max}} = \min(p \cdot V_{\mathrm{break},p}, q \cdot V_{\mathrm{break},q})$. Here, p and q are, respectively, the number of high-side PMOS and low-side NMOS switch devices, and $V_{\mathrm{break},p}$ and $V_{\mathrm{break},q}$ are their breakdown voltages. For example, the symmetric 2×2 cascode in Fig. 2(b) is used in [2] for 3.6-to-1.8-V conversion with $V_{\mathrm{break},i} = 2.5$ V, whereas the asymmetric 3×1 cascode in [3] combines three 1.8-V PMOS devices with only one 4.2-V HV NMOS device for $V_{\mathrm{IN}} = 2.8{-}4.2$ V.

Consequently, the design space theoretically consists of $m \cdot n$ combinations of switch devices and switch bridge topologies. The number of available combinations is considerable, and no option emerges intuitively as the most power-efficient solution. For instance, the use of HV CMOS devices minimizes the number of devices in the switch bridge, but they are not available in all technologies. Furthermore, some of them have significant parasitic losses in high-speed switching applications such as fully integrated dc–dc converters. Cascodes present a similar problem: it is not trivial whether a 2×2 cascode with less I/O devices is more efficient than, for example, a 3×3 cascode with fast core devices. Instead of extensive comparative optimization in the full design space, we propose a method that finds the best topology/device combination for subsequent detailed design.

B. Modeling

The proposed method is based on approximative buck converter component modeling. Loss modeling alternatives of varying complexity are presented in [5]–[8], specifically for high-frequency operation. We assume pulse width modulation and continuous conduction mode operation, which is so far the main mode at $f_{\mathrm{SW}} > 100$ MHz. We also assume an output power (P_{out}) in a multimilliwatt range. Our approach targets simplicity and good comparative accuracy at some cost on absolute accuracy, and includes the main loss sources from [6], as detailed later. Especially at lower P_{out}, smaller sources such as conduction leakage, implementation-dependent level shifters, and bulk conduction may be added to further increase accuracy, at the cost of reduced ease of use.

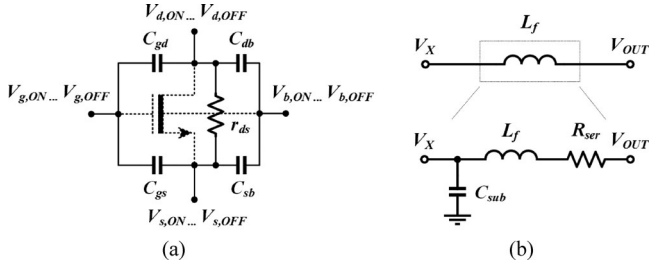

Fig. 3. Component models for comparative loss analysis: (a) MOS transistor and (b) filter inductor L_f.

First, we employ the simplified MOS transistor model in Fig. 3(a). In addition to channel on-resistance r_{ds}, it includes the gate–source (C_{gs}), gate–drain (C_{gd}), drain–bulk (C_{db}), and source–bulk (C_{sb}) capacitances to account for switching losses. Their value is the averaged capacitance when the transistor is switched between the ON/OFF states. Conduction losses in one device are given as

$$P_{\mathrm{res},i} = \alpha \frac{r_{\mathrm{ds0}}}{W_i V_{\mathrm{ov}}} \left(I_L^2 + \frac{I_R^2}{3} \right) \tag{1}$$

where $\alpha = D$ for PMOS devices and $\alpha = 1 - D$ for NMOS devices, D is the switching duty cycle, r_{ds0} is a resistance parameter for a minimum-length unit-width switch, W_i is the designed channel width, V_{ov} is the designed gate overdrive voltage, and I_L and I_R are, respectively, the converter load current and inductor current ripple. For a device modeled as in Fig. 3(a), the switching loss is expressed as

$$P_{\mathrm{cap},i} = W_i f_{\mathrm{SW}} \sum C_{jk0} ([V_{j,\mathrm{ON}} - V_{k,\mathrm{ON}}] - [V_{j,\mathrm{OFF}} - V_{k,\mathrm{OFF}}])^2 \tag{2}$$

where C_{jk0} is the parasitic capacitance between terminals j and k for a unit-width device, and $V_{j/k,\mathrm{ON}}$ and $V_{j/k,\mathrm{OFF}}$, respectively, are the terminal voltages when the device does or does not conduct. The same device type, model, and dynamic loss in (2) are assumed for the switch driver inverters. With a 3:1 tapering factor, the loss $P_{\mathrm{drv},i}$ of one driver converges to 1.5 times the loss of its final stage.

Second, parasitic effects in the integrated inductor L_f can form a significant part of the total loss. As proposed in [5], the inductor loss P_{ind} can be approximated as the sum of series conduction losses and switching losses due to substrate capacitance. Based on the model in Fig. 3(b)

$$P_{\mathrm{ind}} = R_{\mathrm{ind0}} L_f \left(I_L^2 + \frac{I_R^2}{3} \right) + C_{\mathrm{ind0}} L_f V_{\mathrm{IN}}^2 f_{\mathrm{SW}}. \tag{3}$$

where $R_{\mathrm{ind0}} = R_{\mathrm{ser}}/L_f$ and $C_{\mathrm{ind0}} = C_{\mathrm{sub}}/L_f$. They should be extracted in the general design value range.

Third, the values of the output filter components L_f and C_f are obtained for a desired current ripple I_R and output voltage ripple amplitude V_R. Finally, the total power loss is $P_{\mathrm{tot}} = (P_{\mathrm{out}} - \eta P_{\mathrm{in}})/\eta$, where P_{out} and P_{in}, respectively, are the power delivered to the load and consumed from the battery. For a given combination of topology and switch devices, P_{tot}

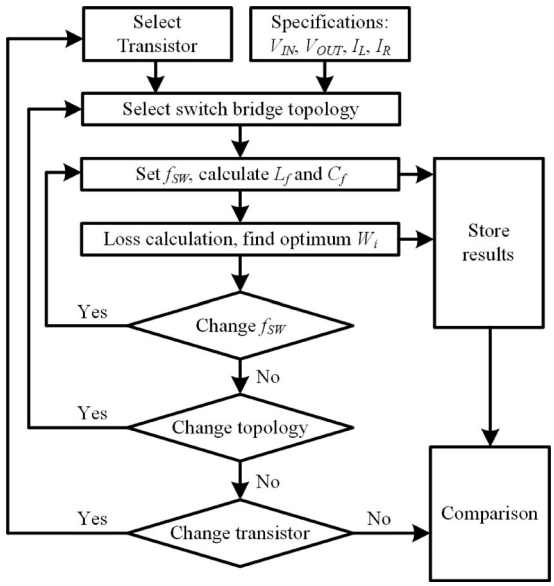

Fig. 4. Logical flow of the proposed switch bridge selection method.

is obtained from (1)–(3) as

$$P_{\rm tot} = \sum (P_{{\rm res},i} + P_{{\rm cap},i} + P_{{\rm drv},i}) + P_{\rm ind}. \qquad (4)$$

C. Comparison of Topologies and Devices

In essence, the proposed approach is to find the minimum $P_{\rm tot}$ analytically for each interesting topology/device combination. Fig. 4 depicts the iteration of combinations. Each topology in turn is optimized analytically with every interesting device type, to approximate the minimum achievable loss $P_{\rm tot}$ in (4). This is done by solving $d(P_{{\rm res},i} + P_{{\rm cap},i} + P_{{\rm drv},i})/dW_i = 0$ separately for each device at each interesting $f_{\rm SW}$. To characterize a device, C_{jk0} and $r_{\rm ds0}$ must be extracted from a simple testbench. In the loss calculation phase, $P_{{\rm res},i}$ from (1) is topology independent, as is $P_{\rm ind}$ from (3). However, $P_{{\rm cap},i}$ in (2) depends on the topology. These equations must thus be derived separately for each topology of interest, and an example is provided in Section III. I_R and V_R are kept constant.

The method is mainly intended for a constant $V_{\rm IN}$ and I_L. However, if required, it can account for minor variation of $V_{\rm IN}$ and I_L in two alternative ways. In both, the optimum W_i and $P_{\rm tot}$ are first calculated for all topology/device combinations at selected points of the specified ($V_{\rm IN}$, I_L) range. Then, 1) the $P_{\rm tot}$ of each resulting fixed-W_i design is used to select the best overall combination and its fixed W_i, or 2) the $P_{\rm tot}$ values are compared as combination-specific sets, and the required nonfixed W_i of the best overall combination are implemented with width control techniques [9].

III. Simulation Example

To illustrate and verify the proposed method, we design and simulate synchronous buck dc–dc converters in 45 and 65-nm CMOS. As general specifications, we define $V_{\rm IN} = 3.3$ V, $V_{\rm OUT} = 1.65$ V, $I_L = I_R = 150$ mA, and $V_R = 80$ mV. The switching frequency $f_{\rm SW}$ can be selected freely.

TABLE I
NMOS/PMOS Device Parameters Used in Switch Bridge Comparison

Param./Circuit	1 × 1 (65 nm)	2 × 2 (65 nm)	2 × 2 (45 nm)	3 × 3 (45 nm)
$V_{\rm break}$ [V]	5	1.8	1.8	1.1
$C_{\rm gs0}$ [fF/μm]	0.45/0.42	0.56/0.55	0.46/0.55	0.30/0.34
$C_{\rm gd0}$ [fF/μm]	0.40/0.37	0.50/0.49	0.46/0.52	0.30/0.33
$C_{\rm db0}$ [fF/μm]	0.45/0.49	0.45/0.34	0.39/0.42	0.37/0.39
$r_{\rm ds0}$ [$\Omega\cdot\mu$m·V]	5807/12780	1513/3876	787/2222	250/714
$V_{\rm th}$ [V]	0.6/−0.6	0.6/−0.6	0.55/−0.5	0.55/−0.55

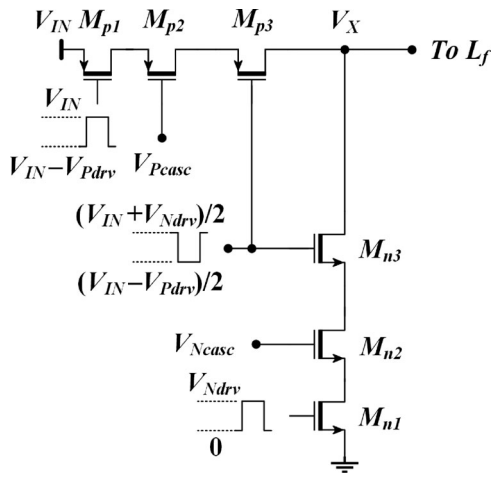

Fig. 5. Schematic of a synchronous buck converter with a 3 × 3 switch bridge and three gate driver signals.

Both CMOS technologies offer core devices and thick-oxide devices, and the 65-nm technology offers a 5-V HV device. In view of $V_{\rm IN} = 3.3$ V, the most straightforward 65-nm options are 1) a 1 × 1 bridge with HV devices (one driver) or 2) a 2 × 2 cascode with 1.8-V I/O devices (two drivers). For 45 nm, we compare 3) a 2 × 2 cascode with 1.8-V I/O devices (two drivers) and 4) a 3 × 3 cascode [6] with 1.1-V core devices (three drivers). Table I summarizes the pertinent unit device data. The topologies are depicted in Fig. 2(a), (b) and Fig. 5, and the respective gate drive voltage amplitudes ($V_{N\rm drv}$ and $V_{P\rm drv}$) are chosen as 3.3, 1.8, and 1.1 V. For the 2 × 2 cascode, $V_{N\rm casc} = 1.8$ V and $V_{P\rm casc} = 1.5$ V, whereas $V_{N\rm casc} = 1.1$ V and $V_{P\rm casc} = 2.2$ V for the 3 × 3 cascode. Device sources are connected to their local bulks.

We then use the method outlined in Section II-C. First, $P_{{\rm res},i}$ is calculated based on (1) for each device in all topologies. Second, $P_{{\rm cap},i}$ is topology dependent, and the equations for the 2 × 2 cascode are derived in [2]. Using Fig. 5 and its defined terminal voltage swings, the respective $P_{{\rm cap},i}$ equations for each device in the 3 × 3 cascode are derived as

$$\begin{aligned} P_{{\rm cap},M_{p1}} \approx\ & W_{p1}(C_{{\rm gs},p1}(V_{\rm IN} - V_{P\rm drv})^2 \\ & + C_{{\rm gd},p1}(V_{P\rm casc} + V_{P\rm drv} - 2V_{\rm IN} - V_{{\rm th}P})^2 \\ & + C_{{\rm db},p1}(V_{P\rm casc} - V_{\rm IN} - V_{{\rm th}P})^2) f_{\rm SW} \qquad (5) \\ P_{{\rm cap},M_{p2}} \approx\ & W_{p2}(C_{{\rm gs},p2}(V_{\rm IN} + V_{{\rm th}P} - V_{P\rm casc})^2 \\ & + C_{{\rm gd},p2}((-V_{IN} - V_{P\rm drv})/2 - V_{{\rm th}P})^2 \\ & + C_{{\rm db},p2}((V_{\rm IN} - V_{P\rm drv})/2 - V_{P\rm casc})^2) f_{\rm SW} \qquad (6) \end{aligned}$$

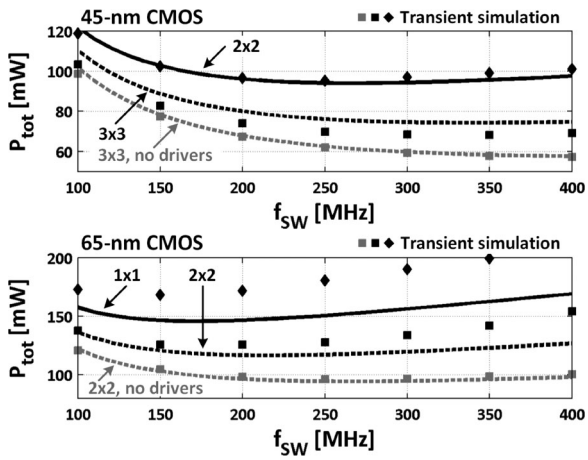

Fig. 6. Comparison of analytical (lines) and simulated (markers) results. (a) Approximated converter losses with 2×2 (I/O) and 3×3 (core) topologies in 45 nm, and (b) 1×1 (HV) and 2×2 (I/O) cascode topologies in 65-nm CMOS.

$$\begin{aligned} P_{\mathrm{cap},M_{p3}} \approx\ & W_{p3}(C_{\mathrm{gs},p3}((V_{N\mathrm{drv}} - V_{\mathrm{IN}})/2 - V_{\mathrm{th}P})^2 \\ & + C_{\mathrm{gd},p3}((V_{N\mathrm{drv}} + V_{P\mathrm{drv}})/2 - V_{\mathrm{IN}})^2 \\ & + C_{\mathrm{db},p3}((V_{\mathrm{IN}} - V_{P\mathrm{drv}})/2 - V_{\mathrm{th}P})^2) f_{\mathrm{SW}} \quad (7) \\ P_{\mathrm{cap},M_{n3}} \approx\ & W_{n3}(C_{\mathrm{gs},n3}((V_{\mathrm{IN}} - V_{P\mathrm{drv}})/2 - V_{\mathrm{th}N})^2 \\ & + C_{\mathrm{gd},n3}((V_{N\mathrm{drv}} + V_{P\mathrm{drv}})/2 - V_{\mathrm{IN}})^2 \\ & + C_{\mathrm{db},n3}((V_{\mathrm{IN}} - V_{N\mathrm{drv}})/2 + V_{\mathrm{th}N})^2) f_{\mathrm{SW}} \quad (8) \\ P_{\mathrm{cap},M_{n2}} \approx\ & W_{n2}(C_{\mathrm{gs},n2}(V_{N\mathrm{casc}} - V_{\mathrm{th}N})^2 \\ & + C_{\mathrm{gd},n2}((V_{\mathrm{IN}} + V_{N\mathrm{drv}})/2 - V_{\mathrm{th}N})^2 \\ & + C_{\mathrm{db},n2}((V_{\mathrm{IN}} + V_{N\mathrm{drv}})/2 - V_{N\mathrm{casc}})^2) f_{\mathrm{SW}} \quad (9) \\ P_{\mathrm{cap},M_{n1}} \approx\ & W_{n1}(C_{\mathrm{gs},n1} V_{N\mathrm{drv}}^2 \\ & + C_{\mathrm{gd},n1}(V_{N\mathrm{casc}} - V_{\mathrm{th}N} + V_{N\mathrm{drv}})^2 \\ & + C_{\mathrm{db},n1}(V_{N\mathrm{casc}} - V_{\mathrm{th}N})^2) f_{\mathrm{SW}}. \quad (10) \end{aligned}$$

The optimum gate width W_i at each value of f_{SW} is found analytically from $d(P_{\mathrm{res},i} + P_{\mathrm{cap},i} + P_{\mathrm{drv},i})/dW_i = 0$. Based on (4), this minimizes the total loss P_{tot}. Finally, $R_{\mathrm{ind}0} = 0.1\ \Omega/\mathrm{nH}$ and $C_{\mathrm{ind}0} = 50$ fF/nH.

Fig. 6 plots the resulting minimum values of P_{tot} for $f_{\mathrm{SW}} = 100{-}400$ MHz for all variants, such that L_f, C_f are recalculated and all device W_i are separately optimized for each f_{SW}. In 65 nm, the 2×2 cascode with 1.8-V I/O devices is potentially more efficient than the 1×1 bridge with HV devices. In light of the greater number of devices in the 2×2 cascode, the result is counter intuitive and highlights the usefulness of the proposed method. The same conclusion holds for 45 nm, where a 3×3 cascode is potentially more efficient than its 2×2 counterpart. For all cases, a greater number of devices is in essence countered by lighter parasitics and lower terminal voltage swings. The absolute loss difference becomes more critical for higher I_L, where the method is particularly useful.

The results from a numerical transient simulation of a corresponding schematic design are included. For reliability, the simulation uses complete BSIM4 MOS device modeling with the solved optimum sizes W_i and four-stage inverter drivers, and L_f uses the model in Fig. 3(b). P_{tot} is calculated in steady-state operation. Fig. 6 mostly shows a good match and confirms the comparative conclusions, with differences especially at high frequencies caused by the simple switch model, and the non-modeled effect of switch r_{ds} on the required D. Indeed, the approximations do not replace detailed design. Furthermore, a cascode complicates the design as compared to single I/O or HV devices, for example, through more drivers. The efficiency advantage must thus be weighed against the increased effort, which is a broad question beyond the limited scope of this letter. Nonetheless, the method offers valuable comparative insight about the topology/device combinations. This is critically useful data when their number is high.

IV. Conclusion

Modern low-voltage nanoscale CMOS technologies offer a wide array of MOS devices with varying characteristics. For fully integrated buck converter design, this creates a large space of possible switch bridge topology and device combinations. To avoid exhaustive simulations, the proposed technology-independent approximation method narrows down the design space and suggests the most power-efficient combination. Converter simulations with core, I/O, and HV devices in 45 and 65-nm CMOS technologies confirmed that the method produces reliable comparative results. The outcome is a sharp focus for subsequent detailed dc–dc converter design.

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