A Novel Primary-Side Controlled Universal-Input AC–DC LED Driver Based on a Source-Driving Control Scheme

Yao Chen, Changyuan Chang, *Member, IEEE*, and Penglin Yang

***Abstract*—A novel primary-side controlled universal-input ac–dc LED driver based on the source-driving control scheme is proposed in this paper, which employs low-voltage control MOSFET M_2 to drive high-voltage power MOSFET M_1 without an auxiliary winding commonly used in the conventional primary-side controlled scheme. The proposed control IC adopts minimum voltage detection circuit to monitor the zero crossing information of secondary winding current. The demagnetization time signal is generated by demagnetization time detection circuit. In addition, the ratio between the secondary winding demagnetization time T_{Demag} and switching period T_S is maintained constant by adopting the intelligent charging and discharging circuit, finally achieving high-precision constant output current. A control IC for the proposed LED driver has been fabricated in TSMC 0.35 μm 5 V/600 V CMOS/LDMOS process. Experimental results of a 3-W circuit prototype show that the constant current precision is within $\pm 1\%$ in a wide range of universal-input ac voltage from 85 to 264 V, and that above 80% efficiency is obtained when driving three 1-W LEDs. The start-up time is only 46 ms under 90 Vac and 60 Hz-input, and the standby power is tested to be lower than 142 mW under 220 Vac and 50 Hz-input.**

***Index Terms*—Constant current (CC), flyback converter, light-emitting diode (LED) driver, primary-side regulation (PSR), source driving.**

I. Introduction

RECENTLY, light-emitting diodes (LEDs) have been developed rapidly as solid-state lighting (SSL) sources. Compared to conventional light sources, LED is much smaller, more longevous, more energy-saving and environmental friendly. LEDs, which will gradually replace the traditional light sources, are widely used in residential lighting, official lighting, commercial lighting and traffic lighting field, etc., beginning to light up the world [1]–[5]. As the core component of the LED lamp, LED driver directly determines the reliability of LED lamp. Therefore, the size, life, cost, and reliability are important for low-power LED drivers in order to be better integrated with the existing lighting fixture [6]–[9].

Nonisolated LED drivers [10], [11] are more attractive than isolated drivers in terms of lower fabrication cost and higher efficiency, but some LED lamp manufacturers prefer isolated driver solutions in consideration of safety issues [12]–[15]. Generally, a flyback converter is widely used in low-power LED driver application due to low cost, electrical isolation, compact volume and simplicity [16]–[20]. In order to achieve constant current (CC) output, the traditional secondary-side regulation (SSR) scheme is usually adopted to monitor the output current information and transfer it to primary side by the feedback control loop directly connected to the secondary side [21]–[23]. A typical application of the SSR scheme requires secondary sensing circuit, an opto-coupler and reference voltage (TL431 as an example) to form a feedback loop, which can achieve high precision output current and provide negative feedback in real time [21], [22]. However, the opto-coupler makes the whole circuit complex and suffers from current-transfer ratio degradation due to temperature rise, which will affect the output performance. Another SSR scheme based on voltage following control and nonlinear carrier control method is presented in [23] to obtain CC output, instead of opto-coupler isolated feedback circuit. But line regulation range of the circuit is limited.

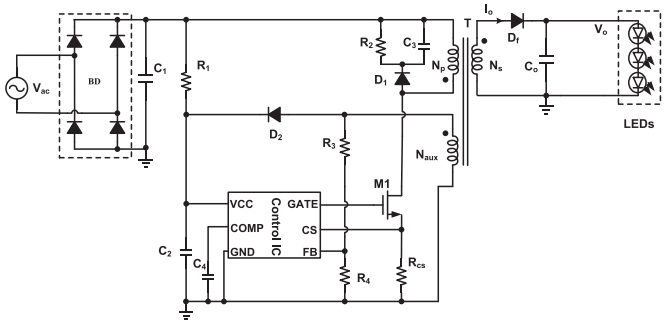

Fig. 1. System diagram of conventional universal-input PSR LED driver.

In recent years, many primary-side regulation (PSR) schemes based on gate driving have been proposed for low-power LED drivers [24]–[28], shown in Fig. 1, which adopt an auxiliary winding to sense output electrical information and provide power for the controller in normal operation. The elimination of opto-coupler and feedback network offers possibility of lower cost, lower standby power, and higher power density [29]–[32].

However, output current accuracy may be influenced owing to the noise of the primary-side current [25], [29], if detecting the primary-side current information directly. In order to avoid the problem, a PSR scheme integrated with current-mode control is proposed in [30], which complicates the controller design

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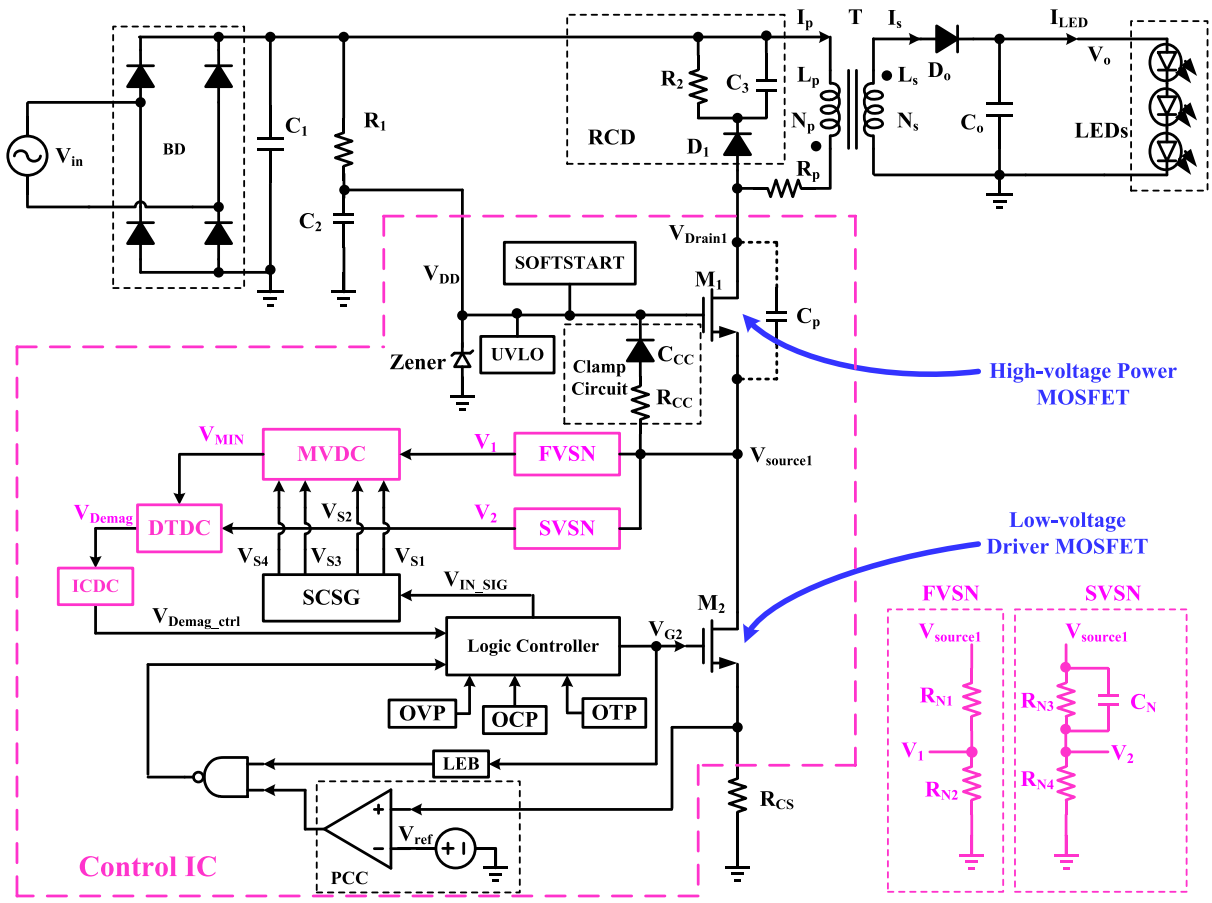

Fig. 2. System diagram of the proposed primary-side controlled universal-input ac–dc LED driver.

and raises the standby power. On the other hand, due to the intrinsic propagation delay of control signals, the primary-side controlled flyback converter experiences a worse output current accuracy [31]. A PSR scheme is proposed to improve the precision of output current at the cost of increasing the start-up time and the complexity of the controller [32]. In addition, the existence of extra auxiliary winding and feedback resistor network in the conventional PSR scheme with gate driving increases the volume and the cost of the low power LED driver.

Considering the aforementioned issues, this paper proposes a novel primary-side controlled universal-input ac–dc LED driver based on the source-driving control scheme. Compared to the conventional primary-side controlled scheme, the proposed controller employs low-voltage control MOSFET M_2 to drive high-voltage power MOSFET M_1 without adding auxiliary winding and feedback network in the conventional primary-side controlled scheme, which greatly reduces the peripheral devices, the volume and the cost of low power LED driver. Accordingly, the proposed control scheme improves the accuracy of output current and reduces the start-up time. Detailed operation principle will be illustrated in Section II. Then, design considerations of key circuits will be presented in Section III. Section IV will show the experimental results.

II. Operation Principle

A. System Overview

Fig. 2 shows system diagram of the proposed primary-side controlled universal-input ac–dc LED driver based on the source-driving control scheme, which consists of bridge rectifier BD, bulk capacitor C_1, the startup resistor R_1, by-pass capacitor C_2, primary-side current sense resistor RCS, RCD snubber circuit, freewheel diode D_o, output capacitor C_o and the control IC. The proposed control IC is mainly composed of clamp circuit, first voltage sampling network (FVSN), second voltage sampling network (SVSN), minimum voltage detection circuit (MVDC), demagnetization time detection circuit (DTDC), intelligent charging and discharging circuit (ICDC), switching control signal generator (SCSG), logic controller and peak current controller (PCC).

In the control IC, as is shown in Fig. 2, clamp circuit sets the source voltage $V_{\rm source1}$ of power MOSFET M_1 to service voltage $V_{\rm DD}$ when low-voltage control MOSFET M_2 turns off, so that M_1 is turned off at the same time. SCSG provides four signals to drive MVDC. FVSN divides $V_{\rm source1}$ into V_1. Meanwhile, SVSN senses $V_{\rm source1}$ and outputs V_2. The minimum voltage $V_{\rm MIN}$ is achieved by MVDC. DTDC generates demagnetization time signal $V_{\rm Demag}$ by a comparison of $V_{\rm MIN}$ and V_2. The ratio

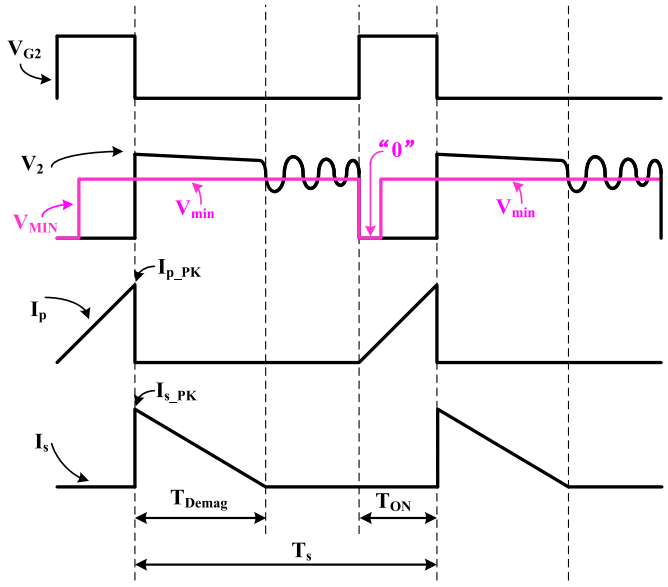

Fig. 3. Key operation principle waveforms of the proposed system.

between the secondary winding demagnetization time T_{Demag} and switching period T_S is maintained constant by adopting ICDC. In addition, the primary peak current is also remained constant by means of PCC. In order to achieve high-precision constant output current, more attention is paid to the design of key circuits (MVDC, DTDC, and ICDC) in the proposed control IC.

B. Principle of CC

The proposed controller operates in discontinuous conduction mode (DCM) and its key operation principle waveforms are depicted in Fig. 3. According to Fig. 2, $V_{\mathrm{G}2}$ is the driving voltage of low-voltage control MOSFET M_2 and V_1 is the output voltage of FVSN. V_{MIN} is the detected minimum voltage signal of V_1, which is generated by FVSN. V_{min} is the sensed minimum voltage value, namely the first resonance voltage valley value of V_1. V_2 is the output voltage of SVSN. Moreover, I_p is primary-side instantaneous current and I_s, secondary-side instantaneous current.

When the system is powered on, the rectified line voltage begins to charge the by-pass capacitor C_2 through the startup resistor R_1. Once the voltage across C_2 reaches service voltage V_{DD} of the control IC, logic controller outputs high level to turn on the low-voltage control MOSFET M_2. Meanwhile, the primary magnetizing inductor current I_p rises linearly from zero with a slope to the peak value I_p_PK, which is proportional to the instantaneous ac line voltage V_{in} and inversely proportional to the primary magnetizing inductor L_p. Thus, the turn-on time T_{ON} satisfies

$$T_{\mathrm{ON}} = L_p \cdot \frac{I_{p\_\mathrm{PK}}}{V_{\mathrm{in}}}. \tag{1}$$

As soon as I_p_PK reaches the internal setting threshold, logic controller outputs low level to turn off the M_2. Then, I_p linearly

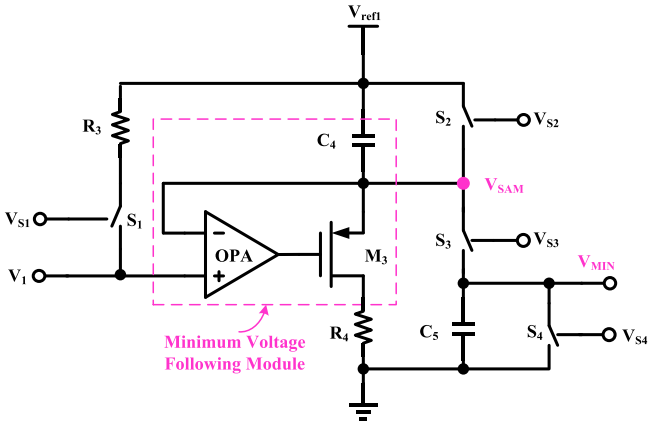

Fig. 4. Design implementation of MVDC.

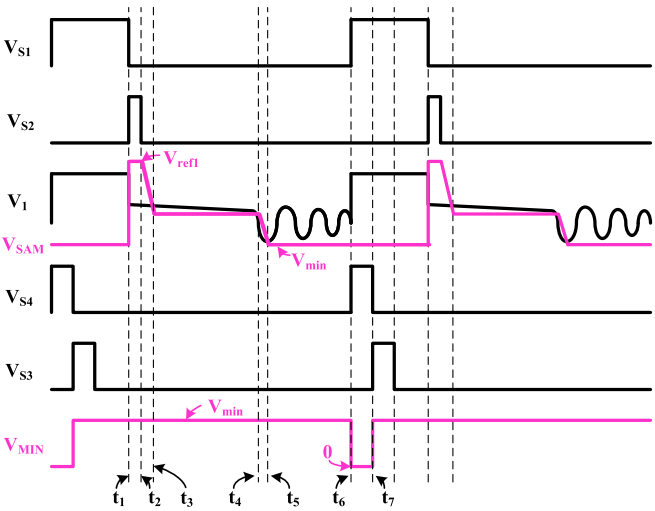

Fig. 5. Key operation waveforms of MVDC.

decreases from I_p_PK to 0. So, I_p_PK is fixed at

$$I_{p\_\mathrm{PK}} = \frac{V_{\mathrm{ref}}}{R_{\mathrm{cs}}}. \tag{2}$$

In (2), V_{ref} is the internal bandgap voltage reference and R_{CS} is the primary-side sense resistor.

When M_2 is turned off, the secondary-side freewheel diode D_{o} conducts and the energy stored in L_p is transferred to the secondary side, which is stored on output capacitor C_{o} partly and consumed by LED loads at the same time. The secondary magnetizing inductor current I_s decreases linearly, which is proportional to the output voltage V_{out} and inversely proportional to the secondary magnetizing inductor L_s. Consequently, the demagnetization time T_{Demag} can be expressed as

$$T_{\mathrm{Demag}} = L_s \cdot \frac{I_{s\_\mathrm{PK}}}{V_{\mathrm{out}}} = L_p \cdot \left(\frac{N_s}{N_p}\right)^2 \frac{I_{s\_\mathrm{PK}}}{V_{\mathrm{out}}}. \tag{3}$$

According to the continuous relationship of transformer ampere-turns, there is

$$I_{p\_\mathrm{PK}} \cdot N_P = I_{S\_\mathrm{PK}} \cdot N_S \tag{4}$$

where N_p and N_s are the turns of primary-side winding and secondary-side winding, respectively, and I_{s_PK} denotes the peak value of I_s. The average output current $I_{\rm LED}$ can be given as

$$I_{\rm LED} = I_{s\_avg} \cdot \frac{T_{\rm Demag}}{T_S} = \frac{I_{s\_PK} \cdot T_{\rm Demag}}{2T_S}. \quad (5)$$

In (5), T_S is the switching cycle of low-voltage control MOSFET M_2, and I_{s_avg} is the average value of the secondary winding current during demagnetization time.

Once I_s reaches 0, the drain and source voltages of power MOSFET M_1 begin to resonate due to the existence of primary magnetizing inductor L_p and parasitic capacitor C_p of M_1. MVDC detects the resonance voltage valley of V_1 output by FVSN to get the zero crossing information of I_s. Then, demagnetization time signal $V_{\rm Demag}$ is generated by DTDC. Finally, the ratio between the secondary winding demagnetization time $T_{\rm Demag}$ and switching period T_S is controlled constant by ICDC.

From (2), (4), and (5), the output current $I_{\rm LED}$ can be rewritten as

$$I_{\rm LED} = \frac{1}{2} \cdot \frac{T_{\rm Demag}}{T_s} \cdot \frac{N_p}{N_s} \cdot \frac{V_{\rm ref}}{R_{\rm CS}}. \quad (6)$$

Equation (6) illustrates that the average output current $I_{\rm LED}$ has nothing to do with input line voltage, magnetizing inductor, loads and so on. More consideration should be taken into how to detect the zero crossing moment of secondary winding current I_s and keep the ratio between the secondary winding demagnetization time $T_{\rm Demag}$ and switching period T_S constant. Key circuits are designed to solve this problem.

III. Design Considerations of Key Circuits

A. MVDC

From Fig. 3, at the zero crossing moment of secondary winding current I_s, both the drain and source voltages of the power MOSFET M_1 begin to oscillate owing to the resonant circuit composed of primary magnetizing inductor L_p and its equivalent resistor R_p, parasitic capacitor C_p of M_1. The drain voltage of M_1 $V_{\rm Drain1}$ can be given as

$$V_{\rm Drain} = V_{\rm in1} + \frac{N_p}{N_s} \cdot V_{\rm out} \cdot e^{-\alpha t} \cdot \cos\left(2\pi \cdot f_r \cdot t\right) \quad (7)$$

where $V_{\rm in1}$ is the rectified voltage, α is the oscillation attenuation coefficient, and f_r is defined as resonance frequency, namely

$$\begin{cases} \alpha = \frac{R_p}{2L_p} \\ f_r = \frac{1}{2\pi\sqrt{L_p \cdot C_p}}. \end{cases} \quad (8)$$

Equation (7) shows that both the drain and source voltages of power MOSFET reach absolute minimum values when $\cos(2\pi f_r t) = -1$.

In order to detect the demagnetization end moment more precisely, a MVDC based on the source-driving control scheme is designed in Fig. 4, which contains minimum voltage following module, bandgap voltage reference $V_{\rm ref1}$, R_3, R_4, C_5, and four control switches. Fig. 5 shows the key operation waveforms of MVDC. In Fig. 4, V_1 is the output voltage of FVSN; $V_{\rm SAM}$ is the minimum voltage sampling signal; output signal $V_{\rm MIN}$ is the detected minimum voltage. SCSG offers four control signals to drive MVDC, which are, respectively, the driving signal V_{S1} of step-up switch S_1, the driving signal V_{S2} of set switch S_2, the driving signal V_{S3} of sampling switch S_3, and the driving signal V_{S4} of reset switch S_4. V_{S1} controls the conduction of S_1 to raise V_1 greater than the minimum voltage during the resonance, avoiding influencing the detection of minimum voltage. $V_{\rm SAM}$ should be set to the bandgap voltage reference $V_{\rm ref1}$ driven by V_{S2} before a new sampling and $V_{\rm MIN}$ should be reset to 0 controlled by V_{S4} before sampling $V_{\rm SAM}$ again at next period. When S_3 is turned on, $V_{\rm SAM}$ is held on C_5 generating minimum voltage signal $V_{\rm MIN}$.

From Fig. 5, at $t = t_1$, S_2 is turned on and $V_{\rm SAM}$ is set to be $V_{\rm ref1}$. At $t = t_2$, S_2 is turned off and $V_{\rm SAM}$ begins to follow the change of V_1 and decrease with a slope determined by C_4. At $t = t_3$, $V_{\rm SAM}$ is lower than V_1 and $V_{\rm SAM}$ keeps unchanged in the interval from t_3 to t_4. At $t = t_4$, $V_{\rm SAM}$ starts to follow the change of V_1 again and decrease with a same slope. At $t = t_5$, $V_{\rm SAM}$ samples the minimum voltage of V_1 and holds unchanged until the moment S_2 is turned on. At $t = t_6$, $V_{\rm MIN}$ is reset to be 0, which helps to sample new $V_{\rm SAM}$.

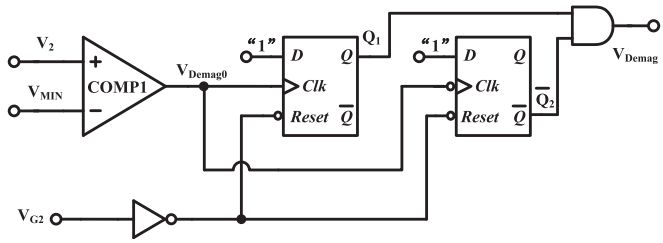

Fig. 6. Design implementation of DTDC.

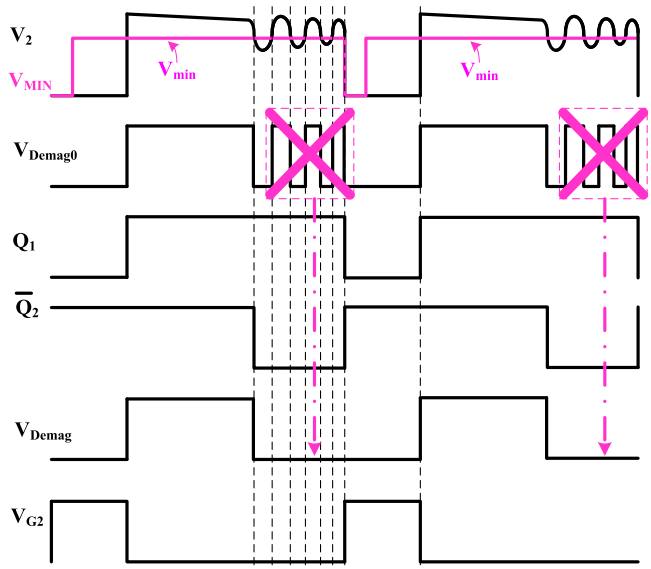

Fig. 7. Key operation waveforms of DTDC.

B. DTDC

DTDC is proposed to bring forth an ideal demagnetization time according to the output voltage V_2 of SVSN and the output signal $V_{\rm MIN}$ of MVDC, shown in Fig. 6, and Fig. 7 reveals

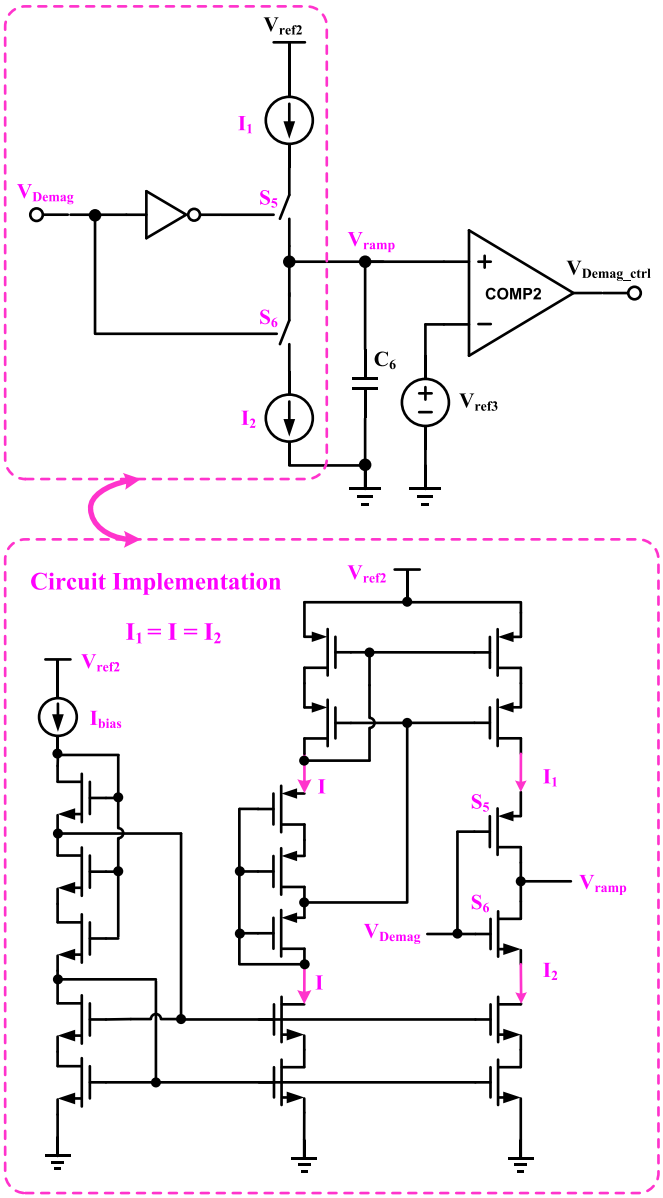

Fig. 8. Design implementation of ICDC.

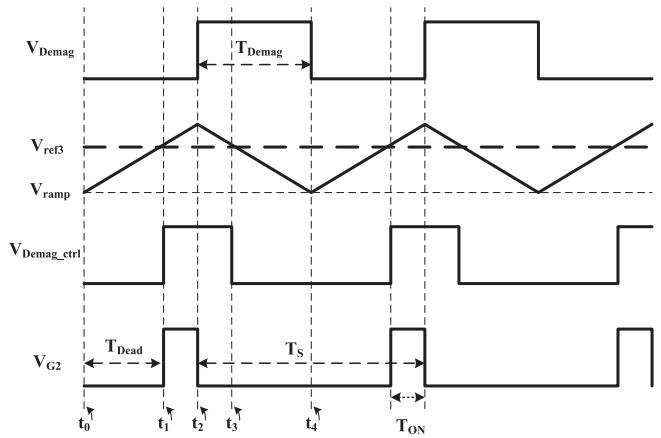

Fig. 9. Key operation waveforms of ICDC.

its key operation waveforms. According to Fig. 6, the structure of the proposed DTDC is simple, only including a comparator COMP1, a NAND date, an AND gate, a rising edge-triggered D flip-flop and a falling edge-triggered D flip-flop. V_{G2} is the gate driving signal of low-voltage control MOSFET M_2 and V_{Demag} is the ideal demagnetization time signal.

As is shown in Fig. 7, due to inherent difference between FVSN and SVSN, $V_{\min}$ is not corresponding exactly to the first resonance voltage valley value of V_2. The nonideal demagnetization time signal V_{Demag0} is engendered by comparison of input signal V_2 and V_{MIN}. In order to remove the harmful part of V_{Demag0}, D inputs of both D flip-flops are set to be high level. The Reset inputs of D flip-flips are asynchronous inputs, which are active low. Therefore, reset signals on Q_1 and Q_2 are generated when V_{G2} changes to high level from low level. Both inputs of AND gate are high level only during the real demagnetization time controlled by V_{G2}, finally obtaining the ideal demagnetization time signal V_{Demag}.

C. ICDC

ICDC is designed to generate a constant ratio between the secondary winding demagnetization time T_{Demag} and switching period T_S to obtain the high-precision CC output. Fig. 8 shows the proposed ICDC and Fig. 9 displays its key operation waveforms. The designed ICDC is composed of two identical current sources, I_1 and I_2, a charging and discharging capacitor C_6, two bandgap voltage reference V_{ref2}, V_{ref3}, a comparator COMP2 and two control switches, S_5 and S_6. V_{ramp} is the sawtooth wave generated by charging and discharging the capacitor C_6. Output signal $V_{\mathrm{Demag\_ctrl}}$ drives the logic controller in control IC.

To avoid the negative effect on current mirror accuracy owing to the variation of V_{ramp}, a cascode current mirror with wide swing is proposed, as shown in Fig. 8. The proposed current mirror can achieve a high output resistance and an optimum compliance voltage regardless of input current level, temperature, power supply voltage and semiconductor process parameters; thus, the impact of V_{ramp} variation is negligible. Both I_1 and I_2 mirror the main branch current I as precisely as possible. Therefore, two identical current, I_1 and I_2, can be obtained by setting the circuit parameters appropriately [33]–[36].

According to Fig. 9, at $t = t_0$, S_5 is turned on and S_6 is turned off. Accordingly, I_1 begins to charge C_6 and V_{ramp} increases linearly with a slope determined by I_1. At $t = t_1$, V_{ramp} rises to V_{ref3} and $V_{\mathrm{Demag\_ctrl}}$ becomes high level to drive the logic controller, making M_2 turn on. At the moment, primary magnetizing inductor starts to store the energy. At $t = t_2$, S_5 is turned off, S_6 is turned on, and C_6 begins to discharge. V_{ramp} decreases with an equivalent slope because of two identical current sources. At $t = t_3$, V_{ramp} comes to V_{ref3} and $V_{\mathrm{Demag\_ctrl}}$ becomes low level, and C_6 continues to discharge. At $t = t_4$, demagnetization time ends and C_6 is charged in the next period.

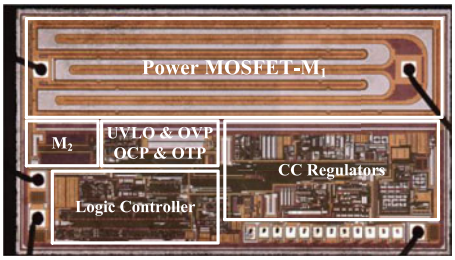

Fig. 10. Micrograph of the fabricated chip.

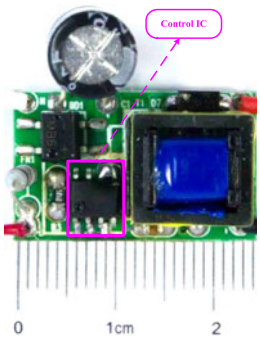

Fig. 11. Photograph of the implemented circuit prototype.

TABLE I
KEY COMPONENTS AND PARAMETERS

Parameters	Symbol	Value
AC input voltage	$V_{\rm in}$	85–264 Vac (RMS)
Output	$V_{\rm out}/I_{\rm LED}$	3.2–10 V/250 mA
Bridge rectifier	BD	1 A/600 V
Primary-side inductance	L_p	2.45 mH
Transformer core	T	EE10
Transformer turns-ratio	N_p/N_s	6.68
Bulk capacitor	C_1	4.7 μF/400 V
Start-up resistor	R_1	940 kΩ
By-pass capacitor	C_2	1 μF/25 V
Primary-side current sense resistor	$R_{\rm CS}$	3 Ω
Output capacitor	$C_{\rm o}$	2.2 μF/25 V
Freewheel diode	$D_{\rm o}$	1 A/100 V

Based on the previous analysis, there are

$$T_S = T_{\rm ON} + T_{\rm Demag} + T_{\rm Dead} \tag{9}$$

$$T_{\rm ON} + T_{\rm Dead} = T_{\rm Demag}. \tag{10}$$

$T_{\rm Dead}$ is dead time of low-voltage control MOSFET M_2.

From (9) and (10), the ratio between the secondary winding demagnetization time $T_{\rm Demag}$ and switching period T_S is obtained as

$$\frac{T_{\rm Demag}}{T_S} = \frac{1}{2}. \tag{11}$$

Associating (6) with (11), the output current $I_{\rm LED}$ can be rewritten as

$$I_{\rm LED} = \frac{1}{4} \cdot \frac{N_p}{N_s} \cdot \frac{V_{\rm ref}}{R_{\rm CS}}. \tag{12}$$

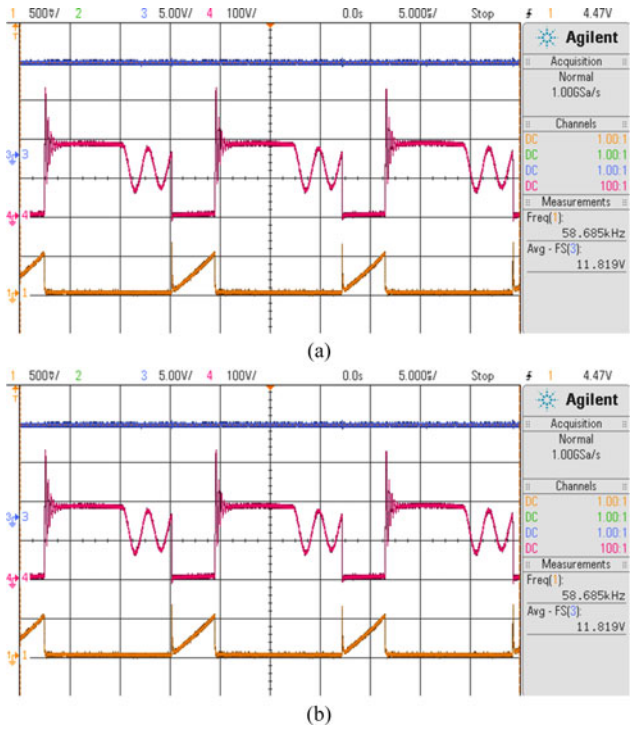

Fig. 12. (a) Measured steady-state waveforms under 90 Vac and 60 Hz-input. Top trace: $V_{\rm DD}$; second trace: $V_{\rm Drain1}$; third trace: $V_{\rm CS}$. (b) Measured steady-state waveforms under 220 Vac and 50 Hz-input. Top trace: $V_{\rm DD}$; second trace: $V_{\rm Drain1}$; third trace: $V_{\rm CS}$.

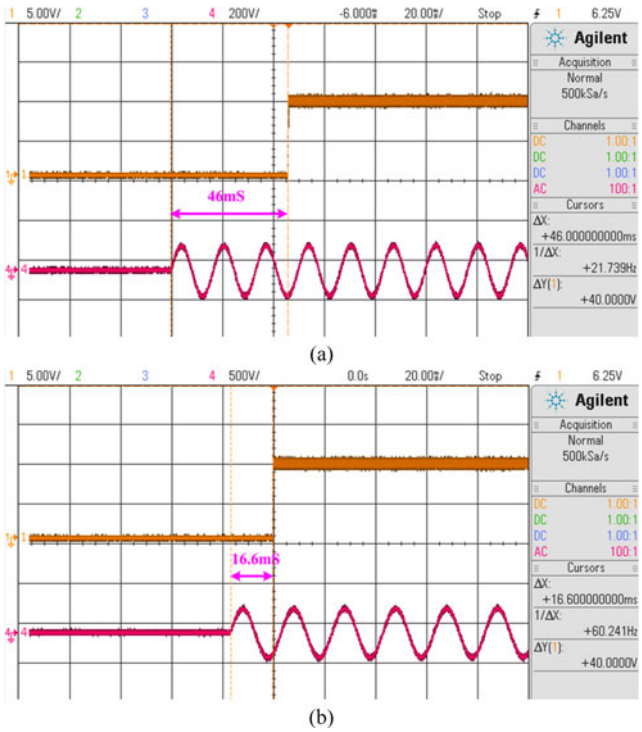

Fig. 13. (a) Measured start-up waveforms under 90 Vac and 60 Hz-input. Top trace: $V_{\rm out}$; second trace: $V_{\rm in}$. (b) Measured start-up waveforms under 220 Vac and 50 Hz-input. Top trace: $V_{\rm out}$; second trace: $V_{\rm in}$.

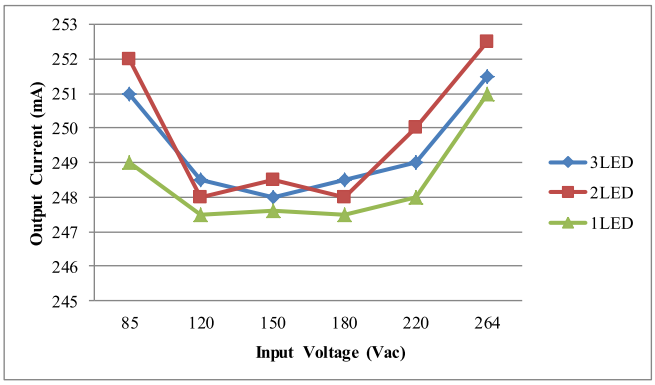

Fig. 14. Measured output current $I_{\rm LED}$ versus ac input voltage $V_{\rm in}$.

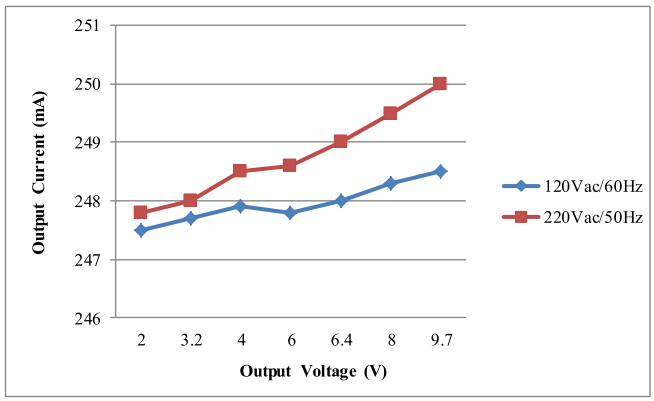

Fig. 15. Measured efficiency versus ac input voltage $V_{\rm in}$.

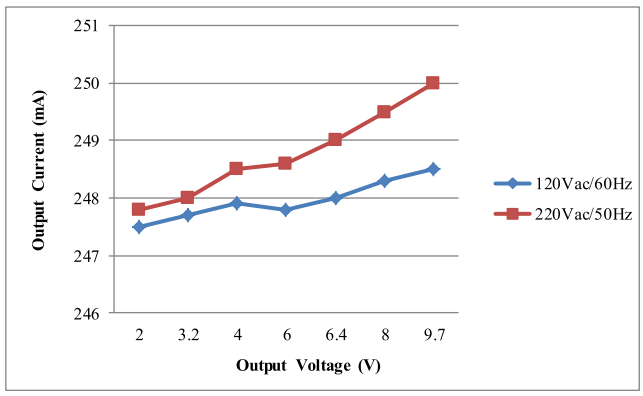

Fig. 16. Measured output current $I_{\rm LED}$ versus ac output voltage $V_{\rm out}$.

In accordance with (3), (5), and (11), the switching frequency f_s can be derived as

$$f_s = \frac{1}{T_S} = \frac{1}{2T_{\rm Demag}} = \frac{1}{8} \cdot \left(\frac{N_p}{N_s}\right)^2 \cdot \frac{V_{\rm out}}{L_p \cdot I_{\rm LED}}. \quad (13)$$

Equation (13) shows that the switching frequency f_s is proportional to output voltage. The heavier the load voltage, the higher the f_s. It is also proved that f_s will remain unchanged when the input line voltage decreases. This is because $T_{\rm Demag}$ will be kept constant from (3). However, accordingly, $T_{\rm ON}$ will increase from (1). Thus, $T_{\rm Dead}$ will decrease according to (10).

IV. Experimental Results

In order to verify the performance of the proposed scheme, a control IC for primary-side controlled universal-input ac–dc LED driver based on the source driver control scheme has been implemented in TSMC 0.35 μm 5 V/600 V CMOS/LDMOS process. A micrograph of the fabricated chip is shown in Fig. 10 and the die size with PADs is 1.2 mm $\times$1.5 mm. The chip, internally integrated a 650 V power VDMOS, includes soft-start, bias, under-voltage-lock-out, over-voltage protection, over-current protection, over-temperature protection, CC regulators, and logic controller.

A 3 W circuit prototype with universal ac input (85–264 Vac) and 9.7 V/250 mA dc output is built to drive three LEDs (1 W: 3.3 V/350 mA), as is shown in Fig. 11, and the designed printed circuit board is only 2.4 cm$\times$1.5 cm. Key components and parameters of the proposed driver are listed in Table I. Compared with other circuit prototypes [25], [37], the proposed circuit has less peripheral components with omitting the auxiliary winding, a freewheel diode, and feedback network. Therefore, the complexity, volume, and cost of the proposed LED driver are obviously reduced.

Additionally, it can be found that only a 2.2-μF output filter ceramic capacitor is employed instead of a conventional bulk electrolytic capacitor [25], [37], [38], which can extend the life span of low power LED driver. The internal bandgap voltage reference $V_{\rm ref}$ of the primary-side peak current control circuit is designed to be 450 mV, and the external current sense resistor $R_{\rm CS}$ is set to be 3 Ω. From (2), the primary-side peak current $I_{\rm p\_PK}$ is calculated to be 150 mA. Considering that the turns-ratio N_p/N_s of the designed transformer is 6.68, the output current $I_{\rm LED}$ is counted to be about 250 mA based on (12). In addition, output current $I_{\rm LED}$ can be regulated by changing the value of external current sense resistor $R_{\rm CS}$ in practical applications.

Fig. 12 shows the steady-state waveforms of the proposed circuit prototype respectively under 90 Vac and 60 Hz-input and 220 Vac and 50 Hz input, driving maximum LED load (three 1-W LEDs in series). In Fig. 12, the top trace is the service voltage $V_{\rm DD}$ of the proposed control IC; the second trace is the drain voltage $V_{\rm Drain1}$ of the high-voltage power MOSFET; the third trace is the sense voltage $V_{\rm CS}$ of the primary-side sense resistor $R_{\rm CS}$. According to Fig. 12, the proposed LED driver operates in DCM and the switching frequency f_s of the steady state is around 60 kHz without the variation of loads, testifying the theoretical analysis of (13).

Start-up time is the interval between the beginning of ac input start-up and the beginning of a steady output. The start-up waveforms of the proposed circuit prototype driving maximum LED load (three 1-W LEDs in series) are shown in Fig. 13. In Fig. 13, the top trace is output voltage $V_{\rm out}$ and the second trace is ac input voltage $V_{\rm in}$. From the experimental results, the start-up time is only 46 ms under 90 Vac and 60 Hz-input, and the start-up time is less than 17 ms under 220 Vac and 50 Hz-input.

TABLE II
COMPARISONS BETWEEN THE PROPOSED METHOD AND THE PRIOR ARTS

Parameter	This work	[25]	[20]	[38]	[37]
Technology	TSMC 0.35 μm 5 V/600 V CMOS/LDMOS	0.18 μm BCD process	0.35 μm BCD process	0.35 μm BCD process	N/A
Chip size (with PADs)	$1.2 \times 1.5\mathrm{mm}^2$	iW3620	N/A	0.76 mm^2	N/A
Topology	Flyback	Flyback	Flyback	Flyback	Flyback
Primary-side inductance	2.45 mH	N/A	3 mH	1.8 mH	1 mH
Output capacitor	2.2 μF	330 μF	N/A	330 μF	660 μF
Output current ripple (220 Vac)	280 mA	N/A	250 mA	300 mA	60 mA
AC input voltage	85–264 Vac	60–260 Vac	85–265 Vac	180–260 Vac	85–265 Vac
Output power	3 W	3 W	5 W	6 W	7 W
Maximum switching frequency	60 kHz	130 kHz	50 kHz	N/A	90 kHz
Maximum efficiency	84%	73.1%	85%	85%	83%
CC accuracy	$\pm$1%	$\pm$6.4%	N/A	$\pm$2%	$\pm$3%
Start-up time(90 Vac)	46 ms	500 ms	600 ms	800 ms	N/A

It is the evident that the start-up of the proposed LED driver is much faster than conventional ones [31], [38].

Fig. 14 depicts the output current I_{LED} versus ac input voltage V_{in} for different LED loads. According to Fig. 14, the average current of output current is around 250 mA when ac input voltage V_{in} changes from 85 to 264 V and LED loads changes from one 1-W LED to three 1-W LEDs in series. The output current line regulation is calculated to be within $\pm 1\%$, which has a much better current precision than those in [25] and [37].

With the same test conditions, Fig. 15 illustrates measured efficiency versus ac input voltage V_{in} for different LED loads. From Fig. 15, the efficiency of the proposed circuit prototype driving three 1-W LEDs is well above 80%, maximum value to 84%. When LED loads are reduced to one 1-W LED, the efficiency decreases to about 60%. It is proved that the heavier the load, the higher the system efficiency, and vice versa.

Fig. 16 shows measured output current I_{LED} versus ac output voltage V_{out}, and load regulation can be counted to be within $\pm 1\%$. It is indicated that the proposed circuit has a good characteristic curve of CC output versus output voltage.

In addition, the standby power of the proposed system is tested only to be 142 mW under 220 Vac and 50 Hz-input, and the output current ripple is close to 280 mA. Finally, Table II shows the performance comparison with the prior arts. From Table II, it is shown that the proposed low power LED driver has a better current precision, a less start-up time and a lower standby power, compared with other works. Simultaneously, low cost is achieved due to the simple control IC and a few peripheral components.

V. CONCLUSION

This paper proposes a novel primary-side controlled universal-input ac–dc LED driver based on the source-driving control scheme. Compared to the conventional primary-side controlled scheme, the proposed source driving structure does not need an auxiliary winding and feedback network, which greatly reduces the peripheral devices, the volume, and the cost of low power LED driver. The theoretical analysis and key circuits are illustrated in this paper. The proposed control IC has been fabricated in TSMC 0.35 μm 5 V/600 V CMOS/LDMOS process. Test results of a 3-W circuit prototype show that the CC precision is within $\pm 1\%$ in a wide range of universal-input ac voltage from 85 to 264 V, and that above 80% efficiency is obtained when driving three 1-W LEDs. In addition, the proposed LED driver has a much shorter start-up time and lower standby power. Thus, the proposed scheme has a promising application in low power LED driver.

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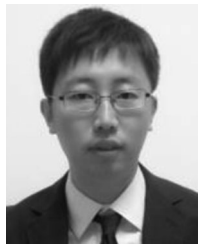

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