Steady-State Analysis and Design of Class-DE Inverter at Any Duty Ratio

Hiroo Sekiya, *Senior Member, IEEE*, Xiuqin Wei, *Member, IEEE*, Tomoharu Nagashima, *Student Member, IEEE*, and Marian K. Kazimierczuk, *Fellow, IEEE*

***Abstract*—This paper presents a steady-state analysis and design equations for the class-DE inverters at any duty ratio and high loaded quality factor, taking into account nonlinear MOSFET drain–source and gate–drain parasitic capacitances with any grading coefficients of the diode junctions. Additionally, maximum operating frequency, power output capability, and power-conversion efficiency of the class-DE inverter are also obtained. It is shown that the maximum operating frequency is the highest when the switch-on duty ratio is 0.25. From the obtained results, it can be stated that the switch-on duty ratio of the class-DE inverter should be specified in the range of $0.25 \leq D < 0.5$.**

***Index Terms*—Class-DE inverter, class-E zero-voltage switching(ZVS)/zero-derivative switching (ZDS) condition, high efficiency, junction grading coefficient, maximum operating frequency, MOSFET nonlinear parasitic capacitance, switch-on duty ratio.**

I. Introduction

THE class-DE inverter [1]–[20] is one of the optimized class-D inverters, which satisfy both zero-voltage switching (ZVS) and zero-derivative switching (ZDS) conditions. Because of ZVS and ZDS operation, the class-DE inverter can operate with high power-conversion efficiency at high operating frequencies. Therefore, the class-DE inverter is applicable to many applications such as RF power supplies [6], induction heating, [7], on-chip converters [8], [9], wireless power transfer systems [10], [11], and so on.

The switch-on duty ratio is one of the most important parameters for achieving the class-E ZVS/ZDS conditions in the class-DE inverter. The steady-state analysis of the class-DE inverter at any duty ratio with linear shunt capacitances was carried out in [12]. There are, however, no design equations from the steady-state analysis of the class-DE inverter at any duty ratio in the papers published until now [12]–[20]. The class-DE inverter at any duty ratio can be designed from the transient analysis [13], [14], or numerical calculations [21], [22]. These design procedures provide accurate design values. However, the design procedure is not simple and it is difficult for designers to obtain an instinctive understanding among design values and circuit characteristics. It is important to obtain design equations of the class-DE inverter at any duty ratio from the steady-state analysis.

The operating frequency is also an important parameter to design the class-DE inverter. It is useful for designers to know the maximum operating frequency in advance. It is known that the shunt capacitances decrease as the operating frequency increases. The shunt capacitances have the minimum values when they consist of only the MOSFET parasitic capacitances. Therefore, the "maximum operating frequency" in this paper is defined as *the operating frequency obtained when the shunt capacitances consist of only the nonlinear MOSFET parasitic capacitances for a specified duty ratio.* Because the MOSFET drain–source and gate–drain parasitic capacitances have a nonlinear characteristic against the voltage across the capacitances [13]–[27], the nonlinearity of the parasitic capacitances should be considered for obtaining the maximum operating frequency. Similar problems were discussed for the class-E inverter in [24]–[27]. In this case, transient analysis like [14] cannot be adopted because analytical solutions of the differential equations cannot be obtained because of the nonlinearity. This increases the importance of the steady-state analysis.

The purpose of this paper is to present a steady-state analysis and design equations of the class-DE inverters at any duty ratio and high loaded quality factor, taking into account the nonlinear MOSFET drain–source and gate–drain parasitic capacitances with any grading coefficient of the diode junction. Additionally, maximum operating frequency, power output capability, and power-conversion efficiency of the class-DE inverter are also derived. From the obtained results, it can be stated that the switch-on duty ratio of the class-DE inverter should be specified in the range of $0.25 \leq D < 0.5$ regardless of the MOFSET parasitic capacitance nonlinearities. A design example along with PSpice-simulation and experimental results indicate the validity of our analysis.

II. Class-DE Inverter

Fig. 1(a) shows a circuit topology of the class-DE inverter [1]–[20]. This inverter consists of input voltage $V_{\rm DD}$, two switching devices S_1 and S_2, (e.g., MOSFETs), shunt capacitances C_{S1} and C_{S2} connected in parallel with the switches, and L_0–C_0–R resonant bandpass filter. Fig. 2 shows example waveforms of the class-DE inverter with the nominal operation for $D = 0.25$.

Manuscript received March 24, 2014; revised June 10, 2014; accepted July 7, 2014. Date of publication July 15, 2014; date of current version February 13, 2015. This work was supported in part by the Scholarship Foundation and Grant-in-Aid for Scientific Research (20334203) of JSPS. Recommended for publication by Associate Editor C. Fernandez.

H. Sekiya and T. Nagashima are with the Graduate School of Advanced Integration Science, Chiba University, Chiba 263-8522, Japan (e-mail: sekiya@faculty.chiba-u.jp; nagashima@chiba-u.jp).

X. Wei is with the Department of Electronics Engineering and Computer Science, Fukuoka University, Fukuoka 814-0180, Japan (e-mail: xiuqinwei@fukuoka-u.ac.jp).

M. K. Kazimierczuk is with the Department of Electrical Engineering, Wright State University, Dayton, OH 45435-0001 USA (e-mail: marian.kazimierczuk@wright.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2339355

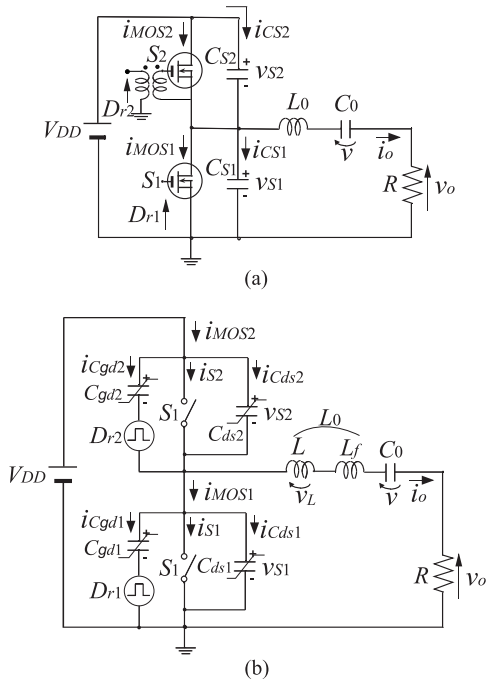


Fig. 1. Class-DE inverter. (a) Circuit topology. (b) Equivalent circuit.

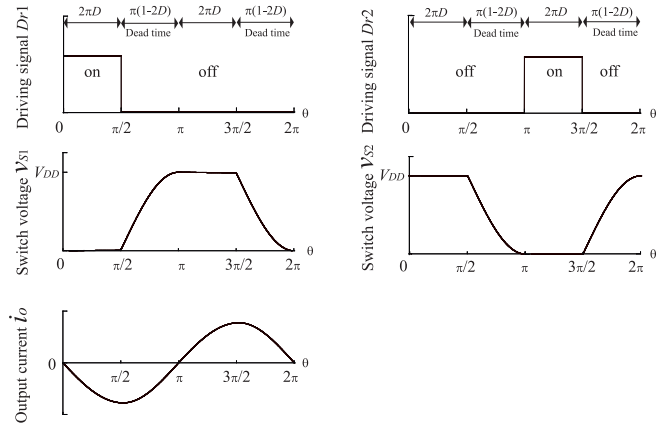


Fig. 2. Nominal waveforms of class-DE inverter for $D = 0.25$.

Both the switches turn ON and OFF alternately. In the cycle of the operating frequency of the class-DE inverter, there are two dead-time intervals when both switches are OFF. During the dead-time intervals, the voltage across one of the switches decreases and reaches zero when the switch turns ON. Additionally, the slope of the voltage is also zero at turn-on instant, that is

$$v_{S1}(2\pi) = 0, \qquad \left.\frac{dv_{S1}(\theta)}{d\theta}\right|_{\theta=2\pi} = 0 \tag{1}$$

$$v_{S2}(\pi) = 0, \qquad \left.\frac{dv_{S2}(\theta)}{d\theta}\right|_{\theta=\pi} = 0. \tag{2}$$

These conditions are called the class-E zero-voltage switching (ZVS) and zero-derivative switching (ZDS) conditions. The dead-time intervals are required to discharge the electric charge stored in the shunt capacitances. Because of the dead-time and the class-E ZVS/ZDS conditions, the switching power losses in the class-DE inverter become zero. Therefore, high power-conversion efficiency can be achieved at high operating frequencies.

III. Nonlinearity of Shunt Capacitances

The shunt capacitances are important components to determine the charge/discharge time of the dead-time intervals, which affect the operating frequency and the duty ratio. From the discussions in the previous papers [3], [15]–[19], it is well known that the smaller shunt capacitances are, the higher the operating frequency becomes. The class-E inverter exhibits the similar characteristic [24]–[27]. Usually, the shunt capacitances are realized by the sum of the external linear capacitances and the MOSFET drain–source nonlinear parasitic capacitances. The drain–source parasitic capacitances of the discrete MOSFETs are determined, which depends on the MOSFET type, though the external linear capacitances can be changed arbitrary as design parameters. When the external shunt capacitances are zero, the shunt capacitance cannot be decreased any more. Namely, the maximum operating frequency obtained when the shunt capacitances are composed of only the MOSFET drain–source capacitance.

The MOSFET drain–source parasitic capacitances, however, are nonlinear and are expressed as

$$C_{\rm ds} = \frac{C_{j01}}{\left(1 + \dfrac{v_S}{V_{\rm bi1}}\right)^{m_1}} \tag{3}$$

where v_S is the drain-to-source voltage, $V_{\rm bi1}$ is the built-in potential between drain and source, C_{j01} is the capacitance at $v_S = 0$, and m_1 is the grading coefficient of the drain–source body diode junction [15]–[27] whose values are in the range of $0.3 \le m < 1$. Additionally, it is necessary and important to consider the effects of MOSFET gate–drain capacitance to the class-E ZVS/ZDS conditions at high frequencies [18], [26]. The MOSFET gate–drain capacitance is often modeled as linear capacitance [26] or the sum of linear and nonlinear capacitances [18]. In this paper, the MOSFET gate–drain capacitance is expressed by a general expression as

$$\begin{aligned} C_{\rm gd} &= C_{\rm gdl} + C_{\rm gdn} \\ &= C_{j02} + \frac{C_{j03}}{\left(1 + \dfrac{v_{\rm gd}}{V_{\rm bi3}}\right)^{m_3}} \\ &= \sum_{k=2}^{3} \frac{C_{j0k}}{\left(1 + \dfrac{v_{\rm gd}}{V_{\rm bik}}\right)^{m_k}} \end{aligned} \tag{4}$$

where $v_{\rm gd}$ is a voltage across the gate-drain capacitance and $C_{\rm gdl}$ and $C_{\rm gdn}$ are linear and nonlinear components of the gate–drain capacitance, respectively, namely $C_{j02} = C_{\rm gdl}$ and $m_2 = 0$. In addition, $V_{\rm bi3}$, C_{j03}, and m_3 are parameters for $C_{\rm gdn}$. Therefore, we should consider the nonlinearities of the MOSFET parasitic capacitances to obtain the maximum operating frequency of the class-DE inverter.

TABLE I
SWITCHING PATTERN

Intervals	S_1	S_2
$0 \le \theta < 2\pi D$	ON	OFF
$2\pi D \le \theta < \pi$	OFF	OFF
$\pi \le \theta < \pi + 2\pi D$	OFF	ON
$\pi + 2\pi D \le \theta < 2\pi$	OFF	OFF

IV. WAVEFORM AND DESIGN EQUATIONS

A. Assumptions

The analysis in this paper is based on the following assumptions:

1) The shunt capacitances consist of only drain–source parasitic capacitances of the MOSFETs.
2) Both the MOSFETs are identical and are modeled as ideal switches and drain–source and gate–drain parasitic capacitances, which are expressed in (3) and (4).
3) All passive elements except the MOSFET parasitic capacitances are linear elements and do not have parasitic resistances.
4) The loaded quality factor of the resonant filter $Q = \omega L_0/R$ is high enough to generate nearly pure sinusoidal output current. The current through the $L_f - C_0$ circuit and the load resistance is sinusoidal at the operating frequency f

$$i_o = I_m \sin(\theta + \varphi) \tag{5}$$

where $\theta = \omega t = 2\pi f t$ represents the angular time. Therefore, only the operating-frequency component is considered for the output-network analysis.
5) From the assumption 4, the output resonant filter whose resonant frequency is $f_r = 1/(2\pi\sqrt{L_0 C_0})$ generates a pure sinusoidal output current with the operating frequency and a proper phase shift of the output current as given in (5). For the theoretical analysis, the inductance L_0, which is physically one component in real circuits, is theoretically divided into L and L_f. The elements L_f and C_0 realize an ideal series-resonant filter whose resonant frequency is equal to the operating frequency f, namely $f = 1/(2\pi\sqrt{L_f C_0})$. From the assumption 4, it can be assumed that the ideal resonant filter generates a pure sinusoidal output current, no phase shift of the output current, and no voltage drop. The combination of the elements L and R causes the proper phase shift of the output current.
6) The MOSFETs are driven by square-waveform signals as shown in Fig. 2. When the MOSFET is OFF, the gate voltage is the same as the source voltage. The switching pattern is the same as that given in Table I.
7) At the end of the dead time, both the switch voltages v_{S1} and v_{S2} satisfy the class-E ZVS/ZDS conditions as given in (1) and (2).

Under the aforementioned assumptions, the equivalent model of the class-DE inverter can be obtained as shown in Fig. 1(b).

B. Definition of Frequencies

In this paper, four kinds of "frequency" appear:

1) the operating frequency is the frequency of the driving signals D_{r1} and D_{r2};
2) the resonant frequency is equal to $1/(2\pi\sqrt{L_0 C_0})$ for the *LC* resonant filter;
3) the maximum operating frequency is the operating frequency obtained when the shunt capacitances include no external linear capacitances for a specified duty ratio;
4) the highest maximum operating frequency is the peak value of the maximum operating frequency against duty-ratio variations at which the class-E ZVS/ZDS conditions are satisfied.

C. Current and Voltage Waveforms

The analysis for steady state is performed in the interval $0 \le \theta < 2\pi$.

For $0 \le \theta < 2\pi D$, the switch S_1 is ON and the switch S_2 is OFF. Therefore, the switch voltages are constant

$$v_{S1}(\theta) = 0 \quad \text{and} \quad v_{S2}(\theta) = V_{\mathrm{DD}}. \tag{6}$$

Because both the gate–drain voltage and the drain–source one are constant, the current through the drain–source capacitances and the gate–drain ones are

$$i_{C_{\mathrm{ds1}}}(\theta) = i_{C_{\mathrm{ds2}}}(\theta) = i_{C_{\mathrm{gd1}}}(\theta) = i_{C_{\mathrm{gd2}}}(\theta) = 0. \tag{7}$$

Additionally, the current through the switch S_2 is

$$i_{S2}(\theta) = 0. \tag{8}$$

From (5) and (8)–(13), the current through the switch S_1 is obtained as

$$i_{S1}(\theta) = -i_o(\theta) = -I_m \sin(\theta + \varphi). \tag{9}$$

For $2\pi D \le \theta < \pi$, both switches are OFF. Thus

$$i_{S1}(\theta) = i_{S2}(\theta) = 0. \tag{10}$$

From the assumption 6, the voltage across the drain–gate capacitances are the same as that across the drain–source capacitances in the identical MOSFET. From the Kirchhoff's current law, we obtain

$$-\omega(C_{\mathrm{ds1}} + C_{\mathrm{gd1}})\frac{dv_{S1}}{d\theta} + \omega(C_{\mathrm{ds2}} + C_{\mathrm{gd2}})\frac{dv_{S2}}{d\theta} = I_m \sin(\theta + \varphi). \tag{11}$$

From (11) and $v_{S1} + v_{S2} = V_{\mathrm{DD}}$, we have

$$\frac{dv_{S1}(\theta)}{d\theta} = \frac{-I_m}{\omega(C_{\mathrm{ds1}} + C_{\mathrm{gd1}} + C_{\mathrm{ds2}} + C_{\mathrm{gd2}})} \sin(\theta + \varphi). \tag{12}$$

From the class-E ZDS condition for v_{S1} in (1), we obtain $\varphi = 0$ and π. In this paper, we consider that the amplitude of the output current I_m is positive. Therefore, the phase difference is determined as

$$\varphi = \pi. \tag{13}$$

By substituting (3) and (4) into (12) and integrating both sides of (12) with $v_{S1}(2\pi D) = 0$, we obtain

$$\omega\sum_{k=1}^{3}\frac{C_{j0k}V_{\rm bik}}{1-m_k}\left[\left(1+\frac{v_{S1}}{V_{\rm bik}}\right)^{1-m_k} - \left(1+\frac{V_{\rm DD}-v_{S1}}{V_{\rm bik}}\right)^{1-m_k} + \left(1+\frac{V_{\rm DD}}{V_{\rm bik}}\right)^{1-m_k} - 1\right] = I_m[\cos(2\pi D)-\cos\theta]. \tag{14}$$

The switch voltages for $\theta = \pi$ are $v_{S1}(\pi) = V_{\rm DD}$ and $v_{S2}(\pi) = 0$ because of the class-E ZVS condition in (2). By substituting $\theta = \pi$ and $v_{S1} = 0$ into (14), the amplitude I_m is

$$I_m = \frac{2\omega}{1+\cos(2\pi D)}\sum_{k=1}^{3}\frac{C_{j0k}V_{\rm bik}\left[\left(1+\frac{V_{\rm DD}}{V_{\rm bik}}\right)^{1-m_k}-1\right]}{(1-m_k)}. \tag{15}$$

By eliminating I_m from (14) and (15), we have

$$\sum_{k=1}^{3}\left[\left(1+\frac{V_{\rm DD}}{V_{\rm bik}}\frac{v_{S1}}{V_{\rm DD}}\right)^{1-m_k} - \left(1+\frac{V_{\rm DD}}{V_{\rm bik}} - \frac{V_{\rm DD}}{V_{\rm bik}}\frac{v_{S1}}{V_{\rm DD}}\right)^{1-m_k} + \left(1+\frac{V_{\rm DD}}{V_{\rm bik}}\right)^{1-m_k} - 1\right] - \frac{2[\cos(2\pi D)-\cos\theta]\sum_{k=1}^{3}\left[\left(1+\frac{V_{\rm DD}}{V_{\rm bik}}\right)^{1-m_k}-1\right]}{1+\cos(2\pi D)} = 0. \tag{16}$$

Generally, the numerical calculations are needed to obtain the switch voltage waveforms. From (16), however, it is seen that the normalized switch voltages $v_{S1}/V_{\rm DD}$ and $v_{S2}/V_{\rm DD}$ are expressed as a function of ratio of the dc-supply voltage to the built-in potentials $V_{\rm DD}/V_{\rm bik}$, grading coefficients of the diode junction m_k, each switch-on interval $2\pi D$, and angular time θ.

For $\pi \le \theta < \pi + 2\pi D$, the switch S_1 is OFF and the switch S_2 is ON. From the same procedure for the first interval, we obtain the waveform expressions as

$$\begin{aligned} v_{S1}(\theta) &= V_{\rm DD}, \quad v_{S2}(\theta) = 0 \\ i_{S1}(\theta) &= i_{CS1}(\theta) = i_{CS2}(\theta) = 0 \\ i_{S2}(\theta) &= i_o(\theta) = -I_m\sin\theta. \end{aligned} \tag{17}$$

For $\pi + 2\pi D \le \theta < 2\pi$, both the switches are OFF. Therefore, the switch currents are given as

$$i_{S1}(\theta) = i_{S2}(\theta) = 0. \tag{18}$$

Following the similar analytical procedure for the second interval with $v_{S1}(\pi + 2\pi D) = V_{\rm DD}$, we obtain the expressions for the switch voltage as

$$\sum_{k=1}^{3}\left[\left(1+\frac{V_{\rm DD}}{V_{\rm bik}}\frac{v_{S1}}{V_{\rm DD}}\right)^{1-m_k} - \left(1+\frac{V_{\rm DD}}{V_{\rm bik}} - \frac{V_{\rm DD}}{V_{\rm bik}}\frac{v_{S1}}{V_{\rm DD}}\right)^{1-m_k} - \left(1+\frac{V_{\rm DD}}{V_{\rm bik}}\right)^{1-m_k} + 1\right] + \frac{2[\cos(2\pi D)+\cos\theta]\sum_{k=1}^{3}\left[\left(1+\frac{V_{\rm DD}}{V_{\rm bik}}\right)^{1-m_k}-1\right]}{1+\cos(2\pi D)} = 0. \tag{19}$$

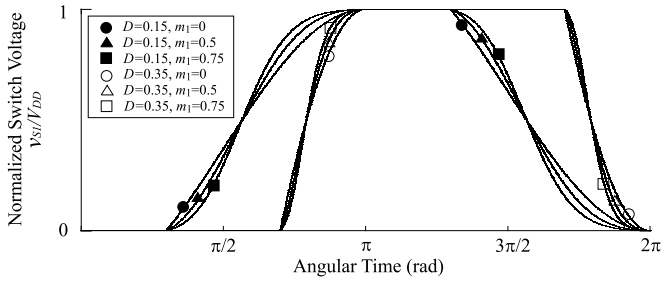


Fig. 3. Example waveforms of normalized switch voltage $v_{S1}/V_{\rm DD}$ for $V_{\rm DD}/V_{\rm bi} = 80$ and $C_{\rm gd} = 0$.

For simplicity, we would like to consider the effects of only the MOSFET gate–drain capacitances in all the plots given in Sections IV–VI. This is because the gate–drain capacitances are sufficiently small compared with the drain–source capacitances. Fig. 3 shows example waveforms of the normalized switch voltage $v_{S1}/V_{\rm DD}$ for $C_{\rm gd} = 0$. It is seen from Fig. 3 that a small duty ratio and a large grading coefficient cause fast changes of the switch voltage. Because a small shunt capacitance and high frequency enhance the slope of switch voltage, there is a possibility that the obtained values of dv_{S1}/dt are close to the maximum rate of the MOSFET, which is usually from 3 to 20 V/ns. A problem for reliable operation of the power inverter occurs if the inverter goes from the nominal operation to the off nominal one when antiparallel diodes conduct current, in particular. Such transition can happen easily when the supply voltage $V_{\rm DD}$ increases only slightly over the specified value.

D. Input Current and Output Voltage, Current, and Power

The input current I_D is given as the average of the current flowing from the dc voltage source $V_{\rm DD}$

$$\begin{aligned} I_D &= \frac{1}{2\pi}\int_0^{2\pi}\left[i_{S2}(\theta) + i_{C{\rm ds}_2}(\theta) + i_{C{\rm gd}_2}(\theta)\right]d\theta \\ &= \frac{1}{2\pi}\int_{\pi}^{\pi+2\pi D} I_m\sin\theta d\theta \\ &= \frac{\omega[1-\cos(2\pi D)]}{\pi[1+\cos(2\pi D)]} \\ &\quad\times\sum_{k=1}^{3}\frac{C_{j0k}V_{\rm bik}\left[\left(1+\frac{V_{\rm DD}}{V_{\rm bik}}\right)^{1-m_k}-1\right]}{(1-m_k)}. \end{aligned} \tag{20}$$

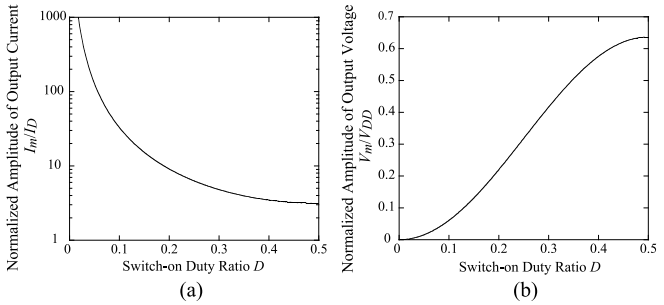


Fig. 4. Normalized output current and voltage as a function of the switch-on duty ratio D. (a) Normalized output current I_m/I_D. (b) Normalized output voltage $V_m/V_{\rm DD}$.

Note that the average value of the current through the MOSFET parasitic capacitance $i_{C\,\rm ds2} + i_{C\,\rm gd2}$ means the average amount of charging/discharging electric charge. Therefore, it is always zero. From (15) and (20), the normalized amplitude of the output current is expressed as

$$\frac{I_m}{I_D} = \frac{2\pi}{1-\cos(2\pi D)}. \tag{21}$$

Using (21), we obtain the input power as

$$P_{\rm dc} = V_{\rm DD} I_D = \frac{I_m V_{\rm DD}[1-\cos(2\pi D)]}{2\pi}. \tag{22}$$

The output power P_o is given by

$$P_o = \frac{I_m V_m}{2} = \frac{R I_m^2}{2} = \frac{V_m^2}{2R} \tag{23}$$

where V_m is the amplitude of the output voltage

$$V_m = R I_m. \tag{24}$$

Ideally, the power-conversion efficiency of the class-DE inverter is 100% on the nominal operation

$$P_{\rm dc} = P_o. \tag{25}$$

From (22), (23), and (25), we can obtain the amplitude of the output voltage normalized with respect to the input voltage as

$$\frac{V_m}{V_{\rm DD}} = \frac{1-\cos(2\pi D)}{\pi}. \tag{26}$$

The analytical results of (21) and (26) show that the amplitude of the output current and voltage are determined by only the input current or voltage, and the duty ratio D. Additionally, the amplitude of the output voltage is proportional to the input voltage at a specified duty ratio in spite of the nonlinearity of the shunt capacitances. This is an important characteristic of the class-DE inverter. Fig. 4 shows the normalized amplitudes of the output current and voltage as functions of the switch-on duty ratio D. The normalized amplitude of the output current goes to infinity with the decrease in D. This is because I_D decreases to zero with the decrease in D, which is confirmed from (20).

From (23) and (26), we have

$$P_o = \frac{V_m^2}{2R} = \frac{V_{\rm DD}^2[1-\cos(2\pi D)]^2}{2\pi^2 R}. \tag{27}$$

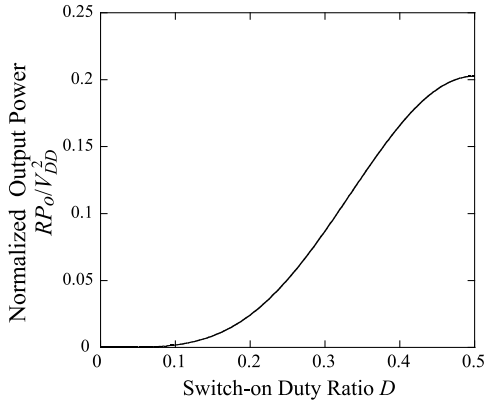


Fig. 5. Normalized output power $RP_o/V_{\rm DD}^2$ as a function of the switch-on duty ratio D.

Fig. 5 shows the normalized output power as a function of the switch-on duty ratio. It is seen from Fig. 5 that the output power increases as the switch-on duty ratio increases.

E. Voltage Across the Load Reactance

Because $i_o = -I_m \sin\theta$, the fundamental component of the voltage $v_L(\theta)$ across the reactance L is expressed as

$$v_L(\theta) = V_L(-\cos\theta) \tag{28}$$

where

$$V_L = \omega L I_m. \tag{29}$$

From (24) and (29), we obtain

$$\frac{V_L}{V_m} = \frac{\omega L}{R}. \tag{30}$$

Because of the assumption 5, the fundamental component of the bottom switch voltage is expressed as

$$v_{S1\rm fund} = v_L(\theta) + v_o(\theta) = -V_L\cos(\theta) - V_m\sin(\theta). \tag{31}$$

Therefore, the normalized magnitude $V_L/V_{\rm DD}$ is derived from the Fourier integral

$$\frac{V_L}{V_{\rm DD}} = \frac{1}{\pi}\int_0^{2\pi} \frac{v_{S1}(\theta)}{V_{\rm DD}}(-\cos\theta)d\theta. \tag{32}$$

The integration in the aforementioned equation can be solved numerically. Here, the function $H(m, V_{\rm DD}/V_{\rm bi}, D)$ is defined as

$$H \equiv \frac{V_L}{V_{\rm DD}} = \frac{1}{\pi}\int_0^{2\pi} \frac{v_{S1}(\theta)}{V_{\rm DD}}(-\cos\theta)d\theta. \tag{33}$$

Fig. 6 shows plots of H as a function of $V_{\rm DD}/V_{\rm bi}$ for $C_{\rm gd} = 0$. In order to illustrate Fig. 6(a), the trapezoidal rule with $2\pi/10\,000$ of grid spacing of θ is used to calculate the integration of (32).

F. Design Equations

From (27), the load resistance R is given as

$$R = \frac{V_{\rm DD}^2[1-\cos(2\pi D)]^2}{2\pi^2 P_o}. \tag{34}$$

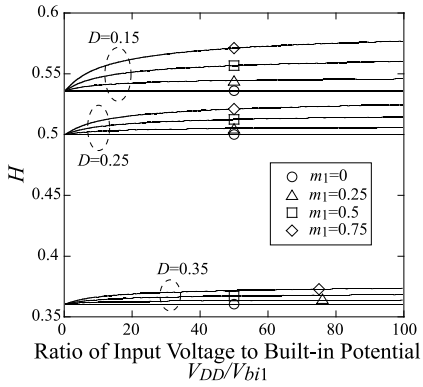


Fig. 6. Plots of H as a function of $V_{\rm DD}/V_{\rm bi1}$ for $C_{\rm gd}=0$.

From the definition of the loaded-quality factor Q, the inductance L_0 is given as

$$L_0=\frac{QR}{\omega}=\frac{QR}{2\pi f}. \tag{35}$$

From (26), (30), and (33), the inductance L is

$$L=\frac{\pi RH}{2\pi f[1-\cos(2\pi D)]}. \tag{36}$$

From (35) and (36), the ideal resonant inductance L_f is obtained as

$$L_f=L_0-L=\frac{R}{2\pi f}\left[Q-\frac{\pi H}{1-\cos(2\pi D)}\right]. \tag{37}$$

The identical resonant filter with the resonant frequency $f=\omega/2\pi$ is realized by L_f and C_0. From $f=1/(2\pi\sqrt{L_fC_0})$ and (37), the resonant capacitance C_0 is expressed analytically as

$$C_0=\frac{1}{2\pi fR\left[Q-\dfrac{\pi H}{1-\cos(2\pi D)}\right]}. \tag{38}$$

In these design equations, we need numerical calculations for obtaining H, which is used for the derivation of C_0 in (38).

V. Maximum Operating Frequency

From (15) and (23), we can obtain another expression of the output power P_o as

$$\begin{aligned}P_o=&\ \frac{I_mV_m}{2}=\frac{RI_m^2}{2}\\ =&\ \frac{2\omega^2R}{[1+\cos(2\pi D)]^2}\\ &\times\left\{\sum_{k=1}^{3}\frac{C_{j0k}V_{\rm bik}\left[\left(1+\dfrac{V_{\rm DD}}{V_{\rm bik}}\right)^{1-m_k}-1\right]}{(1-m_k)}\right\}^2\end{aligned} \tag{39}$$

In this analysis, the shunt capacitances consist of only the MOSFET parasitic capacitances, which are usually not controllable and depend on the type of the MOSFET. Because of the assumption 1 and the definition of the maximum frequency, it

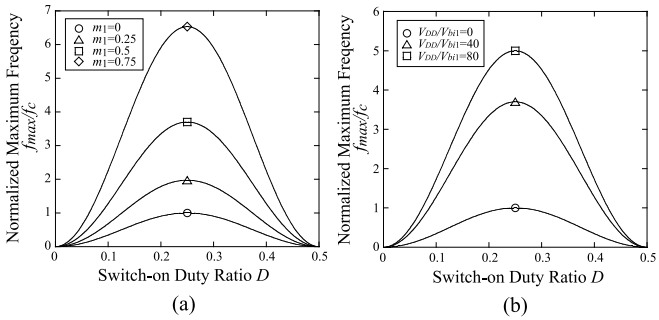


Fig. 7. Normalized maximum operating frequency $f_{\rm max}/f_c$ as a function of D. (a) For $V_{\rm DD}/V_{\rm bi1}=40$ and fixed m_1. (b) For $m_1=0.5$ and fixed $V_{\rm DD}/V_{\rm bi2}$.

can be stated that ω in this analysis is the maximum angular frequency $\omega_{\rm max}$. By equating right-hand side of (27) and that of (39) with $\omega, C_{j0k}, R, V_{\rm DD}$, and $V_{\rm bik}>0$, $0\le m_k<1$, and $\sin^2(\theta)=1-\cos^2(\theta)$, the maximum operating frequency of the class-DE inverter can be expressed as

$$\begin{aligned}f_{\rm max}=&\ \frac{\omega_{\rm max}}{2\pi}\\ =&\ \frac{\sin^2(2\pi D)}{4\pi^2R}\sum_{k=1}^{3}\frac{\dfrac{V_{\rm DD}}{V_{\rm bik}}(1-m_k)}{C_{j0k}\left[\left(1+\dfrac{V_{\rm DD}}{V_{\rm bik}}\right)^{1-m_k}-1\right]}.\end{aligned} \tag{40}$$

It is seen from (40) that the maximum operating frequency is inversely proportional to R. Additionally, it is also seen from (40) that the maximum operating frequency increases as C_{j0k} decreases for fixed m_k. Here, we define the criterion for the frequency f_c as the maximum operating frequency for $m=0$ and $D=0.25$, which is independent of the input voltage $V_{\rm DD}$ [1]. By using $f_{\rm max}$ and f_c, we have normalized maximum operating frequency as

$$\frac{f_{\rm max}}{f_c}=\sin^2(2\pi D)\sum_{k=1}^{3}\frac{\dfrac{V_{\rm DD}}{V_{\rm bik}}(1-m_k)}{\left[\left(1+\dfrac{V_{\rm DD}}{V_{\rm bik}}\right)^{1-m_k}-1\right]}. \tag{41}$$

Fig. 7 shows the normalized maximum operating frequency as functions of the switch-on duty ratio D for $C_{\rm gd}=0$. From Fig. 7 and (41), it is seen that the maximum frequency is symmetry against the duty-ratio variations with respect to $D=0.25$. The highest maximum operating frequency can be obtained at $D=0.25$ for fixed m_k and $V_{\rm DD}/V_{\rm bik}$, namely when MOSFET type is selected. Therefore, by substituting $D=0.25$ into (40), the highest maximum operating frequency is

$$f_{\rm high}=\frac{1}{4\pi^2R}\sum_{k=1}^{3}\frac{\dfrac{V_{\rm DD}}{V_{\rm bik}}(1-m_k)}{C_{j0k}\left[\left(1+\dfrac{V_{\rm DD}}{V_{\rm bik}}\right)^{1-m_k}-1\right]}. \tag{42}$$

Figs. 8 and 9 show the normalized maximum operating frequency as functions of the ratio of the input voltage to the built-in potential $V_{\rm DD}/V_{\rm bi1}$ and the grading coefficient m_1, respectively, for $C_{\rm gd}=0$. It is seen from Figs. 8 and 9 that the

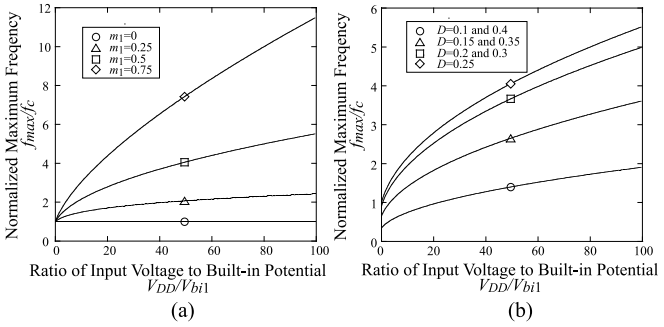


Fig. 8. Normalized maximum operating frequency $f_{\max}/f_c$ as a function of $V_{\rm DD}/V_{\rm bi1}$ for $C_{\rm gd}=0$. (a) For $D=0.25$ and fixed m_1. (b) For $m_1=0.5$ and fixed D.

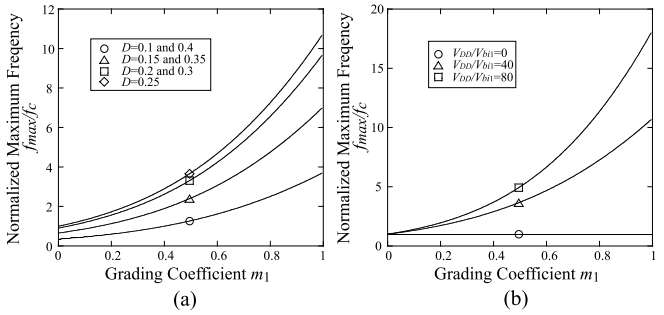


Fig. 9. Normalized maximum operating frequency $f_{\max}/f_c$ as a function of m_1 for $C_{\rm gd}=0$. (a) For $V_{\rm DD}/V_{\rm bi1}=40$ and fixed D. (b) For $D=0.25$ and fixed $V_{\rm DD}/V_{\rm bi1}$.

maximum operating frequency is high for large m_1 and high $V_{\rm DD}/V_{\rm bi1}$. This is because the average value of nonlinear capacitance in one-period operation decreases with increase in m_1 and $V_{\rm DD}/V_{\rm bi1}$. The maximum frequency increases as the shunt capacitance decreases.

VI. Power Output Capability

The class-DE inverter contains two MOSFETs S_1 and S_2. The peak voltage stress is identical to the input voltage $V_{\rm DD}$. In this paper, the shunt capacitances are parasitic elements of the MOSFETs. Therefore, we should consider both the current through the switches and that through the drain–source capacitances in order to obtain the peak current stress of the MOFSETs. The maximum current through the switch S_1, which is expressed as $I_{S\max}$, is identical to that through S_2

$$I_{S\max}=\begin{cases}|I_m||\sin(2\pi D)| & \text{for } 0<D\le 0.25\\ |I_m| & \text{for } 0.25\le D<0.5.\end{cases} \tag{43}$$

Similarly, $I_{C{\rm ds}\max}$ is defined as the maximum current through the drain–source capacitances. The current through the drain–source capacitance and its maximum value can be obtained only numerically. For example, the current through the drain–source capacitance of the bottom MOSFET$i_{C{\rm ds1}}$ is expressed from

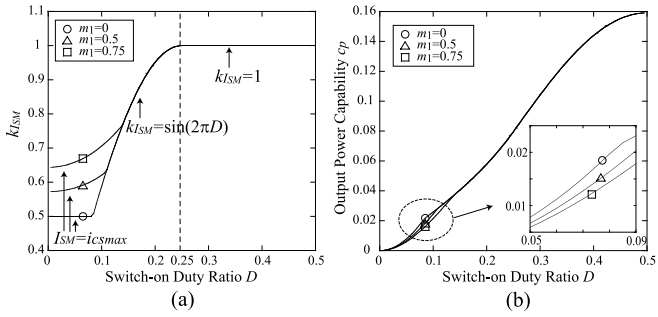


Fig. 10. (a) Maximum-current coefficient $k_{I_{\rm SM}}$ for $C_{\rm gd}=0$. (b) Power output capability c_p.

(12) as

$$i_{C{\rm ds1}}(\theta)=\omega C_{\rm ds1}\frac{dv_{S1}(\theta)}{d\theta}=\frac{C_{\rm ds1}I_m\sin(\theta)}{C_{\rm ds1}+C_{\rm gd1}+C_{\rm ds2}+C_{\rm gd2}}. \tag{44}$$

Note that the currents i_{S1} and $i_{C{\rm ds1}}$ never flow simultaneously due to the assumption 2. Therefore, the maximum current through the MOSFETs $I_{\rm SM}$ is obtained as

$$\begin{aligned}I_{\rm SM}&=\max\{i_{S1}(\theta)+i_{C{\rm ds1}}(\theta)\}\\&=\max\{I_{S\max},I_{C{\rm ds}\max}\}=k_{I_{\rm SM}}I_m\end{aligned} \tag{45}$$

where $k_{I_{\rm SM}}$ is a coefficient obtained from (43) and (44). From (23), (26), and (45), the power output capability is obtained as

$$c_p=\frac{P_o}{2I_{\rm SM}V_{\rm DD}}=\frac{1-\cos(2\pi D)}{4\pi k_{I_{\rm SM}}}. \tag{46}$$

Fig. 10 shows $k_{I_{\rm SM}}$ and c_p as functions of D for $C_{\rm gd}=0$, $V_{\rm DD}/V_{\rm bi}=40$, and fixed m. It can be stated from Fig. 10(a) that $I_{\rm SM}=I_{C{\rm ds}\max}$ for small value of D. From Fig. 3, the slope of the switch voltage rapidly increases as the grading coefficient m increases. Therefore, $I_{\rm SM}$ becomes large for large m. The maximum switch current $I_{\rm SM}$ is independent of the grading coefficients in the region where $I_{\rm SM}=I_{S\max}$. It is seen from Fig. 10(b) that the power output capability is almost independent of the grading coefficients. Small differences, however, appear for small D because of the differences in $k_{I_{\rm SM}}$. We can also see that the power output capability increases with the increase in D.

It can be stated from Figs. 5, 7, and 10 that the switch-on duty ratio should be specified in the range of $0.25\le D<0.5$. This is because: 1) the frequency range is the same as that for $0<D<0.25$, 2) the output power is higher than that for $0<D<0.25$, and 3) the power output capability is also higher than that for $0<D<0.25$.

VII. Power-Conversion Efficiency

In real circuits, the power losses occur in the parasitic resistances of each component. It is assumed that the parasitic resistances are small enough not to affect the waveforms. In this paper, we consider the equivalent series resistance (ESR) of the load network r_{LC} and switch-on resistances r_{S1} and r_{S2} as shown in Fig. 11. In this analysis, $r_S=r_{S1}=r_{S2}$ is assumed because of the assumption 2. The ESRs of the MOSFET

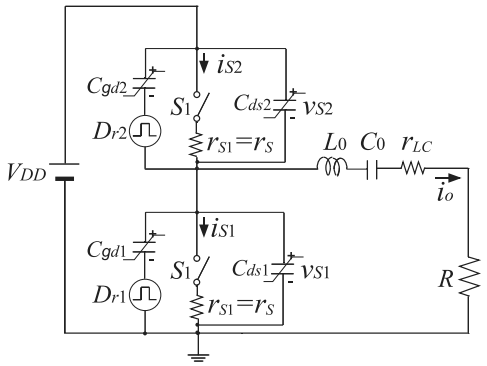


Fig. 11. Equivalent circuit of class-DE inverter including ESRs.

parasitic capacitances are ignored because they are generally much smaller than the other ESRs. The power loss in r_{LC} is obtained as

$$P_{r_{LC}} = \frac{1}{2\pi}\int_0^{2\pi} r_{LC} i_o^2(\theta)d\theta = \frac{r_{LC} I_m^2}{2}. \tag{47}$$

Similarly, the power losses at the switch-on resistances are obtained as

$$\begin{aligned} P_{r_{S1}} &= \frac{1}{2\pi}\int_0^{2\pi} r_S i_{S1}^2(\theta)d\theta = \frac{r_S}{2\pi}\int_0^{2\pi D} I_m^2 \sin^2\theta d\theta \\ &= \frac{r_S I_m^2 [4\pi D - \sin(4\pi D)]}{8\pi}, \\ P_{r_{S2}} &= \frac{r_S}{2\pi}\int_{\pi}^{\pi+2\pi D} I_m^2 \sin^2\theta d\theta \\ &= \frac{r_S I_m^2 [4\pi D - \sin(4\pi D)]}{8\pi} = P_{r_{S1}} \end{aligned} \tag{48}$$

where $P_{r_{S1}}$ and $P_{r_{S2}}$ are the power losses at the switch-on resistances of S_1 and S_2, respectively. From (39), (47), and (48), the power-conversion efficiency η is obtained as

$$\begin{aligned} \eta &= \frac{P_o}{P_o + P_{r_{LC}} + P_{r_{S1}} + P_{r_{S2}}} \\ &= \frac{\frac{RI_m^2}{2}}{\frac{RI_m^2}{2} + \frac{r_{LC} I_m^2}{2} + \frac{r_S I_m^2 [4\pi D - \sin(4\pi D)]}{4\pi}} \\ &= \frac{1}{1 + \frac{r_{LC}}{R} + \frac{r_S [4\pi D - \sin(4\pi D)]}{2\pi R}}. \end{aligned} \tag{49}$$

VIII. Design Example and Experimental Verifications

The design example with the discrete MOSFET devices is given. The design specifications are: operating frequency $f = 1$ MHz, input voltage $V_{\rm DD} = 90$ V, output resistance $R = 57.2\ \Omega$, and loaded quality factor $Q = 5$.

It is considered that the IRF530 MOSFETs, whose breakdown voltage is 100 V, are used as the switching devices. The values of grading coefficient m_k, the built-in potential $V_{\rm bik}$, and C_{j0k} of IRF530 MOSFET are obtained from the "irf.lib" in PSpice device library as given in Table II. Additionally, the drain–source on-resistance of the IRF530 MOSFET is $r_S = 0.16\ \Omega$ from the data sheet. By substituting $D = 0.25$ into (40), the highest maximum operating frequency of the class-DE inverter using IRF530 MOSFETs is obtained as $f_{\rm high} = 1.45$ MHz. It is confirmed, therefore, that the IRF530 MOSFET can be used for these design specifications. From (40), the duty ratio D is obtained as $D = 0.16$ or 0.34. From the output power and power-output-capability point of view, we pick $D = 0.34$. Therefore, $L_0 = 45.2\mu$H is obtained from (35). From the numerical calculations of (33), H is 0.382. Therefore, the resonant capacitance C_0 is 654pF from (38).

TABLE II
Parameters for IRF530

C_{j01}	m_1	V_{bi1}	C_{j02}	m_2	C_{j03}	m_3	V_{bi3}	r_S
$1.03\ nF$	0.501	1.47 V	0.0 pF	0	750 pF	0.673	0.801 V	0.16 Ω

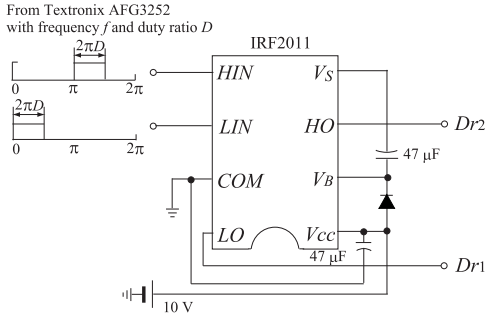


Fig. 12. Driver circuit.

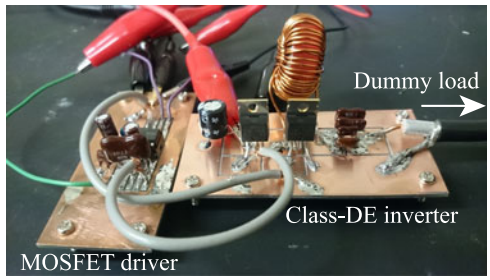


Fig. 13. Implemented circuit.

Fig. 12 shows the driver circuit for experiments. We used an IRF 2011 driver logic and the Textronix AFG3252 dual-channel arbitrary function generator. Figs. 13 and 14 show the implemented circuit for measurements and superimposed experimental and PSpice waveforms onto analytical ones. It can be confirmed from Fig. 14 that all the waveforms satisfied the class-E ZVS/ZDS conditions. Table III gives the analytical predictions and experimental measurements.

For obtaining the experimental-measurement values, element values including the ESR of the load network were measured by the HP 4284A *LCR* meter, root-mean-square value of the output voltage V_o was measured by the Agilent 3458A digital

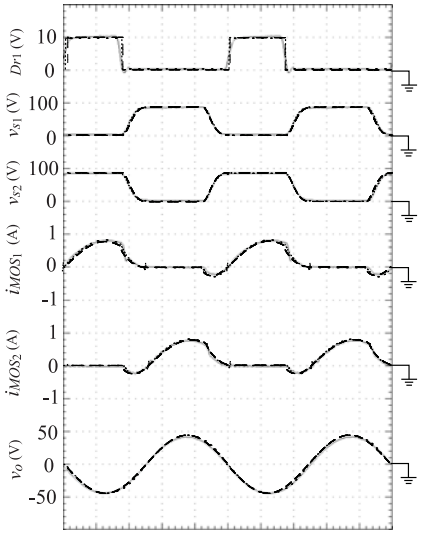


Fig. 14. Waveforms from analytical expressions, PSpice simulation and circuit experiment. Dashed line: analytical waveforms, dotted line: PSpice waveforms, and solid line: experimental waveforms. Vertical: D_{r1}: 10 V/div, v_{S1} and v_{S2}: 100 V/div, i_{MOS1} and i_{MOS2}: 0.5 A/div, and v_o: 50 V/div. Horizontal: 200 ns/div.

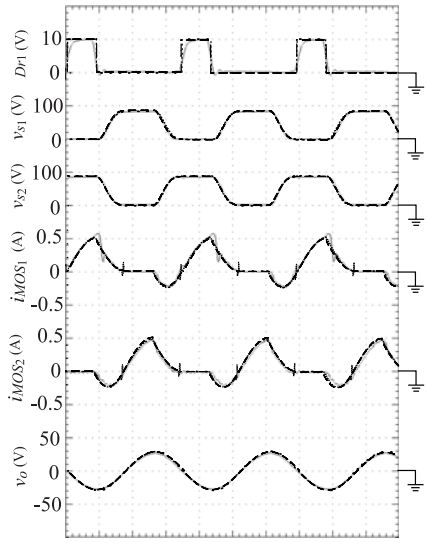


Fig. 15. Waveforms from analytical expressions, PSpice simulation and circuit experiment. Dashed line: analytical waveforms, dotted line: PSpice waveforms, and solid line: experimental waveforms. Vertical: D_{r1}: 10 V/div, v_{S1} and v_{S2}: 100 V/div, i_{MOS1} and i_{MOS2}: 1 A/div, and v_o: 50 V/div. Horizontal: 200 ns/div.

TABLE III
ANALYTICAL PREDICTIONS AND EXPERIMENTAL MEASUREMENTS FOR DESIGN SPECIFICATIONS

	Calculated	Measurement	Difference
f	1 MHz	1.00 MHz	0.0%
V_{DD}	90 V	90 V	0.0%
D	0.34	0.34	0.0%
C_0	654 pF	646 pF	−1.3%
L_0	45.2 μH	44.7 μH	−1.3%
R	57.2 Ω	57.2 Ω	0.0%
r_S	0.16 Ω	–	–
r_{LC}	–	1.30 Ω	–
P_o	17.3 W	16.5 W	−4.6%
η	97.3%*	96.4%	−0.9%

* η is calculated by using the measured value of r_{LC}.

TABLE IV
ANALYTICAL PREDICTIONS AND EXPERIMENTAL MEASUREMENTS FOR HIGHEST MAXIMUM OPERATING FREQUENCY

	Calculated	Measurement	Difference
f	1.45 MHz	1.45 MHz	0.0%
V_{DD}	90 V	90 V	0.0%
D	0.25	0.25	0.0%
C_0	567 pF	556 pF	−1.9%
L_0	31.5 μH	31.9 μH	1.4%
R	57.2 Ω	57.2 Ω	0.0%
r_S	0.16 Ω	–	–
r_{LC}	–	1.01 Ω	–
P_o	7.18 W	6.86 W	−4.5%
η	98.1 %*	97.7 %	−0.4%

* η is calculated by using the measured value of r_{LC}.

multimeter, and V_{DD} and I_D were measured by the Iwatsu VOAC7523 digital multimeter. Additionally, f and D, which were set by the function generator, were used as the measured values of f and D. It is seen from Fig. 14 and Table III that the experimental and PSpice-simulation results agreed with the analytical ones quantitatively, which showed the validity of the analytical expressions in this paper. In the experiment in Fig. 14, 96.4% power-conversion efficiency can be achieved with 1 MHz and 16.5-W output. Additionally, the drive power and the power-added efficiency are 0.33 W and 94.6%, respectively.

Fig. 15 shows analytical, PSpice-simulated, and experimental waveforms for the highest maximum operating frequency. It is confirmed that all the waveforms achieved the class-E ZVS/ZDS conditions. Table IV gives the analytical predictions and experimental measurements. It is also seen from Fig. 15 and Table IV that the experimental and PSpice-simulation measurements showed good agreement with the analytical predictions. The experimental measurements in Fig. 15 showed 97.7% power conversion and 92.0% power added efficiencies with 1.45 MHz and 6.86-W output and 0.44-W drive power.

IX. CONCLUSION

Analytical expressions have been presented for designs of the class-DE inverters at any duty ratio and a high loaded quality factor, taking into account the nonlinear MOSFET drain–source and gate–drain parasitic capacitances with any grading coefficients of the diode junctions. Additionally, maximum operating frequency, power output capability, and power-conversion efficiency of the class-DE inverter have been also obtained. It has been shown that the highest maximum operating frequency occurs when the switch-on duty ratio is 0.25. From the obtained results, it can be stated that the switch-on duty ratio of the class-DE inverter should be specified in the range of $0.25 \leq D < 0.5$. The PSpice-simulation and experimental results indicated the

validity of our analysis. The obtained analytical expressions may extend the potential of the class-DE inverter applications.

REFERENCES

[1] H. Koizumi, T. Suetsugu, M. Fujii, K. Shinoda, S. Mori, and K. Ikeda, "Class DE high-efficiency tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. 43, no. 1, pp. 51–60, Jan. 1996.

[2] S. A. El-Hamamsy, 'Design of high-efficiency RF class-D power amplifier," *IEEE Trans. Power Electron.*, vol. 9, no. 3, pp. 297–308, May 1994.

[3] M. Albulet, "An exact analysis of class-DE amplifier at any output Q," *IEEE Trans. Circuits Syst.*, vol. 46, no. 10, pp. 242–248, Apr. 1999.

[4] H. Sekiya, H. Koizumi, S. Mori, I. Sasase, J. Lu, and T. Yahagi, "FM/PWM control scheme in class DE inverter," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 7, pp. 1250–1260, Jul. 2004.

[5] H. Sekiya, S. Nemoto, J. Lu, and T. Yahagi, "Phase control for resonant dc/dc converter with class DE inverter and class E rectifier," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 1, pp. 254–263, Feb. 2006.

[6] M. Amjad, Z. Salam, M. Facta, and S. Mekhilef, "Analysis and implementation of transformerless LCL resonant power supply for ozone generation," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 650–660, Feb. 2013.

[7] H. Sarnago, O. Lucia, A. Mediano, and J. M. Burdio, "Class-D/DE dual-mode-operation resonant converter for improved-efficiency domestic induction heating system," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1274–1285, Mar. 2013.

[8] T. Suetsugu, and M. K. Kazimierczuk, "Integration of class DE inverter for on-chip power supplies," in *Proc. IEEE Int. Symp. Circuits Syst.*, Island of Kos, Greece, May. 2006, pp. 3133–3136.

[9] T. Suetsugu, and M. K. Kazimierczuk, "Integration of class DE dc-dc converter for on-chip power supplies," in *Proc. IEEE Power Electron. Spec. Conf.*, Jeju, South Korea, Jun. 2006, pp. 1–5.

[10] D. Murthy-Bellur, A. Bauer, W. Kerin, and M. K. Kazimierczuk, "Inverter using loosely coupled inductors for wireless power transfer," in *Proc. IEEE Int. Midwest Symp. Circuits Syst.*, Boise, ID, USA, Aug. 2012, pp. 1164–1167.

[11] K. Inoue, T. Nagashima, X. Wei, and H. Sekiya, "Design of high-efficiency inductive-coupled wireless power transfer system with class-DE transmitter and class-E rectifier," in *Proc. IEEE Conf. Ind. Electron. Soc.*, Wien, Austria, Nov. 2013, pp. 613–618.

[12] J. Modzelewski, "Optimum and sub-optimum operation of high-frequency Class-D zero-voltage-switching tuned power amplifier," *Bull. Polish Acad. Sci., Tech. Sci.*, vol. 46, no. 4, pp. 458–473, Apr. 1998.

[13] L. R. Neorne, "Design of a 2.5-MHz, soft-switching, class-D converter for electrodeless lighting," *IEEE Trans. Power Electron.*, vol. 12, no. 3, pp. 507–516, May 1997.

[14] H. Sekiya, T. Negishi, T. Suetsugu, and T. Yahagi, "Operation of class DE amplifier outside optimum condition," *J. Signal Proccess.*, vol. 10, no. 4, pp. 247–250, Jul. 2006.

[15] A. Alipov and V. Kozyrev, "Push/pull class-DE switching power amplifier," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, Seattle, WA, USA, Jun. 2002, vol. 3, pp. 1635–1638.

[16] H. Sekiya, T. Watanabe, T. Suetsugu, and M. K. Kazimierczuk, "Analysis and design of class DE amplifier with nonlinear capacitances," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 10, pp. 2362–2371, Oct. 2009.

[17] H. Sekiya, X. Wei, and S. Oshikawa, "MOSFET parasitic capacitance effects to class-DE power amplifier," in *Proc. IEEE Elect. Design Adv. Packag. Syst. Symp.*, Nara, Japan, Dec. 2013, pp. 245–248.

[18] H. Sekiya, N. Sagawa, and M. K. Kazimierczuk, "Analysis of class DE amplifier with nonlinear shunt capacitances at any grading coefficient for high Q and 25 % duty ratio," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 924–932, Apr. 2010.

[19] H. Sekiya, N. Sagawa, and M. K. Kazimierczuk, "Analysis of class-DE amplifier with linear and nonlinear shunt capacitances at 25 % duty ratio," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 9, pp. 2334–2342, Sep. 2010.

[20] T. Ezawa, H. Sekiya, and T. Yahagi, "Design of class DE amplifier with nonlinear shunt capacitances for any output Q," *IEICE Trans. Fundam.*, vol. E91-A, no. 4, pp. 927–934, Apr. 2008.

[21] H. Sekiya, S. Oshikawa, and T. Yahagi, "Novel design procedure for class DE amplifier," *J. Circuits, Syst. Comput.*, vol. 17, no. 2, pp. 191–209, Apr. 2008.

[22] H. Sekiya, T. Ezawa, and Y. Tanji, "Design procedure for class E switching circuits allowing implicit circuit equations," *IEEE Trans. Circuits Syst. I,*, vol. 55, no. 11, pp. 3688–3696, Dec. 2008

[23] M. Hayati, A. Lotfi, M. K. Kazimierczuk, and H. Sekiya, "Analysis and design of class-E power amplifier with MOSFET parasitic linear and nonlinear capacitances at any duty ratio," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5222–5232, Nov. 2013.

[24] A. Mediano and P. Molina, "Frequency limitation of a high-efficiency class E tuned RF power amplifier due to a shunt capacitance," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, Anaheim, CA, USA, Jun. 1999, pp. 13–19.

[25] A. Mediano, P. Molina, and J. Navarro, "Class E RF/microwave power amplifier: Linear "Equivalent" of transistor's nonlinear output capacitance, normalized design and maximum operating frequency versus output capacitance," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, Boston, MA, USA, Jun., 2000, pp. 783–786.

[26] X. Wei, H. Sekiya, S. Kuroiwa, T. Suetsugu, and M. K. Kazimierczuk, "Design of class-E amplifier with MOSFET linear gate-to-drain and nonlinear drain-to-source capacitances," *IEEE Trans. Circuits Syst.-I*, vol. 58, no. 10, pp. 2556–2565, Oct. 2011.

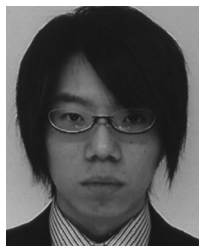
[27] T. Suetsugu and M. K. Kazimierczuk, "Maximum operating frequency of class-E amplifier at any duty ratio," *IEEE Trans. Circuits Syst-II*, vol. 55, no. 8, pp. 768–770, Aug. 2008.

Hiroo Sekiya (S'97–M'01–SM'10) was born in Tokyo, Japan, on July 5, 1973. He received the B.E., M.E., and Ph.D. degrees in electrical engineering from Keio University, Yokohama, Japan, in 1996, 1998, and 2001 respectively.

Since April 2001, he has been with Chiba University, Chiba, Japan, where he is currently an Associate Professor at Graduate School of Advanced Integration Science. From Feb. 2008 to Feb. 2010, he was with Electrical Engineering, Wright State University, Dayton, OH, USA, as a Visiting Scholar. His research interests include high-frequency high-efficiency tuned power amplifiers, resonant dc/dc power converters, dc/ac inverters, magnetic component designs, and digital signal processing for wireless communications.

Xiuqin Wei (S'10–M'12) was born in Fujian, China, on December 7, 1983. She received the B.E. degree from Fuzhou University, Fuzhou, China, in 2005, and the Ph.D. degree from Chiba University, Chiba, Japan, in 2012.

Since April 2012, she has been with Fukuoka University, Fukuoka, Japan, where she is currently an Assistant Professor in the Department of Electronics Engineering and Computer Science. Her research interests include high-frequency power amplifier.



Tomoharu Nagashima (S'11) was born in Saitama, Japan, on February 4, 1989. He received the B.E. and M.E. degrees from Chiba University, Chiba, Japan, in 2011 and 2012, respectively, where he is currently working toward the Ph.D. degree.

His current research interest is in resonant dc/dc power converters, dc/ac inverters, and high-frequency high-efficiency tuned power amplifiers.

Marian K. Kazimierczuk (M'91–SM'91–F'04) received the M.S., Ph.D., and D.Sci. degrees in electronics engineering from the Department of Electronics, Technical University of Warsaw, Warsaw, Poland, in 1971 1978, and 1984, respectively.

Since 1985, he has been with the Department of Electrical Engineering, Wright State University, Dayton, OH, USA, where he is currently a Professor. His research interests include high-frequency high-efficiency switching mode tuned power amplifiers, resonant and PWM dc/dc power converters, dc/ac inverters, high-frequency rectifiers, electronic ballasts, modeling and control of converters, high-frequency magnetics, and power semiconductor devices.