# PV Balancers: Concept, Architectures, and Realization

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***Abstract*—This paper presents a new concept of module-integrated converters called PV balancers for photovoltaic applications. The proposed concept enables independent maximum power point tracking for each module, and dramatically decreases the requirements in terms of electrical rating, size, and manufacturing cost for power converters. The power rating of a PV balancer is less than 20% of its counterparts, and the manufacturing cost is thus significantly reduced. In this paper, two architectures of PV balancers are proposed, analyzed, realized, and verified through simulation and experimental results. It is anticipated that the proposed approach will be a low-cost solution for future photovoltaic power systems.**

***Index Terms*—DC–DC power converters, module-integrated converters (MICs), partial power processing, photovoltaics (PVs), solar energy.**

## I. Introduction

MODULE-INTEGRATED converters (MICs) for photovoltaic systems have been developing very rapidly in recent years [1]–[5]. Compared to past centralized or string technologies [1], MICs perform maximum power point tracking (MPPT) on each module, allowing the modules in a series string to operate at different optimal voltages and currents, thus increasing energy capture by more than 30% when there is temporary shade or a permanent defect on one of modules [2]. Fig. 1 shows three traditional structures of MICs. All these structures can achieve independent MPPT for each module. The dc–ac inverters in Fig. 1(a) are also known as microinverters [4], [5]. The outputs of microinverters are combined at an ac grid. Because the output voltage of a PV module is relatively lower than the voltage of the ac grid, microinverters need to have a high-voltage transformation ratio. Microinverters are well modularized but they suffer from a lower efficiency and a higher cost compared to traditional centralized inverters. In Fig. 1(b), the outputs of dc–dc converters on each PV module are combined in parallel by a common dc bus [1], [6].

This structure could be less expensive but a high-voltage transformation ratio still exists in the dc–dc converters and in centralized dc–ac inverters. In Fig. 1(c), the cascaded dc–dc converters (dc–dc optimizers) are under intensive research recently, the outputs of dc–dc converters are stacked up in series, and the requirement of the voltage transformation at the inverter stage is thus significantly reduced, which is also desirable as it enables the use of a central, high-voltage, high-efficiency inverter [2], [3]. However, under the greatest mismatched conditions, e.g., when one module in the string is generating its maximum power and other modules are completed shaded and generate little power, the MICs in Fig. 1 may be unable to maintain the minimum inverter input voltage. In summary, MIC technologies to date have suffered the key disadvantage that the initial equipment cost is higher. Moreover, MIC electrical efficiency and compactness are also concerns in design.

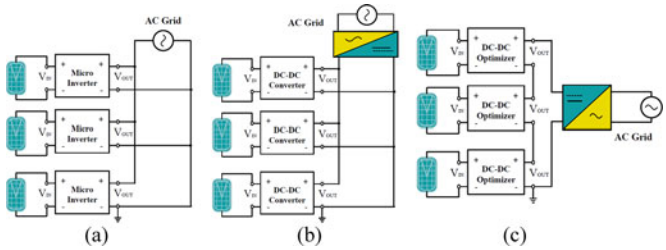


Fig. 1. Three traditional architectures of module level MICs. (a) Microinverter architecture. (b) Parallel dc–dc converter architecture. (c) Cascaded dc–dc (dc–dc optimizer) architecture.

This paper presents a new concept of MIC design called PV balancers. The proposed concept enables independent MPPT for each module, reduces mismatches between different modules, and maximizes the total energy extraction. Compared to the previous solution in Fig. 1(b) and (c), the new concept enables more than 80% reduction in the power rating of an MIC, thus decreasing the manufacturing cost significantly. Even in harsh mismatch conditions, the PV balancer is able to reach the required efficiency and maintain the inverter input voltage. It is anticipated that this approach will reduce the PV converter cost and help reach the eventual goal of $1 per watt for PV systems [7].

Section II of this paper illustrates the concept of PV balancers, introduces two converter architectures based on this concept, addresses the selection of power converters to achieve different architectures, and discusses the advantages and disadvantages of PV balancers. Section III presents the experimental results to verify the concept. The evaluation of the cost and performance of PV balancers as well as two other commercial counterparts are given in Section IV. Section V concludes this paper and introduces future work.

Manuscript received March 28, 2014; revised June 28, 2014; accepted July 10, 2014. Date of publication July 31, 2014; date of current version February 13, 2015. Recommended for publication by Associate Editor K. H. Chen.

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Digital Object Identifier 10.1109/TPEL.2014.2343615

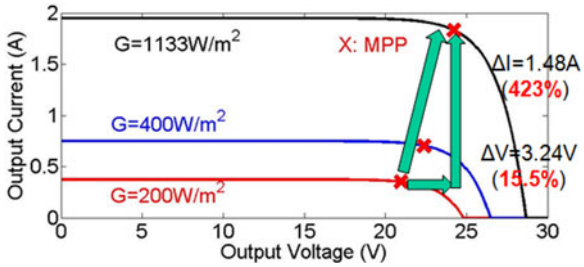


Fig. 2. Solar module *I–V* curves and MPPs.

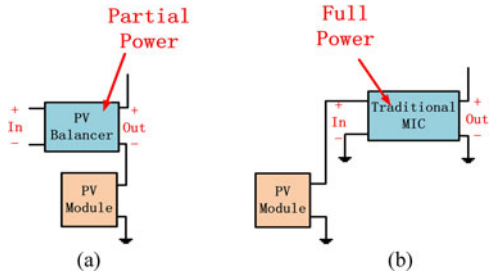


Fig. 3. Comparison of the proposal concept with a traditional MIC. (a) PV balancer. (b) Traditional MIC.

## II. PV Balancers

### A. Concept [8]

The idea of PV balancers comes from observation of *I–V* curves of a solar module shown in Fig. 2. For any given set of operational conditions, modules usually have a single operating point where the values of the output current ($I$) and output voltage ($V$) of a module result in a maximum power output, which is known as the maximum power point (MPP). While the MPP shifts under different solar irradiances, the module output current varies greatly yet the output voltage varies slightly. For instance, Fig. 2 shows that the current varies from 0.35 to 1.83 A from curve $G = 200$ W/m$^2$ (illumination) to curve $G = 1133$ W/m$^2$, and that the voltage only varies from 20.97 to 24.24 V.

This is partly because a solar cell is a p-n junction and its *V–I* characteristics are similar to that of a diode. This observation inspired us to balance the differential voltages between modules instead of using the output voltage of an individual module. Since power = voltage × current, and since the differential voltage is about five times smaller than a single module output voltage, the power rating of an MIC in the new concept is significantly reduced. In Fig. 3, we compare the proposed concept to a traditional MIC.

Fig. 4 shows two possible architectures of PV balancers. PV balancers are essentially dc–dc converters and are integrated into each module and combined into a common dc bus configuration. The dc bus feeds the power to the utility in the inverter stage. The dc bus voltage is higher than the maximum output voltage of PV modules. PV balancers autonomously regulate their output voltage and compensate for the differential voltage between the dc bus and each module. Since the output voltage and output current of each module can be set independently, PV modules operate at their own MPPs, maximizing the energy harvested.

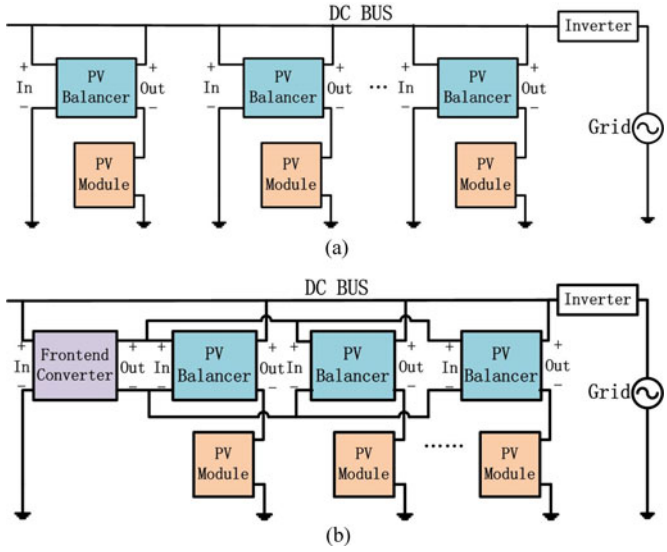


Fig. 4. Two possible architectures of PV balancers. (a) Architecture I of PV balancers. (b) Architecture II of PV balancers.

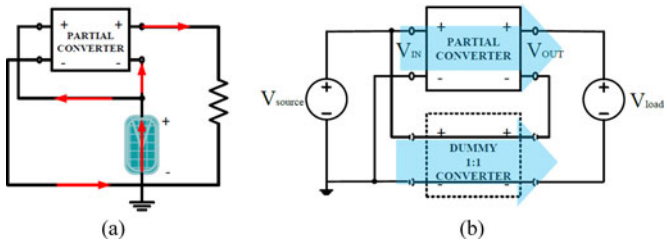


Fig. 5. Typical SCBU topology which is equivalent to an ISOP structure with a dummy bypassed converter. (a) A typical SCBU connection. (b) Equivalent ISOP structure with a dummy bypassed converter.

In Architecture I, the input of PV balancers is from the common dc bus. This architecture is simple and modularized, but the PV balancers have a high-voltage transformation ratio that may incur an extra cost and lower efficiency. In Architecture II, the PV balancers share the front-end converter with the input. The front-end converter steps down the dc bus voltage and feeds relatively low voltage to the PV balancers in each module. This architecture is more economical and efficient. However, the wiring, design, and control are also more complicated.

In [9]–[11], differential currents, rather than voltages are balanced. The PV modules are connected in series and the voltage transformation ratio of the inverter stage is thus reduced. The series-connected boost unit (SCBU) in [12] was derived from the idea of cascading another voltage source on the input. It adds a dc–dc converter to a PV module to reach a series connection, and boosts the output voltage to the load. Fig. 5(a) shows a typical SCBU connection and Fig. 5(b) illustrates SCBU equivalent to an input-series-output-parallel (ISOP) structure with a dummy bypassed converter [13]. The power flow of SCBU is also shown in Fig. 5(b). Because the dummy converter handles

most of power flow and the efficiency of the dummy converter is 100%, the partial power converter only needs to handle a small portion of power flow, the efficiency of the whole system is high, and the merit of processing partial power is obvious.

SCBU also allows a dc/dc converter to handle partial power generated by a PV module, and achieves a low-cost high-efficiency solution for photovoltaic applications. Although the author only applied this concept to a single PV panel, SCBU can be operated in a series connected partial power converter (S-PPC) topology for PV arrays [14]. However, there are still some major differences to identify the idea proposed in this paper from SCBU:

1) First, their circuit connections are not the same. The input of an SCBU is from the PV module connected to it while the input of a PV balancer is from the dc bus. Therefore, the input and the output of a PV balancer can be grounded at the dc bus.
2) Second, their voltage transformation ratios and their input power are different. An SCBU may have a smaller voltage transformation ratio because the output voltage of a PV module is a little lower than the dc bus voltage. But the input power of an SCBU must be received from the PV module connected to it. In comparison, the input power of a PV balancer is from the common dc bus, which is not limited to the PV module connected to it.
3) Third, because the converter in SCBU is connected in series with a PV panel, when either the PV panel or the converter fail, the system fails to deliver power, as it becomes an open circuit, however if using PV balancers, the system can still deliver power because of its parallel configuration.

To understand PV balancers quantitatively, we define $V_{\rm MPP}$ and $I_{\rm MPP}$ as the output voltage and output current of a PV module operating at its maximum power output $P_M$. From the aforementioned definitions, we have

$$P_{\rm MPP} = V_{\rm MPP} I_{\rm MPP}. \tag{1}$$

We define $V_{\rm DC}$ as dc bus voltage, $V_{\rm OUT}$ as the output voltage of a PV balancer, $I_{\rm OUT}$ as the output current of a PV balancer, and $P_{\rm OUT}$ as the output power of a PV balancer. We get

$$V_{\rm OUT} = V_{\rm DC} - V_{\rm MPP}. \tag{2}$$

Because the PV balancer is in series with the PV module at the output, we have

$$I_{\rm OUT} = I_{\rm MPP} \tag{3}$$

$$P_{\rm OUT} = V_{\rm OUT} I_{\rm OUT} = (V_{\rm DC} - V_{\rm MPP}) I_{\rm MPP}. \tag{4}$$

The ratio of the output power of a PV balancer and the output power of a PV module is

$$R_{\rm PwR} = {}^{P_{\rm OUT}}/_{P_{\rm MPP}} = {}^{V_{\rm OUT}}/_{V_{\rm MPP}} = {}^{V_{\rm DC}}/_{V_{\rm MPP}} - 1. \tag{5}$$

As $V_{\rm DC}$ is only a few volts higher than $V_M$, $R_{\rm PWR}$ is usually less than 20%.

We define $P_{\rm LOSS}$ as the power loss of a balancer, $P_{\rm IN}$ as the input power of a balancer and $\eta$ as the efficiency of a PV balancer. We get

$$\eta = \frac{P_{\rm OUT}}{P_{\rm IN}} = 1 - \frac{P_{\rm LOSS}}{P_{\rm OUT} + P_{\rm LOSS}} \approx 1 - \frac{P_{\rm LOSS}}{P_{\rm OUT}}. \tag{6}$$

To compare the efficiency of a PV balancer to a traditional MIC, the power loss of the PV balancer needs to be normalized by the module output power $P_{\rm MPP}$ (which is equal to the input power of the traditional MIC) and the equivalent efficiency of the PV balancer is

$$\eta_E = 1 - \frac{P_{\rm LOSS}}{P_{\rm MPP}} = 1 - R_{\rm PWR} \frac{P_{\rm LOSS}}{P_{\rm OUT}}. \tag{7}$$

As $R_{\rm PWR}$ is usually less than 20%, the equivalent efficiency $\eta_E$ is significantly higher than the PV balancer efficiency $\eta$.

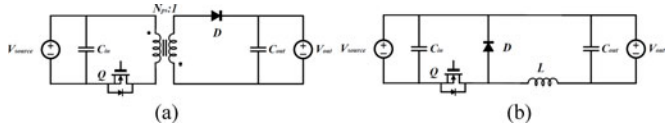


Fig. 6. Implementations of PV balancers. (a) PV balancers in Architecture I and the frontend converter in Architecture II: flyback converter. (b) PV balancers in Architecture II: flipped buck converter. (a) Flyback converter (b) Flipped buck converter.

### *B. Realization*

Many types of power converters are suitable for developing a PV balancer. For the purposes of demonstration, flyback converters are employed as PV balancers in Architecture I as shown in Fig. 6(a). In Architecture II, buck converters are employed as PV balancers for each module as shown in Fig. 6(b) and a flyback converter is employed as the front end as shown in Fig. 6(a). Unlike conventional designs, the outputs of PV balances should be grounded with the common dc bus. So, the buck converter in Fig. 6(b) is flipped from the conventional topology. The dc bus voltage needs to be controlled carefully. If the dc bus voltage is too close to the module output voltage, the voltage transformation ratio of the PV balancer will be too high, although the power rating of the PV balancer will be lower and the equivalent efficiency $\eta_E$ will be low due to high-voltage transformation ratio. If the dc bus voltage is too high, the voltage transformation ratio may be lower but the power rating of the PV balancer would be increased and the equivalent efficiency $\eta_{\rm E}$ will be low due to high $R_{\rm PWR}$.

### *C. Advantages and Disadvantages*

The power rating and power loss of a PV balancer are much smaller than their counterparts shown in Fig. 1. For instance, if the maximum power that a module can produce is 100 W, the dc–dc converters in Fig. 1(b) and (c) should be able to deliver the same maximum power (=100 W). Considering a PV balancer, which compensates up to 20% of the output voltage of a module, the PV balancer thus need to deliver up to $100\ {\rm W} \times 20\% = 20\ {\rm W}$ output power, which is only 1/20 of the maximum power of its counterparts. Assuming both the PV balancer and the traditional MICs can achieve 90% efficiency, the maximum power loss of the PV balancer is up to 2 W,

TABLE I
COMPARISON OF PV BALANCER AND TRADITIONAL MIC

| | PV Balancer | Traditional MIC |
|---|---|---|
| **Power Rating** | 20 W | 100 W |
| **Power Loss** | 2 W | 10 W |
| **Equivalent Efficiency $\eta_E$** | 98% | 90% |

which represents 2% of the maximum output power. In comparison, the maximum power loss of the traditional MIC is up to 10 W, which represents 10% of the maximum output power. Table I summarizes the comparison of power rating and efficiency of a traditional MIC and a PV balancer. Since the size, cost, loss, and other performance aspects of a dc–dc converter is roughly inversely proportional to its power rating, PV balancers will have clear economic advantages over the conventional technology.

PV balancers also achieve an inherent fault tolerance and high reliability. For instance, if a PV module fails, the PV balancer connected to it will disconnect the PV module from the dc bus and there is no adverse influence over other modules. If a PV balancer fails, the output of the PV balancer will be shorted and the PV module connected to it will be reconnected to the dc bus. The PV module can still generate some power though the PV module may not operate at its MPP.

PV balancers may simplify the requirement of energy buffering of a single-phase inverter. In a single-phase inverter system, there is an instantaneous unbalance between the input dc power and the output ac power [1], [5], [15]. An energy buffer is needed to provide reactive power varying at twice the line frequency. Bulky electrolytic capacitors could be used at the inverter input in parallel with PV modules to provide necessary energy buffering, however it will jeopardize the MMPTs of PV modules because of the ripples on the capacitors. Additionally, bulky electrolytic capacitors are not favored in photovoltaic applications because of their low reliability. "Third-port" topologies, which provide the energy storage buffering within an inverter, have been widely investigated [5], [15]. High reliability and small size film capacitors are used in these topologies. However, these topologies need extra switching devices and passive components to achieve the energy buffering and the converter control also becomes complicated. For PV balancers, we could use the input capacitors of the inverter as the energy buffer and let the dc bus voltage contain a ripple resonating at twice the line frequency. As the inverter input is not connected to PV modules directly, there is no coupling between the energy buffer and the MPPTs of PV modules. This approach may simplify the design of energy buffering in a single-phase system.

One of the disadvantages of PV balancers is that they require a high-voltage transformation ratio at the inverter stage. The new transformation ratio is the same as that of a microinverter [4], [5], [15]. Since microinverters have been proved to be highly efficient (>96.5%) and feasible in many studies, this disadvantage is not a fatal flaw of the PV balancer concept. Moreover, the approach presented in this paper may overcome the primary disadvantages of microinverters, e.g., that microinverters have a higher equipment initial cost than a centralized converter, because in this new concept, the number of inverters is reduced and so is ac wiring. Nevertheless, an inverter especially designed for PV balancers will be developed in the future, but that is not within the scope of this paper.

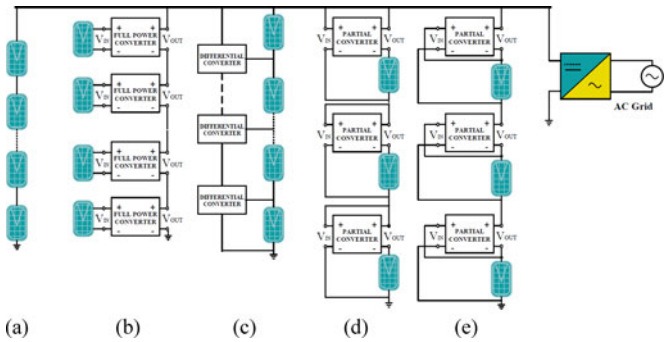


Fig. 7. (a) Traditional PV string. (b) A PV string with cascaded full power dc–dc optimizers. (c) A PV string with differential power converters. (d) A PV string with PV balancers type I. (e) A PV string with PV balancers type II.

Compared to dc–dc converters in Fig. 1(b) and (c), PV balancers may need a larger input and output voltage transformation ratio, which may reduce the efficiency of PV balancers and increase their cost and size. Highly efficient dc–dc converters for the purpose of PV balancers need to be further studied. Compared to microinverters in Fig. 1(a), PV balancers may suffer extra power loss due to low-voltage dc bus. We may estimate the loss as following. Assuming the output power of a PV module is 100 W and the output current is 5 A. If the dc cable is made by the AWG wire size of 5, which has a diameter of 5 mm and a dc resistance of 1.0 mΩ/m, the power loss on the cable will be 0.025 W/m, which is about 0.025% efficiency loss. The loss is insignificant when the number of PV modules is small and the dc bus is short but it may be significant when the number of modules is large and the dc bus is long. Microinverters in Fig. 7(a) mitigate this problem because the output power of PV modules is combined at the ac line which has a higher voltage and less current than the low-voltage dc bus of PV balancers. The dc bus loss of PV balancers could be reduced with a larger gauge of copper wire, but it will incur the extra cost of copper. In high-power photovoltaic applications having a large number of PV modules, the PV balancers could be integrated into string levels instead of into PV modules as shown in Fig. 7(d) and (e) [13]. Compared to the traditional structure in Fig. 7(a), this approach will enable an independent MPPT on each module in the string, minimize the associated dc bus loss and reduce the transformation ratio of the inverter stage. These PV balancers in a PV string share the merits of cascaded dc–dc optimizers as shown in Fig. 7(b) and handles differential solar power similar to the differential power converters in Fig. 7(c) [15].

TABLE II
PV MODULE SPECIFICATIONS

| PV | $^*V_{OC}$ (V) | $^*I_{SC}$ (A) | $V_{MPP}$ (V) | $I_{MPP}$ (A) | $P_{MPP}$ (W) | Illumination (W/m$^2$) |
|---|---|---|---|---|---|---|
| **1** | 24.80 | 0.375 | 20.97 | 0.35 | 7.38 | 200 (1/5 Full) |
| **2** | 26.47 | 0.75 | 22.38 | 0.70 | 15.75 | 400 (2/5 Full) |
| **3** | 28.67 | 1.95 | 24.24 | 1.83 | 44.35 | 1040 (Full) |

$^*I_{SC}$ is the short circuit current and $V_{OC}$ is the open circuit of a PV module.

TABLE III
SPECIFICATIONS OF POWER CONVERTERS

| | | Input Voltage | Output Voltage | Output Current | Output Power |
|---|---|---|---|---|---|
| Flyback in Architecture I | 1 | 28 V | 7.03 V | 0.35 A | 2.48 W |
| | 2 | 28 V | 5.63 V | 0.70 A | 3.96 W |
| | 3 | 28 V | 3.77 V | 1.83 A | 6.89 W |
| Frontend Flyback in Architecture II | | 28 V | 10 V | 1.33 A | 13.32 W |
| Buck in Architecture II | 1 | 10 V | 7.03 V | 0.35 A | 2.48 W |
| | 2 | 10 V | 5.63 V | 0.70 A | 3.96 W |
| | 3 | 10 V | 3.77 V | 1.83 A | 6.89 W |

TABLE IV
COMPARISON OF THE TOTAL POWER RATINGS FOR DIFFERENT TOPOLOGIES IN FIG. 1

| | DC/DC Converter | | DC/AC Inverter | |
|---|---|---|---|---|
| | **Rating (W)** | **Number** | **Rating(W)** | **Number** |
| **MIC (a)** | N/A | 0 | 45 | 3 |
| **MIC (b)** | 45 | 3 | 135 | 1 |
| **MIC (c)** | 45 | 3 | 135 | 1 |
| **Balancer I** | 7 (Flyback) | 3 | 135 | 1 |
| **Balancer II** | 7 (Buck) | 3 | 135 | 1 |
| | 21 (Flyback) | 1 | | |

## III. MEASUREMENT SETUP AND EXPERIMENTAL RESULTS

### A. System Specifications

Three PV modules are modeled under different irradiances, and Table II shows their electrical specifications. The dc bus voltage is set at 28 V for both architectures to balance the power rating and transformation ratio of the PV balancers. The output voltage of the frontend converter in Architecture II is set at 10 V, which is higher than the output voltages of buck converters. Table III shows the values of power converters for both architectures under three different solar irradiances. Table IV as well as Fig. 8 present the power ratings of converters and inverters for different topologies as shown in Fig. 1 as well as PV balancers as shown in Fig. 4.

Fig. 8 illustrates PV balancers in the last two columns have much less power ratings than converters used in MICs shown in Fig. 1. Other pros and cons between the traditional MICs and PV balancers have already been discussed in the last section.

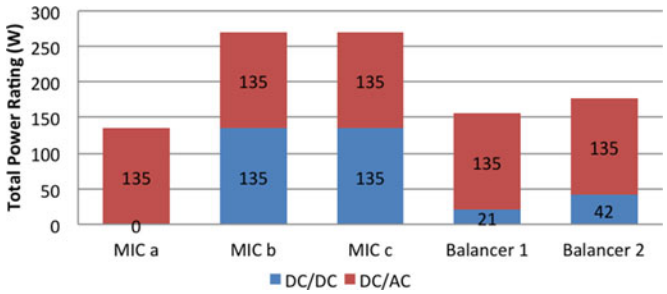


Fig. 8. Comparison of total power rating of converters/inverters for different topologies in Fig. 1.

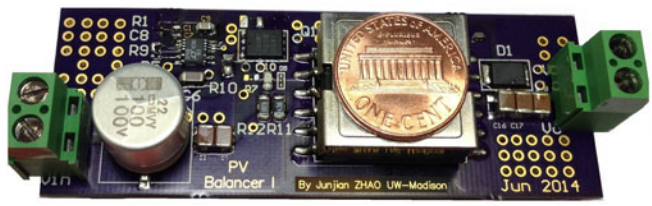


Fig. 9. Flyback-converter prototype in Architecture I and II.

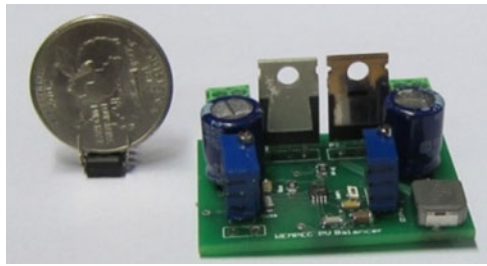

Fig. 10. Buck-converter prototype in Architecture II.

### B. Experimental Setup

This subsection presents the measurement setup and experimental results obtained from the proposed PV balancers on PV modules. In order to demonstrate the proposed two architectures of PV balancers, four flyback-converter prototypes and three buck-converter prototypes were designed and fabricated as PV balancers and were connected to the corresponding PV modules with the specified operating points as shown in Table II. Due to limited space, this paper only presents and analyzes the efficiency for the first architecture. The results for the second architecture are similar.

Fig. 9 shows the flyback converter prototype used for both architectures. Fig. 10 shows the buck converter prototype used in Architecture II. Each flyback converter is designed for a voltage conversion ratio of 3.5 at $D = 0.5$, with a transformer having the primary-to-secondary turns ratio of 3.5:1. LT3748 IC was selected and the remaining design parameters are given in Table III and the details of devices are shown in Table VI.

A systematic hardware block diagram with PV panels connected with PV balancers in Architecture I is shown in Fig. 11. The experimental setup is presented in Fig. 12. Experiments

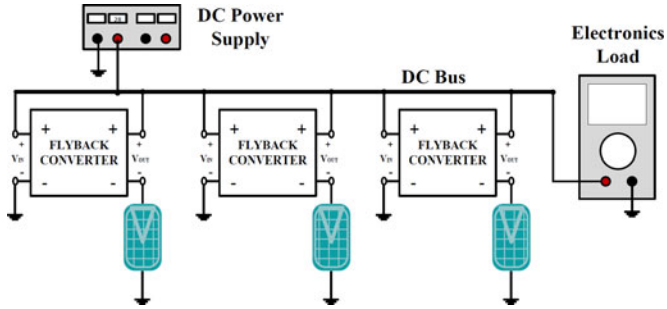


Fig. 11. Block diagram illustrating the experimental setup of Architecture I.

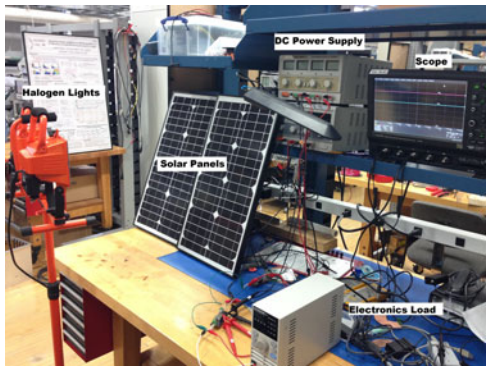


Fig. 12. Experimental setup with PV modules connected with PV Balancers.

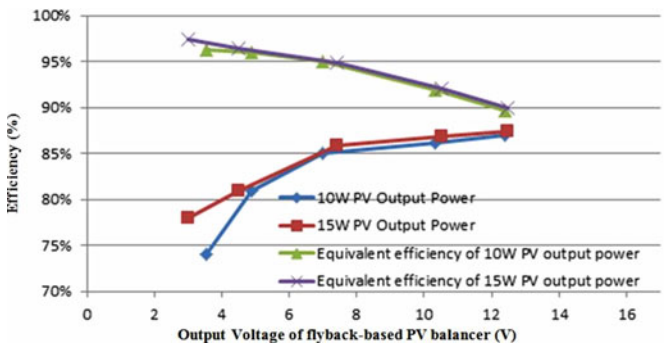


Fig. 13. Efficiency measurements of the flyback converter and the equivalent efficiency in Architecture I under different output power and output voltages of a PV module with a fixed input voltage of 28 V.

were carried out in lab instead of an outdoor field. Ultraviolet filters were applied on halogen lights to emulate various solar irradiation levels. Uniform irradiation on a single PV module was guaranteed and the mismatches of submodules were negligible. The output of each module was connected to a common dc bus via a PV balancer; the dc bus voltage was hold at 28 V by a dc power supply. The output power of PV panels was delivered to an electronic load.

### C. Experimental Results

Fig. 13 shows the efficiency of a PV balancer for different output voltages with a fixed input voltage of 28 V. The efficiency curves under different output power of the PV module are similar with a peak value around 88%. Although the efficiency of a single converter is not as high as commercial converters available on market, the equivalent efficiency still remains high due to the merit of handling partial power.

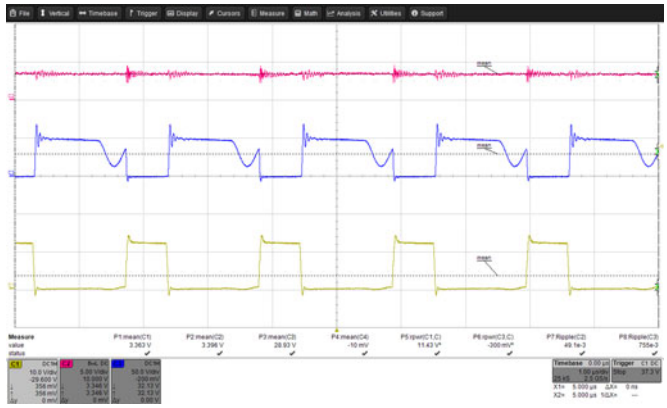

Fig. 14. Gating signal (yellow), drain-to-source voltage of MOSFET (blue) and output voltage (magenta) of the flyback converter in Architecture I.

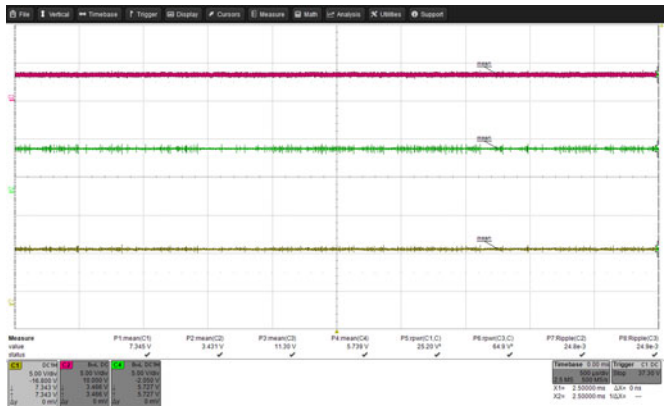

Fig. 15. Experimental results of the output voltages of three PV balancers in Architecture I.

The waveforms of the gating signal, the drain-to-source voltage of MOSFET, and the output voltage of the converter for a duty cycle $D = 0.33$, are shown in Fig. 14. The switching period $T_s$ is 1.9 s. It should be noted that the flyback converter worked under a discontinue conduction mode, and experienced a less-than-half-cycle resonance which has been studied in [16]. However, since the priority of this study is not optimizing the control of flyback converter, the valley switching technique proposed in [16] is not adopted in this paper. Fig. 15 shows the output voltages of three PV balancers in Architecture I with specifications shown in Table III.

## IV. Performance and Cost Evaluation

The previous section illustrates the improvements in the overall equivalent efficiency that can be realized with the use of PV balancer architectures and the hardware implemented as a demonstration. Moreover, because the solar industry is very sensitive to cost, it would be better if an analysis is performed to quantify the cost benefits and tradeoffs.

TABLE V
COMPARISONS OF EFFICIENCIES FOR EVMS AND PV BALANCERS IN ARCHITECTURE I [17], [18]

| | LM5122EVM-1PH | | TPS43060EVM -199 | | PV Balancer I (Flyback Topology) | |
|---|---|---|---|---|---|---|
| **Converter V in** | 20 V | | 24 V | | 28 V | |
| **Converter V out** | 28 V | | 40 V | | 7.03 V | |
| | | | | | 5.63 V | |
| | | | | | 3.77 V | |
| **DC Bus Voltage** | 28 V | | 40 V | | 28 V | |
| **Converter Input Power** | 7.65 W | 91% | 7.64 W | 89% | 3.54 W | 88.9% |
| **Total Efficiency** | 15.32 W | 94% | 15.91 W | 93% | 4.95 W | 93.7% |
| | 44.54 W | 97% | 44.90 W | 98% | 8.11 W | 97.3% |
| **Dimensions** | 5114 $mm^2$ | | 4471 $mm^2$ | | 2903 $mm^2$ | |

TABLE VI
COMPARISON OF EFFICIENCIES FOR EVMS AND PV BALANCERS

| | | PV Balancer I (Flyback) | PV Balancer II | |
|---|---|---|---|---|
| | | | **Flyback** | **Buck** |
| **MOS FET** | **Part Number** | FDT86106LZ | FDT86106LZ | DMG1012 UW-7 |
| | **Voltage Rating** | 100 V | 100 V | 20 V |
| | **Current Rating** | 3.8 A | 3.8 A | 1 A |
| | **Number** | 1 | 1 | 1 |
| | **Price*** | $0.47 | $0.47 | $0.079 |
| **Diode** | **Part Number** | SK310A-TP | SK310A-TP | BYS10-25-E3/TR3 |
| | **Voltage Rating** | 100 V | 100 V | 25 V |
| | **Current Rating** | 3 A | 3 A | 1.5 A |
| | **Number** | 1 | 1 | 1 |
| | **Price*** | $0.10 | $0.10 | $0.087 |
| **Inductors/ Transformers** | **Part Number** | WURTH 750311607 | WURTH 750311607 | M8717 |
| | **Inductance** | N/A | NA | 50 uH |
| | **Current Rating** | 9.5 A | 9.5 A | 9.5 A |
| | **Price*** | $11 | $11 | $0.374 |
| | **No.** | 1 | 1 | 1 |
| **Tot. Price/Panel** | | $11.57 | $11.57 | $0.54 |
| **Tot. Price** | | $34.71 | $13.19 | |
| | | **LM5122EVM-1PH** | **TPS43060EVM-199** | |
| **MOS FET** | **Part Number** | PSMN4R0-40YS | BSC123N08NS3G | |
| | **Voltage Rating** | 40 V | 80 V | |
| | **Current Rating** | 100 A | 55 A | |
| | **Number** | 2 | 2 | |
| | **Price*** | $0.39 | $0.49 | |
| **Diode** | **Part Number** | N?A | N?A | |
| | **Voltage Rating** | N/A | N/A | |
| | **Current Rating** | N/A | N/A | |
| | **Number** | N/A | N/A | |
| | **Price*** | N/A | N/A | |
| **Inductor/ Transformer** | **Part Number** | WURTH 74435561100 | WURTH 74435571500 | |
| | **Inductance** | 10 uH | 15 uH | |
| | **Current Rating** | 15 A | 14 A | |
| | **Price*** | $5.18 | $5.32 | |
| | **No.** | 1 | 1 | |
| **Tot. Price/Panel** | | $5.96 | $6.3 | |
| **Tot. Price** | | $17.88 | $18.9 | |

*All the prices are based on quote for one piece at a price break of 5000 from Digikey.

There are some commercial dc–dc converter evaluation modules (EVMs) which have similar electric specifications for the PV panels mimicked in the lab. These EVMs are full power converters compared to partial power converters as PV balancers. Tables V and VI compare the efficiency and raw cost of these EVMs and balancers, respectively.

The efficiency of PV balancers for Architecture I is approximately 75–85% depending on the output voltage. The equivalent efficiency of PV balancers $\eta_E$ is about 89–97% calculated by (7). Although the efficiency of this first prototype is closed to the efficiencies of these commercial dc–dc converters with similar input/output voltages and an efficiency of more than 89%, PV balancer's power rating is about 20% of the commercial EVMs. Table VI shows the raw costs of the EVMs and balancers which only include switches, inductors, and transformers, since they are the major cost for the converters. Compare to the full power

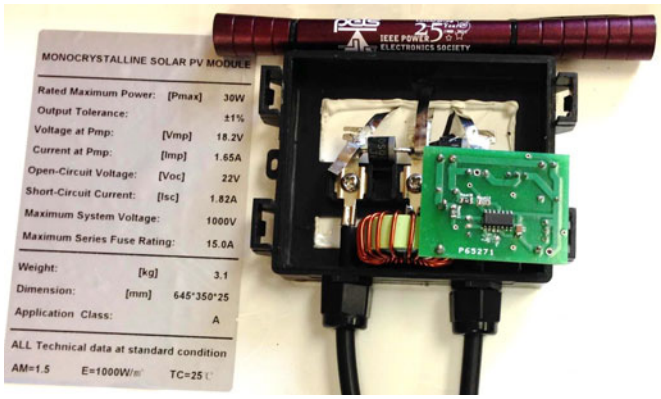


Fig. 16. Photograph showing the PV balancer fit in a solar panel junction box with a pen shown for size comparison. The bypass diode is also visible.

EVMs, Architecture I has more initial cost because transformers are used in flyback converters for each panel; while Architecture II has much less raw cost, since there is only one flyback as the frontend converter with less transformation ratio and buck converters as PV balancers. Moreover, the cost can be further reduced by an optimized design in the future.

These comparison results demonstrate the potential advantages of PV balancers. Partial power processing enables a low-cost design for PV applications. The priority of this paper is to demonstrate the new concept, maximizing power density, efficiency, and cost was not the focus in our first-pass design. Diode rectifiers and less optimized transformer may be responsible for the low efficiency, and the overdesign of PCB increases the raw cost of PV balancers. High efficiency with moderate-designed dc–dc converters for the purposes of the PV balancer concept may be developed in the future. It is also possible to integrate a PV balancer in the junction box of a commercial solar panel for high-volume, low-cost production as shown in Fig. 16.

## V. Conclusion and Future Work

A new concept of MICs called PV balancers has been proposed and verified in this paper. The proposed concept enables independent maximum power point tracking (MPPT) for each module, increases inherent fault tolerances for the whole system, and dramatically decreases the electrical requirements and cost for power converters with only handling partial power of the PV panel, it has a significant economic value for photovoltaic system in the future. Hardware testing results with real PV panel followed by balancers has demonstrated the potential merits mentioned previously. This study has only compared the efficiency and cost between PV balancers and full power converters which have similar electrical specifications of the PV panels available on the market, a more thorough research and comparison between real MIC and PV balancer applied in a field solar system need to be carried out in the future. Moreover, different topologies such as resonant converters need to be investigated to further minimize the cost and size of PV balancers. Future work will also include power converter optimization, dc bus voltage control, and developing a highly efficient inverter for PV balancers.

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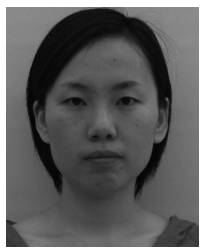

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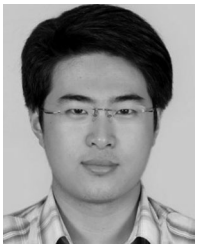

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