ON/OFF Control of a Modular DC–DC Converter Based on Active-Clamp *LLC* Modules

Hien Nguyen, *Member, IEEE*, Regan Zane, *Senior Member, IEEE*, and Dragan Maksimović, *Senior Member, IEEE*

***Abstract*—This paper studies ON/OFF control of a dc–dc system that contains multiple active-clamp *LLC* resonant modules operating in parallel. The architecture and the ON/OFF control method yield high overall efficiency and fast transient responses. Two converter models are introduced: 1) a high-frequency model to determine a gate timing sequence that enables fast ON/OFF control, and 2) an averaged model to assist in the system control loop design. The models and the ON/OFF control method are verified by experiments on a prototype consisting of two 1-MHz, 24–3.3-V, 5-W active-clamp *LLC* modules. The performance of PI and PID system controllers is compared, and capacitor size is analyzed by simulations on systems containing up to 20 modules.**

I. Introduction

In point-of-load (POL) applications, multiphase buck-based converters are widely used to meet the high-current low-voltage load demand, and to improve transient performance and efficiency over wide load range [1]–[6]. The number of phases can be changed dynamically to improve light-load efficiency further [7]. In radio-frequency dc–dc power conversion applications, the approach of turning the number of modules (or phases) ON or OFF has been proposed not only to improve the light-load efficiency but also to facilitate the output voltage regulation [8]. This cell-modulation-regulated approach is illustrated in Fig. 1. Each module in the system is designed to operate at one operating point at its highest efficiency. In order to provide the required output power and to regulate the output voltage, the controller fully turns on a certain number of modules, while fine control is accomplished by turning one module ON or OFF in a pulse-width-modulated (PWM) manner. Such a control method requires the converter modules to have quick turn-ON/OFF feature and relatively high output impedance. This architecture has been verified by experiments using hysteretic control of one module [8]–[14]. Fixed-frequency PWM with hysteretic override on one module is introduced by Hu *et al.* [15]. The approach is to derive a first-order plant transfer function of the converter and design a PI controller, using the PWM ON/OFF duty cycle as the control variable. However, this method is implemented on only one module, while extensions to multiple parallel modules have not been addressed. A sigma-delta modulator is suggested for multiple-module system control [8], but is not studied in detail.

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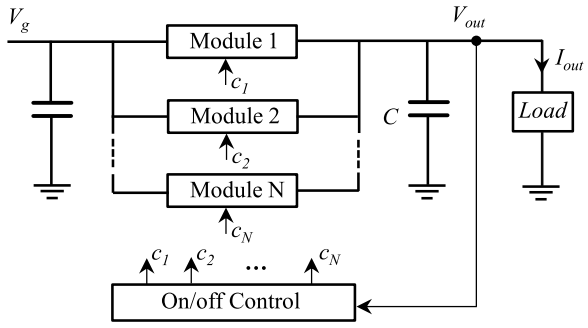


Fig. 1. Cell-modulation-regulated architecture.

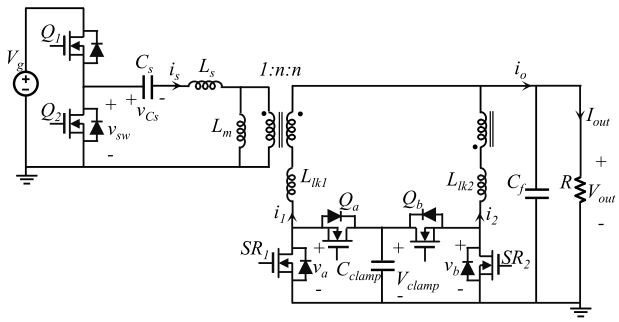


Fig. 2. Active-clamp *LLC* resonant converter.

A similar approach has been pursued in POL applications where an interleaved multiphase buck converter is treated as a multilevel power analog-to-digital converter (ADC) [16]–[18]. In this case, each buck phase is equivalent to a voltage source in series with a low output impedance, leading to a second-order control-to-output transfer function of the system. However, the buck converter has limitations in large-step-down, high-current, and high-frequency applications because of the low duty cycle and high switching losses. In order to address these limitations, an active-clamp *LLC* resonant converter shown in Fig. 2 has been proposed [19], [20]. In this converter, all devices operate at nearly 50% duty cycle, and switching losses are reduced significantly due to soft-switching operation. The active-clamp circuitry suppresses the voltage oscillation across the rectifier devices, caused by transformer's secondary-side leakage inductance and MOSFET drain-to-source capacitances. This modification provides an opportunity to integrate secondary-side MOSFETs and control circuitry in a low-voltage CMOS process. Moreover, the converter has high output impedance

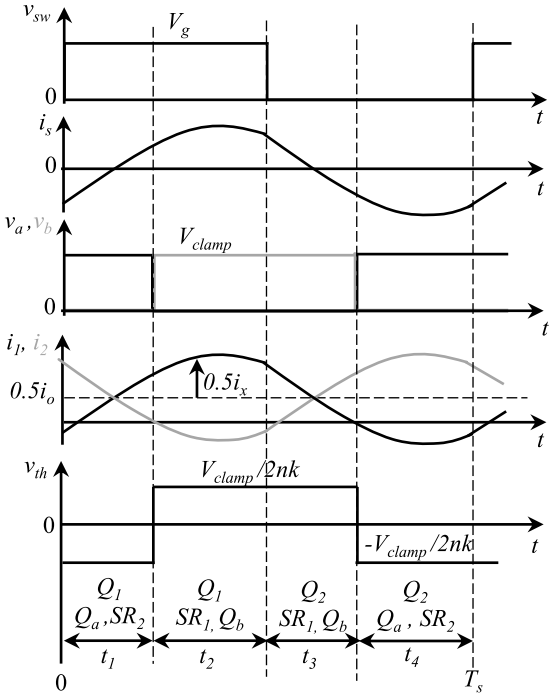


Fig. 3. Typical waveforms of active-clamp *LLC* converter in one switching cycle. Note that $k = 1 + \frac{L_{lk}/2n^2}{L_m}$.

(i.e., can be approximated as a constant current source), which makes it suitable for the multiple-parallel-module architecture presented in [8]. Note that adding an active-clamp circuit is not the only solution to suppress the oscillation voltage in an *LLC* converter. Another possible option is to increase the resonant inductance L_s [21]. In a large-voltage-step-down high-switching-frequency application, L_s becomes smaller, and a small transformer turn ratio may limit how much larger L_s can be increased.

This paper presents an ON/OFF control in the multiple-parallel-module architecture, using the active-clamp *LLC* resonant converter as the module topology [19]. Section II describes briefly the active-clamp *LLC* converter's operation. Section III gives an overview of converter modeling. Section IV describes system modeling, ON/OFF controller design, and implementations for two types of systems: hysteretic control for one module, and standard PI or PID compensator followed by hysteretic quantizer for a multiple module system. Section V presents simulation and experimental results using multiple 1-MHz, 24–3.3-V, 5-W module prototypes. Section VI discusses the output capacitor size of the proposed ON/OFF-controlled multimodule system and considers between hysteresis and fixed frequency ON/OFF control. Conclusions are given in Section VII.

II. Operation of Active-Clamp *LLC* Converter

Fig. 3 shows the waveforms of input switching node voltage $v_{\rm sw}$, primary-side current i_s, voltages across rectifier devices v_a and v_b, secondary-side currents i_1 and i_2, and Thevenin

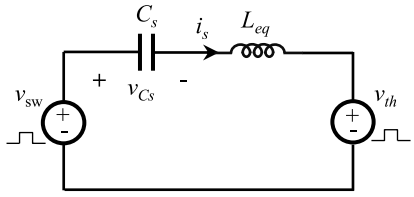


Fig. 4. High-frequency model of an active clamp *LLC* converter.

equivalent voltage $v_{\rm th}$, which is introduced in Section III. Three pairs of switches (Q_1, Q_2), (SR_1, Q_a), and (SR_2, Q_b) are controlled by complementary gate drive signals with dead times. The figure also includes the list of conducting devices during each subinterval t_1, t_2, t_3, and t_4. The subintervals can be calculated offline using the high-frequency model presented in Section III-A.

In steady state, $t_1 = t_3$, $t_2 = t_4 = T_s/2 - t_1$, and all devices are switched at almost 50% duty cycle. During the first subinterval, Q_1, SR_2, and Q_a are ON and capacitor $C_{\rm clamp}$ clamps v_a at twice the output voltage $V_{\rm out}$. This subinterval ends at t_1, when SR_2 is turned OFF at zero current, along with Q_a turning OFF as well as Q_b and SR_1 turning ON. During the second subinterval, voltage v_b across SR_2 is clamped at $2V_{\rm out}$. This subinterval ends at $T_s/2$ when Q_1 is OFF and Q_2 is turned ON at zero-voltage switching, assuming the resonant tank elements are designed for the desired above-resonance operation. The two remaining subintervals are similar to the first two. As opposed to the standard *LLC* converter, when SR_2 or SR_1 is turned OFF, the energy stored in each secondary-side leakage inductance is not dissipated through oscillation but is recycled by the clamp circuitry. In addition, since both secondary sides conduct currents continuously at 180° phase shift, there is significantly less current ripple on the output capacitor.

III. Converter Modeling

The ON/OFF control of the active-clamp *LLC* resonant converter requires two types of models. The first one is a high-frequency model including details of the four subintervals in a switching cycle. The second one is an averaged model for the output current, as well as the output and clamp voltages. From this averaged model, the multiple-parallel-module dc–dc system model can be derived, leading to a system compensator design approach.

A. High-Frequency Model

According to [20], an active-clamp *LLC* converter can be modeled as an equivalent *LC* circuit shown in Fig. 4, where

$$L_{\rm eq} = L_s + \left[(L_{lk}/2n^2)//(L_m)\right]. \tag{1}$$

The voltage $v_{\rm th}$ is defined as

$$v_{\rm th} = (v_b - v_a)/(2nk) \tag{2}$$

where the parameter k is

$$k = 1 + \frac{L_{lk}/2n^2}{L_m}. \tag{3}$$

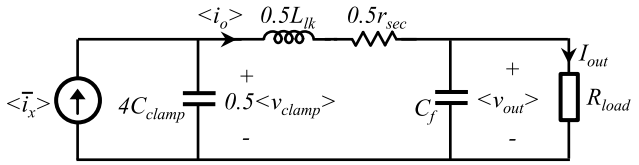


Fig. 5. Averaged model of an active clamp *LLC* converter.

The voltage v_{sw} and $v_{\rm th}$ waveforms can be found in Fig. 3. In order to study the relationship between primary-side current i_s and the current i_x transferred to the secondary sides, another equation is required

$$\frac{di_s}{dt} = nk\frac{di_x}{dt} + k\frac{v_{\rm th}}{L_m}. \tag{4}$$

Note that the current i_x is a component of secondary-side currents: $i_1 = 0.5(i_o + i_x)$ and $i_2 = 0.5(i_o - i_x)$, where i_o is the unfiltered output current. State-plane analysis is used to determine the subinterval lengths t_1, t_2, t_3, and t_4 in steady state, in order to obtain zero-current switching on the secondary-side devices, and to calculate a turn-on timing sequence to reach steady state within the first switching cycle [20].

B. Averaged Model

By averaging unfiltered output current i_o, output voltage $v_{\rm out}$, and clamp voltage $v_{\rm clamp}$ over T_s, the averaged model shown in Fig. 5 is derived from a set of equations

$$C_f\frac{d\langle v_o(t)\rangle}{dt} = \langle i_o(t)\rangle - I_{\rm out} \tag{5a}$$

$$C_{\rm clamp}\frac{d\langle v_{\rm clamp}(t)\rangle}{dt} = 0.5\left[\langle \bar{i}_x(t)\rangle - \langle i_o(t)\rangle\right] \tag{5b}$$

$$L_{lk}\frac{d\langle i_o(t)\rangle}{dt} = \langle v_{\rm clamp}(t)\rangle - 2\langle v_{\rm out}(t)\rangle - r_{\rm sec}\langle i_o(t)\rangle \tag{5c}$$

where the averaged variable $\langle \bar{i}_x\rangle$ is defined as

$$\langle \bar{i}_x(t)\rangle = \frac{1}{T_s}\left(-\int_{t_1,t_4} i_x(t)dt + \int_{t_2,t_3} i_x(t)dt\right) \tag{6}$$

and $r_{\rm sec}$ is the total parasitic resistance on one secondary side. A simpler averaged model based on this derivation is presented and verified in Section IV-B.

IV. Controller Design and Implementation for Multiple-Parallel-Module DC–DC System

The hysteretic control of one module is introduced in Section IV-A. In order to facilitate multimodule system modeling and simulation, a simplified averaged model is suggested in Section IV-B. After the system's control-to-output transfer function is derived from the simplified averaged model, the controller design and implementation are presented in Section IV-C.

TABLE I
Prototype Components List

	Prototype 1	Prototype 2
Q_1, Q_2	CSD17313Q2	
$SR_{1,2}, Q_{a,b}$	CSD16301Q2	
Gate drivers	EL7104	
n	0.4	
C_s (nF)	11.6	15.52
L_s (μH)	3.14	3.60
L_m (μH)	6.90	6.90
L_{lk} (nH)	320	30
Magnetic core	0L42020UG	CL41805EC
ADC for $v_{\rm out}$	THS1030	THS1215
ADC for v_{sw}	AD9280	

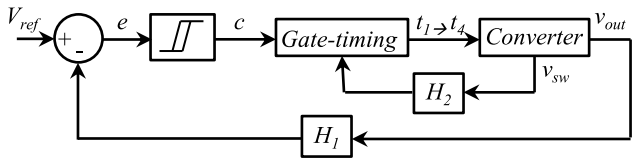
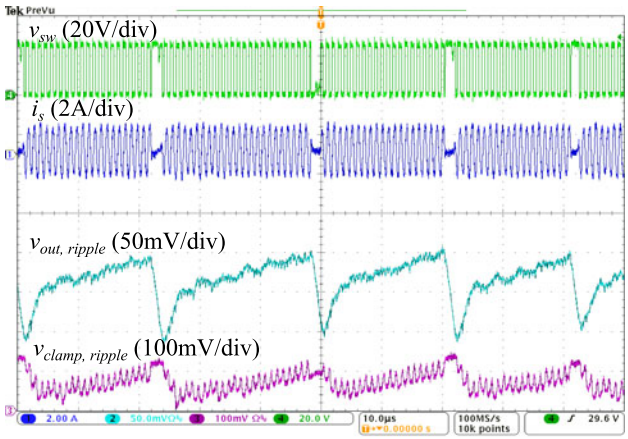


Fig. 6. Hysteretic control diagram for one module.

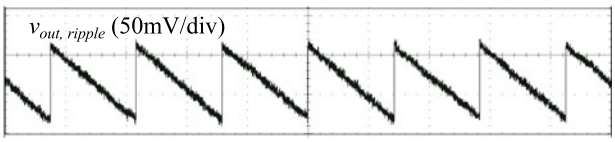
A. Hysteretic Control of One Module

A 1-MHz, 24–3.3-V, 5.5-W experimental prototype (prototype 1) is built to evaluate hysteretic ON/OFF control of one module. Table I lists the resonant tank values and device part numbers. The clamp and output capacitors are 8.8 and 47 μF, respectively. In the control loop diagram (see Fig. 6), the hysteresis band is chosen to be $\pm$50 mV. The gate-timing block is implemented as follows: at the rising edge of control signal c, the gate-timing block reads the initial value of v_{C_s} and uses a six-row lookup table to determine the turn-on timing sequence that brings the converter to steady-state operation within the first switching cycle; after that, steady-state timing is used. The lookup table is created using state-plane analysis of the high-frequency model in Fig. 4 [20]. The turn-on timing is more accurate when the lookup table contains more rows, but at the expense of a longer processing time. The initial v_{C_s} can be obtained easily by sensing voltage $v_{\rm sw}$ across the input switching node. When the converter is OFF, the low-voltage oscillation across rectifier devices is reflected to the primary side and causes ringing at $v_{\rm sw}$ with a frequency of approximately 2.3 MHz. Therefore, a low-pass filter is required in order to sense the correct initial value of v_{C_s}.

Fig. 7(a) shows experimental waveforms of switching node voltage $v_{\rm sw}$, primary-side current i_s, output voltage ripple $v_{\rm out,ripple}$, and clamp voltage ripple $v_{\rm clamp,ripple}$ at 90% load (or 1.5 A). It can be seen that i_s comes close to steady state in less than 1 μs. Output voltage varies from 3.25 to 3.35 V at 45-kHz ON/OFF PWM frequency. At mid-range load currents, the PWM frequency can reach up to 130 kHz. The controller is able to regulate the output voltage at no load as shown in Fig. 7(b). The converter's efficiency is recorded at various loads and is shown in Fig. 8. Compared to fixed-frequency PWM, the hysteretic controller reduces the PWM ON/OFF frequency at



(a) 10μs /horizontal div



(b) 10ms /horizontal div

Fig. 7. Experimental results for hysteretic control of one module at (a) 90% load and (b) no load.

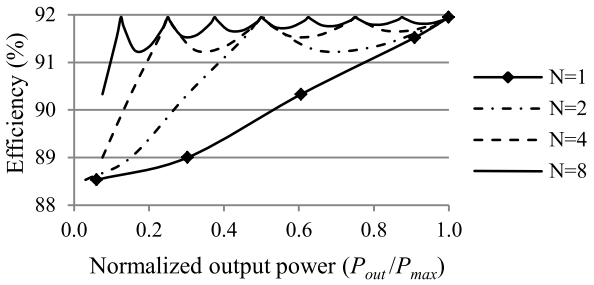


Fig. 8. Efficiency at various loads of one module (experimental) and multiple-module systems (projected).

light load, which helps improve the light-load efficiency. As an example, the efficiency at 10% load is 85% if a fixed 100-kHz ON/OFF frequency is implemented, whereas the efficiency is close to 89% by using hysteretic ON/OFF control. Predicted overall efficiency of a system containing up to eight modules is also shown in Fig. 8, based on the fact that in a system's steady state, at most one module is operating in the ON/OFF PWM mode, while the others are either fully ON or OFF. It is seen that systems of eight or more modules perform at efficiency higher than 90% over a wide load range.

B. Simplified Averaged Model

The averaged model in Fig. 5 is a third-order system with damping resistance equal to $0.5r_{\rm sec}$. Based on the observation from experiments that the output voltage is well damped, the leakage inductance in the averaged model can be omitted. Additionally, since $\langle \bar{i}_x(t) \rangle$ can quickly reach its steady state I_o (maximum supply current of the converter), the output is

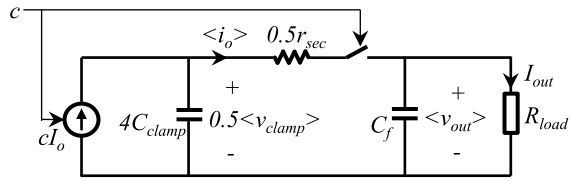


Fig. 9. Simple averaged models of one module for simulation.

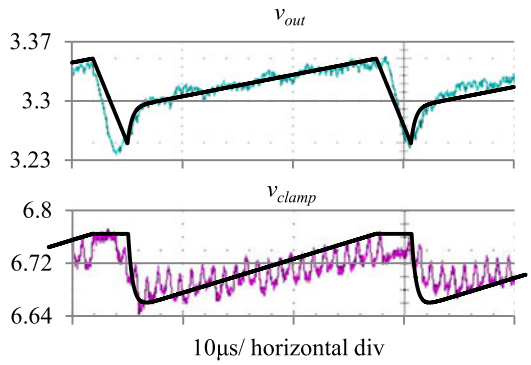


Fig. 10. Output and clamp voltage waveforms from experiment (in gray), and simulation of simple averaged model (in black). The results are both obtained on the same conditions: ±50 mV hysteresis band and 90% load.

approximated as a constant current source controlled by the ON/OFF control signal c. Based on these assumptions, a simpler model (see Fig. 9) is then obtained and verified by experiments. Fig. 10 shows an example of how the simple model predicts $v_{\rm out}$ and $v_{\rm clamp}$ similar to the experimental results. The waveforms are obtained for the same conditions: ±50 mV hysteresis band and 90% load. The model explains why there is a fast ramp up at the output voltage right after the converter is turned ON. During the converter's off-time, the clamp capacitor is disconnected from the circuit and its voltage stays at approximately twice the programmed maximum output voltage. That means the voltage across $4C_{\rm clamp}$ in the model stays at the maximum value $V_{\rm ref} + \Delta V_{\rm ripple}$. On the other hand, the output capacitor C_f is discharged until it reaches the programmed minimum value $V_{\rm ref} - \Delta V_{\rm ripple}$. Therefore, when the converter is turned ON again, C_f is first charged by both $4C_{\rm clamp}$ and the current source I_o. When the two capacitors reach an equilibrium voltage, they are both charged by I_o. Given the output voltage ripple of $\pm\Delta V_{\rm ripple}$, a helpful approximation for PWM ON/OFF frequency is

$$f_{\rm pwm} = M_i(1 - M_i)\left(\frac{I_o}{2C_f \Delta V_{\rm ripple}}\right) \tag{7}$$

where $M_i = I_{\rm out}/I_o$. The maximum PWM frequency happens at load current equal to $I_o/2$

$$f_{\rm pwm,max} = \frac{I_o}{8C_f \Delta v_{\rm out}}. \tag{8}$$

When there are multiple parallel modules in the system, the schematic is shown in Fig. 11. The simulation model is set up as shown in Fig. 12(a). Because all modules share the same clamp and output capacitors, the fast ramp up at $v_{\rm out}$ does not happen

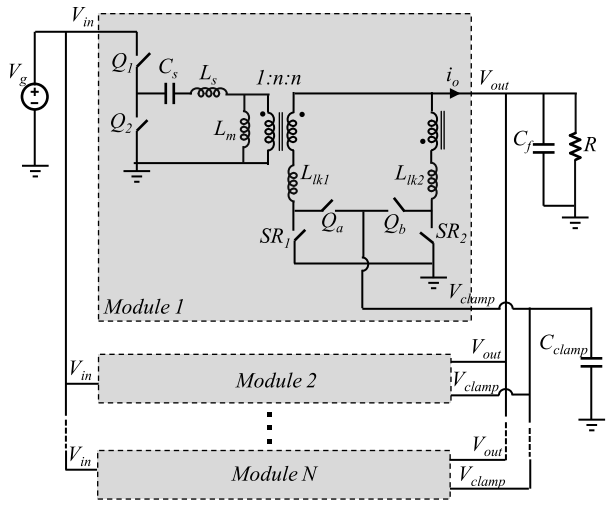


Fig. 11. Schematic of *N*-module active-clamp *LLC* converter.

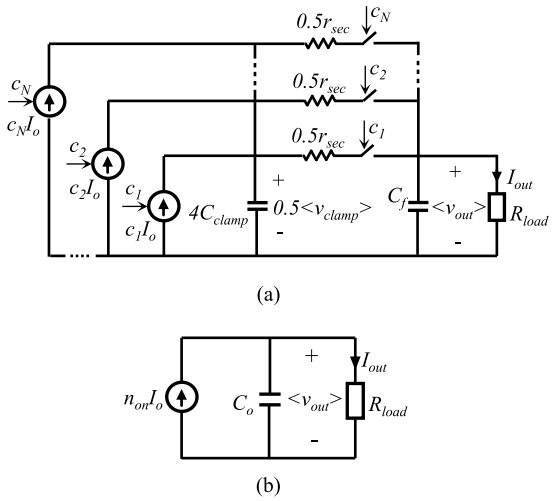


Fig. 12. Simple averaged models of *N*-module system: (a) for simulation and (b) for compensator design.

as long as there is at least one module fully ON, or $4C_{\rm clamp}$ is always connected to C_f. Based on this simple averaged model, an ideal first-order model for an *N*-module system is derived and shown in Fig. 12(b), where $C_o = C_f + 4C_{\rm clamp}$. The control variable for this system is the number $n_{\rm on}$ of ON modules. The control-to-output transfer function, from $n_{\rm on}$ to the output voltage $v_{\rm out}$ is found

$$G_{vn}(s) = \frac{I_o R_{\rm load}}{1 + \frac{s}{1/(C_o R_{\rm load})}} = \frac{G_{vn0}}{1 + \frac{s}{2\pi f_{vn0}}}. \tag{9}$$

As discussed earlier, at light load when $n_{\rm on} \le 1$, (9) is only an approximation because $4C_{\rm clamp}$ does not always participate in the circuit's operation in this case.

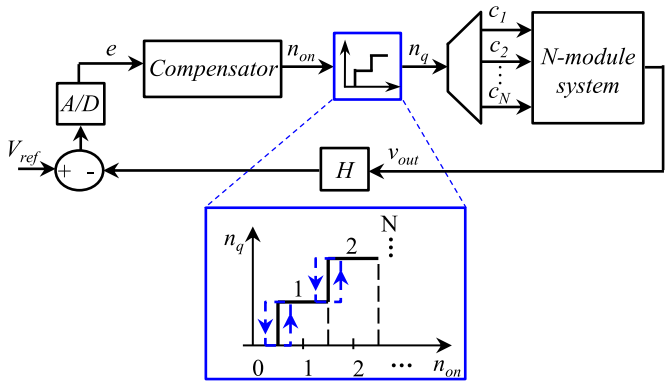


Fig. 13. ON/OFF control implementation for an *N*-module system.

C. Controller Design and Implementation for an N-Module System

After the control-to-output transfer function is derived, a controller can be designed and implemented. The control implementation for an *N*-module system is presented in Fig. 13. The output voltage is sensed and compared to a reference voltage $V_{\rm ref}$. An ADC samples the voltage difference, or error e, and sends it to a compensator to determine the number of ON modules $n_{\rm on}$. When the controller is implemented digitally, the compensator design needs to take into account sensing and computational delay.

A quantizer realizes ON/OFF control by converting $n_{\rm on}$ into a quantized number n_q, and also by limiting the number range from 0 to *N*. In steady state, n_q alternates between two consecutive numbers, which generates PWM ON/OFF control of one module, while the others are either fully ON or OFF. Hysteresis is added to the quantizer block in order to obtain a practical ON/OFF PWM frequency, preferably less than one-fourth of the switching frequency. This practical value is chosen as follows. Assuming an ideal PI compensator, the output voltage ripple in steady state can be estimated as a product of the quantizer hysteresis band and the compensator's proportional gain. Given an approximately constant output voltage ripple, the same reasoning as in Section IV-B shows that the maximum ON/OFF frequency occurs when the load current is half of one module's current supply, or $I_o/2$. Since it takes the first switching cycle for a module to reach steady state upon turning ON, a conservative choice of the module ON time is $2T_s$. At the load current of $I_o/2$, the ideal ON/OFF duty cycle is 50%, which results in the minimum PWM period of $4T_s$. This means the maximum ON/OFF frequency is equal to one-fourth of the switching frequency.

Finally, given the quantized number n_q, a multiplexer simply sends out individual ON/OFF commands c_i to the modules. Each module is controlled by digital gate-timing with lookup table to determine start-up and steady-state sequence t_1 to t_4, as described in Section IV-A.

Design examples are demonstrated for a dc–dc system containing two modules in parallel, each being the same 1-MHz, 24–3.3-V, 5-W module. In order to avoid the effect of output voltage ripple at twice the switching frequency, the sampling

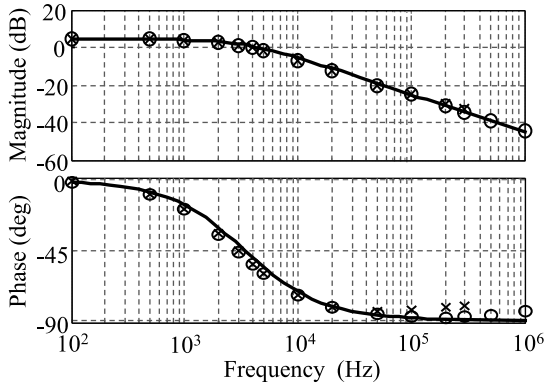


Fig. 14. Bode plots of control-to-output transfer function, using the ideal $G_{vn}(s)$ expression in (9) (solid line), simulations of averaged model (o) and switched converter (x).

rate is chosen to be 2 MHz. The total delay is $T_{\rm delay} = 560$ ns, which is the sum of 500-ns ADC latency delay, 20-ns gate driver delay, and approximately 40-ns computational delay. First, the values of output and clamp capacitors need to be determined. By setting the steady-state voltage ripple at ± 30 mV and limiting $f_{\rm pwm,max} \leq 200$ kHz in (8), C_f is found to be at least 32 μF. The choice for $C_{\rm clamp}$ is not as critical as C_f—it only needs to maintain the 6.6-V clamp voltage with less than 10% ripple in steady state. With $C_{\rm clamp} = 2$ μF and $C_f = 35$ μF, the dc gain and corner frequency of control-to-output transfer function at maximum load are

$$G_{vn0} = \frac{V_{\rm ref}}{N} = 1.65 = 4.3 \text{ dB}$$

$$f_{vn0} = \frac{NI_o}{2\pi C_o V_{\rm ref}} = 3.4 \text{ kHz}.$$

Fig. 14 shows Bode plots of the system control-to-output transfer function, using the ideal $G_{vn}(s)$ expression in (9), the PLECS simulation of averaged model shown in Fig. 12(a), and the PLECS simulation of switched converter implemented with turn-on timing sequence. The simulation data are obtained using a brute force method: adding perturbation to the control variable (number of on modules) at different frequencies, and recording the response at the converter output voltage. At perturbation frequencies closer to the switching frequency, the switched converter behaves nonlinearly. This is due to the fact that each module is not an ideal current source, especially when the modules' on time is relatively close to the switching period. Therefore, the switched converter simulation results are shown in Fig. 14 for up to 300 kHz. The simulation results validate both the averaged and ideal models presented in Fig. 12.

After the ideal control-to-output transfer function is validated, the next step is to design a digital controller for the system. Fig. 15 shows the block diagram of a digital controller for the multimodule system, which is represented by the continuous-time transfer function $G_{vn}(s)$. Sensing and computational delay is included in the delay block. Output voltage error e is sampled by the ADC every $T_{\rm sample}$. At the same rate, the controller $G_c(z)$ calculates and updates the digital command $n_{\rm on}^*$, which is converted into analog value $n_{\rm on}$ by a zero-order hold (ZOH).

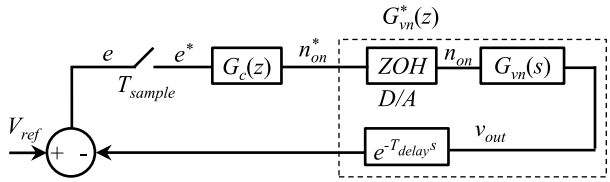


Fig. 15. Block diagram of digital control for an *N*-module system, including sensing and computational delay.

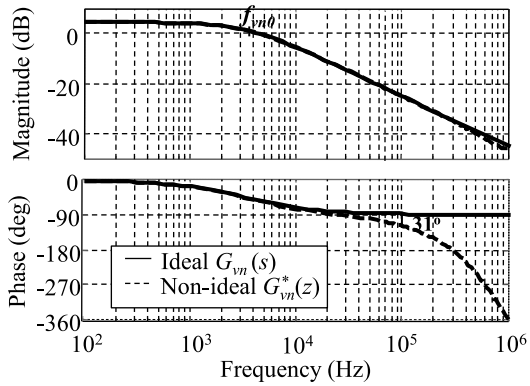


Fig. 16. Bode plots of control-to-output transfer functions for an ideal continuous-time system $G_{vn}(s)$, and nonideal discrete-time system $G_{vn}^*(z)$.

High resolution of $n_{\rm on}$ is assumed for the control model, and therefore, the quantization block is not included. According to [22], a continuous-time compensator $G_c(s)$ can be designed first for the ideal transfer function $G_{vn}(s)$. The equivalent discrete-time compensator $G_c(z)$ is found using the bilinear mapping from continuous-time to discrete-time domain, with prewarping at the crossover frequency. In order to evaluate the compensator $G_c(z)$, z-transform of the continuous transfer function preceded by a ZOH is determined, taking delay into account

$$G_{vn}^*(z) = (1 - z^{-1})\mathcal{Z}\left(e^{-T_{\rm delay}s}\frac{G_{vn}(s)}{s}\right). \quad (10)$$

This can be found using ZOH mapping available in tools such as MATLAB.

Fig. 16 shows Bode plots of control-to-output transfer functions for ideal continuous-time system $G_{vn}(s)$ and discrete-time system with delay $G_{vn}^*(z)$. Compared to the ideal system, $G_{vn}^*(z)$ has a similar magnitude but its phase drops by 31° at 100 kHz. This should be considered when designing the compensator using standard frequency-domain techniques.

A compensator can be of PI or PID type

$$G_{c\rm PI}(s) = G_\infty\left(1 + \frac{2\pi f_L}{s}\right) \quad (11)$$

$$G_{c\rm PID}(s) = G_0\frac{\left(1 + \frac{2\pi f_L}{s}\right)\left(1 + \frac{s}{2\pi f_z}\right)}{\left(1 + \frac{s}{2\pi f_p}\right)}. \quad (12)$$

A PI compensator is simpler, while a PID compensator can result in a faster response. For both controller designs, the crossover frequency f_c is chosen to be 100 kHz (one-tenth the switching

frequency), and the low-frequency zero f_L is set at 9 kHz (less than one-tenth of f_c). Considering the 31° phase drop of $G_{vn}(z)$ at 100 kHz , a phase margin φ_m is set to 76° for the analog PID compensator template. The methods in [23] yield $G_\infty = 18$ for the PI compensator, $G_0 = 22$, $f_z = 121$ kHz, and $f_p = 82$ kHz for the PID compensator. As discussed earlier, the designed compensators are mapped from continuous-time into discrete-time domain. Because of time delay, the compensated loop gain of the nonideal discrete-time system $T^*(z) = G^*_{vn}(z)G_c(z)$ has a phase margin of 56° for PI and 45° for PID compensator.

When there are very few modules in parallel, the PID controller may not be significantly more beneficial than the PI type because of the control variable saturation. A more detailed comparison between the two is presented in Section V.

V. Simulation and Experimental Results

For multiple-module systems, both simulations and experiments use a 24–3.3-V, 5-W module prototype. The resonant tank components and part numbers are listed in Table I (prototype 2). Different from prototype 1 in the hysteretic control of a single module, this prototype uses smaller planar magnetics [20]. This section is arranged as follows. In Section V-A, experimental results are shown for a two-module system. The results are compared to simulations in order to validate the developed model. Further results on systems containing more than two modules are obtained by simulations in Section V-B.

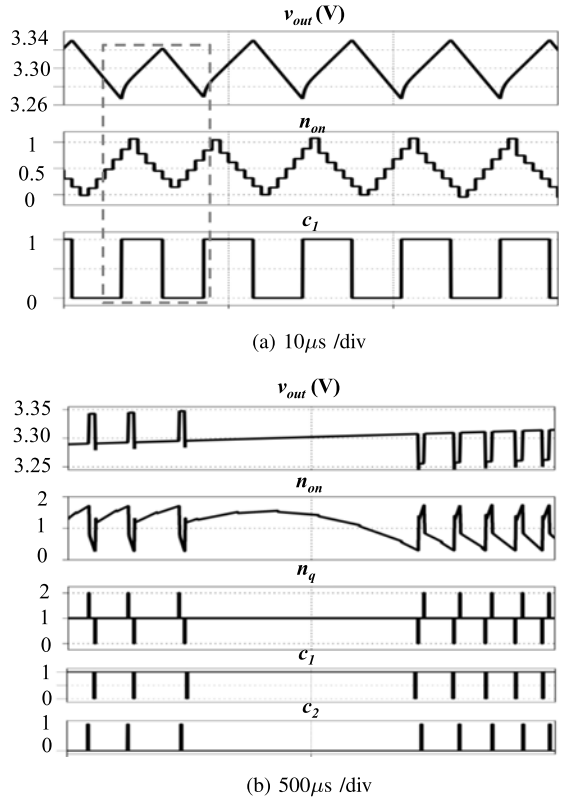


Fig. 17. Simulation results for the two-module system controlled by PI compensator in steady state: (a) 0.75-A load current and (b) 1.5-A load current.

A. Two-Module System

1) Simulation Results: In MATLAB/Simulink with built-in PLECS library, the power stage is set up as shown in Fig. 12(a). The control loop replicates the prototype digital controller, including ADC sampling, quantization, and the estimated computational and sensing delay. Simulations are performed for a two-module system, using the values of $C_{\rm clamp}$, C_f, and compensators designed in Section V-C.

Fig. 17 shows the simulation results in steady state for the two-module system controlled by the PI compensator. Two operating points are specifically studied in detail: 0.75-A output load corresponding to worst-case ON/OFF frequency, and 1.5-A output load corresponding to worst-case voltage ripple.

As discussed in Section IV-C, the PWM ON/OFF frequency is the highest at 0.75-A output (half of one module's current capacity). In the simulation, a hysteresis band of 0.2 is chosen to keep the frequency less than 250 kHz or one-fourth the switching frequency. The output voltage ripple stays within $\pm 1\%$ of the referenced 3.3-V output voltage. Ideally, the ON/OFF frequency and duty cycle stay constant in steady state. However, Fig. 17(a) shows that the frequency varies from 180 to 250 kHz and PWM duty cycles are not always 50%. This inconsistency also causes some smaller output ripple during a shorter PWM period. The reasons behind this behavior are related to power losses and PWM resolution. Because of power losses, the duty cycle is slightly different from 50%. Since the output voltage is sampled at 2 MHz, the PWM resolution is 500 ns, which is one-tenth of approximately 5-μs PWM period. The controller resolves this low resolution issue by adjusting the ON and OFF times over a certain interval, resulting in an average duty cycle that meets the requirement. This variation in duty cycle can be considered a form of limit cycling [24].

The other special operating point is at 1.5-A load, very close to one module's current capacity of 1.52 A. A quick turn-OFF of first module, which lasts for at least 500 ns, causes a quick dip in output voltage. Both modules are then turned ON to compensate for the voltage drop. Turning ON the second module causes the voltage to increase quickly, which consequently forces both modules to be turned OFF, and so on. This explains why two, instead of one module, are ON/OFF modulated. As a result, the voltage ripple is the largest, which is $\pm 1.5\%$ of the referenced voltage, not meeting the design specifications. However, with more modules in parallel, the output capacitor becomes larger, keeping the worst-case steady-state ripple within specifications.

The same capacitance value of 35 μF is used to study step-load transient responses, shown in Fig. 18. Along with the output voltage $v_{\rm out}$ and load current $i_{\rm out}$, the compensator's output $n_{\rm on}$ and quantizer's output n_q are shown during both step-up and step-down transients between 5% load (0.15 A) and 95% load (2.89 A). The output capacitor is sufficient to maintain the output voltage within less than 5% of the nominal voltage. However, the transient-time is affected by the compensator output saturation. At load step-up, the compensator demands a higher $n_{\rm on}$, corresponding to a higher current supply. However, the system is limited to only two modules, thus limiting the transient

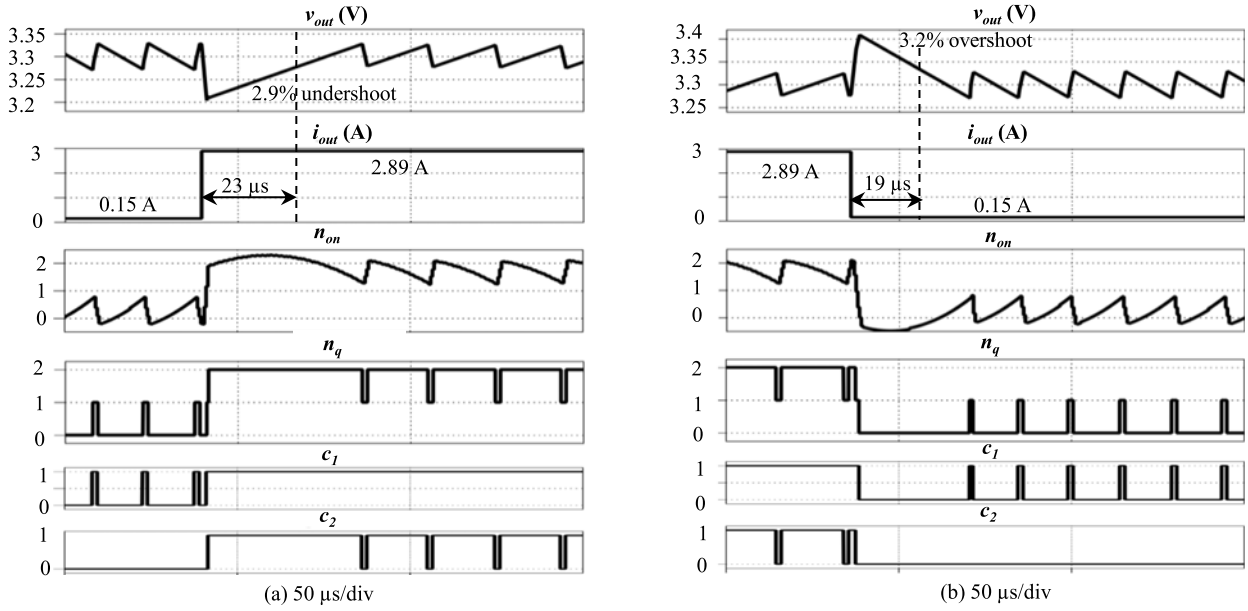


Fig. 18. Simulation transient response of two-module system controlled by PI compensator: (a) load step-up from 5% to 95% and (b) load step-down from 95% to 5%.

TABLE II
COMPARISON BETWEEN PI AND PID COMPENSATORS FOR THE TWO-MODULE SYSTEM

	PI	PID
5% load to 95% load		
- Voltage undershoot (%)	2.9	2.9
- Settling time (μs)	23	23
- Maximum $n_{\rm on}$	2.3	2.7
95% load to 5% load		
- Voltage overshoot (%)	3.2	3.3
- Settling time (μs)	19	20
- Minimum $n_{\rm on}$	-0.4	-0.9

performance. After two modules are fully turned ON, the equivalent capacitor C_o is charged by a small difference between the supply and load currents. It takes 23 μs to return within 1% error in the output voltage. Similarly, at load step-down, the output capacitor C_f is discharged slowly by a small load current, resulting in 19 μs settling time. Because the participating capacitor in this case is only C_f, the step-down settling time is faster. In systems containing more modules, C_f is more dominant in the expression $C_o = C_f + 4C_{\rm clamp}$, and the settling time difference between step-up and step-down transients becomes less significant.

Table II compares the step-load transient performance of two compensators. The PID compensator demands a higher $n_{\rm on}$ than the PI type. However, because the compensator output is saturated, the voltage change and settling time are similar in both cases. The minimum and maximum values of $n_{\rm on}$ suggest that if the system had three or more modules, the PID compensator would be more beneficial. For the two-module system, a simple PI compensator is sufficient.

2) Experimental Results: The designed PI controller, hysteretic quantizer, and gate timing with lookup table are implemented digitally in Verilog HDL on a Virtex-IV FPGA board. The ADC samples the output voltage at 10 MHz with a latency delay of five clock cycles and the equivalent quantization of 2 mV. The controller reads the sensed voltage every five samples to avoid output ripple effects. This makes the equivalent sampling rate equal to 2 MHz.

Fig. 19(a) and (b) shows the experimental steady-state results when the load current is 0.75 and 1.5 A, respectively. As predicted by simulation at 1.5-A load, both modules are ON/OFF modulated, causing the largest output voltage ripple of about $\pm$50 mV. It is verified that PWM of two modules does not affect the system's efficiency in this case. At 0.75-A output, the PWM ON/OFF frequency is the highest, ranging from 167 to 182 kHz, and the duty cycle does not stay constant. In general, the voltage ripples are somewhat larger than in simulations because each module does not behave exactly as an ideal current source that can be turned ON/OFF instantaneously, as assumed in the model. When a module is turned OFF, depending on the resonant current direction, the body diode of one primary-side switch may keep conducting. The worst observed delay is approximately 300 ns, increasing $v_{\rm out}$ up to 10 mV. When a module is turned ON, it takes the first switching cycle to reach steady state. The worst observed delay is about 600 ns, adding 16 mV to the output voltage ripple.

Transient responses at load step-up and step-down are shown in Fig. 19(c) and (d), respectively. Because the modules are nonideal current sources, the voltage change is larger than in simulations, but it is still within 5% of the nominal voltage. The settling time in both load steps is slightly longer than predictions because of the higher output voltage change of around 4.5% compared to 3% in simulation. Despite some differences

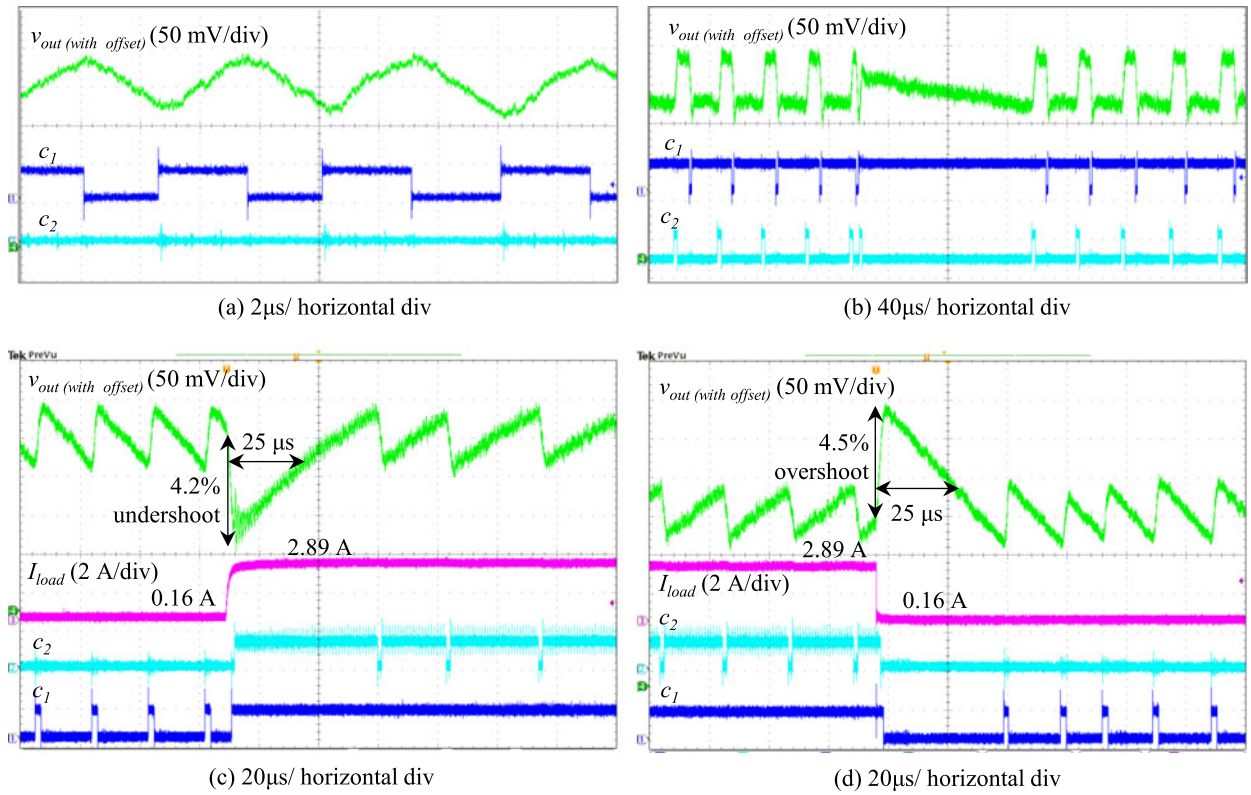


Fig. 19. Experimental results of two-module system in: (a) steady state, 0.75 A load current, (b) steady state, 1.5 A load current, (c) load step-up transient, 5% to 95%, and (d) load step-down transient, 95% to 5%.

between simulations and experiments, simulation remains a viable tool to verify a controller design for systems containing large number of modules in parallel.

B. Twenty-Module System

This section evaluates compensators for a 90-W 20-module system using simulations. Based on the previous design and verifications on the two-module system, the capacitance is scaled by the number of modules to guarantee a voltage change within 5% at large load steps, $C_{\rm clamp} = N(\mu{\rm F})$ and $C_f = 17.5N(\mu{\rm F})$. For $N = 20$, the capacitor values are $C_{\rm clamp} = 20\,\mu$F and $C_f = 350\,\mu$F. The PI and PID compensators are designed using the same method as in the two-module system. Assuming the same delay and keeping the same crossover frequency and phase margin, all the poles and zeros in the compensator functions (11) and (12) are the same as in the two-module system. Only the gains are scaled by the number of modules

$$G_{\infty(N-{\rm module})} = 0.5NG_{\infty(2-{\rm module})}$$
$$G_{0(N-{\rm module})} = 0.5NG_{0(2-{\rm module})}.$$

When there are more modules in parallel, the saturation effect of $n_{\rm on}$ and comparison between PI and PID compensators can be studied in more detail. Saturation at step-load transient happens when 1) the steady-state value of $n_{\rm on}$ corresponding to the final load current reaches its minimum or maximum value (less than 1 or greater than $N-1$) and 2) during transient interval, the compensator command is out of range ($n_{\rm on} < 0$ or $n_{\rm on} > N$). Consequently, the system reaches its limit and cannot supply larger surplus current to charge or discharge the output capacitor upon sudden change in load. Given a certain output capacitor value and initial load value, the settling time depends on the compensator's capability and the final load value (i.e., how close it is to the system's supply limit).

Different step-up scenarios, starting at the same 0.5 A load current, are examined in simulations for both PI and PID compensators. Fig. 20 compares the transient performance of the two compensators at different load steps: 80%, 90%, and 95%. In the figure, Δ is the output voltage undershoot and $t_{\rm settle}$ is the time it takes $v_{\rm out}$ to reach within 1% error compared to its nominal value. For both compensators, saturation has little effect on transient voltage overshoot. At around 95% load step, the settling time is very sensitive to saturation. A small change to final load value from 28.5 to 28.8 A results in 4–5 μs longer settling time. At load steps less than 95%, the PID compensator offers faster settling time, thanks to its capability to turn ON more modules at a faster rate. Note that at 90% load step, the PID compensator can still outperform the PI type even when a light saturation happens ($n_{\rm on}$ is 20% higher than the maximum number of modules). The PID compensator loses its benefit when saturation is worse ($n_{\rm on}$ overshooting is higher than 33%).

Considering both step-up and step-down transients, if this system is designed to supply a load range from 5% to 95% of its power rating, the saturation effects during large load-steps can be minimized and the PID compensator performs better. In a scenario when the sensing delay is reduced, the phase margin of

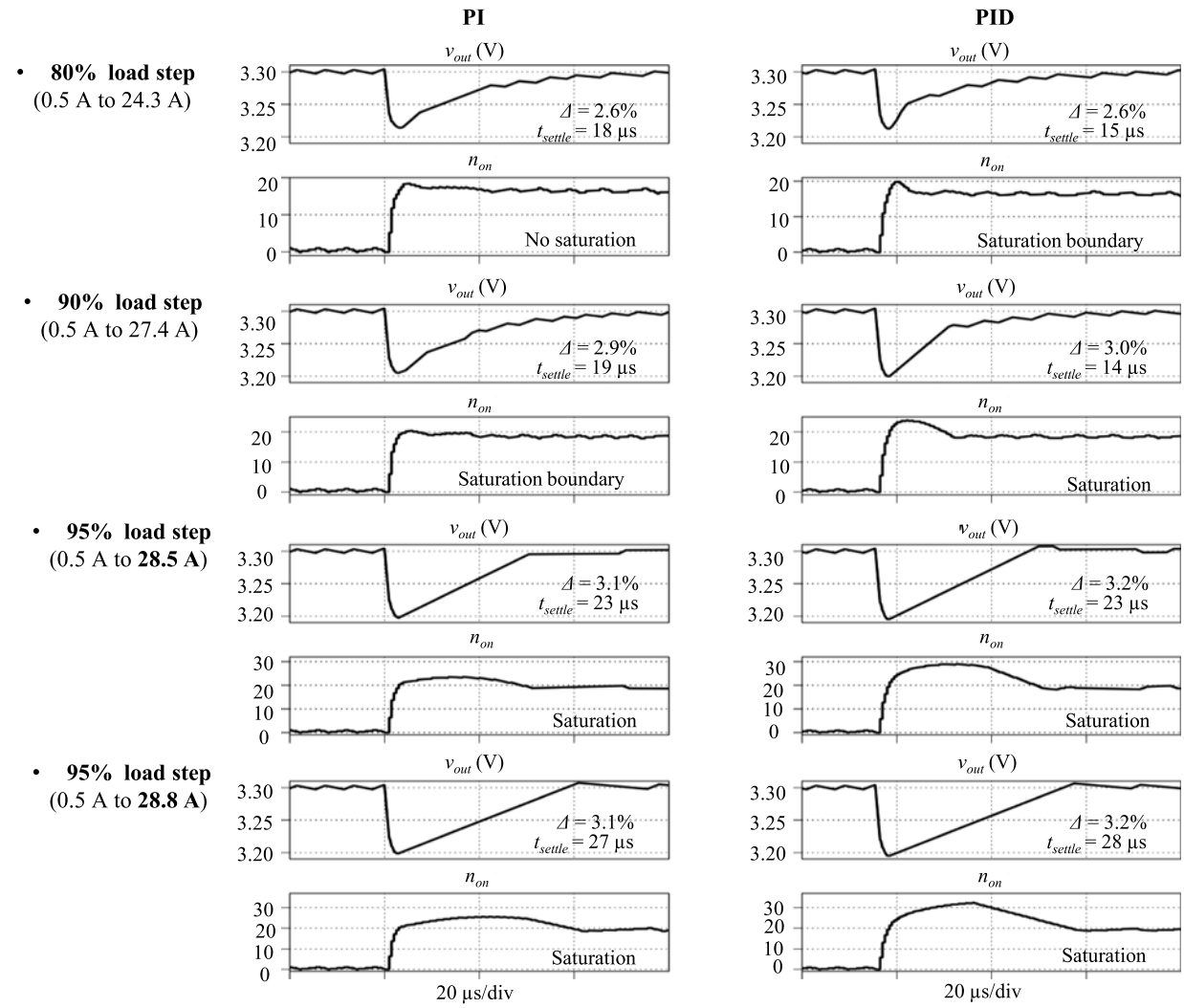


Fig. 20. Comparison between PI and PID compensators for a 20-module system at different load steps.

the PI-compensated loop gain becomes higher compared to the analysis in Section IV-C. That means the PI controller updates $n_{\rm on}$ at a slower rate upon load steps with less command undershoot or overshoot. Therefore, the PID controller will show more significant benefits over the PI type [19].

VI. Discussions

A. Output Filter Capacitor Size

For systems based on 5-W modules presented in this paper, it is shown that when the number of modules in parallel is small, the output capacitor is mainly determined by the output voltage ripple in steady state, not the voltage change during step-load transients. The output capacitance of 11.7 μF per 1-A load guarantees a voltage change of less than 5% at 100% step-load transient. However, at $N = 2$, such a capacitance value yields large worst-case voltage ripple, $\pm 1.5\%$ of the nominal voltage. In order to meet a stricter voltage ripple requirement of less than $\pm 0.5\%$, a system of six or more modules is needed, or a larger output filter capacitor must be used.

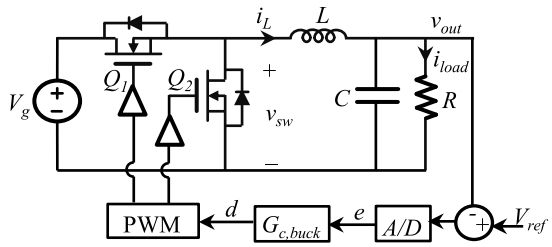


Fig. 21. Control loop diagram for a synchronous buck converter.

Regarding step-load response only, a synchronous buck converter with digital PID voltage controller is considered in comparison with the proposed ON/OFF controlled *N*-module active-clamp *LLC* converter. The purpose of the comparison is to evaluate the proposed architecture and the control method in terms of capacitor size and transient performance, using the buck converter as a reference. Fig. 21 shows the voltage control loop of a synchronous buck converter. The ADC's quantization, delay, and sampling rate are the same as in the ON/OFF

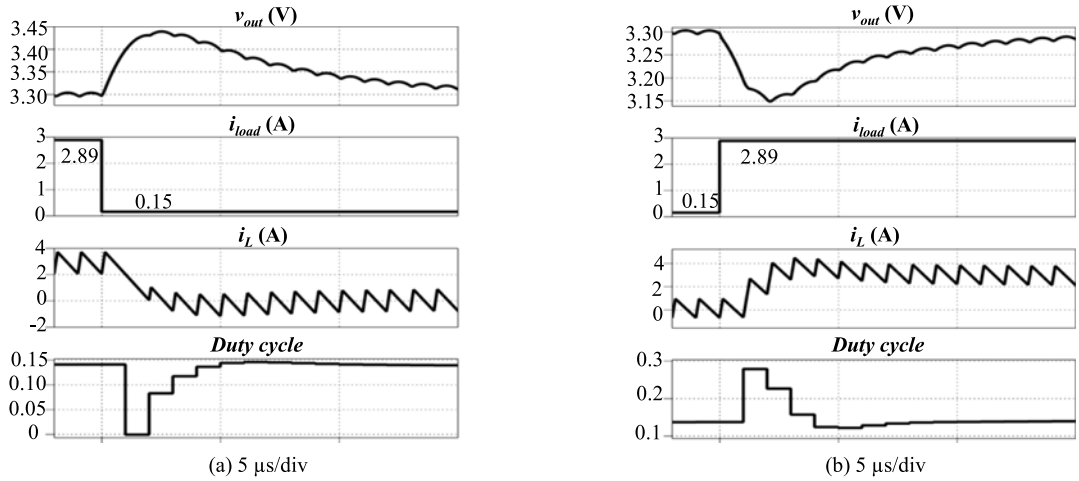


Fig. 22. Simulation results of 10-W buck converter at (a) 95% to 5% load step down and (b) 5% to 95% load step up.

controlled modular converter. The digital compensator, PWM, and power circuit are set up and simulated in MATLAB/Simulink with PLECS library. The duty cycle is updated right before the beginning of each switching cycle.

Corresponding to any *N*-module active-clamp *LLC* system, an ideal buck converter is designed at the same power rating, converting 24-V input to 3.3-V output voltage, and operating at the same 1-MHz switching frequency. The design specifications are: $\pm 0.5\%$ output voltage ripple and $\pm 5\%$ transient voltage change, and compensator's crossover frequency of 100 kHz. Following the same design process as in [25], the *LC* output filter is determined for the given design requirements. First of all, the inductance L is chosen such that the PID compensator with 100-kHz crossover frequency operates at the linear/saturation boundary upon large step load. The inductor value is found to be $L = 3.6/N$ (μH), which corresponds to $\pm 25\%$ inductor current ripple at full load. The smallest output capacitance is then derived as a function of N: $C = 13.5N(\mu\text{F})$. To maintain the output voltage within 5% of the nominal value during step-load transients, the PI ON/OFF control of the *N*-module active-clamp *LLC* converter requires 30% larger output capacitance compared to the PID voltage control of a single-phase buck converter. This is due to the fact that when turned ON, each active-clamp *LLC* module takes the first switching cycle to reach its nominal output current. During that time the output capacitor keeps being charged or discharged.

The step-load settling time can be compared between the proposed system and a voltage-controlled buck converter that uses two different output capacitance values: the smallest design value $C = 13.5N$ (μF), and the same value as in the *N*-module active-clamp *LLC* converter $C = 17.5N$ (μF). Corresponding to each output filter size, the control-to-output transfer function is found and a PID compensator $G_{c,\text{buck}}$ can be designed [23]. The designed compensator, taking into account computational and sensing delay, has a phase margin of 45° at 100-kHz crossover frequency. An example is shown in Fig. 22 for a 10-W buck converter's step-load response.

When the output current steps down from 95% to 5% load, the duty cycle reaches zero in the next switching cycle, allowing the inductor current i_L to ramp down quickly to zero [see Fig. 22(a)]. This proves that the compensator operates at the linear/saturation boundary. When the output current steps up from 5% to 95% load, the controller increases i_L to no more than 50% of the 3-A rating [see Fig. 22(b)]. In practice, the inductor should be designed properly so that it is not saturated at a high overshooting current.

The performances can be compared in terms of step-load settling time obtained by simulations. Fig. 23 compares the settling time of the three configurations at different normalized power ratings P/P_0, where P_0 is the power of one active-clamp *LLC* module. The value of P/P_0 is also equal to the number of *LLC* modules in parallel. It is shown that the multimodule active-clamp *LLC* converter maintains the same settling time at any power rating. When the converter's power is at least 35 W, or $N \geq 7$, it settles the output voltage faster than the synchronous buck converter using the same output capacitance. Compared to the buck converter using the smallest allowed capacitance, the proposed system settles faster when the power level is at least 30 W, or $N \geq 6$. Note that the PI ON/OFF controller's gain is scaled with the number of modules N. At larger N, the computational delay may be longer, but it is still insignificant compared to the dominant delay of the ADC. Therefore, the controller's performance will not be affected much.

There are other considerations for the comparison. It is well understood that an interleaving multiphase buck converter with phase-shedding control presents advantages, especially at higher current levels [1], [2], [7]. Furthermore, due to current ripple cancellation, a smaller inductance can be used, which helps improve transient responses. A time-optimal controller for the buck converter could also be applied to obtain a faster settling time [6]. Nevertheless, the comparison is focused on a single-phase buck converter with conventional linear PID controller as a basic reference case. This comparison can serve as a starting point for more detailed comparative evaluations against multiphase buck and other approaches suitable for POL applications.

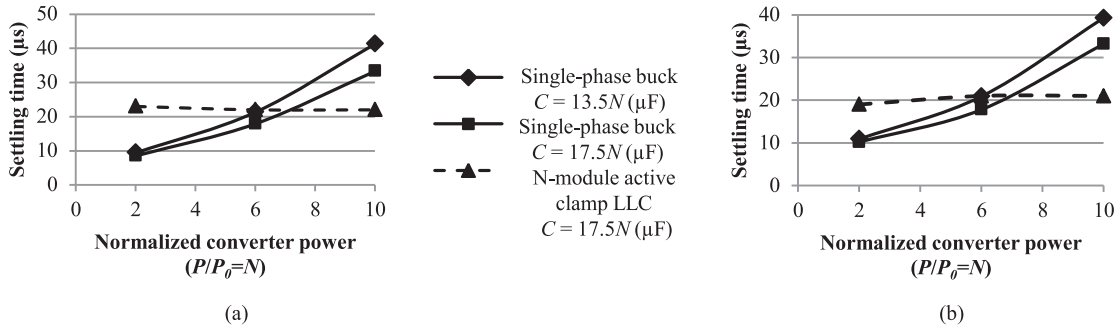


Fig. 23. Settling time of synchronous buck and multimodule active-clamp *LLC* converters at different power ratings when (a) load steps up from 5% to 95% and (b) load steps down from 95% to 5%.

In summary, for systems containing at least six 5-W active-lamp *LLC* modules, the proposed ON/OFF control method meets the strict voltage ripple requirement for POL applications. Compared to a single-phase buck converter with PID voltage controller, the proposed system requires 30% more output capacitance to maintain the same transient voltage deviation. This gap can be reduced by increasing the switching frequency of the active-clamp *LLC* modules since the modules take less time to reach the steady state. In that case, the converter needs to be carefully designed to obtain a good efficiency. When the single-phase buck converter uses the same output capacitance as the multimodule active-clamp *LLC* converter, the *LLC* converter shows a competitively fast step-load transient response at an output current of 11 A or higher.

B. Hysteresis Versus Fixed-Frequency ON/OFF Control

Adding hysteresis to the $n_{\rm on}$ quantizer varies the ON/OFF PWM frequency. This is helpful when the PWM time resolution is low and when there are few modules in parallel. In the two-module system example, the PWM time resolution is 500 ns. It limits the PWM duty cycle resolution over all load range, especially when the PWM is fixed at 200 kHz to maintain the acceptable output voltage ripple. The fixed PWM frequency can only be reduced by increasing the output capacitor, which is not desirable. Hysteresis control yields two degrees of freedom, module's on time and PWM switching period. Therefore, it helps to minimize the duty cycle resolution issue at various loads. The fixed-frequency ON/OFF control method is suitable when the PWM frequency is much smaller than the output voltage ripple frequency as in [15] and [16], or in systems consisting of more active-clamp *LLC* modules, allowing a larger output capacitor.

VII. Conclusion

This paper presents methods to model and design an ON/OFF controller for a multiple-parallel-module dc–dc system using active-clamp *LLC* resonant converter modules. The architecture and the control method yield high overall efficiency and fast transient responses. Two converter models are introduced: 1) a high-frequency model to determine a gate timing sequence leading to fast module turn-ON capability; and 2) an averaged model to assist the system control loop design. The standard frequency-domain techniques are proposed to design the system control loop, using the number of ON modules as the control variable.

The models and the ON/OFF control method are verified by experiments on a prototype containing two 1-MHz, 24–3.3-V, 5-W active-clamp *LLC* modules. Steady-state and transient responses are evaluated experimentally in the two-module system, and by simulations for a larger 20-module system. The results show that, in a POL dc–dc system consisting of at least six 1-MHz, 24–3.3-V, 5-W *LLC* modules operating in parallel, a standard PI or PID compensator can regulate the output voltage in steady state. However, compared to a synchronous buck converter with PID voltage controller, the proposed system requires 30% more output capacitor in order to maintain the same transient voltage deviation (less than 5% of referenced value). For systems rated at 11 A or more, the proposed architecture and control method perform with competitively fast step-load transient responses compared to the voltage-controlled buck converter using the same output capacitor.

In the studied ON/OFF controller, it is important to note the saturation effect of the control variable, which may limit the settling time upon large step-load transients. In the 20-module system example, the PID controller can tolerate saturation of the control variable and has a faster step-load response than the PI controller.

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