Minimization of the DC Component in Transformerless Three-Phase Grid-Connected Photovoltaic Inverters

Qingzeng Yan, Xiaojie Wu, Xibo Yuan, *Member, IEEE*, Yiwen Geng, and Qi Zhang

***Abstract*—The dc component is a special issue in transformerless grid-connected photovoltaic (PV) inverter systems and may cause problems regarding system operation and safety. IEEE standard 1547-2003 has defined the limit for dc component in the grid-side ac currents, e.g., below 0.5% of the rated current. The dc component can cause line-frequency power ripple, dc-link voltage ripple, and a further second-order harmonic in the ac current. This paper has proposed an effective solution to minimize the dc component in three-phase ac currents and developed a software-based approach to mimic the blocking capacitors used for the dc component minimization, the so-called virtual capacitor. The "virtual capacitor" is achieved by adding an integral of the dc component in the current feedback path. A method for accurate extraction of the dc component based on double time integral, as a key to achieve the control, has been devised and approved effective even under grid-frequency variation and harmonic conditions. A proportional-integral-resonant controller is further designed to regulate the dc and line-frequency component in the current loop to provide precise control of the dc current. The proposed method has been validated on a 10-kVA experimental prototype, where the dc current has been effectively attenuated to be within 0.5% of the rated current. The total harmonic distortion and the second-order harmonic have also been reduced as well as the dc-link voltage ripple.**

***Index Terms*—Controller, dc component, proportional-integral-resonant (PIR) transformerless three-phase PV inverters, virtual capacitor.**

I. INTRODUCTION

GRID-CONNECTED photovoltaic (PV) systems often include a line transformer between the power converter and the grid. The transformer guarantees galvanic isolation between the grid and the PV systems, thus fulfilling safety standards. Furthermore, it ensures that no direct current (dc) is injected to the grid [1]. However, the low-frequency (50 or 60 Hz) transformer is bulky, heavy, and expensive and its power loss brings down the overall system efficiency. To eliminate the transformer and to achieve cost, size, and weight reduction as well as efficiency improvement, the research and interest on "transformerless" power conversion is growing [1]–[5].

There are several issues associated with transformerless structures, such as dc component in the inverter output (grid) current, ground leakage current (due to common-mode voltage and parasitic capacitance), and the voltage-level mismatch between the solar panel (inverter) and grid [2], [6]. Among them, the dc component can affect the normal system operation and cause safety concerns. Standards have therefore been established in many countries to limit the level of the dc component, for example, below 0.5% of the rated output current (e.g., IEEE Standard 1547-2003) [7], [8]. Therefore, this paper will investigate effective solutions to minimize the dc component in a PV system.

The dc component can have negative impacts on the power system in the following ways [9], [11]:

1) The dc component can affect the operating point of the transformers in the power system. The transformer cores are driven into unidirectional saturation with consequent larger excitation current. The service lifetime of the transformer is reduced as a result with further increased hysteresis and eddy current losses and noise.
2) The dc component can circulate between inverter phase legs as well as among inverters in a paralleled configuration. The dc component circulation affects the even current and loss distribution among paralleled inverters.
3) The dc component injected to the grid can affect the normal operation of the loads connected to the grid, for example, causing torque ripple and extra loss in ac motors.
4) The corrosion of grounding wire in substations is intensified due to the dc component.

There are several sources leading to the dc components in grid-connected inverters: 1) asymmetry in the switching behavior of power semiconductor devices, 2) imparity in gate driver circuits, 3) device turn-on and turn-off delays, 4) nonidentical device voltage drops (on-state resistance, saturation voltage, etc.), and 5) sampling biases from the ac current and ac voltage sensors, etc. [12]–[16].

Minimization of the dc component in transformerless PV inverters has been extensively investigated in literatures [12]. Several solutions have been developed which can be grouped into two categories: passive methods and active methods. For example, coupling transformers and blocking capacitors are inserted on the inverter ac side to minimize the dc component. The main disadvantage of this kind of passive methods is the increased cost, weight, and physical size of the system as well as extra power loss. There are other methods by using

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alternative or special inverter topologies such as two-level or three-level half-bridge configurations [1, 17], which are not extendable to other inverter topologies. Regarding active methods, autocalibrating techniques for dc-link sensors in two-level and three-level single-phase inverters were proposed in [13] and [14], which are effective to minimize the dc component caused by sampling biases of the ac current sensors. However, these methods are not suitable for the dc component caused by other sources, e.g., asymmetry in switching behavior and an extra dc-link current sensor is required. In [16] and [18]–[22], the authors use different methods to extract the dc component from the output current, and add feedback compensation to minimize it, which are only used in single-phase systems. To the authors' knowledge, at the time of writing, only the technique in [15] is for three-phase systems, which detects and uses the line-frequency voltage ripple on the dc-link to build an indirect feedback loop to compensate the dc component of the output current. However, since the dc components are not measured and feedback directly, the method cannot guarantee that the dc component in each phase is minimized effectively. The dc component minimization methods of single-phase PV inverters differ from that of three-phase PV inverters. In three-phase PV inverters, dc component may exist in each phase and flow between phases. It is more challenging to minimize the dc component for all the three phases at the same time due to their couplings.

Among the above solutions, "virtual capacitor" concept was proposed in [22] to minimize the dc component in single-phase PV inverters. It replaces the physical capacitor which could block the dc component on the ac side with a novel control strategy. Based on that, this paper further analyzes the difference and challenges of using this method for three-phase inverter systems and extends the control strategy to three-phase PV inverters by integrating the extracted dc component and adding it in the current feedback path. A proportional-integral-resonant (PIR) controller is also designed to provide a precise control for both dc and line-frequency signals [23], [24].

Note that though the dc component minimization method can be implemented in each phase, e.g., by a per-phase PI controller, this paper specifically investigates how to implement that in a synchronous rotational frame (*d, q* frame) where existing three-phase PV inverters control systems are normally based, e.g., with a dual closed-loop control. Therefore, the proposed dc-component minimization method can be relatively easily added to the existing three-phase systems. The virtual capacitor amplifies the dc component in the feedback loop to achieve an effective minimization of the dc component. A comprehensive method to design the virtual capacitor and the PIR controller with simple implementation has been given in this paper.

In the proposed control strategy, an accurate dc component measurement and extraction is critical. Several methods can be used to measure the dc component, e.g., by shunt resistors [18], voltage transformers [19], mutual coupled inductors [20], and integral methods [8], etc. Among them, only the integral methods do not need extra hardware. However, the performance of the conventional integral method based on fundamental-period integral degrades under line-frequency variations. In this paper, a new integral method based on the sliding window iteration algorithm and double time integral is presented. This method is effective in the extraction of the dc component even for currents with frequency fluctuations and harmonics.

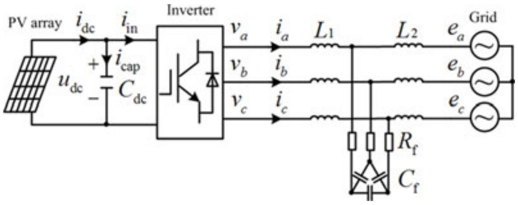


Fig. 1. Transformerless three-phase PV inverter system.

The paper is structured as follows. The impact of the dc component on the system power flow is analytically derived in Section II and a line-frequency power ripple is found at both dc and ac sides of the inverter. Then, the virtual capacitor concept and its application in single-phase systems are explained, based on which a dc component minimization strategy for three-phase systems has been developed in Section III. Section IV presents an accurate dc component extraction method based on the sliding window iteration algorithm, which is critical to achieve the proposed dc-component minimization. In Section V, a PIR controller is designed based on the system model to meet both dynamic performance as well as current-loop stability, and also the design of the dc-link voltage loop is described. The effectiveness of the proposed strategy for the dc component minimization has been experimentally validated on a 10-kVA solar power generation system and the results are given in Section VI.

II. IMPACT OF THE DC COMPONENTS ON PV SYSTEMS

A typical three-phase transformerless PV inverter system is shown in Fig. 1. The PV array is connected to the grid via a three-phase voltage-source two-level inverter and an *LCL* filter. The capacitors of the *LCL* filter can be configured with a delta or star connection. In this paper, a delta connection is used to reduce the required capacitor and cost as opposed to the star connection, which has the benefit of smaller short-circuit current. The dual closed-loop control strategy, which comprises a current loop and a dc-link voltage loop in the synchronous rotational frame, is a relatively common control strategy in three-phase PV inverters [25].

In order to analyze the impact of dc components on the three-phase PV systems, the dc components have been added in the system model in addition to the line (fundamental)-frequency components. If other harmonics are neglected and only the dc and line-frequency components are concerned, F can be defined as an electrical variable (e.g., for ac-side voltage and current) and is expressed as in (1) in each coordinate (three-phase stationary (abc), two-phase stationary ($\alpha\beta$), and two-phase rotational (dq))

$$\begin{cases} F_a = F_{a0} + F_{a1} \\ F_b = F_{b0} + F_{b1} \\ F_c = F_{c0} + F_{c1} \end{cases}, \begin{cases} F_\alpha = F_{\alpha 0} + F_{\alpha 1} \\ F_\beta = F_{\beta 0} + F_{\beta 1} \end{cases}, \begin{cases} F_d = F_{d0} + F_{d1} \\ F_q = F_{q0} + F_{q1} \end{cases} \tag{1}$$

where the subscript 0 denotes the dc component and the subscript 1 denotes the line-frequency component. Note that the zero component in conventional coordinate transformation is not taken into account due to the three-wire system. If there are dc components in the *abc* coordinate, they will also exist in the form of dc or line-frequency components in $\alpha\beta$ and *dq* coordinates, respectively.

In a three-phase three-wire system, there is no current flowing through the neutral point and hence

$$\begin{cases} F_{a0} + F_{b0} + F_{c0} = 0 \\ F_{a1} + F_{b1} + F_{c1} = 0. \end{cases} \tag{2}$$

With (1) and (2), the coordinate transformations of the dc components from *abc* coordinate to $\alpha\beta$ and *dq* coordinate can be expressed as

$$\begin{aligned} \begin{bmatrix} F_{\alpha 0} \\ F_{\beta 0} \end{bmatrix} &= \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} F_{a0} \\ F_{b0} \\ F_{c0} \end{bmatrix} \\ &= \begin{bmatrix} F_{a0} \\ \frac{\sqrt{3}}{3} F_{b0} - \frac{\sqrt{3}}{3} F_{c0} \end{bmatrix} \end{aligned} \tag{3}$$

$$\begin{aligned} \begin{bmatrix} F_{d1} \\ F_{q1} \end{bmatrix} &= \frac{2}{3} \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \\ &\cdot \begin{bmatrix} F_{a0} \\ F_{b0} \\ F_{c0} \end{bmatrix} = \begin{bmatrix} F_{a0}\cos\theta + \frac{\sqrt{3}}{3}(F_{b0} - F_{c0})\sin\theta \\ \frac{\sqrt{3}}{3}(F_{b0} - F_{c0})\cos\theta - F_{a0}\sin\theta \end{bmatrix} \end{aligned} \tag{4}$$

where θ is the angle between the *dq* coordinate and *abc* coordinate, for example, the grid angle in a grid-voltage oriented vector control.

As seen in (3) and (4), by the coordinate transformation, F_{a0}, F_{b0}, and F_{c0} (dc components) in the stationary *abc* frame can be transformed into $F_{\alpha 0}$ and $F_{\beta 0}$ in the stationary $\alpha\beta$ frame and then F_{d1} and F_{q1} (line-frequency) in *dq* frame. Therefore, the voltage and current in the control loop of each frame will contain both dc and line-frequency components.

The synthesized vector $\boldsymbol{F}$ of dc components can be decomposed in the frames shown in Fig. 2, where $\boldsymbol{F}$ is a stationary vector. Since the *dq* frame rotates anticlockwise, the dc component in the synchronous *dq* frame appears in the form of a negative-sequence line-frequency component.

According to the instantaneous power theory [26], [27], the system active power p_{ac} and reactive power q_{ac} can be expressed in (5) and (6) in the *dq* frame, where the mark "·" and the mark "×" are the inner and outer product of vectors, respectively

$$\begin{aligned} p_{\text{ac}} &= \frac{3}{2} \begin{bmatrix} \boldsymbol{U}_d \\ \boldsymbol{U}_q \end{bmatrix}^{\mathrm{T}} \cdot \begin{bmatrix} \boldsymbol{I}_d \\ \boldsymbol{I}_q \end{bmatrix} = \frac{3}{2} \begin{bmatrix} u_{d0} + u_{d1} \\ u_{q0} + u_{q1} \end{bmatrix}^{\mathrm{T}} \cdot \begin{bmatrix} i_{d0} + i_{d1} \\ i_{q0} + i_{q1} \end{bmatrix} \\ &= \frac{3}{2} \Bigg(\underbrace{u_{d0} i_{d0} + u_{q0} i_{q0}}_{\text{DC component}} + \underbrace{u_{d0} i_{d1} + u_{d1} i_{d0} + u_{q0} i_{q1} + u_{q1} i_{q0}}_{\text{Line-frequency fluctuation}} \\ &\quad + \underbrace{u_{d1} i_{d1} + u_{q1} i_{q1}}_{\text{2nd fluctuation}} \Bigg) \end{aligned} \tag{5}$$

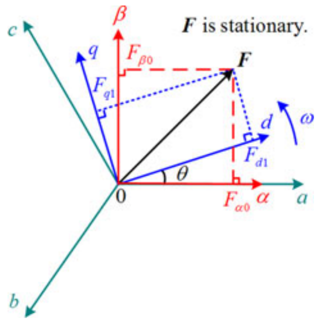


Fig. 2. Coordinate transformation of dc components.

$$\begin{aligned} q_{\text{ac}} &= \frac{3}{2} \left| \begin{bmatrix} \boldsymbol{U}_d \\ \boldsymbol{U}_q \end{bmatrix}^{\mathrm{T}} \times \begin{bmatrix} \boldsymbol{I}_d \\ \boldsymbol{I}_q \end{bmatrix} \right| = \frac{3}{2} \left| \begin{bmatrix} u_{d0} + u_{d1} \\ u_{q0} + u_{q1} \end{bmatrix}^{\mathrm{T}} \times \begin{bmatrix} i_{d0} + i_{d1} \\ i_{q0} + i_{q1} \end{bmatrix} \right| \\ &= \frac{3}{2} \Bigg(\underbrace{u_{q0} i_{d0} - u_{d0} i_{q0}}_{\text{DC component}} + \underbrace{u_{q0} i_{d1} + u_{q1} i_{d0} - u_{d0} i_{q1} - u_{d1} i_{q0}}_{\text{Line-frequency fluctuation}} \\ &\quad + \underbrace{u_{q1} i_{d1} - u_{d1} i_{q1}}_{\text{2nd fluctuation}} \Bigg). \end{aligned} \tag{6}$$

As seen, both the active and reactive power contains a constant dc power (desired), a line-frequency, and a second-order power fluctuation due to the dc component in the voltage and current (undesired). Further, with grid-voltage orientated vector control under unity power factor operation for PV applications, where $u_{q0} = 0$, $i_{q0} = 0$, (5), and (6) can be simplified to (7) and (8) if assuming the second-order fluctuations is negligible compared to the other two components

$$p_{\text{ac}} = \frac{3}{2} \Bigg(\underbrace{u_{d0} i_{d0}}_{\text{DC component}} + \underbrace{u_{d0} i_{d1} + u_{d1} i_{d0}}_{\text{Line-frequency fluctuation}} \Bigg) \tag{7}$$

$$q_{\text{ac}} = \frac{3}{2} \Bigg(\underbrace{u_{q1} i_{d0} - u_{d0} i_{q1}}_{\text{Line-frequency fluctuation}} \Bigg). \tag{8}$$

As seen in (7) and (8), line-frequency fluctuations will appear in both active power p_{ac} and reactive power q_{ac} when the dc components in the ac voltage and ac current are considered. The reactive power only circulates in the inverter phase legs at the ac side and does not affect the dc side. In comparison, the line-frequency active power fluctuations will impact the dc-link

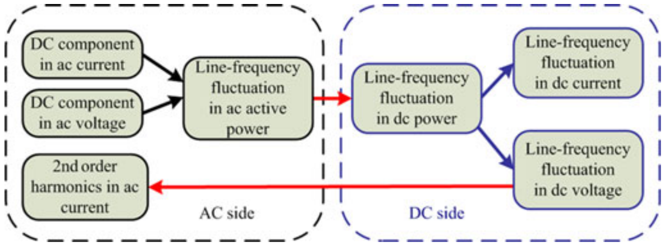


Fig. 3. Influences of dc component on PV systems.

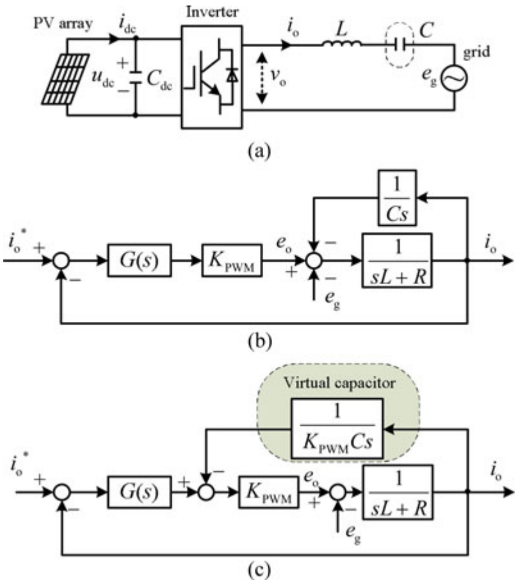


Fig. 4. Virtual capacitor concept of a single-phase grid-connected PV inverter: (a) circuit diagram of a single-phase grid-connected PV inverter with the blocking capacitor, (b) current control loop diagram, and (c) equivalent transformation of the current control loop with virtual capacitor concept.

power, e.g., causing voltage ripple in the dc-link [15], which in return will generate a second-order harmonic in the ac current [28]. Therefore, effective solution to minimize the dc component is important apart from the reasons given in the introduction part. The impact of dc components on PV systems is illustrated in Fig. 3.

III. MINIMIZATION OF DC COMPONENT IN THREE-PHASE GRID-CONNECTED PV SYSTEMS

A. Virtual Capacitor Concept of Single-Phase Grid-Connected PV Inverters

One way to block the dc component is to put a capacitor *C* in series with the ac side of the inverter as shown in Fig. 4(a). However, in order to reduce the capacitive reactance at other frequencies, the capacitor value needs to be large, which increases the size and cost of the system. This series capacitor may also affect the system dynamic response and reduce transmission efficiency [18]. Nevertheless, the physical capacitor can be replaced by software-based method and advanced control strategy which mimics the operation of the series capacitor in a single-phase PV system [22].

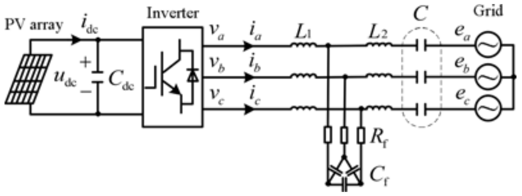


Fig. 5. Circuit diagram of a three-phase grid-connected PV inverter with blocking capacitors.

The circuit diagram of a single-phase PV inverter with a blocking capacitor is shown in Fig. 4(a). The ac-side mathematical model in the time and frequency domain can be expressed as in (9) and (10), respectively

$$L\frac{di_{\rm o}}{dt}+\frac{1}{C}\int i_{\rm o}dt+Ri_{\rm o}=e_{\rm g}-v_{\rm o} \tag{9}$$

$$I_{\rm o}(s)=\frac{Cs}{LCs^2+RCs+1}[E_{\rm g}(s)-V_{\rm o}(s)] \tag{10}$$

where v_o and i_o are the inverter output voltage and current, respectively; e_g is the gird voltage; $V_o(s)$, $I_o(s)$, and $E_g(s)$ are the Laplace transforms of v_o, i_o, and e_g in the frequency domain, respectively; *L* is the filter inductance; *R* is the line equivalent resistance; and *C* is the blocking capacitor. Substituting the operator *s* in (10) with $j\omega$, $I_o(j\omega)$ equals zero when $\omega = 0$ (dc). This indicates that the blocking capacitor can minimize the dc component effectively.

The current control loop diagram of the single-phase PV inverter with the blocking capacitor is shown in Fig. 4(b), where i_o^* is the reference current; *G*(*s*) is the controller transfer function, and K_{PWM} is the gain of pulse width modulator. If the capacitor voltage feedback terminal (1/*Cs*) is moved to the front of the pulse width modulator ($K_{\rm PWM}$), the control diagram can be equivalently transformed to the structure shown in Fig. 4(c). As seen, the blocking capacitor *C* in Fig. 4(b) is replaced with an integral and feedback block, the so-called virtual capacitor. This virtual capacitor can be implemented with software-based method and avoids the uses of physically large and expensive ac capacitors to block the dc component.

B. Mathematical Model of the Three-Phase PV Inverter With Blocking Capacitors in the Synchronous Frame

Based on the virtual capacitor concept in the single-phase system, this section aims to derive the three-phase system models with blocking capacitors in different frame and examine the suitability of applying the virtual capacitor concept to three-phase systems in each frame. Fig. 5 shows the circuit diagram of a three-phase PV inverter with blocking capacitors (*C*).

When deriving the mathematical model, the well-damped *LCL* filter in Fig. 5 is treated as an equivalent *L* filter at low frequencies [29]. The time-domain ac-side average model [30] in the stationary *abc* frame can be expressed as

$$\begin{cases} L\dfrac{di_a}{dt}+\dfrac{1}{C}\displaystyle\int i_a dt+Ri_a=e_a-v_a \\ L\dfrac{di_b}{dt}+\dfrac{1}{C}\displaystyle\int i_b dt+Ri_b=e_b-v_b \\ L\dfrac{di_c}{dt}+\dfrac{1}{C}\displaystyle\int i_c dt+Ri_c=e_c-v_c \end{cases} \tag{11}$$

where L is the equivalent inductance, which includes the inverter-side inductance L_1 and the grid-side inductance L_2. The definitions of other variables in (11) are denoted in Fig. 5. Especially, v_a, v_b, and v_c are the average values of inverter side voltage over a switching period. Note that the inverter duty cycle is not included in the average model in (11) to simplify the control design. A more rigorous inverter small-signal model can be found in [31].

With the coordinate transformation, the system mathematical model in stationary $\alpha\beta$ frame is given in

$$\begin{cases} L\dfrac{di_\alpha}{dt}+\dfrac{1}{C}\displaystyle\int i_\alpha dt+Ri_\alpha=e_\alpha-v_\alpha \\ L\dfrac{di_\beta}{dt}+\dfrac{1}{C}\displaystyle\int i_\beta dt+Ri_\beta=e_\beta-v_\beta. \end{cases} \tag{12}$$

In order to further derive the models in frequency domain on the synchronous rotational *dq* frame, complex vectors are synthesized from scalars in $\alpha\beta$ and *dq* frame as shown in

$$\begin{cases} \boldsymbol{f}_{\alpha\beta}=f_\alpha+jf_\beta \\ \boldsymbol{f}_{dq}=f_d+jf_q \end{cases} \tag{13}$$

where ***f*** is a general complex vector which can represent voltage and current.

With the complex vector expression in (13), the system model in α-β frame in (12) can be transformed to the complex vector form as given in

$$L\frac{di_{\alpha\beta}}{dt}+\frac{1}{C}\int \boldsymbol{i}_{\alpha\beta}\mathrm{d}t+R\boldsymbol{i}_{\alpha\beta}=\boldsymbol{e}_{\alpha\beta}-\boldsymbol{v}_{\alpha\beta}. \tag{14}$$

Correspondingly, the mathematical model in the frequency domain in the $\alpha\beta$ frame is given by

$$\boldsymbol{I}_{\alpha\beta}(s)=\frac{Cs}{LCs^2+RCs+1}[\boldsymbol{E}_{\alpha\beta}(s)-\boldsymbol{V}_{\alpha\beta}(s)]. \tag{15}$$

If the operator *s* of the stationary $\alpha\beta$ frame in (15) is substituted by the operator $s+j\omega$ in the synchronous frame [32], (15) can be transformed to (16) for the *dq* frame

$$\boldsymbol{I}_{\mathrm{dq}}(s)=\frac{C(s+j\omega)}{LC(s+j\omega)^2+RC(s+j\omega)+1} \times[\boldsymbol{E}_{\mathrm{dq}}(s)-\boldsymbol{V}_{\mathrm{dq}}(s)]. \tag{16}$$

Substituting (13) into (16), the mathematical model for the three-phase system with blocking capacitors in *dq* frame can be derived as

$$\begin{cases} I_d(s)(LCs^2+RCs-LC\omega^2+1)-I_q(s)(2LC\omega s \\ \quad +RC\omega)=[E_d(s)-V_d(s)]Cs-[E_q(s)-V_q(s)]C\omega \\ I_d(s)(2LC\omega s+RC\omega)+I_q(s)(LCs^2+RCs-LC\omega^2 \\ \quad +1)=[E_d(s)-V_d(s)]C\omega+[E_q(s)-V_q(s)]Cs. \end{cases} \tag{17}$$

As shown in (17), after adding blocking capacitors to the ac side of the power circuit, there are strong couplings between the *d*-axis and *q*-axis (e.g., i_d, i_q), which is very difficult to be decoupled. This indicates that the virtual capacitor concept applied to the three-phase inverters should not be in the standard synchronous rotational *dq* frame but in the stationary *abc* frame.

C. DC Component Minimization in Three-Phase PV Inverters With DC-Component Feed-Forward and PIR Controllers

Based on the above analysis, this section investigates how to implement the "virtual capacitor" concept for three-phase systems in the stationary frame and to be further integrated to the standard PV inverter current control loop in the *dq* frame with a PIR controller.

The standard three-phase inverter current loop normally adopts a proportional-integral (PI) controller in the *dq* frame to regulate the *d*-axis and *q*-axis currents. The PI controller in *dq* frame is equivalent to a proportional-resonant (PR) controller in the stationary *abc* frame [33, 34], given the resonant frequency of the R controller is selected as the line frequency (rotational frequency). Therefore, the current control loop of three-phase inverters with blocking capacitors in stationary *abc* frame can be represented as shown in Fig. 6(a), where the variables with the subscript *abc* denote the vectors of the three-phase voltages and currents. The gain of the pulse width modulator (K_{PWM}) is assumed to be unity to simplify the derivation.

The PR controller is effectively a proportional (P) controller if only the dc component is taken into account, and the diagram for the dc component is shown in Fig. 6(b), where the variables with the subscript *abc*0 denote the vectors of the three-phase dc components. If the capacitor voltage feedback terminal (1/*Cs*) in Fig. 6(b) is moved to the feedback path as shown in Fig. 6(c), where K_P is the proportional gain, the physical blocking capacitor *C* in Fig. 6(b) can then be replaced with an integral and a feed-forward term (algorithm). Thus, the virtual capacitors are achieved in a three-phase PV system in the stationary *a-b-c* frame.

To achieve the zero steady-state error for the dc component, Fig. 6(d) replaces the P controller in Fig. 6(c) with an integral (I) controller. Then, in order to apply the dc component minimization method to the standard dual closed-loop control system in a synchronous frame, Fig. 6(d) is then transformed to a mixed *abc* and *dq* frame as shown in Fig. 6(e). The reference current $\boldsymbol{i}^*_{abc0}$, the grid voltage $\boldsymbol{e}_{abc0}$, and the current controller is implemented in synchronous frame ($\boldsymbol{i}^*_{abc0}$, $\boldsymbol{e}_{abc0}$, and the I controller are transformed into $\boldsymbol{i}^*_{dq1}$, $\boldsymbol{e}_{dq1}$, and the R controller, respectively). The "virtual capacitor" in the feedback path is still implemented in the stationary *a-b-c* frame.

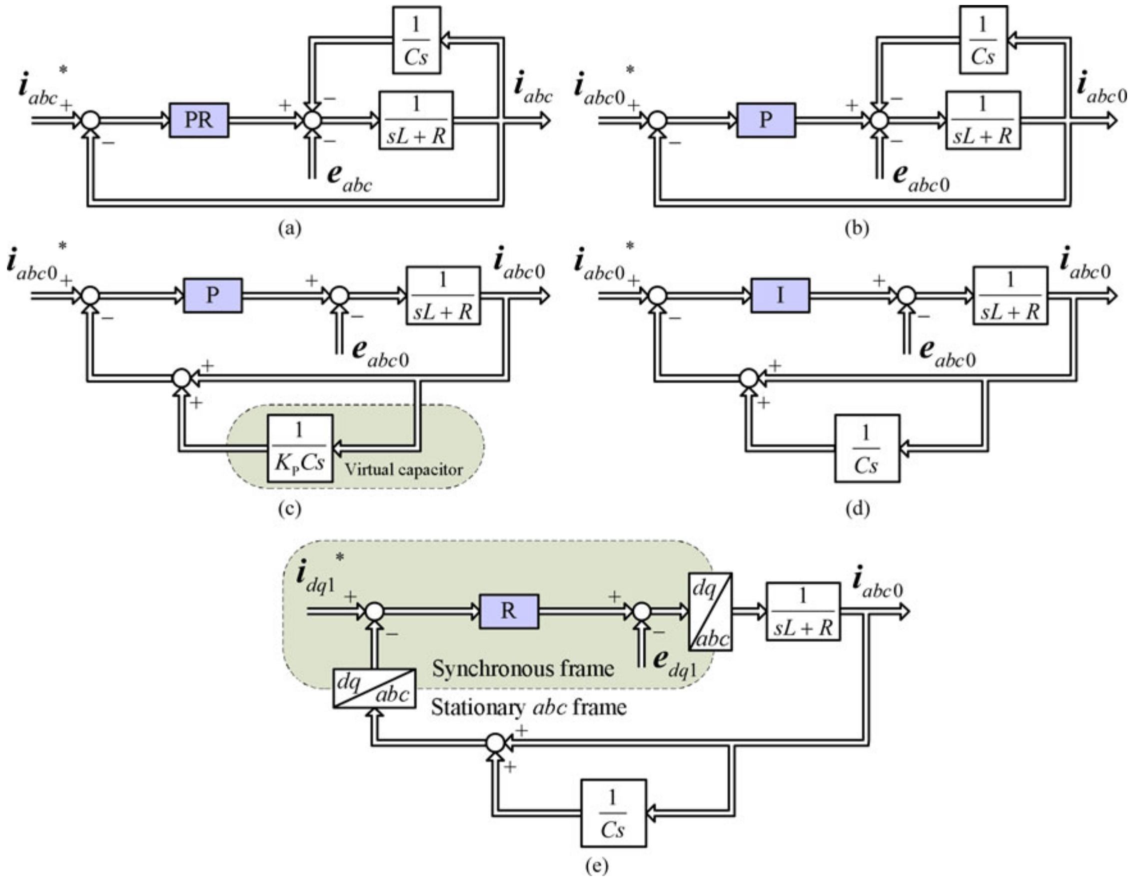


Fig. 6. Virtual capacitor implementation for a three-phase PV inverter: (a) current control loop in stationary *a-b-c* frame, (b) dc component control loop in stationary *a-b-c* frame, (c) equivalent transformation of the dc component control loop with virtual capacitor, (d) dc component control loop based on an integral (I) controller, and (e) dc component control loop in a mixed frame (*d-q* and *a-b-c*).

With this approach, the standard three-phase inverter control structure based on the *dq* frame can still be used. Only an additional R controller needs to be added to the conventional PI controller. In addition, a feed-forward term, representing the virtual capacitor, has been added to the current feedback path as shown in Fig. 6(e).

The new control structure based on the dc component feed-forward (in the feedback path of the inverter-side current [35]) and PIR controllers for dc component minimization is shown in Fig. 7. As derived in Section II, the dc component in the ac-side currents will appear in the inner current control loop (e.g., i_d, i_q) in the form of a negative-sequence line-frequency current. Therefore, the R controller and PI controller are combined into a PIR controller to provide a precise control for both the dc and line-frequency (negative sequence) signals for the current loop. The virtual capacitor concept is implemented by integrating the measured dc component, which is added as a feed-forward term on the feedback path, as shown in the dashed rectangle in Fig. 7. In the outer voltage loop, a PI controller is used to enable the dc link voltage u_{dc} to track the reference voltage u_{dc}^*, thus achieving maximum power point tracking (MPPT).

In Fig. 7, K_0 is the integral gain of the dc component and $K_0 = 1/C$. The larger the value of K_0 is, the smaller the virtual capacitor is, and the faster the integrator responses. However, smaller virtual capacitor will lead to larger fluctuations in the steady-state errors. On the other hand, smaller K_0 means larger virtual capacitor and slower integral responses. The steady-state errors become smaller and a stable operation of the PV systems is achieved. Since the dc minimization does not need a very fast response, a relatively small value of K_0 (large virtual capacitor) is suggested in this paper.

IV. DC COMPONENT EXTRACTION BASED ON SLIDING WINDOW ITERATION

In the control strategy shown in Fig. 7, an accurate dc component measurement and extraction is the key to implement the virtual capacitor concept and achieve the overall dc component minimization. As mentioned, the dc component needs to be minimized within 0.5% of the rated output current (e.g., IEEE Standard1547-2003). Compared with the ac component, the dc component is very small and an accurate dc component extraction is challenging. In PV inverters, the Hall-effect current sensors are widely used to measure the ac-side currents (including both ac and dc components) due to their smaller size, isolated output, and wide bandwidth (e.g., from dc to several hundred kilohertz) [36]. In this paper, an integral method based

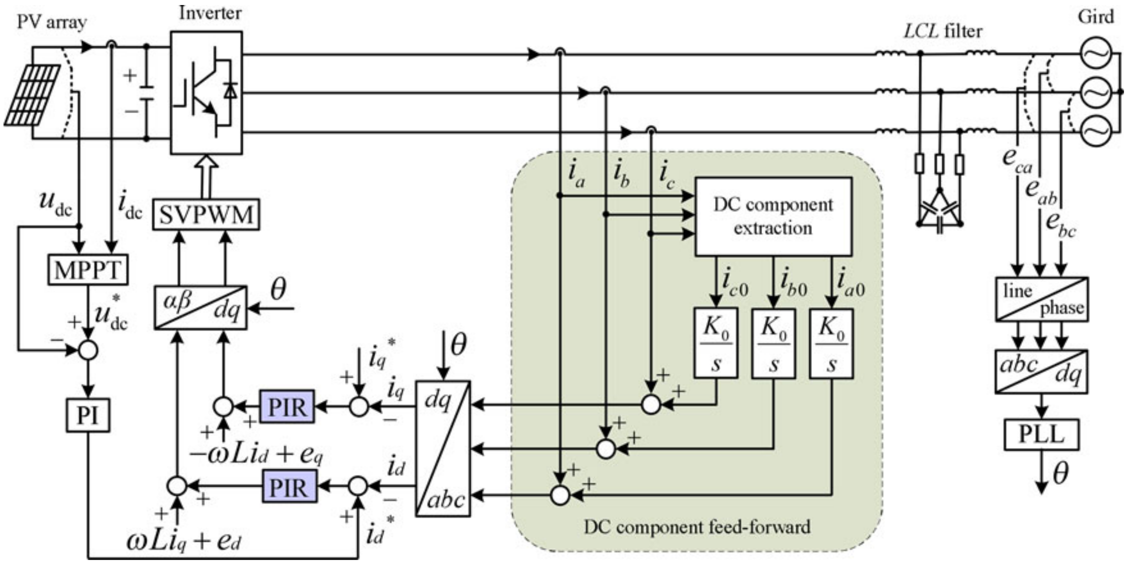


Fig. 7. DC component minimization strategy based on dc component feed-forward and PIR controllers.

on the sliding window iteration algorithm is used to accurately extract the dc component from the ac-side currents.

Taking the ac-side Phase A current i_a, for example, i_a can be expressed as in (18) if considering both the dc component and other ac components of different frequencies (e.g., harmonics)

$$i_a = i_{a0} + \sum_{h=1,2,3\cdots} I_h \sin(2\pi h f_1 t + \varphi_h) \tag{18}$$

where i_{a0} is the dc component, f_1 is the line frequency. I_h, hf_1, and φ_h are the amplitude, frequency, and phase angle of the fundamental and harmonic components. Averaging the integration of (18) in the interval from t_0 to $t_0 + T$ yields

$$\frac{1}{T}\int_{t_0}^{t_0+T} i_a dt = \frac{1}{T}\left[\int_{t_0}^{t_0+T} i_{a0} dt + \int_{t_0}^{t_0+T} \sum_{h=1,2,3\cdots} I_h \sin(2\pi h f_1 t + \varphi_h) dt\right]. \tag{19}$$

When $T = T_1 = 1/f_1$, the second term in the right side of (19) becomes

$$\int_{t_0}^{t_0+T_1} \sum_{h=1,2,3\ldots} I_h \sin(2\pi h f_1 t + \varphi_h) dt = 0. \tag{20}$$

Hence, with (19) and (20), the dc component i_{a0} can be obtained by

$$i_{a0} = \frac{1}{T_1}\int_{t_0}^{t_0+T_1} i_a dt. \tag{21}$$

The next step is to implement the expression in (21) to obtain the dc component i_{a0} accurately without significant calculation burden. If assuming the number of sampling times in a fundamental period (T_1) is *N*, *dt* in (21) can be substituted by the sampling interval Δt and $\Delta t = T1/N$. If τ is defined as *t*/*N*, then I_a $(k\tau)$ is the *k*th sampling value. Substituting the definite integration in (21) by the accumulation of the integrand, the discrete expression of i_{a0} is given by

$$i_{a0} = \frac{1}{N\Delta t}\sum_{k=0}^{N-1} i_a(k\tau)\Delta t = \frac{1}{N}\sum_{k=0}^{N-1} i_a(k\tau). \tag{22}$$

To achieve a real-time dc component extraction, (22) should accumulate the sampling values for *N*–1 times in one fundamental period. The amount of calculation is therefore significant given a high sampling frequency. To decrease the amount of calculation, sliding window iteration is used in (23) to replace (22)

$$\begin{aligned} i_{a0} &= \frac{1}{N}\sum_{k\,=\,N_{\mathrm{cur}}-N+1}^{N_{\mathrm{cur}}} i_a(k\tau) \\ &= \frac{1}{N}\sum_{k\,=\,N_{\mathrm{cur}}-N}^{N_{\mathrm{cur}}-1} i_a(k\tau) - i_a[(N_{\mathrm{cur}}-N)\tau] + i_a(N_{\mathrm{cur}}\tau) \end{aligned} \tag{23}$$

where N_{cur} is the sliding pointer which represents the current sampling point. After completing the summation of one fundamental period for initialization, *N*–1 additions of (22) is simplified as one addition and one subtraction of (23). As a result, the amount of calculation is reduced. The dc component calculation method based on the sliding window iteration is illustrated in Fig. 8.

If the frequency of the fundamental component is constant (e.g., fixed 50 or 60 Hz), the above calculation method is effective and accurate regardless of harmonic components. However, in practice, the line frequency may vary in a certain range (e.g., within 1%). Even though this variation is small, it will degrade the performance of the method. To test the performance of the dc-component extraction method under line-frequency deviation, the line frequency f_1 is set to be 49.5 Hz. The measured ac-side current signal i_a is assumed to be in the form as shown

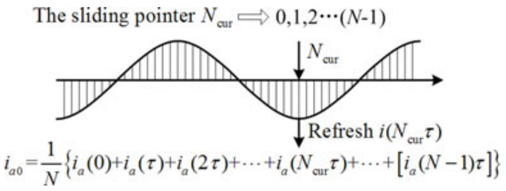


Fig. 8. Diagram of the dc component calculation based on the sliding window iteration.

in (24), which contains a dc component (step signal at 0.08 s), a fundamental component ($f_1 = 49.5$ Hz), and fifth- and seventh-order harmonics

$$i_a = 0.5\varepsilon(t-0.08) + 10\sin(2\pi f_1 t) + 1.5\sin(10\pi f_1 t) + 0.5\sin(14\pi f_1 t) \tag{24}$$

.

The dc component extraction method is implemented and tested in MATLAB/Simulink. Simulation results of the dc component extraction method under frequency deviation and with harmonics [in the form of (24)] are shown in Fig. 9. Fig. 9(a) shows the measured ac-side current signal which contains fifth- and seventh-harmonics as well as a dc component appearing from 0.08 s. Fig. 9(b) shows the dc component in the current signal with amplitude of 0.5 A. Fig. 9(c) shows the simulation results of the dc component extraction method. As seen, although the average value of the dc component is estimated correctly as 0.5 A, line-frequency fluctuation exists in i_{a0} because of the frequency deviation. However, compared to the original current i_a in Fig. 9(a), the ac components (including the harmonics) have been attenuated effectively. To further eliminate the ripple on the extracted dc component in Fig. 9(c), a second time integral is added over the result obtained in Fig. 9(c), with which the ripple can be effectively attenuated, and the result is shown in Fig. 9(d). As seen, the exact dc component can accurately reflect the original dc signal [shown in Fig. 9(b)] after a short transition time.

Note that the measuring time of one time integral is one line-frequency period T_1, and double time integral requires $2T_1$. With more integral times, the precision of the measurement is higher but the measuring time is longer. In practice, two time integrals can achieve both satisfactory precision and measuring speed.

In addition, dc biases (offset) in sensors, signal conditioning circuits, and A/D chips have negative impact on the component measurement as well. These biases should be calibrated either online or offline and need to be subtracted from the measuring results. In this way, the influence of the biases can be eliminated.

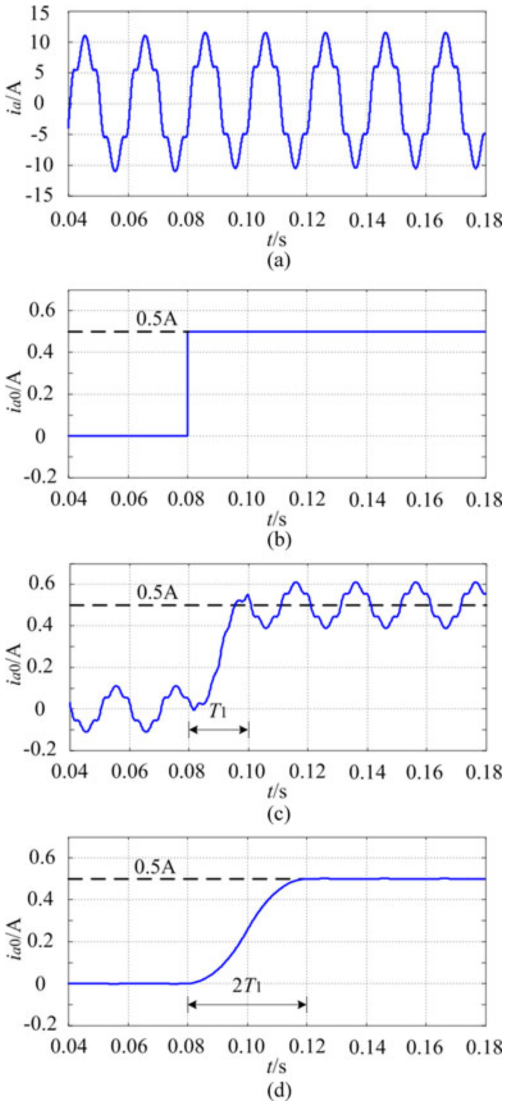


Fig. 9. Simulation results of the dc component extraction method with harmonics and frequency deviation: (a) the measured phase A current i_a, (b) the superposed dc component, (c) the dc component extraction result with one time integral, and (d) the dc component extraction result with two time integrals.

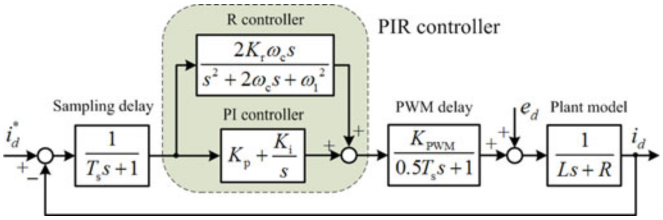


Fig. 10. d-axis current control loop based on the PIR controller.

V. PIR CONTROLLER DESIGN

As mentioned, when taking the dc component in the ac-side currents into account, the current loop in the dq frame is composed of both a dc component and a line-frequency component (negative sequence). The dc component in the rotational frame comes from the line-frequency ac components in the phase currents. The line-frequency component in the rotational frame comes from the dc component in the phase currents. To provide an effective control for both dc and line-frequency signals in the dq frame, a proportional-integral-resonant (PIR) controller is used. Taking the d-axis current control loop, for example, considering the sampling delay and the PWM delay, the current control loop based on the PIR controller is shown in Fig. 10, where T_s is the sampling period, K_p is the proportional gain, K_i is the integral gain, and K_r is the resonant gain. ω_1 is the resonant (center) frequency of the R controller, which is the same as the line frequency in this case. ω_c is the cutoff frequency of the R controller to reduce the sensitivity against the slight frequency variations [37].

In Fig. 10, the PI controller is used to regulate the dc component transformed from the fundamental currents. The R controller is used to regulate and minimize the line-frequency component transformed from the dc component. The parameters of the PI controller should be set to guarantee a good dynamic and steady-state performance of the current loop. The parameters of the R controller are set for the dc component minimization.

Regarding the PI controller, using the pole-zero compensation technique, controller gains can be selected as $K_p/K_i = L/R$. Considering dynamic response and stability, the parameters of the PI controller are set as $K_p = 2.7$ and $K_i = 300$ for $L = 2.7$ mH and $R = 0.3\ \Omega$.

An infinite gain at the resonant frequency of the R controller can eliminate the steady-state error. In the improved R controller with $2\omega_c$ added to the denominator as shown in Fig. 10 [34], the gain at the resonant frequency is limited yet with improved performance under line-frequency fluctuation. Nevertheless, the gain can be adjusted by K_r. Regarding ω_c, smaller ω_c provides better frequency selectivity but difficult for digital implementation. Larger ω_c leads to a wider bandwidth around the resonant frequency and a better robustness for the frequency deviation. However, the gain at the resonant frequency will be lower with a subsequent larger steady-state error. In practice, a value between 5–15 rad/s of ω_c has been found to provide a good compromise [38]. ω_c is selected as 5 rad/s in this paper.

Merging the small time constants in Fig. 10, the open-loop transfer function of the current loop can be expressed as, (25), shown at the bottom of the page.

Further, the equivalent open-loop transfer function with respect to the resonant gain $K_{\rm r}$ is given by, (26), shown at the bottom of the page.

With (26), the root locus of the current loop with K_r varying from 0 to infinite is represented in Fig. 11. As shown, when $K_r < 985$, the closed-loop characteristic roots are on the left-half plane, which indicates a stable system. K_r is selected as 69.5 in this case to achieve sufficient stability margin as well as relatively high gain around the resonant frequency.

The theoretical and experimental open-loop frequency responses of the current loop with the designed PIR controller are shown in Fig. 12. As seen, the experimental frequency response agrees well with the theoretical design. As expected, the bode plot has both high gain at dc and line-frequency. The phase margins (Pm = 58.1°) indicates that the designed current loop is stable [39].

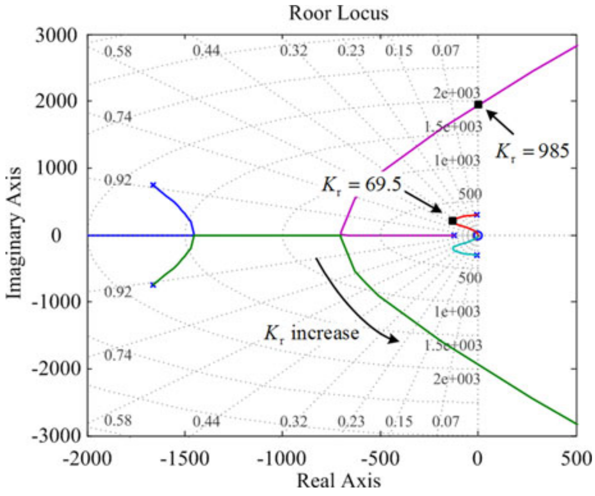


Fig. 11. Root locus of the current loop with K_r varying from 0 to infinite.

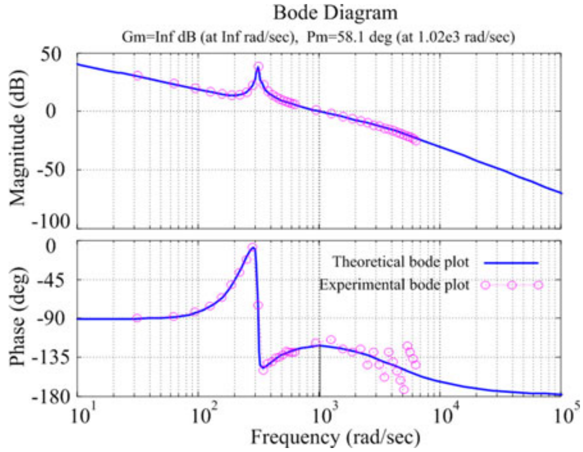


Fig. 12. Theoretical and experimental open-loop bode plot of the current loop with a PIR controller for $L = 2.7\,\mathrm{mH}$, $R = 0.3\,\Omega$, $\omega_c = 5\,\mathrm{rad/s}$, $K_p = 2.7$, $K_i = 300$, and $Kr = 69.5$.

In addition to the current control loop, the dc-link voltage loop can be designed [40]. Since the R controller only works on the line-frequency component in the rotational frame which comes from the dc component, and the dc component is very

$$H_{\rm o\_PIR}(s) = \left(\frac{1}{1.5T_{\rm s}s+1}\right) H_{\rm PIR}(s) \left(\frac{1}{Ls+R}\right) = \frac{K_{\rm p}s^3 + (2K_{\rm p}\omega_{\rm c} + K_{\rm i} + 2K_{\rm r}\omega_{\rm c})s^2 + (K_{\rm p}\omega_1^2 + 2K_{\rm i}\omega_{\rm c})s + K_{\rm i}\omega_1^2}{(1.5T_{\rm s}s+1)(s^3 + 2\omega_{\rm c}s^2 + \omega_1^2 s)(Ls+R)} \tag{25}$$

$$H_{K{\rm r}}(s) = \frac{2K_{\rm r}\omega_{\rm c}s^2}{\left(\begin{array}{l} 1.5LT_{\rm s}s^5 + (3LT_{\rm s}\omega_{\rm c} + L + 1.5RT_{\rm s})s^4 + (1.5LT_{\rm s}\omega_1^2 + 2L\omega_{\rm c} + 3RT_{\rm s}\omega_{\rm c} + R + K_{\rm p})s^3 \\ +(L\omega_1^2 + 1.5RT_{\rm s}\omega_1^2 + 2R\omega_{\rm c} + 2K_{\rm p}\omega_{\rm c} + K_{\rm i})s^2 + (R\omega_1^2 + K_{\rm p}\omega_1^2 + 2K_{\rm i}\omega_{\rm c})s + K_{\rm i}\omega_1^2 \end{array}\right)} \tag{26}$$

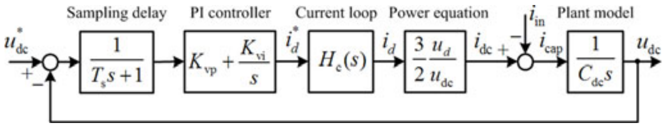


Fig. 13. DC-link voltage loop.

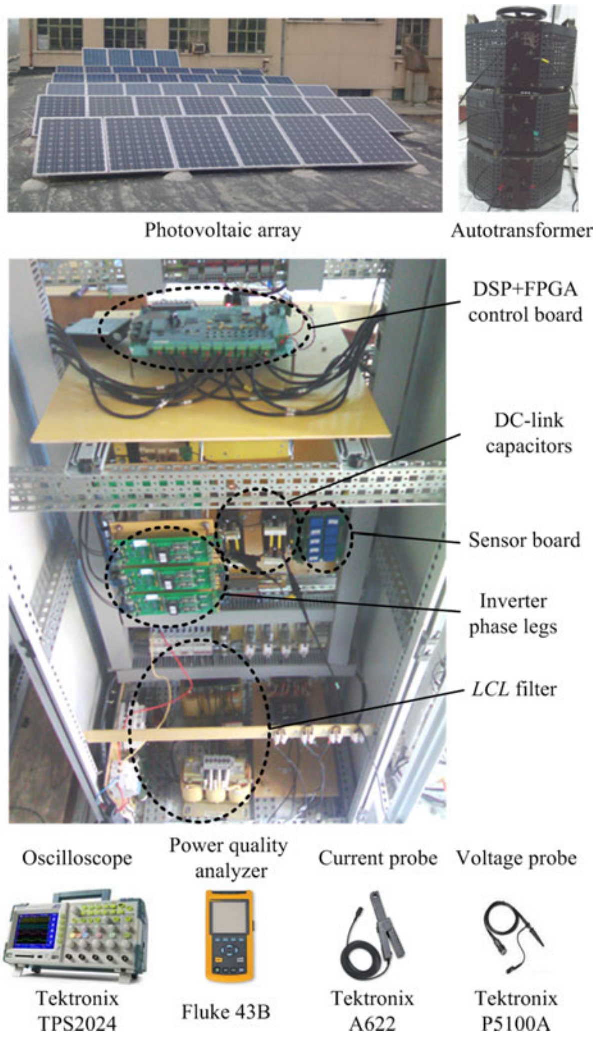


Fig. 14. Experimental setup and test equipment.

small compared with the ac component, the R controller can be neglected to simple the design of the dc-link voltage loop. Then, the close-loop transfer function of the current loop can be expressed as

$$H_\mathrm{c}(s) = \frac{K_\mathrm{i}K_\mathrm{PWM}}{1.5T_\mathrm{s}Rs^2 + Rs + K_\mathrm{i}K_\mathrm{PWM}} \approx \frac{K_\mathrm{i}K_\mathrm{PWM}}{Rs + K_\mathrm{i}K_\mathrm{PWM}}. \tag{27}$$

According to (7), and neglecting the switching losses, the equation between the active power of the ac side and the power of the dc side can be expressed as

$$\frac{3}{2}u_d i_d \approx u_\mathrm{dc} i_\mathrm{dc}. \tag{28}$$

TABLE I
PARAMETERS OF THE TEST SYSTEM

Symbol	Parameter	Value
S	Rated power	10 kVA
f_1	Line frequency	50 Hz
u_{RMS}	Grid phase voltage (RMS)	150 V
u_{dc}	Reference dc-link voltage	430 V
f_{PWM}	Switching frequency	5 kHz
T_s	Sampling period	0.2 ms
C_f	Capacitance of the *LCL* filter	4.7 μF
R_f	Damping resistor of the *LCL* filter	5 Ω
C_{dc}	DC-link capacitor	2200 μF
L_1	Inverter-side inductance	1.5 mH
L_2	Grid-side inductance	1.2 mH
K_p	Proportional gain of the current loop	2.7
K_i	Integral gain of the current loop	300
K_r	Resonant gain of the current loop	69.5
K_0	Integral gain of the dc component	25
K_{vp}	Proportional gain of dc-link voltage loop	3
K_{vi}	Integral gain of dc-link voltage loop	600

As shown in Fig. 1, the dc-side currents can be expressed as

$$\begin{cases} C_\mathrm{dc}\dfrac{du_\mathrm{dc}}{dt} = i_\mathrm{cap} \\ i_\mathrm{cap} = i_\mathrm{dc} - i_\mathrm{in}. \end{cases} \tag{29}$$

With (27)–(29), the dc-link voltage loop can be established as shown in Fig. 13 where K_{vp} and K_{vi} are the proportional gain and the integral gain of the dc-link voltage loop, respectively. Considering dynamic response and stability, as well as the ability of regulating the line-frequency dc-link voltage ripple, the parameters of the PI controller are set as $K_{vp} = 3$ and $K_{vi} = 600$ to achieve a cutoff frequency of 160 Hz with a larger loop gain at the line frequency.

VI. *Experimental Test and Results*

A 10-kVA transformerless three-phase grid-connected PV inverter system is set up to verify the proposed dc component minimization strategy. The power generated from the PV array is transferred to the grid via the inverter and a three-phase autotransformer. The PV array is composed of 42 serial-parallel-connected PV panels (every 14 panels in series then paralleled). The maximum power, open-circuit voltage, and short-circuit current of each panel are 240 W, 37.47 V, and 8.53 A, respectively, under the standard test conditions (Irradiance: 1000 W/m^2; Spectrum AM: 1.5; Module temperature: 25 °C). The hardware setup and the main measurement instruments are shown in Fig. 14. The control board is based on TI TMS320F28335 DSP and Spartan-3 XC3S400 FPGA. The DSP is mainly used for mathematical calculations and control algorithm implementation. The FPGA is used for PWM generation, inverter protection, and peripherals control.

The system parameters are given in Table I, including voltage and power ratings, filter components as well as parameters for the PIR controller of the current loop, the PI controller of the dc-link voltage loop (same as designed in Section V), and the integral gain for the dc component feed-forward term. The system switching frequency is 5 kHz.

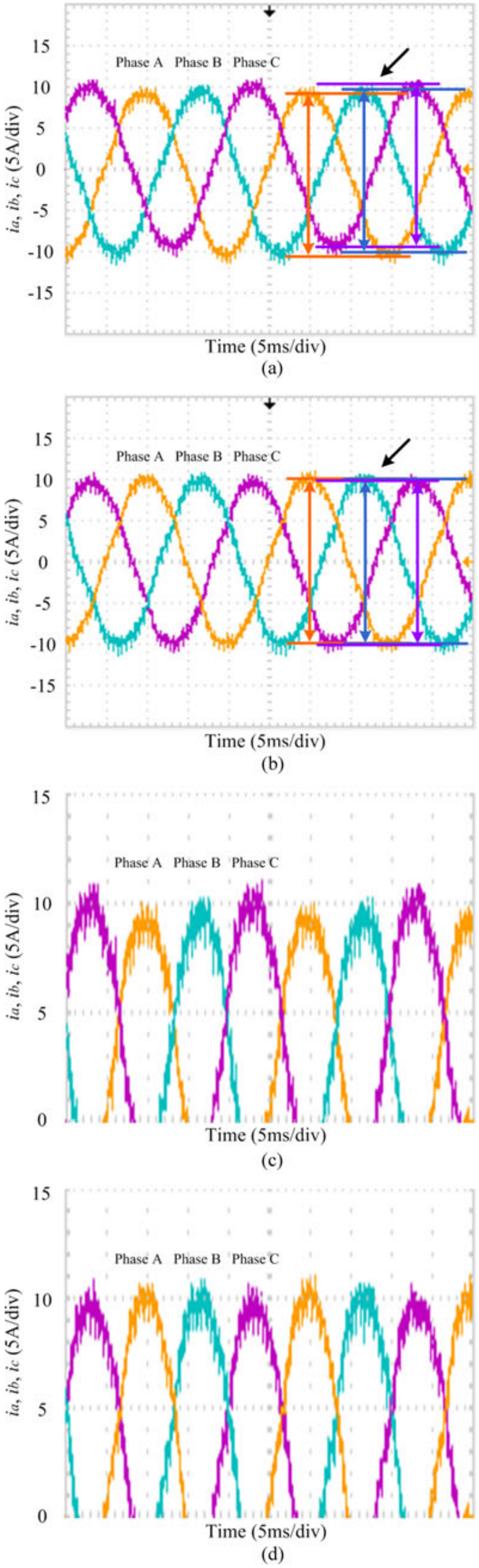


Fig. 15. Three-phase grid-side currents in the grid-connected PV inverters: (a) Without the proposed dc component minimization strategy. (b) With the proposed dc component minimization strategy. (c) Zoom-in detail of Fig. 15(a), and (d) Zoom-in detail of Fig. 15(b).

In order to clearly see the effectiveness of the control strategy on dc component minimization, bias voltages (2, 1, and −3 V) are superposed artificially on the measured grid voltages (e_a, e_b, and e_c), respectively, leading to large dc components in the ac-side currents. Then, the proposed control strategy is tested to verify the effectiveness of dc component minimization.

Fig. 15 shows the experimental results of the three-phase grid-side currents. The current reference is 7-A rms. As seen in Fig. 15(a), without applying the dc component minimization strategy, there are dc offsets in the three-phase currents. In comparison, as shown in Fig. 15(b), with the dc component minimization strategy, the dc components have been effectively reduced. In order to show the dc components (offset) of the three-phase currents more clearly, the upper half of the currents in Fig. 15(a) and (b) have been zoomed in as shown in Fig. 15(c) and (d), respectively.

Tables II and III further show the percentage of the dc component and each individual harmonics with and without the dc component minimization as well as the total THD. The results are obtained by the power quality analyzer (Fluke 43B). As seen in Table III, with the proposed dc component minimization strategy, both the dc component and the second-order harmonics (induced by the dc component as explained in Section II) in the three-phase currents are reduced, compared with the results shown in Table II. Especially, the dc component has been effectively attenuated below 0.5% as defined by IEEE Standard 1547-2003. In addition, the THD has also been reduced from (4.3%, 3.3%, and 3.8%) to (2.7%, 2.6%, and 2.8%), respectively. These results have shown the effectiveness of the proposed dc component minimization strategy.

Fig. 16(a) shows the transient response of the dc components when the proposed dc component minimization control is applied. As seen, the dc components have been successfully attenuated with the proposed strategy after the control is applied. Fig. 16(b) further shows the details of the dc components which are effectively attenuated between −0.0125 and 0.0125 A.

Fig. 17 shows the comparison of steady-state errors of the *d*-axis (Δi_d) and *q*-axis (Δi_q) currents with the standard PI controllers and the control strategy with PIR controllers, respectively. As explained in Section II, with the presence of dc component, there will be line-frequency component in the *d*-axis and *q*-axis currents. The standard PI controller has limited control capabilities at the line-frequency in the *dq* frame. As a result, there are steady-state errors in the *d*-axis and *q*-axis currents as shown in Fig. 17(a). In contrast, with the PIR controller, this error can be effectively attenuated with the resonant controller as shown in Fig. 17(b). Therefore, the *d*-axis and *q*-axis currents can track the reference well and the dc current is minimized.

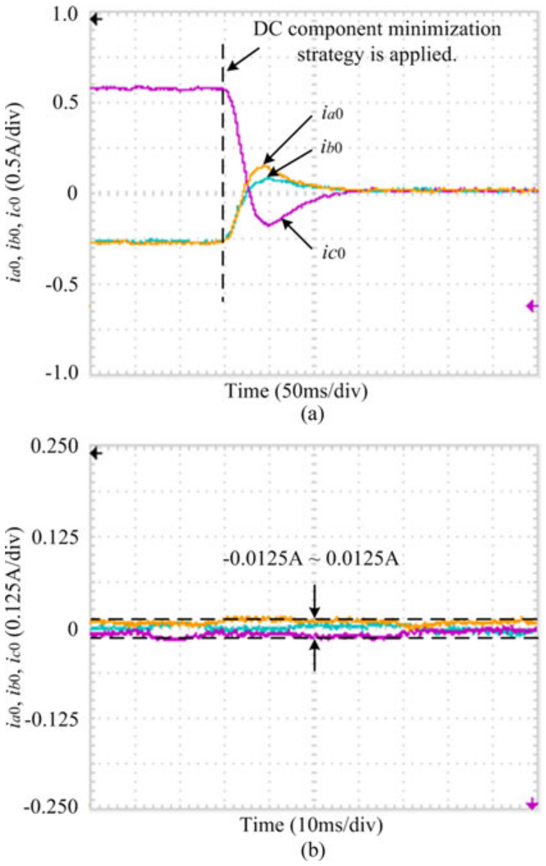
The inverter dc-link voltage and current waveform with and without the proposed dc component minimization strategy is further shown in Fig. 18. As explained in Section II, the dc component will cause line-frequency ripple on the dc-link voltage (power), which is evident as shown in Fig. 18(a). With the dc component minimization control, this ripple can be effectively reduced as shown in Fig. 18(b). This again validates the

TABLE II
HARMONICS AND THD OF THE THERE-PHASE CURRENTS WITHOUT THE DC COMPONENT MINIMIZATION STRATEGY

Three-phase Currents		Harmonics Order												**THD**
		DC	1	**2**	3	4	5	6	7	8	9	10	11	
i_a	Current value (A)	**0.31**	7.00	**0.23**	0.06	0.07	0.04	0.01	0.07	0.01	0.01	0.00	0.13	
	% of fundamental	**4.4%**	100%	**3.4%**	0.8%	1.0%	0.5%	0.1%	1.0%	0.1%	0.1%	0.0%	2.0%	**4.3%**
i_b	Current value (A)	**0.27**	6.97	**0.12**	0.04	0.08	0.07	0.02	0.06	0.01	0.01	0.01	0.13	
	% of fundamental	**3.8%**	100%	**1.7%**	0.6%	1.2%	1.0%	0.3%	0.8%	0.1%	0.1%	0.2%	1.9%	**3.3%**
i_c	Current value (A)	**0.57**	7.00	**0.21**	0.03	0.06	0.05	0.02	0.06	0.01	0.02	0.03	0.11	
	% of fundamental	**8.2%**	100%	**3.0%**	0.4%	0.8%	0.7%	0.3%	0.8%	0.2%	0.3%	0.4%	1.6%	**3.8%**

TABLE III
HARMONICS AND THD OF THE THERE-PHASE CURRENTS WITH THE DC COMPONENT MINIMIZATION STRATEGY

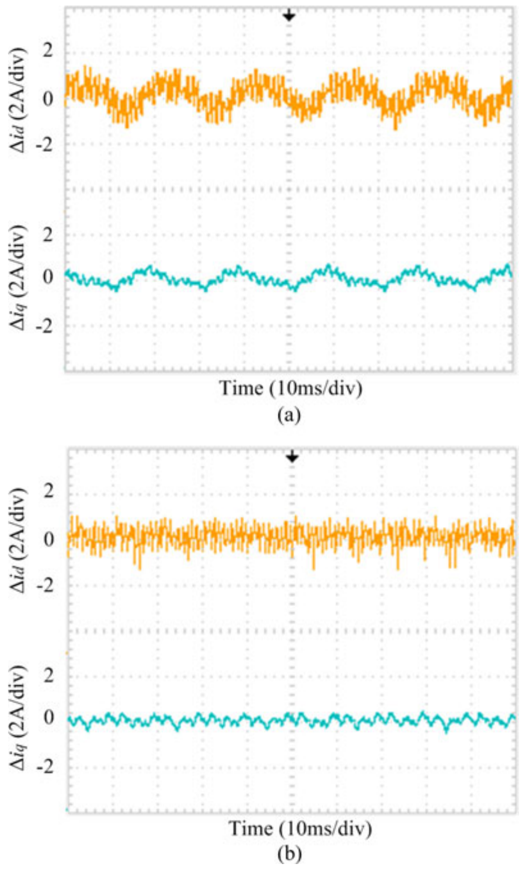
Three-phase Currents		Harmonics Order												**THD**
		DC	1	**2**	3	4	5	6	7	8	9	10	11	
i_a	Current value (A)	**0.00**	6.97	**0.04**	0.08	0.06	0.05	0.00	0.09	0.00	0.01	0.00	0.11	
	% of fundamental	**0.0%**	100%	**0.06%**	1.2%	0.8%	0.7%	0.0%	1.3%	0.0%	0.1%	0.0%	1.5%	**2.7%**
i_b	Current value (A)	**0.01**	7.00	**0.04**	0.04	0.04	0.06	0.01	0.11	0.02	0.01	0.01	0.11	
	% of fundamental	**0.2%**	100%	**0.5%**	0.5%	0.6%	1.0%	0.2%	1.5%	0.3%	0.1%	0.1%	1.5%	**2.6%**
i_c	Current value (A)	**0.01**	6.94	**0.07**	0.02	0.04	0.13	0.01	0.06	0.01	0.01	0.01	0.08	
	% of fundamental	**0.1%**	100%	**1.0%**	0.3%	0.5%	2.0%	0.2%	0.8%	0.1%	0.1%	0.1%	1.2%	**2.8%**



(a)

(b)

Fig. 16. DC components (a) transient response when the proposed dc component minimization strategy is applied, and (b) close up view after the control strategy is used.



(a)

(b)

Fig. 17. Steady-state errors of d-axis (Δi_d) and q-axis (Δi_q) current with (a) PI controller and (b) PIR controller.

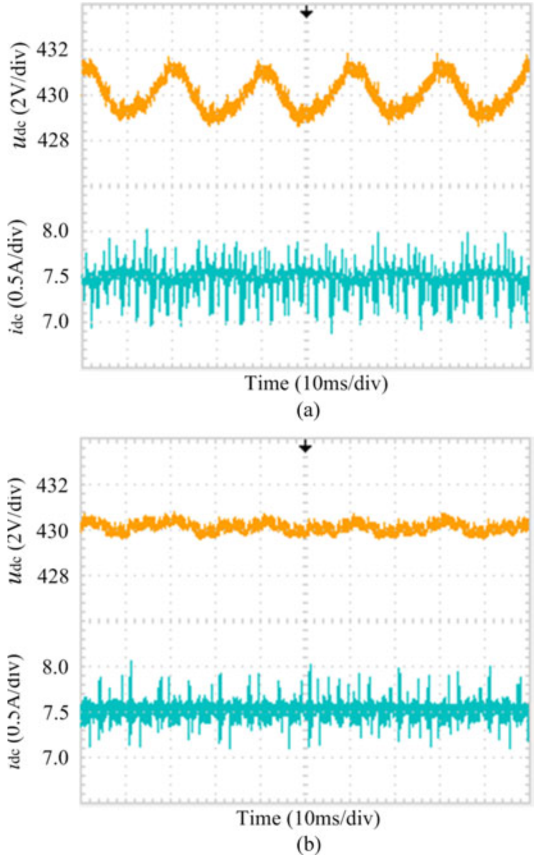


Fig. 18. Inverter dc-link voltage and current: (a) without the proposed dc component minimization strategy, (b) with the proposed dc component minimization strategy.

proposed dc component minimization strategy and its impact on the system performance.

VII. CONCLUSION

This paper has presented an effective method to minimize the dc component in a three-phase transformerless grid-connected PV system. The dc component can introduce line-frequency power ripple in the system and further cause dc-link voltage ripple and second-order harmonics in the ac currents. A software-based "virtual capacitor" approach has been implemented to minimize the dc component via a feed-forward of the dc component. The dc component can be accurately obtained using the sliding window iteration and double time integral even under frequency variation and harmonic conditions. A PIR controller has been designed to enable the precise regulation of both the dc and line-frequency components in the *d*-*q* frame. Experimental results have validated the proposed method, where the dc component has been reduced below 0.5% and the dc-link voltage ripple has been attenuated as well.

The proposed method can be well adopted in the existing PV systems for dc component minimization by adding software programs for dc-component extraction, dc-component feed-forward term as well as the resonant controller in the current control loops.

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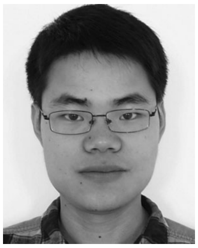

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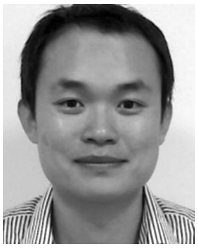

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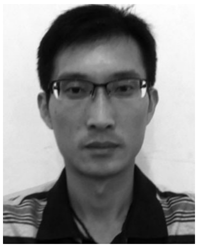

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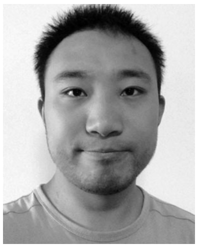

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