Extended Application of D-Σ Digital Control to a Single-Phase Bidirectional Inverter With an *LCL* Filter

Tsai-Fu Wu, *Senior Member, IEEE*, Li-Chiun Lin, Ning Yao, Yu-Kai Chen, *Member, IEEE*, and Yuan-Chih Chang, *Member, IEEE*

***Abstract*—Division-summation (D-Σ) digital control has been successfully applied to the single-phase bidirectional inverter with an *LC* filter, which can cover wide inductance variation and achieve precise inverter current tracking. However, high frequency ripple current injection to the grid cannot be avoided, and an *LCL* filter is therefore required. Since there typically exist grid voltage harmonics, the injected grid current will contain harmonic components due to the effect of the *LCL*-filter capacitor. This paper presents an extended application of the D-Σ digital control associated with a filter-capacitor-current compensation to reduce the injected grid-current harmonics. The control laws of the inverter with the D-Σ digital control and compensation approach are derived in detail, and the reduction of grid-current harmonics is analyzed. With the proposed approaches, the phase margin between the output impedance of the inverter and grid impedance can be higher than 80° from low to high frequencies, and the inverter can achieve high harmonic voltage rejection ratio up to 39th harmonic, which is relatively suitable for weak grid connection. Experimental results measured from a 5-kW single-phase bidirectional inverter have verified the feasible application of the D-Σ digital control and proposed compensation.**

***Index Terms*—Division-summation (D-Σ) digital control, dc distribution system, grid connection (GC), *LCL* filter, power factor correction (PFC), wide inductance variation.**

I. Introduction

SINGLE-PHASE bidirectional inverters have been adopted widely for dc-microgrid applications, of which they can operate in grid-connection mode (GC) or rectification mode with power factor correction (PFC). Fig. 1 shows a conventional inverter with a typical *LCL* filter [1]–[7] to improve grid-current harmonics which are caused by switching action and grid-voltage distortion. However, the inverter with an *LCL* filter is subjected to instability issue, which in turn will result in grid-current distortion. Many attempts have been proposed for single-phase inverters [3]–[15] and three-phase ones [16]–[19] to stabilize system operation and reduce grid-current harmonics due to distorted grid voltage. Conventionally, the inverters were modulated with SPWM or SVPWM as voltage sources and with various controls, such as adaptive current control sensing all of the state variables of the *LCL* filter [4], proportional-resonant and repetitive control [5], current feedback [11], [12], full feedforward of grid voltage [13] and multisliding surface [14]. These control strategies can improve gird current with low distortion, while their output impedances have not been presented to investigate the stability of a grid-connected inverter with an *LCL* filter and finite grid impedance. The author [6] has proposed an impedance-based stability criterion for the inverter and this concept has been further deducted by Yang *et al.* [7] to propose an impedance shaping approach for improving stability when the inverter is connected to a weak grid condition. The impedance shaping approach [7] is feasible, but the output impedance of the inverter at low frequency is close to the phase of −90°. This will result in oscillation when the grid impedance is high (i.e., a weak grid condition). Similarly, the studied inverter [7] was modulated with SPWM as a voltage source, controlled by a PI controller, and filtered with an *LCL* filter to yield grid current. This kind of control is somewhat loose and sluggish, and its output impedance is not high enough that the inverter cannot be modeled as a current source. Moreover, the inverter inductance varying with its current has not been considered in the

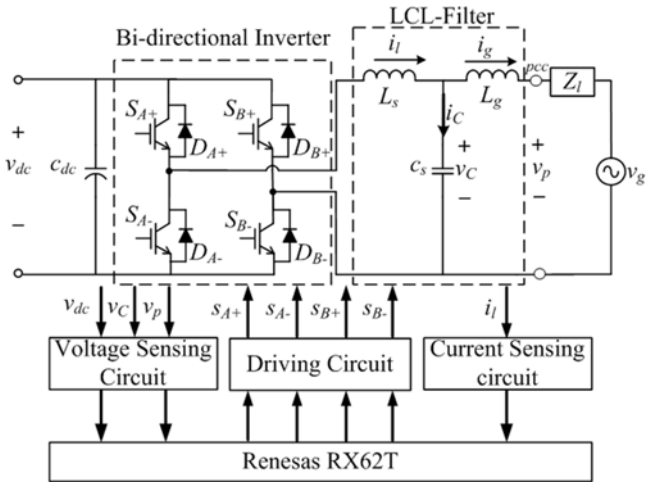

Fig. 1. Circuit diagram of a single-phase bidirectional inverter with an *LCL* filter and its control blocks.

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controller design, which might result in instability at high-power applications.

Recently, the researchers [20], [21] have proposed the D-Σ digital control for single-phase and three-phase inverters with *LC* filters to cover wide inductance variation and to track sinusoidal inverter current reference precisely. With an *LC* filter and D-Σ control, however, the grid-current distortion due to switching action and grid-voltage harmonics has not been improved yet. This paper presents an extended application of the D-Σ digital control associated with filter-capacitor-current compensation (FCCC) to a single-phase bidirectional inverter with an *LCL* filter and with wide filter-inductance variation. The proposed approach will modify the inverter current reference to cover the capacitor current under distorted line voltage, which in turn can shape grid current sinusoidally. Theoretical analysis of the proposed method is first presented and the impedance-based stability analysis [6] is adopted to investigate the stability of the inverter with an *LCL* filter and finite-grid impedance. Experimental results measured from a 5-kW single-phase bidirectional inverter are presented to verify the analysis and discussion.

As described in [20] and [21], the inverters with wide inductance variation (over seven times), due to soft-saturation core material, will cause current oscillation and result in high current ripple which will affect the current tracking accuracy. The generally used core materials for inverters are ferrite (gapped), molybdenum permalloy powder (MPP), or high flux. Ferrite core has to be added with air gap to increase its saturation margin, but for its low flux density [22]–[24], its volume will be much larger than the others with the same saturation point. Thus, in this study, the inductors constructed with MPP core are adopted.

II. Review of D-Σ Digital Control

For GC and rectification applications, control systems are used to track grid-current references. With a digital control system, only can the total inductor-current variation and error over one switching cycle be compensated to determine the next-cycle control. Thus, in deriving the control laws for the inverter with the D-Σ control, one switching cycle is first divided into two time intervals, corresponding to two operational modes, and each of which is corresponding to a portion of the total current variation. The two portions are then summarized to obtain the total inductor-current variation over one switching cycle. In the following, derivations of the control laws for GC and rectification modes are reviewed and presented [20].

A. GC Mode

In GC mode and with bipolar operation, the operational principle of the full-bridge inverter shown in Fig. 1 is similar to that of two buck converters operated in positive and negative half-line cycles, respectively.

1) Division (D): Based on the buck-converter operational principle, it will lead to two operational modes, magnetization and demagnetization of the inductor, within one switching period. Thus, we can divide one period into two portions and apply KVL to yield the following state equations:

$$\Delta i_{l,\mathrm{mag}} = \frac{v_{\mathrm{dc}} - v_c}{L_s(i_l)} dT_s \tag{1}$$

and

$$\Delta i_{l,\mathrm{dem}} = -\frac{v_{\mathrm{dc}} + v_c}{L_s(i_l)}(1-d)T_s \tag{2}$$

where T_s is the switching period, $L_s(i_l)$ is the measured inductance which is a function of inductor current i_L, and d denotes a duty ratio.

2) Summation (Σ): The total current variation over one switching period can be obtained by summarizing the previous two state equations, which can be expressed as

$$\Delta i_L = \frac{v_{\mathrm{dc}} - v_c}{L_s(i_l)} dT_s - \frac{v_{\mathrm{dc}} + v_c}{L_s(i_l)}(1-d)T_s \tag{3}$$

where

$$\Delta i_l = \Delta i_{l,\mathrm{mag}} + \Delta i_{l,\mathrm{dem}}.$$

From (3), the control law, d_{GC}, for GC mode can be determined as

$$d_{\mathrm{GC}} = \frac{1}{2} + \frac{v_c}{2v_{\mathrm{dc}}} + \frac{\Delta i_l \cdot L_s(i_l)}{2v_{\mathrm{dc}} \cdot T_s}. \tag{4}$$

The digital control uses reference current difference $(\Delta I_{gr}(n+1) = I_{gr}(n+1) - I_{gr}(n))$ as a feedforward signal and the current error $(\Delta i_l(n) = I_{gr}(n) - i_l(n))$ to derive the control for next switching cycle. Finally, the total current difference $\Delta i_l(n+1)$ at time step n+1 can be expressed as follows:

$$\Delta i_l(n+1) = \Delta I_{\mathrm{gr}}(n+1) + K_p \cdot \Delta i_l(n). \tag{5}$$

To be consistent with the feedforward gain, compensation gain K_p is chosen to be unity. With the information of $\Delta i_l(n+1)$, the control d_{GC} shown in (4) can be obtained to control the switches shown in Fig. 1, and it is expressed as

$$d_{\mathrm{GC}}(n+1) = \frac{1}{2} + \frac{v_c(n)}{2v_{\mathrm{dc}}(n)} + \frac{(\Delta I_{\mathrm{gr}}(n+1) + \Delta i_l(n)) \cdot L_s(i_l)}{2v_{\mathrm{dc}} \cdot T_s}. \tag{6}$$

B. Rectification Mode

When the bidirectional inverter is operated in rectification mode with PFC, the inverter acts like a boost converter which is just the complementary operation of a buck converter in GC mode. The control law of d_{Rec} in rectification mode can be determined as

$$\begin{aligned} d_{\mathrm{Rec}}(n+1) &= \overline{d_{\mathrm{GC}}}(n+1) = 1 - d_{\mathrm{GC}}(n+1) \\ &= \frac{1}{2} + \frac{v_c(n)}{2v_{\mathrm{dc}}(n)} + \frac{(\Delta I_{\mathrm{gr}}(n+1) + \Delta i_l(n)) \cdot L_s(i_l)}{2v_{\mathrm{dc}} \cdot T_s}. \end{aligned} \tag{7}$$

With the control law, the D-Σ digital control can track the inverter current reference precisely cycle by cycle to yield sinusoidal inverter current i_l.

III. FCCC

In the previous design and implementation of an inverter with an *LC* filter [20], [21], current-tracking command I_{gr} for inverter current i_l is a fundamental sinusoidal function. With the D-Σ control, the inverter can track I_{gr} precisely for the inverter current. However, grid-current i_g distortion will become serious when the inverter is with an *LCL* filter and the grid has significant voltage harmonics. It can be proved that when grid voltage v_g contains harmonics, filter-capacitor current i_c, as shown in Fig. 1, will also contain harmonic components. Thus, to inject fundamental sinusoidal current waveform into the grid, the new current reference, i^*_{lr}, for the inverter current i_l should be determined as

$$i^*_{lr} = I_{\rm gr} + \tilde{i}_c \tag{8}$$

where

$$I_{\rm gr} = I_M \sin(\omega T_S) \tag{9}$$

is the grid reference current and $\tilde{i}_c$ is the estimated capacitor current which can be calculated as follows:

$$\tilde{i}_c = \frac{C_s(v_c(n+1) - v_c(n))}{T_s} \tag{10}$$

where $v_c(n+1)(=\tilde{i}_c)$ can be estimated as follows:

$$\tilde{v}_c(n+1) = v_p(n) + \frac{L_g(I_{\rm gr}(n+1) - I_{\rm gr}(n-1))}{T_S} \tag{11}$$

where $v_c(n)$ is the sensed capacitor voltage and $v_p(n)$ is the sensed voltage at PCC. Reference I_{gr} is in phase with voltage v_p and I_M is the amplitude of I_{gr}. The proposed compensation scheme is designed to filter out the effect of capacitor current containing low harmonic components up to 60×39th Hz (= 2.34 kHz). The design rule of the filter can be found from [25]. In this study, $L_s = 1.5$ mH, $L_g = 500$ μH, and $C_s = 10$ μF were selected. With the FCCC and the D-Σ control, the inverter can track the modified current reference i^*_{lr} precisely for inverter current i_l, which can ensure sinusoidal current (i_g) injection to the grid. An overall control block diagram in s-domain is shown in Fig. 2.

Conventionally, a single-phase inverter was modulated with SPWM to become an ac voltage source with the amplitude of $MV_{\rm dc}$, where *M* is the modulation gain and $V_{\rm dc}$ is the dc-side voltage. During grid-current tracking control, the compensated current error will tune the modulation gain and go through the *LCL* filter to yield the output grid current i_g. This control process for grid-current tracking is typically sluggish and loose. Unlike the conventional approach, the proposed is to control the inverter to be a current source i_l and it is compensated with an estimated capacitor current $\tilde{i}_c$. With this control process, it is equivalent that the current $(i_l - \tilde{i}_c)$ will be just filtered through an inductor L_g to yield grid current i_g, as shown in Fig. 2(a). Thus, the grid current can be controlled tightly and with fast response. Moreover, the output impedance Z_o can have high phase margin with respect to grid impedance Z_l, which can ensure stability under weak grid condition. Note that in the digital implementation, the v_C in (6) and (7) is substituted with $\tilde{i}_c(n+1)$.

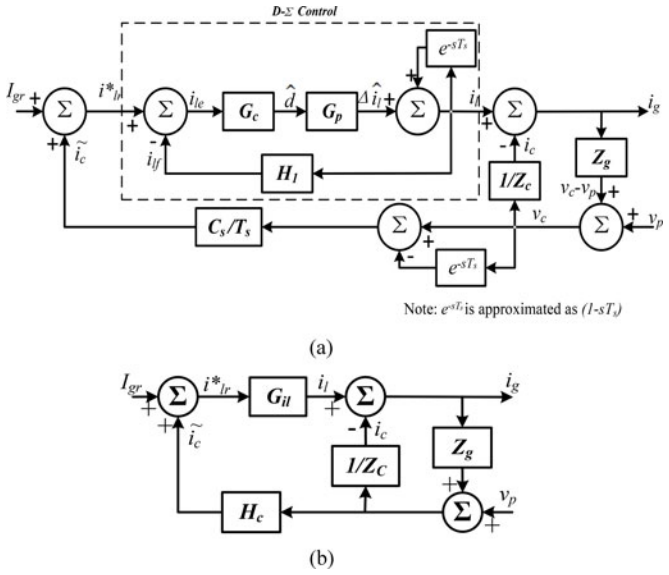

Fig. 2. Control block diagram of the proposed FCCC and based on D-Σ digital control: (a) s-domain model and (b) equivalent transformation.

In Fig. 2(a), the inner inverter-current plant $G_p(=\Delta\hat{i}_l/\hat{d}$ can be derived from the control law shown in (6) as follows:

$$G_p = \frac{\partial \Delta i_l}{\partial d} = \frac{\Delta \hat{i}_l}{\hat{d}} = \frac{2v_{\rm dc}T_S}{L_S}. \tag{12}$$

The compensator G_c is designed as

$$G_c = \frac{1}{G_p} = \frac{L_S}{2v_{\rm dc}T_S} \tag{13}$$

which can cancel the variation of inductance L_s, dc-voltage $v_{\rm dc}$ and switching period T_s, increasing robustness of grid-current tracking. The rest of the parameters shown in Fig. 2(a) are given as follows: $H_1 = 1$, $Z_g = sL_g$, $Z_C = 1/sC_s$, and e^{-sT_s} is approximated with a first-order Taylor series, $(1 - sT_s)$. An equivalent transformation of the control block diagram in Fig. 2(a) is shown in Fig. 2(b), in which

$$G_{il} = \frac{G_cG_p}{1 + G_cG_pH_1 - e^{-sT_s}} \tag{14}$$

and

$$H_c = \frac{C_s(1 - e^{-sT_s})}{T_s}. \tag{15}$$

To investigate the tracking capability of grid current i_g to its reference I_{gr}, harmonic voltage rejection ratio of i_g to v_p, and grid impedance accommodatibility, the following transfer functions are derived:

$$G_{ig} = \left.\frac{i_g}{I_{\rm gr}}\right|_{v_p=0} = \frac{G_{il}}{1+T} \tag{16}$$

$$G_{iv} = \left.\frac{i_g}{v_p}\right|_{I_{\rm gr}=0} = \frac{-T}{Z_g(1+T)}. \tag{17}$$

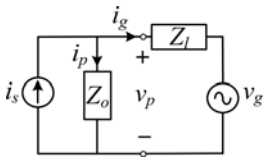

Fig. 3. Equivalent circuit of the controlled current-source inverter connected to the grid with grid impedance Z_l.

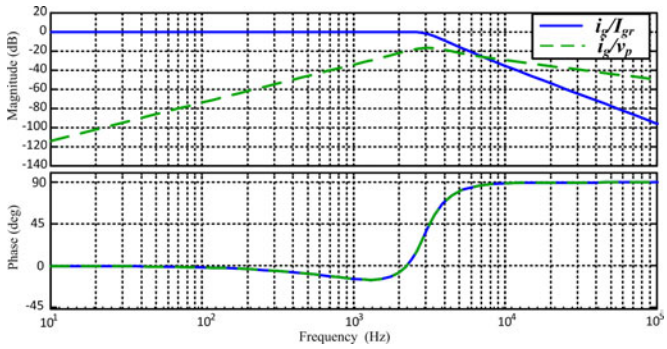

Fig. 4. Bode plots of grid reference current I_{gr} to grid current i_g transfer function (i_g/I_{gr}) and grid voltage v_g to grid current i_g transfer function (i_g/v_g).

And Z_o by definition is shown as follows:

$$Z_o = \frac{-1}{G_{iv}} = \frac{Z_g(1+T)}{T} \tag{18}$$

where the loop gain T is expressed as

$$T = \frac{Z_g}{Z_c} - H_c Z_g G_{il}. \tag{19}$$

An equivalent circuit of the grid-connected inverter can be represented in a Norton-equivalent-circuit form, as shown in Fig. 3, where Z_l denotes the grid impedance.

Based on the previous transfer functions, the Bode plots of i_g/I_{gr} and i_g/v_p are shown in Fig. 4, from which it can be observed that at frequency below 2.5 kHz, grid current i_g can track its reference I_{gr} tightly, and reject the harmonic voltage of v_p with 40 dB/dec. Note that there exists around 10° phase lagging at frequency between 600 Hz and 2 kHz, but it will not affect the tracking capability at fundamental frequency. Since high-order harmonic components are typically not significant, the phase lagging will not deteriorate in harmonic-voltage rejection. Moreover, the tracking capability and rejection ratio are independent of L_s. The impedance plots of Z_o and Z_l are shown in Fig. 5, in which Z_l is assumed to be a resistor 0.01 Ω in series with an inductor 1 mH. It can be seen that at the intersection point of Z_o and Z_l, the phase margin is around 80°, and at higher Z_l, the phase margin will be always 90°. Again, the impedance of Z_o is independent of L_s of which its inductance varies with the current over wide range. It can be also observed that the proposed approach yields high output impedance (80 dB) at line frequency 60 Hz. The limitation of the proposed approach is that the dc-side voltage $V_{\rm dc}$ must be higher than $v_C (= i_g(Z_g + Z_l) + v_g)$ to ensure control freedom.

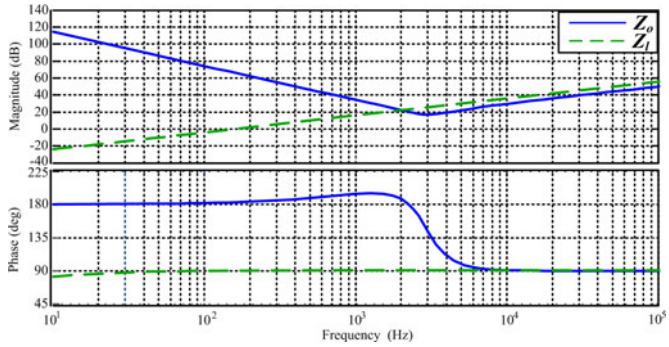

Fig. 5. Bode plots of inverter output impedance Z_o and grid impedance Z_l.

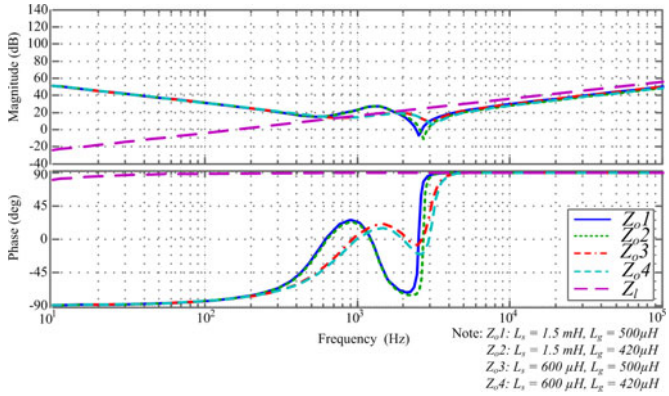

Fig. 6. Impedance plots of Z_l and Z_o under a conventional SPWM approach and with variable inductance L_s and L_g.

In fact, it is natural that only when $v_{\rm dc}$ is higher than v_C, the inverter current i_l can be controlled.

For comparison, the impedance plots of Z_o and Z_l under a conventional SPWM approach with a PI controller and with variable inductance L_s and L_g are shown in Fig. 6. It can be seen that output impedance Z_o varies with L_s and L_g; it is only 40 dB at 60 Hz, and when L_s is with higher inductance (1.5 mH), the phase margin is only around 15°. Moreover, when Z_l increases, the intersection point of Z_l and Z_o will move toward low frequency, resulting in phase margin even lower than 5° and having stability problems. Note that higher inductance L_s is necessary for an inverter with bipolar operation to reduce current ripple. An overall block diagram for implementing the D-Σ control law and the FCCC with time step indicated is shown in Fig. 7.

IV. Experimental Results

In the experiment, the grid voltage v_g is 220 V and the frequency is 60 Hz. Based on the aforementioned specification and analysis, parameter design of the power stage is summarized in Table I. The inverter inductance varies from 1.5 mH to 600 μH, the switching frequency is 20 kHz, the capacitance C_s is 10 μF, and inductance L_g varies from 500 to 420 μH. The power diodes are realized with silicon carbide, which have no reverse recovery

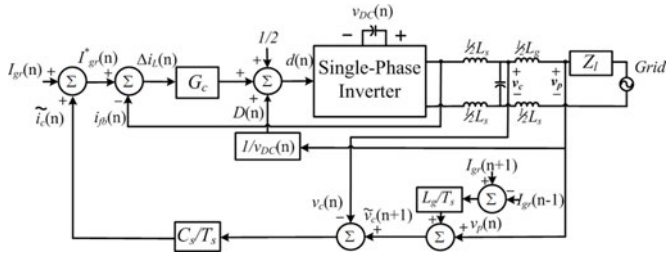

Fig. 7. Control block diagram for implementing the proposed FCCC and D-Σ digital control with time step indicated.

TABLE I
SYSTEM PARAMETERS OF THE INVERTER PROTOTYPE

Parameters	Symbols	Values
DC-bus voltage	v_{DC}	360–400 V
AC output voltage	v_{N}	220 V_{rms}
Maximum rated power	P_{max}	5 kW
Line frequency	f_l	60 Hz
Inverter inductors	L_s	600 μH–1.5 mH
Filter capacitor	C_s	10 μF
Inductance	L_g	420–500 μH
Grid inductance	L_l	2 mH, 5 mH
Power switch	IGBT G40N60A4	$V_{CE}(on)typ. = 1.28$ V, $V_{CES} = 600$ V, and $I_{C(TC=25°C)} = 70$ A
Power diode (silicon carbide)	CREE C3D20060D	$V_{F(TJ=25°C)}$typ. $= 1.5$ V Zero-recovery time
Switching frequency	f_s	20 kHz

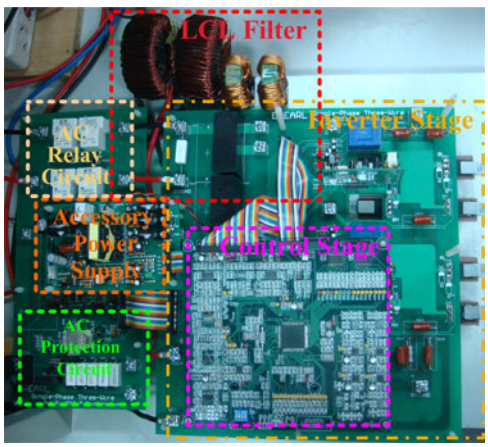

Fig. 8. Photograph of the designed single-phase bidirectional inverter system.

time. A photograph of the designed single-phase bidirectional inverter is shown in Fig. 8.

The harmonic components of the output currents were measured up to 20th harmonic with a power analyzer WT1600. The test conditions of grid voltage harmonics are based on a programmable ac source, Chroma 61512, which can provide up to 39th harmonic for the ac voltage.

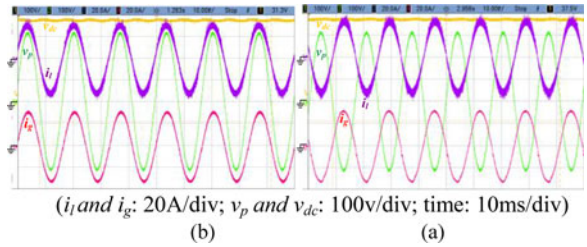

Fig. 9. Measured waveforms of inverter current i_l, grid current i_g, and grid voltage v_p in (a) GC mode and (b) rectification mode under 5 kW and no harmonic voltage. ($Z_l = 2$ mH.)

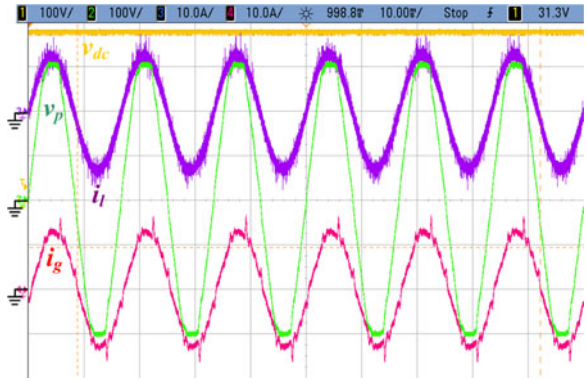

Fig. 10. Measured waveforms of inverter current i_l (THD: 1.5%) and grid current i_g (THD: 4.3%) in GC mode and under 2 kW, with harmonic voltage ($V_{\mathrm{THD}} = 3\%$) and without FCCC. ($Z_l = 2$ mH.)

A. Test With D-Σ Control

Fig. 9(a) and (b) shows the measured inverter current i_l, grid current i_g, dc-bus voltage v_{dc}, and pcc voltage v_p waveforms in GC mode and rectification mode under 5 kW load condition. It can be seen that the inverter current i_l waveform is sinusoidal, verifying the feasibility of the designed inverter with D-Σ digital control. Moreover, the inverter was tested with distorted grid voltages. In Fig. 10, when the pcc voltage has obvious distortion ($V_{\mathrm{THD}} = 3\%$), the inverter current i_l can still maintain sinusoidal current waveform (total harmonic distortion (THD) <1.5%) with the proposed D-Σ digital control, but without FCCC, the grid current i_g comes out with high distortion (THD >4%).

B. Test With FCCC

To test the feasibility of the proposed FCCC, the programmable ac source was employed to build four grid-voltage-distortion conditions, which are shown in Table II. In the test, the grid impedance Z_l is set to a pure inductor of 2 mH. Figs. 11–14 show inverter current i_l, grid current i_g, ac voltage v_p, and dc-bus voltage v_{dc} waveforms in GC mode. In case I test condition, the THD of voltage v_p is around 18.5%. Without the proposed FCCC, the inverter can track sinusoidal current reference for inverter current i_l, but grid current i_g is highly distorted and its THD is 18.8%, as shown in Fig. 11(a). From Fig. 11(b), it can be seen that the inverter tracks new current reference for i_l

TABLE II
THREE TEST CONDITIONS OF GRID DISTORTION

Case	Harmonic order	%	Measured item	Without FCCC (GC mode)	With FCCC (GC mode)	Without FCCC (rectification mode)	With FCCC (rectification mode)
Case I	5	9.8	PF	0.96	0.98	0.96	0.98
	7	15.8	V_{THD} (%)	18.5	18.4	18.4	18.4
	8	2.16	I_{THD} (%)	18.8	3.2	18.7	2.8
Case II	3	4.9	PF	0.98	0.99	0.98	0.99
	5	1.6					
	7	2.7		6.4	6.4	6.4	6.4
	11	1.4	V_{THD} (%)				
	15	2	I_{THD} (%)	9.4	3.8	9.3	3.3
	17	1.1					
Case III	3	17.8	PF	0.96	0.98	0.96	0.98
			V_{THD} (%)	17.8	17.7	17.7	17.8
			I_{THD} (%)	17.7	2.1	17.8	2.0
Case IV	7	4.6	PF	0.97	0.98	0.97	0.98
	9	1	V_{THD} (%)	4.9	5.1	4.9	5.0
	21	0.9					
	39	0.7	I_{THD} (%)	5.1	2.5	5.1	2.6

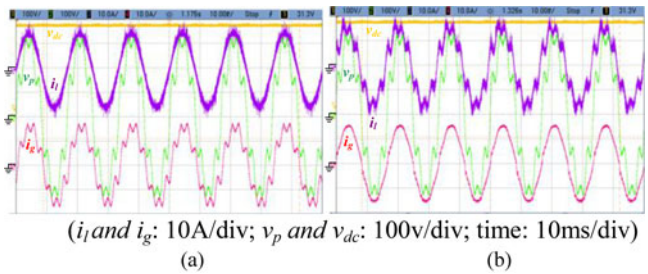

Fig. 11. Measured waveforms of inverter current i_l, grid current i_g, and grid voltage v_p (a) without and (b) with FCCC in GC mode and under case I test condition. ($Z_l = 2$ mH.)

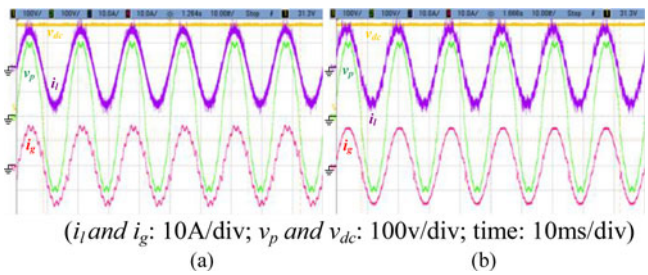

Fig. 12. Measured waveforms of inverter current i_l, grid current i_g, and grid voltage v_p (a) without and (b) with FCCC in GC mode and under case II test condition. ($Z_l = 2$ mH.)

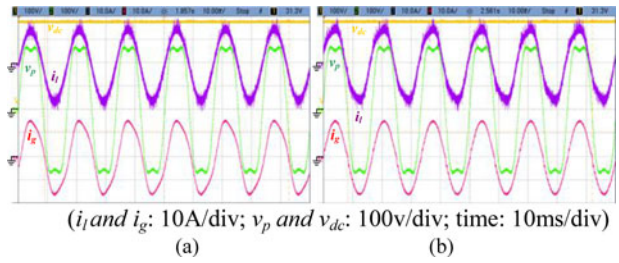

Fig. 13. Measured waveforms of inverter current i_l, grid current i_g, and grid voltage v_p (a) without and (b) with FCCC in the GC mode and under case III test condition. ($Z_l = 2$ mH.)

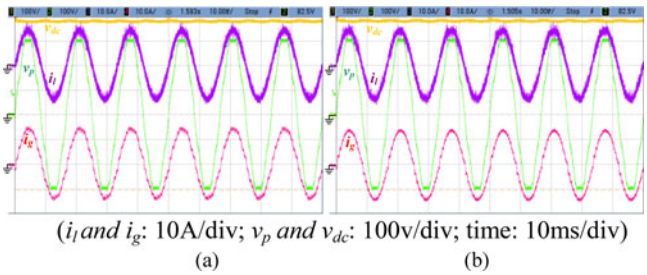

Fig. 14. Measured waveforms of inverter current i_l, grid current i_g, and grid voltage v_p (a) without and (b) with FCCC in the GC mode and under case IV test condition. ($Z_l = 2$ mH.)

so as the grid-current distortion can be filtered out, in which the THD of the grid current is reduced to 3.2%. In cases II and III test conditions, the THDs of the grid currents are reduced from 9.4% to 3.8% and from 17.7% to 2.1%, respectively. In case IV test condition, the grid voltage is distorted with a 39th harmonic, and the THD of the grid current can be reduced from 5.1% to 2.5% with the FCCC. Figs. 15–18 show those in rectification mode. In case I test condition, the THD of voltage v_p is around 18.4%. Without the FCCC, the inverter can track sinusoidal current reference for i_l, but grid current i_g is highly distorted again, and its THD is 18.7%, as shown in Fig. 15(a). From Fig. 15(b), it can be seen that the inverter tracks new current reference for the inverter current so as the grid-current distortion can be filtered out, in which the THD of the grid current is reduced to 2.8%. In cases II–IV test conditions, the THDs of the grid currents are reduced from 9.3% to 3.3%, from 17.8% to 2.0%, and from 5.1% to 2.6%, respectively, verifying the proposed current compensation. Fig. 19(a) shows those under a step-load change from 2 to 4 kW, with grid inductor $L_l = 5$ mH, and with low THD v_p, and Fig. 19(b) shows those with high THD v_p. It can

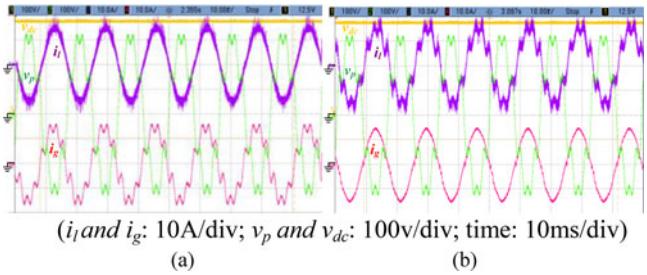

Fig. 15. Measured waveforms of inverter current i_l, grid current i_g, and grid voltage v_p (a) without and (b) with FCCC in rectification mode and under case I test condition. ($Z_l = 2$ mH.)

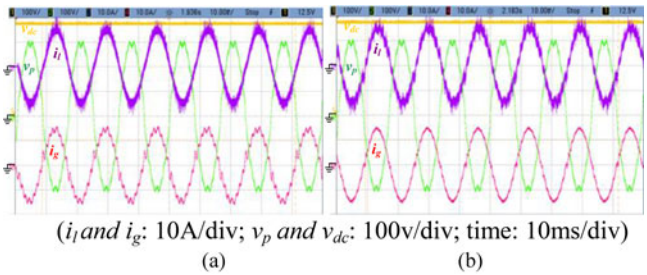

Fig. 16. Measured waveforms of inverter current i_l, grid current i_g, and grid voltage v_p (a) without and (b) with FCCC in rectification mode and under case II test condition. ($Z_l = 2$ mH.)

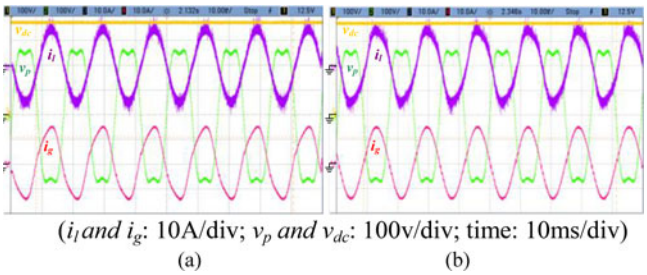

Fig. 17. Measured waveforms of inverter current i_l, grid current i_g, and grid voltage v_p (a) without and (b) with FCCC in rectification mode and under case III test condition. ($Z_l = 2$ mH.)

be seen that when the power is changed, the grid current i_g can still maintain sinusoidal waveforms without obvious distortion. Fig. 20 shows the plots of current and voltage waveforms under the variations of capacitance C_s and inductance L_g. From the grid current i_g waveforms, it can be observed that the proposed control and compensation are not sensitive to these variations.

V. Conclusion

An extended application of the D-Σ digital control associated with FCCC to a single-phase inverter with an *LCL* filter and wide filter-inductance variation has been presented in this paper. The D-Σ digital control has been first reviewed to derive the control laws for inverter current tracking. With the control laws, the controller can tune loop gains corresponding to inductance variation cycle by cycle. Additionally, the FCCC can improve grid-current distortion under distorted grid

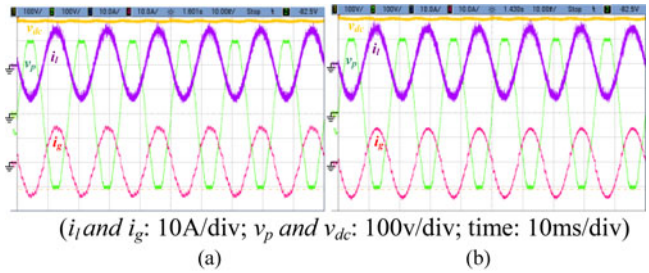

Fig. 18. Measured waveforms of inverter current i_l, grid current i_g, and grid voltage v_p (a) without and (b) with FCCC in rectification mode and under case IV test condition. ($Z_l = 2$ mH.)

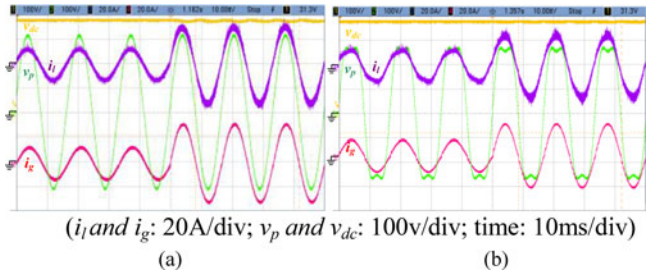

Fig. 19. Measured waveforms of inverter current i_l, grid current i_g, and grid voltage v_p under a step-load change from 2 to 4 kW and (a) with low THD v_g, and (b) with high THD v_g. ($Z_l = 5$ mH.)

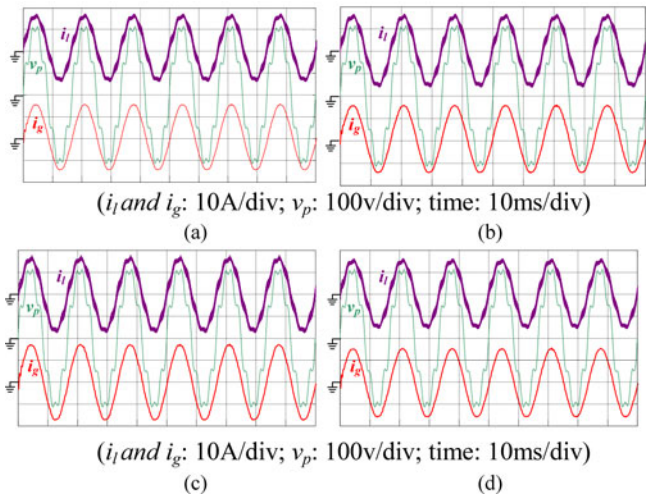

Fig. 20. Simulated results of inverter current i_l, grid current i_g, and grid voltage v_p: (a) C_s with +5% error, (b) C_s with –5% error, (c) L_g with +5% error, and (d) L_g with –5% error in the GC mode and under case I test condition. ($Z_l = 2$ mH.)

V. Conclusion

voltages. Moreover, the proposed approaches control the inverter to become a current source which can achieve tight grid-current tracking, high harmonic-voltage-rejection ratio and high phase margin even under weak grid condition. Analytical results, Bode plots of i_g/I_{gr} and i_g/v_p, and impedance plots have confirmed the tracking capability and stability of the grid current under weak grid condition, and experimental results have verified the feasibility of the extended application of the D-Σ digital control and the FCCC.

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