# Embedded Control of *n*-Level DC–DC–AC Inverter

B. Dastagiri Reddy, Anish N. K., M. P. Selvan, *Member, IEEE*, and S. Moorthi, *Member, IEEE*

***Abstract*—A generalized multilevel inverter (MLI) with front-end dc–dc conversion stage followed by a synchronized H-bridge is presented. By using this configuration along with the proposed embedded control, any desired number of levels (*n*) in the output voltage can be produced. The dc–dc conversion stage employs an asynchronous buck converter. The duty cycle of dc–dc converter is varied in the form of *m*-level piecewise constant (PWC) unidirectional sine wave to produce a similar output voltage across the dc-link capacitor. The unidirectional PWC voltage is made into *n*-level ac voltage, where $n = (2m - 1)$, by the synchronized H-bridge. Hence, it is named as dc–dc–ac MLI. An 8-bit Xilinx SPARTAN 3AN field programmable gate array (FPGA)-based digital controller is utilized for the simultaneous generation of high-frequency switching pulses for dc–dc converter and synchronized fundamental frequency switching pulses for H-bridge. The desired number of levels in ac output voltage and its frequency are the essential inputs to the pulse generation algorithm implemented in FPGA. The proposed MLI is simulated in MATLAB/Simulink environment; its functioning is verified with resistive (*R*) and resistive–inductive (*R–L*) loads. The hardware prototype of MLI is built in the laboratory and its performance is validated with *R*, *R–L* loads, and few home appliances.**

***Index Terms*—DC–DC–AC multilevel inverter (DDA-MLI), embedded controller, field programmable gate array (FPGA), piecewise constant (PWC).**

## NOMENCLATURE

| | |
|---|---|
| $C$ | Filter capacitance. |
| $C_{\min}$ | Minimum value of $C$. |
| CCM | Continuous conduction mode. |
| FF | Fundamental frequency. |
| $f_C$ | Corner frequency. |
| $f_S$ | Switching frequency. |
| FPGA | Field programmable gate array. |
| HF | High frequency. |
| IGBT | Insulated gate bipolar transistor. |
| $I_O$ | Output current of dc–dc converter. |
| $I_{O\max}$ | Maximum value of $I_O$. |
| $I_{O\min}$ | Minimum value of $I_O$. |
| $L$ | Inductance. |
| $L_{\min}$ | Minimum value of $L$ for CCM operation. |
| $M_{\mathrm{VDC}}$ | DC voltage transfer function of the dc–dc converter. |
| $m$ | Number of levels in PWC unidirectional sine wave. |
| $n$ | Number of levels in ac output voltage. |
| $P_O$ | Output power of dc–dc converter. |
| $P_{O\max}$ | Maximum of $P_O$. |
| $P_{O\min}$ | Minimum of $P_O$. |
| PWC | Piecewise constant. |
| $r_C$ | Equivalent series resistance of $C$. |
| $r_{C\max}$ | Maximum value of $r_C$. |
| $R_L$ | DC load resistance. |
| $R_{L\max}$ | Maximum value of $R_L$. |
| $R_{L\min}$ | Minimum value of $R_L$ |
| $S$ | Power semiconductor switch of the dc–dc converter. |
| $S_1$–$S_4$ | Power semiconductor switches of the H-bridge. |
| $T_{\mathrm{ON}}$ | Conduction period of S. |
| $T_{\mathrm{OFF}}$ | Non-conduction period of S. |
| THD | Total harmonic distortion. |
| $V_{\mathrm{AC}}$ | AC output voltage of H-bridge. |
| $V_C$ | Voltage across $C$. |
| $V_{C\mathrm{avg}}$ | Average of $V_C$. |
| $V_{\mathrm{DC}}$ | Input dc voltage of dc–dc converter. |
| $V_{\mathrm{gs}}$ | Gate voltage of $S$. |
| $V_{gs1} - V_{gs4}$ | Gate voltages of $S_1$–$S_4$. |
| $V_r$ | Peak-to-peak value of $V_C$ ripple voltage. |
| $\Delta i_{L\max}$ | Maximum inductor ripple current. |
| $\delta$ | Duty cycle. |
| $\eta$ | Efficiency of the converter. |

Manuscript received March 12, 2014; revised May 29, 2014; accepted July 7, 2014. Date of publication July 25, 2014; date of current version February 13, 2015. Recommended for publication by Associate Editor M. Saeedifard.

B. Dastagiri Reddy, M. P. Selvan, and S. Moorthi are with Hybrid Electrical Systems Laboratory, Department of Electrical and Electronics Engineering, National Institute of Technology, Tiruchirappalli 620015, India (e-mail: dastagirireddy9@gmail.com).

Anish N. K. was with the Hybrid Electrical Systems Laboratory, Department of Electrical and Electronics Engineering, National Institute of Technology, Tiruchirappalli 620015, India. He is now with Qualcomm Incorporated, Bangalore 560066, India (e-mail: anish12321@gmail.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2341245

## I. INTRODUCTION

THE POWER industry is revived with widespread integration of renewable energy sources and highly efficient power transmission and distribution facilities, where the continued technological advancements in power electronics are being exercised. The multilevel power converter, one of such advancements, plays a significant role in medium- and high-power applications in the contemporary power industry due to its various advantages [1]–[4].

The concept of multilevel inverter (MLI) was introduced in 1975 and its applications began with a three-level topology. Subsequently, several MLI topologies were developed. The topologies of high-power MLIs are classified into three main types, namely, flying capacitor (FC) MLI, diode clamped or neutral point clamped MLI, and cascaded H-bridge (CHB) MLI [5]–[8]. Nevertheless, the MLI has also been found to be a better solution in low-power ranges when compared to its conventional counterparts [9], [10].

Regrettably, these inverters do have few drawbacks as well. One particular disadvantage is the necessity for a greater number of power semiconductor switches with associated gate drive

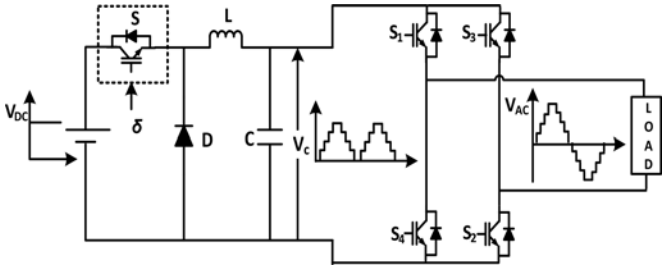


Fig. 1. Circuit diagram of DDA-MLI.

circuits, resulting in more expensive and complex systems. Likewise, the control complexity in balancing the voltage across the capacitors of FC-MLI and requirement of separate dc sources of equal voltage in CHB-MLI topology are noteworthy [11], [12]. Many topologies and control methods were addressed by several authors to overcome the aforementioned drawbacks [13]–[33]. It is apparent from [34] that still there is a need for new topologies and control algorithms. Hence, a dc–ac inverter topology, presented in [35] is derived in the present study for developing an MLI with a new control algorithm.

The organization of this paper is as follows. The circuit description and operation of dc–dc–ac multilevel inverter (DDA-MLI) is presented in Section II. The MATLAB simulations with a comparative study among the conventional topologies and the power loss analysis are described in Sections III and IV, respectively. The experimental results are presented and discussed in Section V and followed by Section VI, which concludes this paper with highlights of the inference from simulation and experimentation.

## II. Circuit Description and Operation of DDA-MLI

The circuit diagram of DDA-MLI is shown in Fig. 1, in which a dc–dc converter of buck configuration is coupled with an H-bridge. The power semiconductor switch *S*, can be a single high-voltage switch or a series combination of low-voltage switches, which can meet the necessary full $V_{\rm DC}$ hold-off requirement. Since insulated gate bipolar transistors (IGBTs) of 600 V to 6.5 kV are commercially available [36]–[39], single IGBT or a series combination of two IGBTs is ample to meet the hold-off requirement in low- and medium-power applications. The average output voltage of buck converter, which is a function of duty cycle and input voltage, is given as

$$V_{\rm Cavg} = \left(\frac{T_{\rm ON}}{T_{\rm ON} + T_{\rm OFF}}\right) V_{\rm DC} = \delta V_{\rm DC}. \tag{1}$$

The duty cycle ($\delta$) is varied in an *m*-level positive piecewise constant (PWC) sinusoidal fashion, so that the $V_C$ will naturally be a unidirectional *m*-level PWC sine wave that is made into a *n*-level ac voltage by a synchronized H-bridge. The relation between *m* and *n* is given as

$$n = (2m - 1). \tag{2}$$

The magnitude and frequency of the output, $V_{\rm AC}$, are controlled by the duty cycle of dc–dc converter.

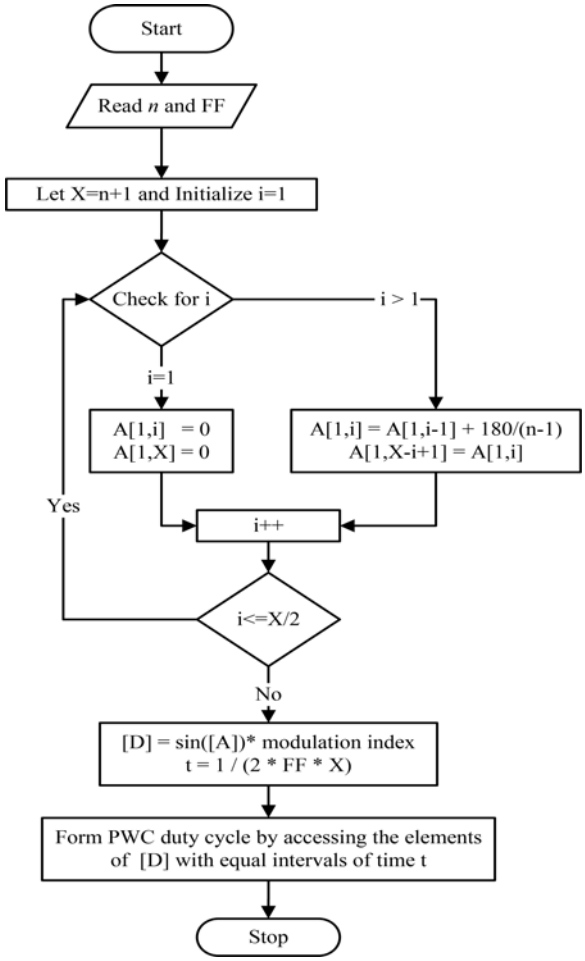


Fig. 2. Flowchart for generation of *m*-level PWC duty cycle.

### A. Generation of m-Level PWC Duty Cycle

A method for varying the duty cycle of dc–dc converter is presented as a flowchart depicted in Fig. 2. An array [A] is filled with angles of equal intervals between 0–90° and 90–0° based on the selected value of *n*. The sine value of elements of [A] is calculated by *sine ()* function and then multiplied with the modulation index. Then the product is stored in an array [D]. The PWC duty cycle is formed by accessing the elements of [D] at equal intervals of time *t*, which is a function of desired fundamental frequency.

In the proposed MLI, as the duty cycle of buck converter is continuously varied, a special care has been taken in the design of its components. The design is executed in such a way that the output has to follow the dynamic change in the duty cycle and make the system more robust for load current variations [40].

### B. Design of Buck Converter Parameters

In order to make the output voltage of buck converter to follow the sinusoidal variation of duty cycle, it is operated in CCM. The procedure for the design of buck converter with the given specifications of $V_{\rm DC}$, $V_C$, $I_{O\,\rm min}$, $I_{O\,\rm max}$, $f_S$, *and* $V_r/V_C \leq 1\%$ is described in the following steps:

*Step (i):* Compute the maximum and minimum values of the output power as follows:

$$P_{O\max} = V_{C\text{avg}} I_{O\max} \tag{3}$$

$$P_{O\min} = V_{\text{Cavg}} I_{O\min}. \tag{4}$$

*Step (ii):* Calculate the minimum and maximum values of the load resistance as

$$R_{L\min} = \frac{V_{\text{Cavg}}}{I_{O\max}} \tag{5}$$

$$R_{L\max} = \frac{V_{\text{Cavg}}}{I_{O\min}}. \tag{6}$$

*Step (iii):* Evaluate the dc voltage transfer function of the buck converter as

$$M_{\text{VDC}} = \frac{V_{\text{Cavg}}}{V_{\text{DC}}}. \tag{7}$$

In the investigated topology, the maximum average output voltage (at $n = 255$, $V_C$ is a fully rectified sine wave) of buck converter is given as

$$V_{\text{Cavg}} = \frac{2V_{\text{DC}}}{\pi} = 0.637V_{\text{DC}}. \tag{8}$$

*Step (iv):* Estimate the duty cycle of buck converter with efficiency $\eta$ as

$$\delta = \frac{M_{\text{VDC}}}{\eta}. \tag{9}$$

*Step (v):* Calculate the minimum inductance required to maintain the converter in CCM as [40].

$$L_{\min} = \frac{V_{\text{Cavg}}(1-\delta)}{2f_S I_{O\min}} = \frac{\delta(V_{\text{DC}} - V_{\text{Cavg}})}{2f_S I_{O\min}}. \tag{10}$$

*Step (vi):* Select an inductance *L*, whose value is higher than $L_{\min}$. Then compute $\Delta i_{L\max}$ as follows [40]:

$$\Delta i_{L\max} = \frac{V_{C\text{avg}}(1-\delta)}{f_S L}. \tag{11}$$

*Step (vii):* Select the value of $r_c$ satisfying the following condition:

$$r_C < \left( r_{C\max} = \frac{V_r}{\Delta i_{L\max}} \right). \tag{12}$$

*Step (viii):* Compute the minimum value of filter capacitor by (13) and select the value of *C* higher than $C_{\min}$ to satisfy the condition given by (14) [40]:

$$C_{\min} = \frac{\delta}{2f_S r_C} \tag{13}$$

$$f_C = \frac{1}{2\pi\sqrt{\text{LC}}} \ll f_S. \tag{14}$$

TABLE I
LIST OF PARAMETER VALUES

| | | |
|---|---|---|
| Specifications | $V_{\text{DC}}$ | 200 V |
| | $I_{O\min}$ | 0.2 A |
| | $I_{O\max}$ | 10 A |
| | $f_S$ | 35 kHz |
| | *FF* | 50 Hz |
| Designed Parameters | *L* | 1 mH |
| | *C* | 10 $\mu$F |

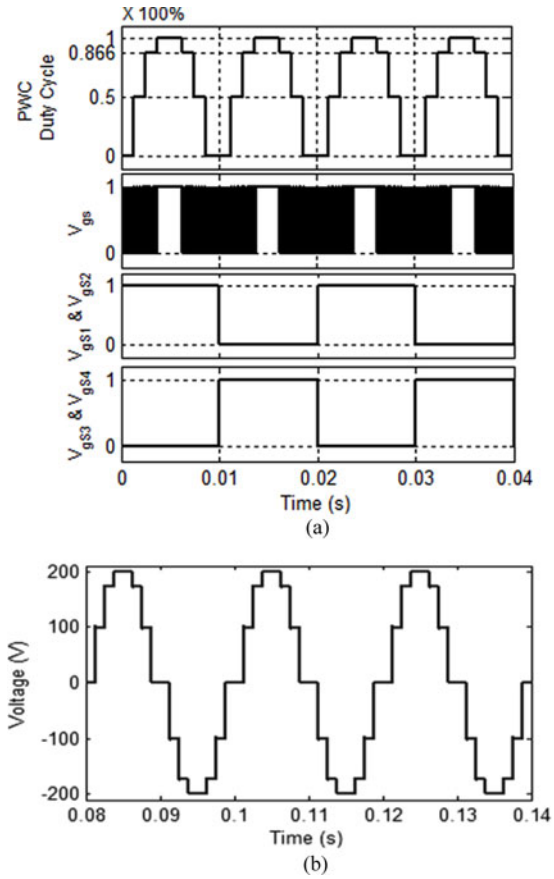


Fig. 3. (a) Four-level PWC duty cycle and corresponding switching pulses. (b) Seven-level output ac voltage.

## III. SIMULATION OF DDA-MLI

The circuit shown in Fig. 1 along with the method for varying duty cycle shown in Fig. 2 has been simulated in MATLAB/Simulink. The specifications considered for the design of filter parameters of dc–dc converter and the values of *L* and *C* obtained from the aforementioned design procedure are tabulated in Table I.

The results obtained from the simulations are presented in Figs. 3–5. The four-level PWC duty cycle and corresponding switching pulses; $V_{gs}$ for *S* of dc–dc converter and $V_{gs1}$–$V_{gs4}$ for $S_1$–$S_4$ of H-bridge are shown in Fig. 3(a). The corresponding seven-level ac voltage of four-level PWC is presented in Fig. 3(b). It is clear from Fig. 3 that with the designed parameters, the output of dc–dc converter, $V_C$, exactly followed the

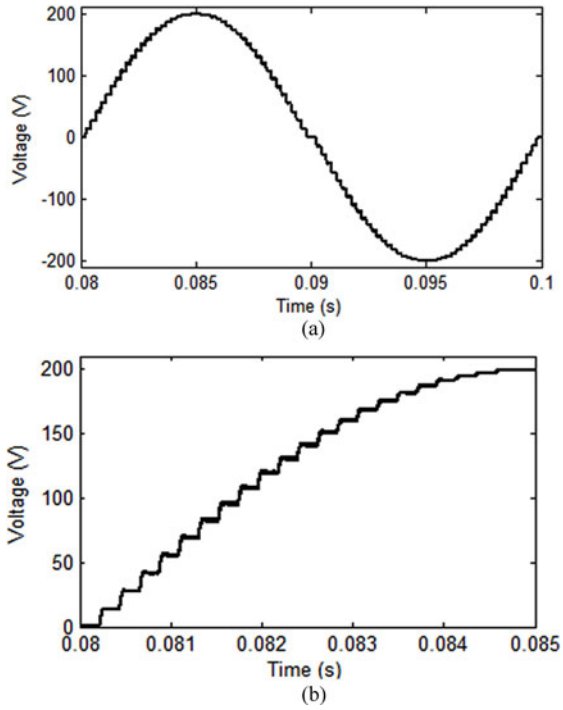


Fig. 4. (a) 45-level output ac voltage. (b) 45-level output ac voltage (zoomed view).

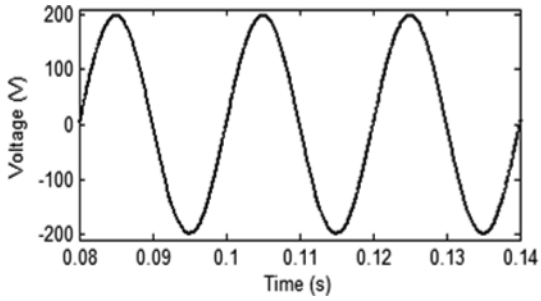


Fig. 5. 255-level output ac voltage.

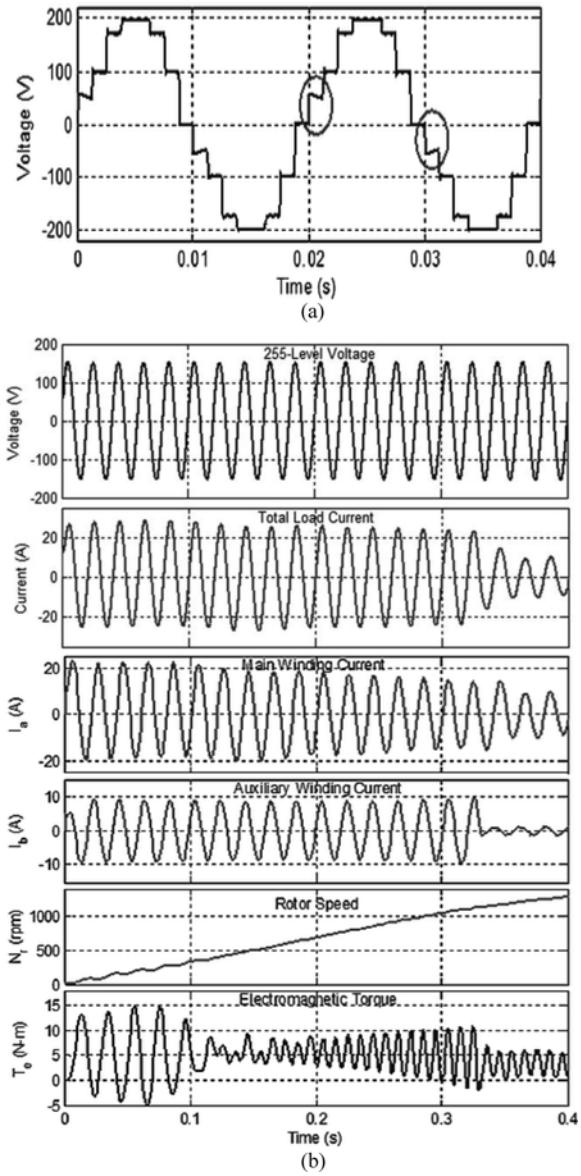


Fig. 6. (a) Effect of load inductance on seven-level voltage. (b) Parameters of 110 V, 50 Hz 0.25 hp motor.

duty cycle variation. In addition, a good quality of output ac voltage is produced by the generation of synchronized HF and FF switching pulses.

The 45-level and 255-level output ac voltage waveforms are shown in Figs. 4 and 5, from which it is clear that the DDA-MLI is capable of generating any number of levels in the output ac voltage, with single dc source and employing few power semiconductor switches.

Further, the capability of DDA-MLI for feeding high inductive loads is examined. The effect of load inductance on seven-level output ac voltage is shown in Fig. 6(a). The zero level of seven-level voltage waveform is shifted to 50 V, as the regenerative energy due to the inductive load increases the capacitor voltage prior to the duty cycle variation. Interestingly, the percentage THD of the voltage waveform has improved to 14.38% from 17% while feeding such inductive loads.

In addition to this, the performance of DDA-MLI is examined with a 110 V, 50 Hz, 0.25 hp capacitor-run-capacitor-start motor load. A 255-level output voltage of the proposed DDA-MLI topology and the waveform of total current drawn by the single-phase motor load are shown in Fig. 6(b). The parameters of the selected motor such as main winding current, auxiliary winding current, rotor speed, and electromagnetic torque are also itemized in Fig. 6(b). The results presented in Fig. 6(a) and (b) explicitly show that the proposed MLI is capable of feeding low-power factor loads too.

A comparative study is performed with conventional MLI topologies including a topology, namely reversing voltage topology, presented in a recent paper [18], based on the quality of the output ac voltage for different levels. Fig. 7 is a bar chart depicting the comparison of the percentage THD values of unfiltered

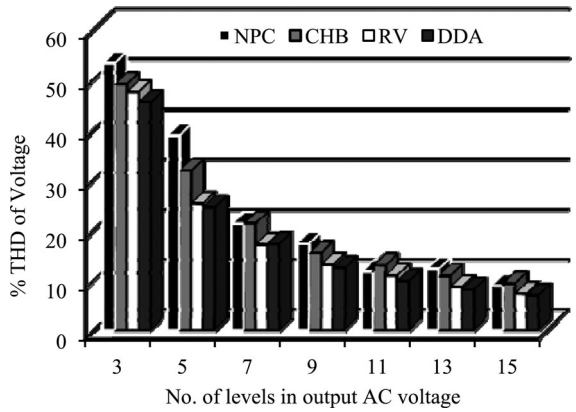


Fig. 7. %THD of unfiltered output ac voltage.

output voltage obtained from different topologies for different levels. It is apparent from the comparative study that the quality of output voltage of DDA-MLI topology is better than that of other topologies for any number of levels in output voltage.

## IV. Power Loss Analysis

An analysis of switching and conduction power losses in the proposed DDA-MLI with different levels in output ac voltage has been quantitatively carried out using MATLAB/ Simulink. Inverters of 1 kW and 60 kW power rating with an input dc voltage of 200 V and 1100 V, respectively, are considered for this analysis. Using the preswitching and postswitching values of voltage across the device, current flowing through the device, and junction temperature, the switching and conduction power losses of IGBT have been calculated based on the device datasheet. Similarly, the reverse recovery and conduction power losses of diode have also been estimated. Simulations have been carried out with 25 °C as initial heat sink temperature and 45 °C as the maximum permissible temperature rise.

The power losses of 1 kW DDA-MLI, considering commercially available FGH40N60SFD IGBTs (600 V, 40 A) and HFA15PB60 ultra fast recovery diode (600 V, 15 A), have been computed for different levels in output ac voltage and shown as a line chart in Fig. 8(a).

Similarly, the estimated power losses of 60 kW DDA-MLI considering FF225R17ME4_B11 IGBT module (1700 V, 225 A), for different levels in output ac voltage are presented in Fig. 8(b). From Fig. 8(a) and (b), it is clear that the total power loss increases with the increase in number of levels and furthermore the increase in total power loss depends on the power rating of DDA-MLI and the type of IGBT.

Further, the variations in efficiency of 1 kW and 60 kW DDA-MLI with respect to the number of levels in ac output voltage are presented in Fig. 9. The switching power loss of DDA-MLI is comparatively low since it has only one power semiconductor switch operating at HF and the rest (four power semiconductor switches of H-bridge) are operating at FF and hence it has high efficiency. The estimated efficiency of 255-level DDA-MLI with 1 kW and 60 kW power rating are 97.04% and 91.26%,

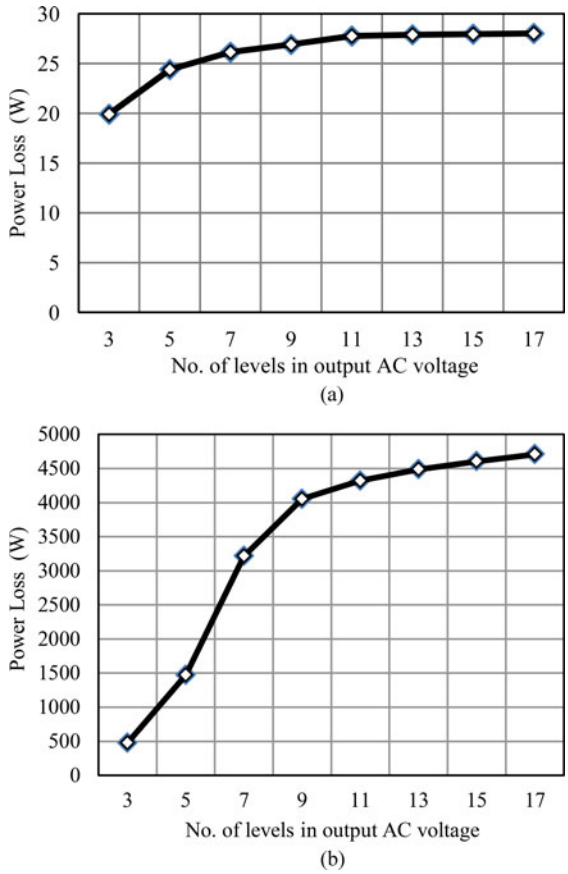


Fig. 8. (a) Power loss in 1 kW DDA-MLI. (b) Power loss in 60 kW DDA-MLI.

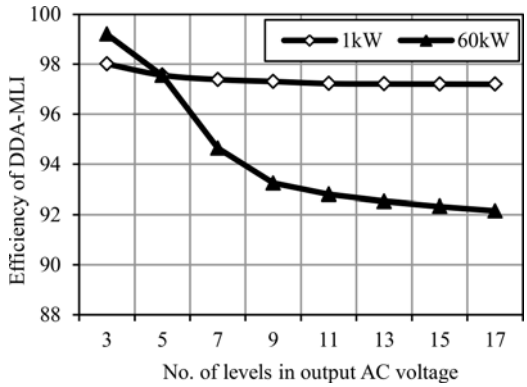


Fig. 9. Efficiency of DDA-MLI.

respectively. From the above analysis, it is confirmed that a tradeoff between the quality of output voltage and efficiency is required while selecting the required number of levels in output ac voltage.

## V. Experimentation of DDA-MLI

As a follow-up, based on the satisfactory simulation results, the hardware implementation of DDA-MLI has been attempted

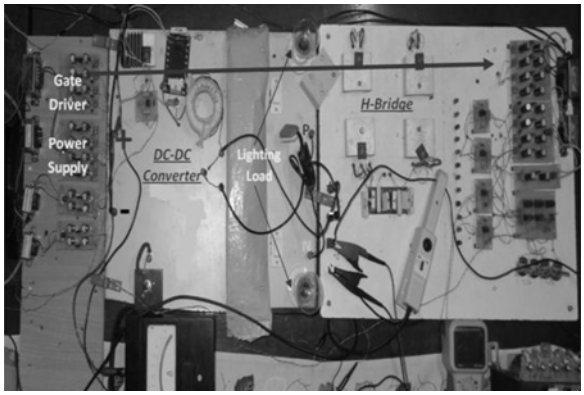


Fig. 10. Laboratory setup of DDA-MLI.

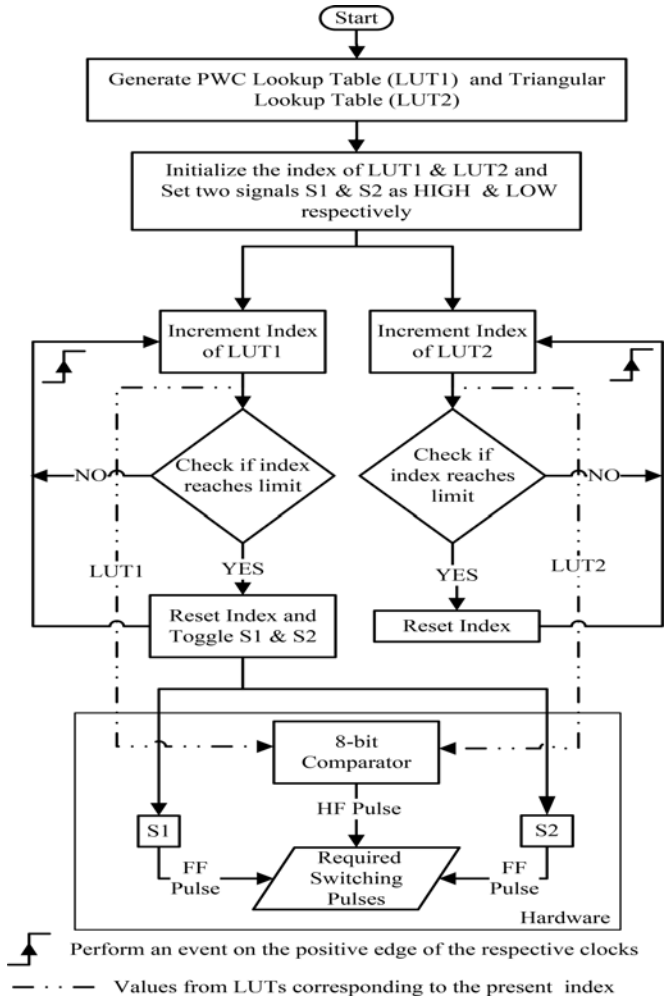


Fig. 11. Algorithmic flow of proposed-embedded controller.

and a photograph of the hardware setup built in the laboratory is shown in Fig. 10. The procedure for implementing the algorithm for generating high frequency switching pulses for dc–dc converter and synchronized fundamental frequency switching pulses for H-bridge in FPGA is detailed in Fig. 11.

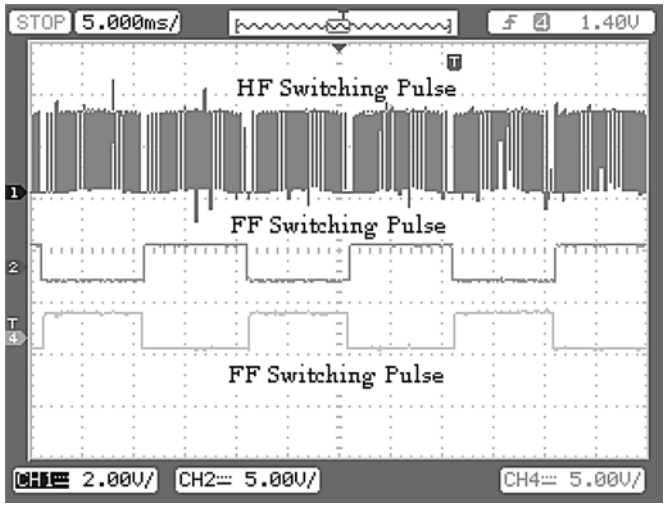


Fig. 12. Switching pulses generated by FPGA.

### A. Proposed Embedded Controller

An embedded controller using 8-bit Xilinx SPARTAN 3AN FPGA is developed for the simultaneous generation of HF switching pulse to the dc–dc converter and the synchronized FF switching pulses to the H-bridge. The algorithmic flow of the embedded controller is depicted in Fig. 11.

The generation of HF switching pulse involves a comparison between PWC wave of double the desired FF and a HF triangular repeating sequence of selected switching frequency. Since the proposed control scheme is working in open loop, the reference signal (PWC) and the triangular repeating sequence are generated internally in FPGA. Two arrays, which serve as lookup tables are created for storing the 8-bit binary values of PWC and triangular waves. The instantaneous values for both the lookup tables are generated using C code. The formulation of PWC lookup table is done as per the flowchart shown in Fig. 2. The triangular lookup table is formulated with the help of up-down counter, which counts up from 0 to 255 and counts down from 255 to 0.

After constructing lookup tables, two pointers are initialized to refer the indices of the lookup tables and a signal “S1” and its complement “S2” are set. The values available in PWC and triangular lookup tables are accessed at appropriate rate based on FF and HF, respectively. The values thus accessed are fed to the comparator implemented in hardware. The output of comparator, which is a logical 1-bit value is the required HF switching pulse for the dc–dc converter. Further, the signals “S1” and “S2” are toggled whenever the index of PWC lookup table is reset. The signals “S1” and “S2” are used as synchronized FF switching pulses for the H-bridge. The switching pulses generated by the FPGA for all the five power semiconductor switches are recorded using Agilent digital storage oscilloscope (DSO 1004A) and presented in Fig. 12.

The prototype has been tested with different values of input dc voltage like 50 V, 200 V, and finally 320 V. Charged capacitors, batteries, and renewable energy voltage sources can be

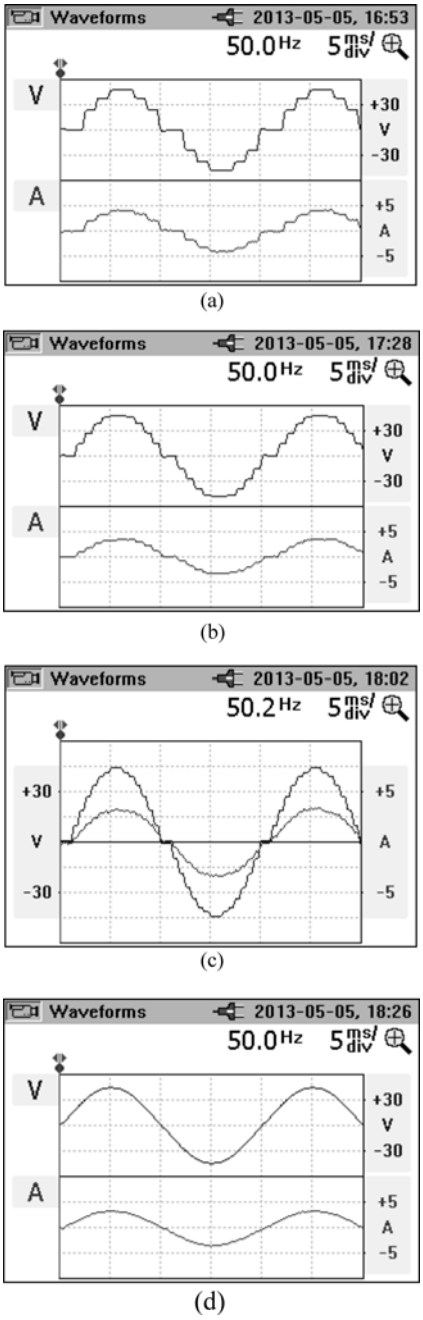


Fig. 13. (a) Seven-level output ac voltage and load current. (b) 11-level output ac voltage and load current. (c) 15-level output ac voltage and load current. (d) 255-level output ac voltage and load current.

used as input dc source for the proposed MLI. All the events during experimentation have been recorded using FLUKE 345 PQ clamp meter. Fig. 13 (a)–(d) shows the 7-, 11-, 15-, and 255-level output voltage and load current waveforms for an input dc voltage of 50 V. The percentage THD values of unfiltered output voltage with different levels obtained from simulation and experimentation are tabulated in Table II, which are found to be in close agreement with each other. Similarly, the waveforms of three- and five-level output voltage with 200 V dc as input are presented in Fig. 14(a) and (b), respectively, where the load

TABLE II
%THD OF UNFILTERED OUTPUT VOLTAGE

| No. of Level ($n$) | % THD of output voltage | |
|---|---|---|
| | Simulation | Experimentation |
| 3 | 45.38 | 45.6 |
| 5 | 24.45 | 25.3 |
| 7 | 17.14 | 17 |
| 9 | 12.39 | 12.6 |
| 11 | 9.76 | 10.4 |
| 13 | 8.06 | 8.4 |
| 15 | 6.88 | 7.2 |
| 17 | 5.84 | 6.4 |
| 19 | 5.13 | 5.3 |
| 21 | 4.61 | 4.7 |
| 255 | 0.37 | 1.4 |

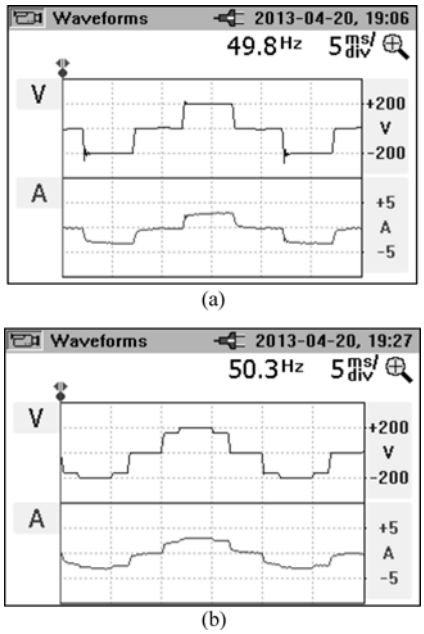


Fig. 14. (a) Three-level output ac voltage and load current. (b) Five-level output ac voltage and load current.

current waveform is smoother than the voltage because of the presence of load inductance. From Figs. 13 and 14, it is asserted that the DDA-MLI is capable of producing any number of levels in output ac voltage with single dc source and employing fewer components.

Finally, the prototype of DDA-MLI built in the laboratory is ascertained for supplying home appliances. A combination of incandescent lamp, compact fluorescent lamp, and fan (motor) loads has been simultaneously tested with an input voltage of 320 V dc. A photograph depicting the working of the prototype of DDA-MLI with lighting loads (CFL: 11 W-2 nos., 5 W-2 nos., incandescent bulb: 60 W-2 nos., 40 W-1 no., 25 W-1 no.) and a pedestal fan (60 W) as a motor load is shown in Fig. 15. The recorded voltage and current waveforms, voltage harmonic spectrum, and a snapshot of power analyzer are presented in Fig. 16.

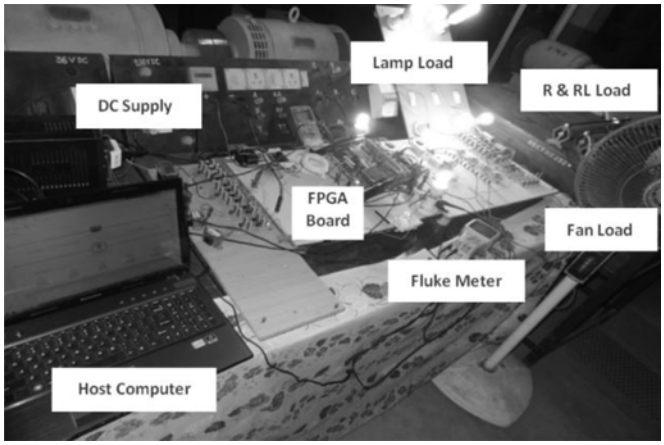


Fig. 15. Complete laboratory setup of DDA-MLI.

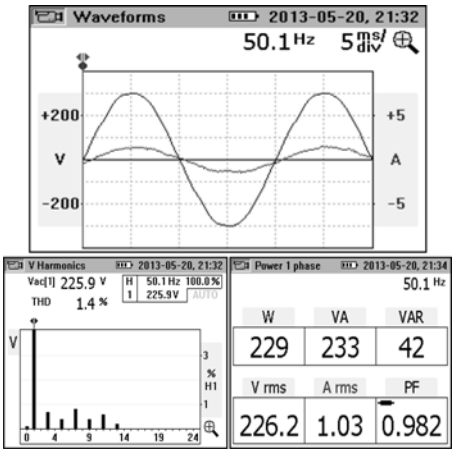


Fig. 16. Experimental results of DDA-MLI feeding home appliances.

Based on the simulation and experimental investigation, it is validated that the proposed embedded control algorithm performs very effectively in producing an output ac voltage of different levels using reduced number of components. Hence, this topology along with the proposed control algorithm can be a good candidate for converters used in various low- and medium-power applications such as uninterrupted power supply and renewable energy systems.

## VI. Conclusion

A multilevel voltage source inverter with single dc source and reduced number of components, which can produce any desired number of levels in output voltage, is presented. This topology along with the proposed embedded control results in minimized control complexity, low switching loss, less cost, and high efficiency. A method for varying the duty cycle of front end dc–dc converter of proposed MLI in an $m$-level positive PWC sinusoidal fashion, considering the desired number of levels ($n = 2m - 1$) in ac output voltage and its frequency as inputs is developed. FPGA-based algorithm for generating high-frequency switching pulses for dc–dc converter and synchronized fundamental frequency switching pulses for H-bridge is employed. Further, a performance comparison of the proposed and conventional MLI topologies is presented. The performance of DDA-MLI is verified by MATLAB simulation and validated by laboratory experimentation. From the simulation and experimental investigation, it is concluded that the proposed embedded control algorithm performs very effectively in producing an output ac voltage of different levels with single dc source and employing reduced number of components.

## References

[1] I. Abdalla, J. Corda, and L. Zhang, "Multilevel DC-link inverter and control algorithm to overcome the PV partial shading," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 14–18, Jan. 2013.

[2] M. Hamzeh, A. Ghazanfari, H. Mokhtari, and H. Karimi, "Integrating hybrid power source into an islanded MV microgrid using CHB multilevel inverter under unbalanced and nonlinear load conditions," *IEEE Trans. Energy Convers.*, vol. 28, no. 3, pp. 643–651, Sep. 2013.

[3] E. Pouresmaeil, D. Montesinos-Miracle, and O. Gomis-Bellmunt, "Control scheme of three-level NPC inverter for integration of renewable energy resources into AC grid," *IEEE Syst. J.*, vol. 6, no. 2, pp. 242–253, Jun. 2012.

[4] J. Li, J. Liu, D. Boroyevich, P. Mattavelli, and X. Yaosuo, "Three-level active neutral-point clamped zero-current-transition converter for sustainable energy systems," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3680–3693, Dec. 2011.

[5] J. Rodriguez, J.-S. Lai, and F. Zheng Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[6] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[7] P. W. Hammond, "A new approach to enhance power quality for medium voltage AC drives," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 202–208, Jan./Feb. 1997.

[8] T. A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, and M. Nahrstaedt, "Multicell converters: Basic concepts and industry applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 955–964, Oct. 2002.

[9] A. R. Beig and A. Dekka, "Experimental verification of multilevel inverter-based standalone power supply for low-voltage and low-power applications," *IET Power Electron.*, vol. 5, no. 6, pp. 635–643, Jul. 2012.

[10] S. De, D. Banerjee, K. Siva Kumar, K. Gopakumar, R. Ramchand, and C. Patel, "Multilevel inverters for low-power application," *IET Power Electron.*, vol. 4, no. 4, pp. 384–392, Apr. 2011.

[11] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[12] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pe´rez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[13] E. Babaei, M. F. Kangarlu, and M. A. Hosseinzadeh, "Asymmetrical multilevel converter topology with reduced number of components," *IET Power Electron.*, vol. 6, no. 6, pp. 1188–1196, Jul. 2013.

[14] M. F. Kangarlu and E. Babaei, "Cross-switched multilevel inverter: An innovative topology," *IET Power Electron.*, vol. 6, no. 4, pp. 642–651, Apr. 2013.

[15] M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 625–636, Feb. 2013.

[16] M. R. Banaei, H. Khounjahan, and E. Salary, "Single-source cascaded transformers multilevel inverter with reduced number of switches," *IET Power Electron.*, vol. 5, no. 9, pp. 1748–1753, Nov. 2012.

[17] M. F. Kangarlu, E. Babaei, and S. Laali, "Symmetric multilevel inverter with reduced components based on non-insulated dc voltage sources," *IET Power Electron.*, vol. 5, no. 5, pp. 571–581, May 2012.

[18] E. Najafi and A. H. M. Yatim, "Design and implementation of a new multilevel inverter topology," *IEEE Trans. Ind. Electron.*, vol. 59, no. 11, pp. 4148–4154, Nov. 2012.

[19] M. R. Banaei, A. R. Dehghanzadeh, E. Salary, H. Khounjahan, and R. Alizadeh, "Z-source-based multilevel inverter with reduction of switches," *IET Power Electron.*, vol. 5, no. 3, pp. 385–392, Mar. 2012.

[20] Z. Li, P. Wang, Y. Li, and F. Gao, "A novel single-phase five-level inverter with coupled inductors," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2716–2725, Jun. 2012.
[21] J.-I. Itoh, Y. Noge, and T. Adachi, "A novel five-level three-phase PWM rectifier with reduced switch count," *IEEE Trans. Power Electron.*, vol. 26, no. 8, pp. 2221–2228, Aug. 2011.
[22] Y.-H. Liao and C.-M. Lai, "Newly-constructed simplified single-phase multistring multilevel inverter topology for distributed energy resources," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2386–2392, Sep. 2011.
[23] S. Mekhilef and M. N. A. Kadir, "Novel vector control method for three-stage hybrid cascaded multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1339–1349, Apr. 2011.
[24] J. Ewanchuk, J. Salmon, and A. M. Knight, "Performance of a high-speed motor drive system using a novel multilevel inverter topology," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1706–1714, Sep./Oct. 2009.
[25] P. Lezana, J. Rodriguez, and D. A. Oyarzun, "Cascaded multilevel inverter with regeneration capability and reduced number of switches," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1059–1066, Mar. 2008.
[26] G. S. Perantzakis, F. H. Xepapas, and S. N. Manias, "A novel four-level voltage source inverter—Influence of switching strategies on the distribution of power losses," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 149–159, Jan. 2007.
[27] Z. Cheng and B. Wu, "A novel switching sequence design for five-level NPC/H-bridge inverters with improved output voltage spectrum and minimized device switching frequency," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2138–2145, Nov. 2007.
[28] G. Mondal, K. Gopakumar, P. N. Tekwani, and E. Levi, "A reduced-switch-count five-level inverter with common-mode voltage elimination for an open-end winding induction motor drive," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2344–2351, Aug. 2007.
[29] Y. Shi, X. Yang, Q. He, and Z. Wang, "Research on a novel capacitor clamped multilevel matrix converter," *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1055–1065, Sep. 2005.
[30] G.-J. Su, "Multilevel DC-link inverter," *IEEE Trans. Ind. Appl.*, vol. 41, no. 3, pp. 848–854, May/Jun. 2005.
[31] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.
[32] T. A. Meynard, H. Foch, F. Forest, C. Turpin, F. Richardeau, L. Delmas, G. Gateau, and E. Lefeuvre, "Multicell converters: Derived topologies," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 978–987, Oct. 2002.
[33] T. Chaudhuri, A. Rufer, and P. K. Steimer, "The common cross-connected stage for the 5L ANPC medium voltage multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2279–2286, Jul. 2010.
[34] M. Malinowski, K. Gopakumar, and J. Rodriguez, "Guest editorial," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2194–2196, Jul. 2010.
[35] Z. Yang and P. C. Sen, "Analysis of a novel bidirectional DC-to-AC inverter," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 47, no. 5, pp. 747–757, May 2000.
[36] A. Sanchez-Ruiz, M. Mazuela, S. Alvarez, G. Abad, and I. Baraia, "Medium voltage–high power converter topologies comparison procedure, for a 6.6 kV drive application using 4.5 kV IGBT Modules," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1462–1476, Mar. 2012.
[37] S. S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and comparison of 4-kV neutral-point-clamped, flying-capacitor, and series-connected H-bridge multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1032–1040, Jul./Aug. 2007.
[38] D. Krug, S. Bernet, S. S. Fazel, K. Jalili, and M. Malinowski, "Comparison of 2.3-kV medium-voltage multilevel converters for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2979–2992, Dec. 2007.
[39] V. Zorngiebel, M. Hecquard, E. Spahn, A. Welleman, and S. Scharnholz, "Modular 50-kV IGBT switch for pulsed-power applications," *IEEE Trans. Plasma Sci.*, vol. 39, no. 1, pp. 364–367, Jan. 2011.
[40] K. Marian and K. Czuk, *Pulse*-Width Modulated *DC–DC* Power Converters. New York, NY, USA: Wiley, 2008.

**B. Dastagiri Reddy** was born in Proddutur, India. He received the B.Tech. degree in electrical and electronics engineering from the Jawaharlal Nehru Technological University, Anantapur, India, in 2009, and the M.Tech. degree in power electronics from the same university in 2011. He is currently working toward the Ph.D. degree at the National Institute of Technology, Tiruchirappalli, India.

His research interests include dc–dc converter, dc–ac converter, and power electronic applications to renewable energy.

**Anish N. K.** received the B.Tech. degree in electrical and electronics engineering from the National Institute of Technology, Tiruchirapalli, India, in 2013. He is currently working toward the M.S. degree at the Birla Institute of Technology and Science, Pilani, India.

He is currently working as an Associate Engineer at Qualcomm Inc., Bangalore, India. His research interests include FPGA-based power controllers, logic and system design using hardware descriptive languages and embedded systems.

**M. P. Selvan** (M'13) received the B.E. degree in electrical and electronics engineering from Manonmaniam Sundaranar University, Tirunelveli, India, in 1999, the M.E. degree in power systems from the National Institute of Technology, Tiruchirappalli, India, in 2000, and the Ph.D. degree in computer applications in power systems from the Indian Institute of Technology, Madras, India, in 2006.

He has 13 years of teaching and research experience in the field of power systems. He is currently an Assistant Professor in the Department of Electrical and Electronics Engineering and associated with the Hybrid Electrical Systems Laboratory of the National Institute of Technology, Tiruchirappalli. He has published more than 75 technical research papers in various national as well as international conferences and journals. His research interests include distribution system analysis, distributed generators, microgrid, custom power devices, and power quality.

**S. Moorthi** (M'13) received the B.E. degree in electrical and electronics engineering from the University of Madras, Chennai, India, and the M.E. degree in applied electronics from the PSG College of Technology, Coimbatore, India, in 2001 and 2003, respectively. He received the Ph.D. degree in the field of VLSI for communication circuits in 2008 from Anna University, Chennai.

He has been working as a Faculty in the Department of Electrical and Electronics Engineering, National Institute of Technology, Tiruchirappalli, India, since 2007, and is associated with the Hybrid Electrical Systems Laboratory. He was a Postdoctoral Fellow of Erasmus Mundus External Cooperation Window initiated under EURINDIA Programme and has done postdoctoral research on memory design for reconfigurable architectures at the Royal Institute of Technology, Stockholm, Sweden, during 2010–2011. His research interests include VLSI for signal processing and embedded systems.