Dead-Time Compensation Method Based on Current Ripple Estimation

Tomoyuki Mannen, *Student Member, IEEE*, and Hideaki Fujita, *Senior Member, IEEE*

***Abstract*—This paper discusses the voltage error caused by the dead time in voltage-source PWM converters. The theoretical analysis in this paper derives the nonlinear voltage error paying attention to the parasitic output capacitance in each switching device. The analytical result reveals that the turn-off current or the switching current ripple strongly affects the voltage error. In addition, it is clarified that the conventional compensation methods based on linear and three-level approximation are suitable under small and large current ripple conditions, respectively. A simple calculation method of current ripples in three-phase PWM converters is also developed to estimate the turn-off currents. Turn-off transition compensation method which is a new compensation method based on the analysis is developed and compared with three different conventional methods in experiments using a 200-V, 5-kW three-phase grid-connection converter. The proposed method exhibits a good compensation performance having a lower voltage THD than the conventional methods in all over the operating range.**

***Index Terms*—Current ripples, dead time, grid connection converters, output stray capacitance.**

I. Introduction

RECENTLY the switching frequency of voltage-source PWM converters tends to become higher to miniaturize the volume and to improve the performance. Increasing the switching frequency achieves reduction of the inductance and capacitance values which are almost inverse proportional to the switching frequency. A high switching frequency also makes it possible to reduce the control delay, resulting in an improved current response. For this reason, wide-band gap semiconductors, such as SiC, GaN, and so on, are expected to increase the switching frequency by their improved switching performance [1], [2].

Voltage-source converters need a dead time, which is the blanking period where both upper and lower switching devices are turned off to avoid the short circuit of its dc link. It is well known that the dead time causes a voltage error resulting in a current distortion in grid-connection converters or a torque ripple in motor-drive inverters. The duration of the dead time should be set to an proper value with an adequate margin, paying attention to the rise and fall times and the turn-on and turn-off times in the switching devices, the tail current in IGBTs, the reverse recovery time in antiparallel diodes, the associated EMI issues, and the delay time in the gate drive circuits [3]. As the switching frequency increases, a switching cycle are reduced. As a result, the voltage error of the dead time has become remarkable because the rate of the dead time to the switching cycle is increasing [4].

Current feedback control has the capability to compensate the voltage error and to mitigate the current distortion caused by the dead time, if a high feedback gain is applicable to the controller. Recent grid-connection converters are equipped with a high-order switching-ripple filter using small inductors [5]. The filter makes it possible to suppress grid current ripples effectively and to reduced the total volume of the inductors. However, the small ac inductor may cause a stability problem in case of a high feedback gain. Thus, the feedback gain is limited by the stability reason, and it is difficult for the current feedback control to suppress the current distortion caused by the dead time [6].

To solve these stability problem, repetitive controllers have been proposed [7], [8]. The repetitive controller calculates the current error in the converter and compensates the current or voltage reference in the next cycle of the grid voltage. The repetitive controller can suppress the current distortion caused not only by dead time but also by other disturbances. However, it is only applicable to a repetitive current/voltage reference, and has a slow dynamic response. Therefore, it is difficult to be applied to motor drive applications because the frequency is variable and a sudden load change may occur.

Reference [9] has proposed a soft-switched PWM converter having an additional resonant circuit on the ac side of the converter. This topology can achieve zero voltage switching operation to reduce the switching power loss at a high frequency switching. Moreover, the output converter voltage has no voltage error caused by the dead time because the corresponding antiparallel diode turns on during the dead time. However, the on-state power loss is not negligible because a large resonant current additionally flows through the converter and the resonant circuit.

Various compensation methods have been proposed to reduce the voltage error caused by the dead time in voltage source PWM converters [10]–[15]. These methods are classified into the following three categories: two-level approximation compensation method (ACM) [10], [11], linear ACM [12] and three-level ACM [13]–[15]. Reference [16] has measured the detailed converter voltage waveforms during the dead time and implies that the voltage error is strongly related with the amplitude of the current ripple because of the existence of output capacitance in switching devices. The result in [16] suggests that it is difficult for the conventional compensation methods to calculate voltage error accurately.

Manuscript received April 7, 2014; revised July 14, 2014; accepted August 13, 2014. Date of publication September 4, 2014; date of current version February 13, 2015. Recommended for publication by Associate Editor M. Ponce-Silva.

The authors are with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo 152-8552, Japan (e-mail: mannen.t@akg.ee.titech.ac.jp; hf@ieee.org).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2352716

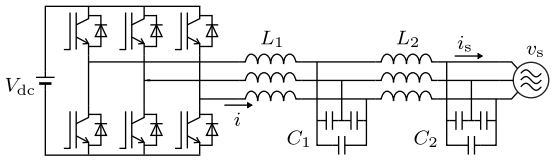

Fig. 1. Circuit configuration of a three-phase grid-connection converter equipped with a cascaded switching-ripple filter.

To improve the compensation performance, [13] considers the zero current clamping condition in which no antiparallel diode commutation during the dead time. A feedforward compensation method using a look-up table has been proposed [14]. In this method, the voltage error has been obtained from a circuit simulation considering charging and discharging the output capacitance, the results are stored in the look-up table and used as the compensating voltage. A compensating method directly detecting the voltage error from the converter voltage is also proposed [17]. However, these methods are difficult to be implemented in a popular microcontroller because they need a high-speed A/D converter and/or a field programmable gate array (FPGA).

This paper discusses the voltage error caused by dead time and proposes a new compensation method based on the analysis. The theoretically analysis in this paper analyses the converter voltage and the average voltage error in one switching cycle, considering the output stray capacitance of the switching devices. Current ripple analysis in three-phase PWM converters is conducted to estimate the turn-off current, and proposes a new voltage error compensating method based on the turn-off transition. The turn-off transition based compensation method (TTCM) calculates the compensating voltage from the analytical results of the voltage error and the turn-off current.

Experiments are conducted by using a 5-kW voltage-source PWM inverter to verify the viability of the theoretical analysis and the proposed TTCM. As a result, it is clarified that the voltage error is strongly affected by the turn-off current which is the current during the dead time. Thus, the analysis also reveals that the two-level and linear ACMs are suitable to systems having a relatively small current ripple, and the three-level ACM is better choice when the current ripple is relatively large. Moreover, it is confirmed that the proposed TTCM shows a very low harmonic distortion compared with the conventional ACMs.

II. Experimental Setup

Fig. 1 shows the circuit configuration of the experimental three-phase grid-connection converter rated at 5 kVA, and its circuit parameters are listed in Table I. The main circuit of the converter is a conventional three-phase bridge circuit using a dual in-line package intelligent power module (DIP-IPM: PS21869, 600 V, 50 A, Mitsubishi). The converter is equipped with a cascaded ripple filter on its ac side, which consists of ac inductors L_1 and L_2 and filter capacitors C_1 and C_2. Although the current ripples through L_1 as large as 4 A in peak, the filter circuit makes it possible to eliminate current ripples flowing out to the grid effectively. The switching frequency was set to be $f_{sw} = 20$ kHz ($T_{sw} = 50$ μs), and the dead time was $T_{DT} = 3$ μs in the following experiments.

TABLE I
Circuit Parameters of the Experimental Circuit

L_1	0.3 mH	f_{sw}	20 kHz
C_1	3 μF	T_{sw}	50 μs
L_2	0.1 mH	T_{DT}	3 μs
C_2	0.22 μF	V_{dc}	330 V
		f_s	50 Hz

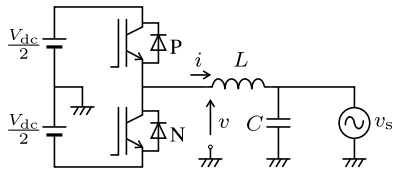

Fig. 2. Simplified single-phase circuit of the three-phase grid-connection converter.

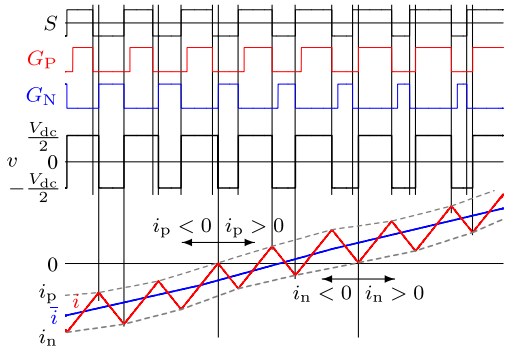

Fig. 3. Current ripples around zero crossing in PWM control.

III. Conventional Dead-Time Compensation

A. Voltage Error in Dead Time

Fig. 2 shows a simplified half-bridge circuit of the three-phase PWM converter. The converter voltage is controlled to be $v = V_{dc}/2$ or $v = -V_{dc}/2$ when either upper IGBT P or lower IGBT N is turned on by the gate signals. During the dead-time period, either upper or lower antiparallel diode may conduct, and the converter voltage v depends on the direction of the converter current i. In the conventional theory, v is assumed to be

$$v = \begin{cases} \dfrac{V_{dc}}{2}, & (i < 0) \\ -\dfrac{V_{dc}}{2}, & (i > 0). \end{cases} \tag{1}$$

Fig. 3 shows the relations between the converter current i and a voltage error caused by the dead time. In Fig. 3, S is an ideal switching function generated by a PWM controller, and G_P and G_N are the gate signals for the upper and lower IGBTs. Here, it is assumed that the turn-on edges of G_P and G_N are delayed by dead time T_{DT}. As the converter current

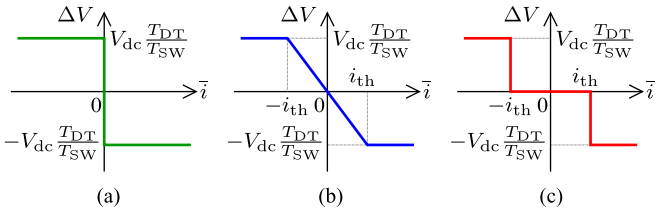

Fig. 4. Compensating voltages ΔV in conventional compensation methods. (a) Two-level ACM. (b) Linear ACM. (c) Three-level ACM.

i contains current ripples, $i_{\rm p}$ and $i_{\rm n}$ are defined as the current when the corresponding IGBT is turned off. And $\bar{i}$ is assumed to be an ideal average current which includes no current ripple. In a practical system, $\bar{i}$ can be obtained as a sampled value when using a synchronous sampling [18] or as the reference value for the current regulator.

When $i_{\rm p} > 0$ and $i_{\rm n} < 0$ as shown in Fig. 3, the converter voltage v immediately changes after the turn-off of the IGBT, and thus, the edges of the converter voltage meet to those in the switching function S. On the other hand, when $i_{\rm n} > 0$, the pulsewidth of the converter voltage is shortened by $T_{\rm DT}$, and the pulsewidth is lengthened when $i_{\rm p} < 0$, compared with the original pulsewidth of S. For this reason, an amount of voltage error appears in the converter voltage v. Therefore, the average voltage error in a switching cycle $T_{\rm SW}$ is given by

$$v_{\rm DT} = \begin{cases} V_{\rm dc}\dfrac{T_{\rm DT}}{T_{\rm SW}}, & (i_{\rm p} < 0) \\ 0, & (0 < i_{\rm p}, i_{\rm n} < 0) \\ -V_{\rm dc}\dfrac{T_{\rm DT}}{T_{\rm SW}}, & (0 < i_{\rm n}). \end{cases} \tag{2}$$

If the controller could detect the ripple current $i_{\rm ripple}$ or the turn-off currents $i_{\rm p}$ and $i_{\rm n}$, it can calculate the voltage error by using (2) and compensate the voltage error by shifting the edges of the gate pulses or subtracting the expected voltage error from the voltage reference for the PWM controller. As a result, the converter voltage v could have the same pulsewidth as the switching function S, and the average converter voltage agrees with the voltage reference. However, a specially designed detection circuit using fast A/D converters and FPGAs would be required to detect the turn-off currents $i_{\rm p}$ and $i_{\rm n}$, because popular microcontrollers cannot sample them.

B. Conventional Dead-Time Compensation Methods

Fig. 4 shows the relation between the converter current $\bar{i}$ and the compensating voltage ΔV used in conventional dead-time compensation methods. These methods calculate the compensating voltage by using relatively simple approximations calculated from the sampled converter current $\bar{i}$ or the current reference instead of $i_{\rm p}$ and $i_{\rm n}$. Thus, these compensation can easily be implemented in popular microcontrollers.

Fig. 4(a) shows the compensating voltage of a two-level ACM [10], [11]. The compensating voltage is directly calculated from the direction of $\bar{i}$ as given by

$$\Delta v = \begin{cases} V_{\rm dc}\dfrac{T_{\rm DT}}{T_{\rm SW}}, & (\bar{i} < 0) \\ -V_{\rm dc}\dfrac{T_{\rm DT}}{T_{\rm SW}}, & (0 < \bar{i}). \end{cases} \tag{3}$$

In this method, the compensating voltage is suddenly changed at zero crossings of $\bar{i}$. Thus, a small offset in the detected current may cause a relatively large voltage error in the approximation. Moreover, this method may cause an excessive compensation voltage when $0 < i_{\rm p}$ and $i_{\rm n} < 0$, because the voltage error is expected to be zero as given by (2).

Fig. 4(b) illustrates the compensating voltage of a linear ACM [12], which is given by

$$\Delta v = \begin{cases} V_{\rm dc}\dfrac{T_{\rm DT}}{T_{\rm SW}}, & (\bar{i} < -i_{\rm th}) \\ -V_{\rm dc}\dfrac{T_{\rm DT}}{T_{\rm SW}}\dfrac{\bar{i}}{i_{\rm th}}, & (-i_{\rm th} < \bar{i} < i_{\rm th}) \\ -V_{\rm dc}\dfrac{T_{\rm DT}}{T_{\rm SW}}, & (i_{\rm th} < \bar{i}) \end{cases} \tag{4}$$

where $i_{\rm th}$ is a threshold current for calculating the compensating voltage. Equation (2) suggests that it is better to set threshold current to be equal to or around the peak value of the current ripple. This method does not include a sudden change in the compensating voltage around the zero crossing of the converter current.

Fig. 4(c) shows the compensating voltage of a three-level ACM [14], [15], given by

$$\Delta v = \begin{cases} V_{\rm dc}\dfrac{T_{\rm DT}}{T_{\rm SW}}, & (\bar{i} < -i_{\rm th}) \\ 0, & (-i_{\rm th} < \bar{i} < i_{\rm th}) \\ -V_{\rm dc}\dfrac{T_{\rm DT}}{T_{\rm SW}}, & (i_{\rm th} < \bar{i}). \end{cases} \tag{5}$$

This method provides zero compensating voltage when the converter current is in a range of $-i_{\rm th} < \bar{i} < i_{\rm th}$. This method can compensate the voltage error in the whole converter current range when the threshold current $i_{\rm th}$ agrees with the ripple current $i_{\rm ripple}$. However, it is difficult to choose a suitable threshold current because the ripple current is changed according to the phase angle over the sinusoidal converter current.

IV. Analysis of the Voltage Error Considering Parasitic Capacitance

A. Actual Converter Voltage Waveforms

Fig. 5 shows experimentally measured converter voltage waveforms around the turn off of the switching devices. Fig. 5(a) is measured during the commutation from the upper device P to the lower device N. In case of a relatively large turn-off current at $i_{\rm p} = 1.0$ A, the converter voltage changes from $+165$ V to -165 V within 1 μs. On the other hand, the output capacitance are not completely charged or discharged during the dead time of 3 μs in case of $i_{\rm p} = 0.2$ A. Then, the lower device is turned on and forces the converter voltage to be -165 V at the end

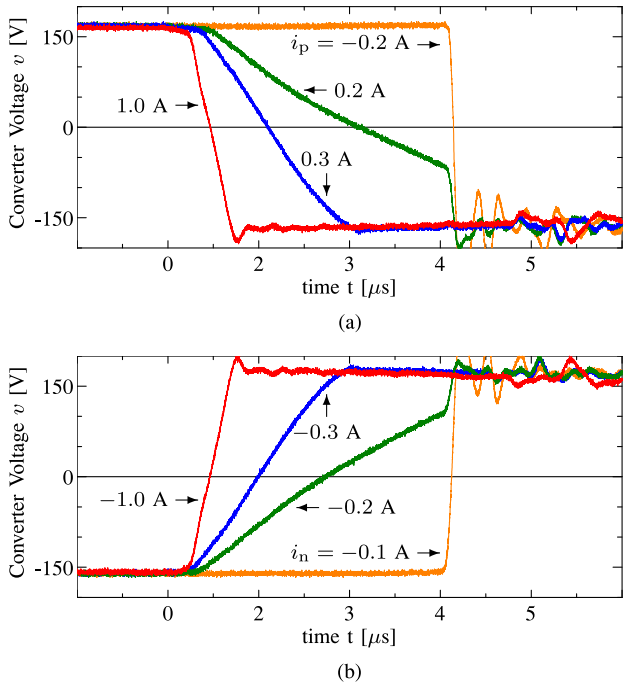

Fig. 5. Experimental waveforms of the converter voltage where dead time was set to $T_{\rm DT} = 3$ μs and the corresponding IGBT is turned off at $t = 0$. The commutation (a) from switch P to N and (b) from switch N to P.

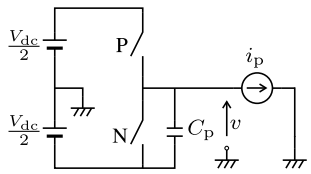

Fig. 6. Single-phase equivalent circuit for analysis of voltage error caused by a dead time.

of the dead time. Fig. 5(b) is in case of the commutation from the lower device N to the upper device P. As the same manner, the converter voltage waveform in the commutation is strongly affected by the turn-off current $i_{\rm n}$.

B. Effect of the Output Capacitance

Fig. 6 shows a single-phase equivalent circuit considering parasitic capacitance $C_{\rm p}$. In Fig. 6, the two IGBTs in Fig. 2 are replaced with two ideal switches and the parasitic capacitance $C_{\rm p}$ which is considered as the sum of the output stray capacitance in the upper and lower switching devices.

The following discussion considers the transition where switch P is turned off and switch N is turned on with dead time $T_{\rm DT}$. It is also assumed that the converter current is fixed at a turn-off current $i = i_{\rm p}$, which is represented by the current source in Fig. 6. Since $i_{\rm p}$ flows through $C_{\rm p}$ after the turn off of switch P, the converter voltage v linearly changes as given by

$$v = \frac{V_{\rm dc}}{2} - \frac{i_{\rm p}}{C_{\rm p}} t. \tag{6}$$

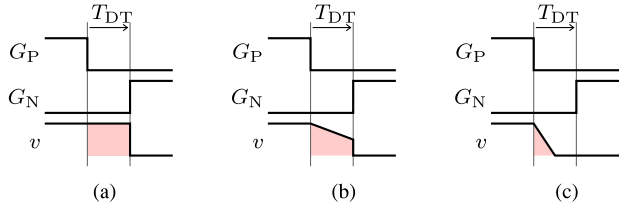

Fig. 7. Waveforms of gate signals and converter voltage v under the three different conditions: (a) $i_{\rm p} < 0$, (b) $0 < i_{\rm p} < I_{\rm C}$, and (c) $I_{\rm C} < i_{\rm p}$.

Here, a critical current is defined as $I_{\rm C} = C_{\rm p} V_{\rm dc} / T_{\rm DT}$. The converter voltage reaches $v = -V_{\rm dc}/2$ at the end of the dead time, when $i_{\rm p} = I_{\rm C}$.

Fig. 7 shows waveforms of the gate signals and converter voltage in three different cases of the turn-off current. Fig. 7(a) assumes a negative turn-off current $i_{\rm p} < 0$. The converter voltage v does not change after the turn-off of the switch P because the antiparallel diode still conducts and the current continuously flows through it. After the turn-on of switch N, the converter voltage becomes $v = -V_{\rm dc}/2$. Therefore, the average voltage error in case of $i_{\rm p} < 0$ is given by

$$V_{\rm DTp}(i_{\rm p}) = V_{\rm dc} \frac{T_{\rm DT}}{T_{\rm SW}}. \tag{7}$$

In Fig. 7(b), the turn-off current is in a range of $0 < i_{\rm p} < I_{\rm C}$. Then, the converter current discharges the parasitic capacitance $C_{\rm p}$ during the dead time. However, switch N is turned ON before the converter voltage reaches $v = -V_{\rm dc}/2$. Thus, the average voltage error proportionally decreases to $i_{\rm p}$, as given by

$$V_{\rm DTp}(i_{\rm p}) = V_{\rm dc} \frac{T_{\rm DT}}{T_{\rm SW}} \left(1 - \frac{i_{\rm p}}{2I_{\rm C}}\right). \tag{8}$$

On the contrary, the parasitic capacitance $C_{\rm p}$ can be completely discharged to zero before the end of the dead time in case of $I_{\rm C} < i_{\rm p}$. After the discharge, the converter voltage is fixed at $v = -V_{\rm dc}/2$ because of a conduction of the antiparallel diode connected to switch N. In this case, the average voltage error is inverse proportional to the turn-off current, which is represented by

$$V_{\rm DTp}(i_{\rm p}) = V_{\rm dc} \frac{T_{\rm DT}}{2T_{\rm SW}} \frac{I_{\rm C}}{i_{\rm p}}. \tag{9}$$

C. Voltage Error Against the Current Ripples

Fig. 8 shows the average voltage error caused by the dead time as a function of turn-off currents. The average voltage error in the commutation from switch P to switch N is summarized as follows:

$$V_{\rm DTp}(i_{\rm p}) = \begin{cases} V_{\rm dc} \dfrac{T_{\rm DT}}{T_{\rm SW}}, & (i_{\rm p} < 0) \\ V_{\rm dc} \dfrac{T_{\rm DT}}{T_{\rm SW}} \left(1 - \dfrac{i_{\rm p}}{2I_{\rm C}}\right), & (0 \le i_{\rm p} \le I_{\rm C}) \\ V_{\rm dc} \dfrac{T_{\rm DT}}{2T_{\rm SW}} \dfrac{I_{\rm C}}{i_{\rm p}}, & (I_{\rm C} < i_{\rm p}). \end{cases} \tag{10}$$

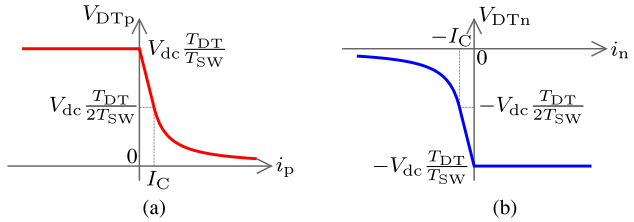

Fig. 8. Average voltage error against the turn-off currents (a) from switch P to N and (b) from switch N to P.

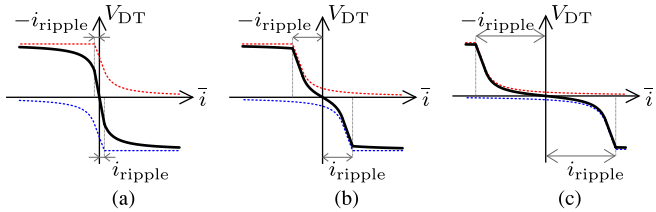

Fig. 9. Average voltage error against the converter current $\bar{i}$ under three different current ripple conditions: (a) $i_{\mathrm{ripple}} \ll I_{\mathrm{C}}$, (b) $i_{\mathrm{ripple}} \simeq I_{\mathrm{C}}$, and (c) $i_{\mathrm{ripple}} \gg I_{\mathrm{C}}$.

As the same manner, the switching transition from switch N to switch P also causes a similar average voltage error given by

$$V_{\mathrm{DTn}}(i_{\mathrm{n}}) = \begin{cases} V_{\mathrm{dc}}\dfrac{T_{\mathrm{DT}}}{2T_{\mathrm{SW}}}\dfrac{I_{\mathrm{C}}}{i_{\mathrm{n}}}, & (i_{\mathrm{n}} < -I_{\mathrm{C}}) \\ -V_{\mathrm{dc}}\frac{T_{\mathrm{DT}}}{T_{\mathrm{SW}}}\left(1+\dfrac{i_{\mathrm{n}}}{2I_{\mathrm{C}}}\right), & (-I_{\mathrm{C}} \le i_{\mathrm{n}} \le 0) \\ -V_{\mathrm{dc}}\dfrac{T_{\mathrm{DT}}}{T_{\mathrm{SW}}}, & (0 < i_{\mathrm{n}}). \end{cases} \tag{11}$$

Fig. 9 shows the relation between the average converter current $\bar{i}$ and the total average voltage error V_{DT}. The turn-off currents can be defined as follows:

$$i_{\mathrm{p}} = \bar{i} + i_{\mathrm{ripple}} \tag{12}$$

$$i_{\mathrm{n}} = \bar{i} - i_{\mathrm{ripple}} \tag{13}$$

where the i_{ripple} is the peak value of the converter current ripples. The total average voltage error in Fig. 9 can be obtained by substituting (12) and (13) into (10) and (11) and by adding V_{DTp} and V_{DTn}.

In a case of a small i_{ripple}, the polarity of the voltage error V_{DT} is changed around a zero crossing of the converter current $\bar{i}$, as shown in Fig. 9(a). On the other hand, the voltage error V_{DT} is almost proportional to $\bar{i}$ between $\pm i_{\mathrm{ripple}}$ in a case that i_{ripple} is almost equal to I_{C}, as shown in Fig. 9(b). In this case, linear ACM seems to be better than the other two conventional compensation methods. Furthermore, in a case that i_{ripple} is large, three-level ACM is more effective among the three conventional methods.

Figs. 10 and 11 show the measured voltage error against the average converter current. Fig. 10 was measured in case of using an IGBT module (CM200TU-12H, 600 V, 200 A, Mitsubishi), and its critical current was I_{C} =0.2 A. Fig. 11 was also measured by using the IGBT module, which 4.7 nF snubber capacitors were installed into every leg of as artificial output capacitors. The critical current in Fig. 11 was I_{C} =0.7 A in this measurement. Figs. 10 and 11 are measured under conditions of i_{ripple} =0.3, 2, and 4 A, respectively. The output capacitance or the critical current strongly affects to the steepness around the ripple current $\pm i_{\mathrm{ripple}}$. The larger output capacitance or critical current makes the steepness easier. These plots are very close to the characteristics in the three cases in Fig. 9. Thus, it is clarified that the measured voltage error also agrees well with theoretical results.

Fig. 12 shows squared errors ε against the normalized current ripple $i_{\mathrm{ripple}}/I_{\mathrm{C}}$ and the threshold current i_{th} used for the calculation. The squared error ε is defined by

$$\varepsilon = \frac{1}{V_{\mathrm{dc}}\frac{T_{\mathrm{DT}}}{T_{\mathrm{SW}}}}\int_{-\infty}^{\infty}\left(V_{\mathrm{DT}}(\bar{i}) - \Delta V(\bar{i})\right)^2 d\bar{i}. \tag{14}$$

The squared error allows us to compare the performance of different compensating methods. In Fig. 12(a), the threshold current i_{th} is adjusted to minimize the squared error according to the i_{ripple}, as shown in Fig. 12(b). The horizontal axes in Fig. 12 are the current ripple which is normalized by I_{C}. The two-level ACM has the minimum squared error of $\varepsilon = 1$ around $i_{\mathrm{ripple}}/I_{\mathrm{C}} = 0.8$, and the squared error increases according to i_{ripple}. The linear ACM has a smaller squared error than the three-level ACM in a range of $i_{\mathrm{ripple}}/I_{\mathrm{C}} < 5.8$. On the other hand, the three-level ACM exhibits the smallest squared error among three ACMs in a range of $i_{\mathrm{ripple}}/I_{\mathrm{C}} > 5.8$. As shown in Fig. 12(b), the threshold current should be adjusted according to the current ripple in order to minimize the squared error. The threshold currents in Fig. 12(b) are almost proportional to the normalized ripple current $I_{\mathrm{ripple}}/I_{\mathrm{C}}$ in a large current ripple range.

For example, the normalized current ripple is calculated as $i_{\mathrm{ripple}}/I_{\mathrm{C}} = 18$ in case of the converter used in following experiments, because $I_{\mathrm{C}} = 0.2$ A and $i_{\mathrm{ripple}} = 3.6$ A. Therefore, the three-level ACM is more suitable for the grid-connecting converter. On the other hand, the linear ACM could compensate the voltage error better than the three-level compensation method if the inductance of the ac inductors were 1 mH or grater because of $i_{\mathrm{ripple}}/I_{\mathrm{C}} = 5.4$. Generally, the current ripple i_{ripple} is changed according to the phase angle of the voltage reference for the PWM control. Since the effect of the voltage error is significant around the zero crossing of the converter current, it is possible to decide the suitable compensation method based on the ripple current at $\bar{i} = 0$.

D. Turn-Off Current of a Three-Phase Converter

Fig. 13 shows the circuit configuration of a three-phase grid-connected voltage-source converter. Here, it is assumed that the grid is balanced three-phase voltage source and ac inductors are only considered. In this model, the voltages applied across the

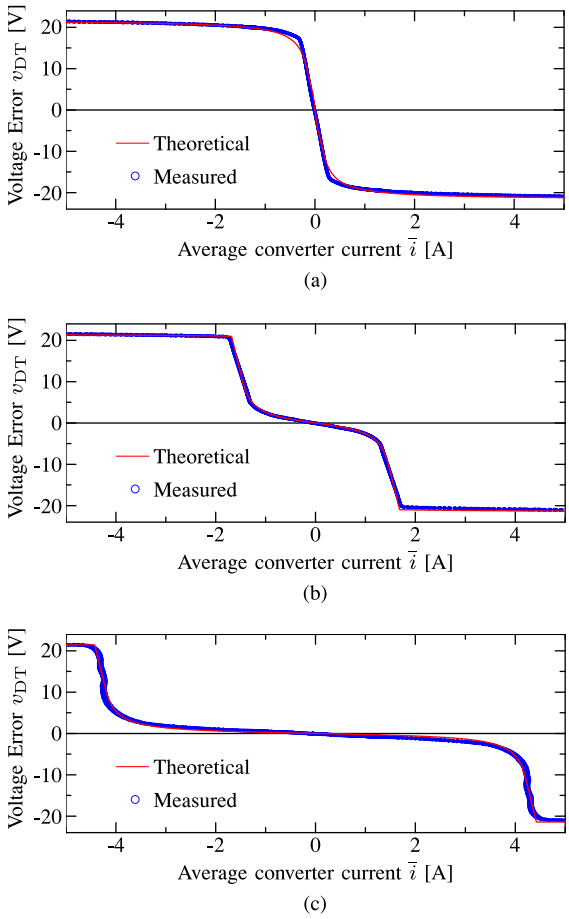

Fig. 10. Measured total voltage error $v_{\rm DT}$ against the average converter current: (a) $i_{\rm ripple} = 0.3$ A, (b) $i_{\rm ripple} = 2$ A, and (c) $i_{\rm ripple} = 4$ A.

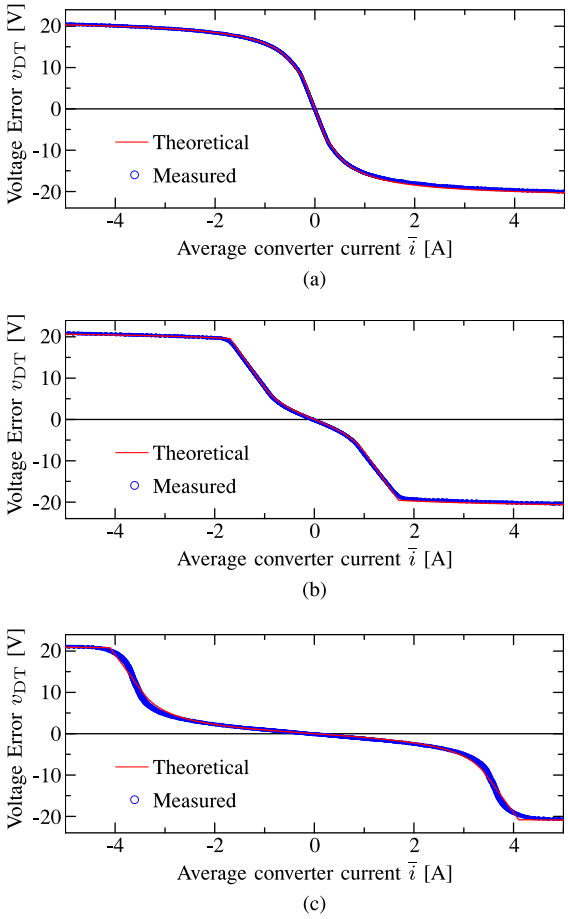

Fig. 11. Measured total voltage error $v_{\rm DT}$ against the average converter current where using an additional output capacitor of 4.7 nF. (a) $i_{\rm ripple} = 0.3$ A, (b) $i_{\rm ripple} = 2$ A, and (c) $i_{\rm ripple} = 4$ A.

ac inductors are given by

$$\begin{cases} v_{\rm La} = L\dfrac{di_{\rm a}}{dt} = v_{\rm a} - v_{\rm sa} - v_{\rm o} \\ v_{\rm Lb} = L\dfrac{di_{\rm b}}{dt} = v_{\rm b} - v_{\rm sb} - v_{\rm o} \\ v_{\rm Lc} = L\dfrac{di_{\rm c}}{dt} = v_{\rm c} - v_{\rm sc} - v_{\rm o} \end{cases} \tag{15}$$

where $v_{\rm o}$ is the potential of the neutral point of the three-phase voltage source regarding to the middle point of the dc link. Since $v_{\rm sa} + v_{\rm sb} + v_{\rm sc} = 0$ and $i_{\rm a} + i_{\rm b} + i_{\rm c} = 0$, the neutral-point potential is represented by

$$v_{\rm o} = \frac{v_{\rm a} + v_{\rm b} + v_{\rm c}}{3}. \tag{16}$$

As the converter voltages $v_{\rm a}, v_{\rm b}, v_{\rm c}$ have rectangle voltage waveforms having $\pm V_{\rm dc}/2$, the controller can calculate $\frac{di_{\rm a}}{dt}$, $\frac{di_{\rm b}}{dt}$, $\frac{di_{\rm c}}{dt}$ from (15) and predict the converter current waveforms $i_{\rm a}$, $i_{\rm b}$, and $i_{\rm c}$ by means of time integral.

Fig. 14 shows voltage and current waveforms of a three-phase PWM control method based on a triangle carrier signal. In this figure, voltage references are assumed to $v_{\rm a}^* > v_{\rm b}^* > v_{\rm c}^*$. For example, the turn-off current of the upper switch in the a-phase can be obtained from the following time integral:

$$i_{\rm ap} = \int_{t_0}^{t_{\rm ap}} \frac{v_{\rm La}}{L} dt + i_{\rm a0} \tag{17}$$

where $t_{\rm ap}$ is the turn-off time of the upper switch in the a-phase and $i_{\rm a0}$ is the initial value of the a-phase converter current at t_0. Because the inductor voltage consists of a three-level rectangle voltage waveform as shown in Fig. 14, the above integral operation can be replaced with some summations and multiplications, as the following equation:

$$\begin{aligned} i_{\rm ap} = \; & i_{\rm a0} - v_{\rm sa}(t_{\rm cp} - t_0) + \left(\frac{V_{\rm dc}}{3} - v_{\rm sa}\right)(t_{\rm bp} - t_{\rm cp}) \\ & + \left(\frac{2V_{\rm dc}}{3} - v_{\rm sa}\right)(t_{\rm ap} - t_{\rm bp}). \end{aligned} \tag{18}$$

The turn-off time of the upper switch in the a-phase $t_{\rm ap}$ can be calculated from the a-phase voltage reference, given by

$$t_{\rm ap} = \left(\frac{1}{4} + \frac{v_{\rm a}^*}{2V_{\rm dc}}\right) T_{\rm sw} + t_0. \tag{19}$$

Thus, the turn-off currents in the three-phase converter can be calculated by using only a relatively simple multiply-accumulate operation. Eliminating $t_{\rm ap}$, $t_{\rm bp}$, $t_{\rm cp}$ from (18), the turn-off

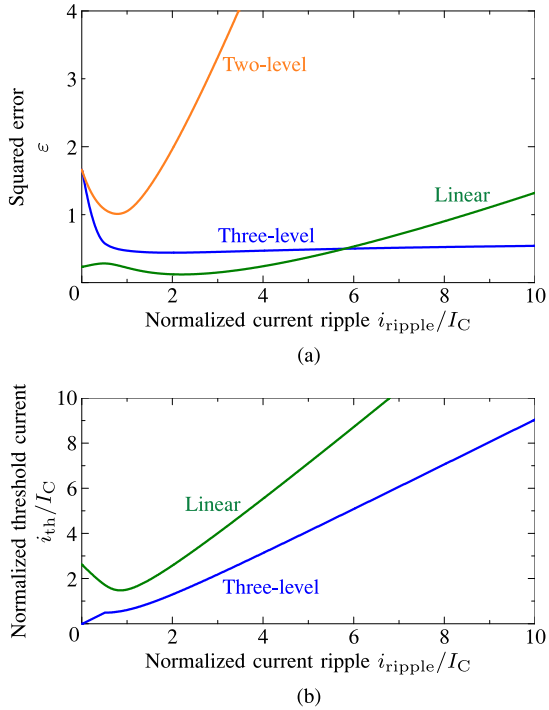

Fig. 12. The relations between (a) squared error ε and the current ripple $i_{\rm ripple}/I_{\rm C}$ and (b) threshold current $i_{\rm th}$ versus current ripple $i_{\rm ripple}/I_{\rm C}$.

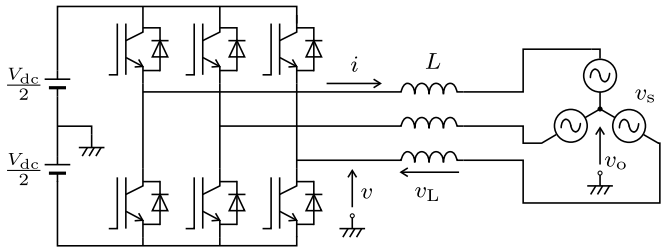

Fig. 13. Grid-connected three-phase PWM converter circuit.

currents in the three-phase converter are obtained by

$$i_{\rm ap} = \left(\frac{v_{\rm a}^*}{3} - \frac{v_{\rm b}^*}{6} - \frac{v_{\rm c}^*}{6} - \frac{v_{\rm sa}}{4} - \frac{v_{\rm sa}v_{\rm a}^*}{2V_{\rm dc}}\right)\frac{T_{\rm sw}}{L} + i_{\rm a0} \quad (20)$$

$$i_{\rm an} = \left(\frac{v_{\rm a}^*}{3} - \frac{v_{\rm b}^*}{6} - \frac{v_{\rm c}^*}{6} - \frac{3v_{\rm sa}}{4} + \frac{v_{\rm sa}v_{\rm a}^*}{2V_{\rm dc}}\right)\frac{T_{\rm sw}}{L} + i_{\rm a0} \quad (21)$$

$$i_{\rm bp} = \left(\frac{v_{\rm b}^*}{6} - \frac{v_{\rm c}^*}{6} - \frac{v_{\rm sb}}{4} - \frac{v_{\rm sb}v_{\rm b}^*}{2V_{\rm dc}}\right)\frac{T_{\rm sw}}{L} + i_{\rm b0} \quad (22)$$

$$i_{\rm bn} = \left(\frac{v_{\rm b}^*}{2} - \frac{v_{\rm a}^*}{3} - \frac{v_{\rm c}^*}{6} - \frac{3v_{\rm sb}}{4} + \frac{v_{\rm sb}v_{\rm b}^*}{2V_{\rm dc}}\right)\frac{T_{\rm sw}}{L} + i_{\rm b0} \quad (23)$$

$$i_{\rm cp} = \left(-\frac{v_{\rm sc}}{4} - \frac{v_{\rm sc}v_{\rm c}^*}{2V_{\rm dc}}\right)\frac{T_{\rm sw}}{L} + i_{\rm c0} \quad (24)$$

$$i_{\rm cn} = \left(\frac{2v_{\rm c}^*}{3} - \frac{v_{\rm a}^*}{3} - \frac{v_{\rm b}^*}{3} - \frac{3v_{\rm sc}}{4} + \frac{v_{\rm sc}v_{\rm c}^*}{2V_{\rm dc}}\right)\frac{T_{\rm sw}}{L} + i_{\rm c0}. \quad (25)$$

The controller can estimate the turn-off currents $\hat{i}_{\rm p}$ and $\hat{i}_{\rm n}$ from (20) through (25). As (20) through (25), the errors in $i_{\rm a0}$, $i_{\rm b0}$, and $i_{\rm c0}$ directly appear in the estimated turn-off currents. Thus, synchronous sampling technique [18] was introduced to minimize the error caused by the switching ripples in the converter current. It is also effective to use the current reference as the initial current, instead of the detected current. As a result, the controller can calculate an accurate average voltage error from (10) and (11) which can also be used as the compensating voltage ΔV for the dead time. The compensating voltage based on the above analysis is represented by

$$\Delta V = V_{\rm DTp}(\hat{i}_{\rm p}) + V_{\rm DTn}(\hat{i}_{\rm n}). \quad (26)$$

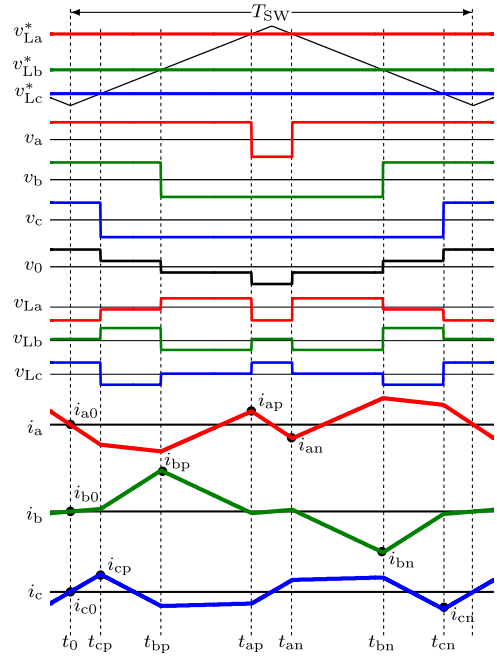

Fig. 14. Voltage and current waveforms of a three-phase PWM method based on a triangle carrier signal.

V. Experiment Results

Fig. 15 shows experimental voltage waveforms measured under the conditions of no compensation and four different compensation methods. A three-phase resistive load was connected to the converter in Fig. 1 instead of the grid, in order to eliminate the effect of the current feedback performance and the harmonic distortion in the grid voltage. In the experiments, a sinusoidal three-phase balanced voltage reference was provided to the converter. The rms line-to-line voltage of the reference was set to 150 V, and its frequency was 50 Hz. In addition, the threshold current $i_{\rm th}$ was set to be minimized the voltage THD for each compensation method. The voltage THD was calculated from the harmonic components in the u-phase voltage up to the 50th order, which is measured by using Fourier analysis.

Fig. 15(a) shows the load voltage waveform without compensation. It seems a trapezoidal wave shape having a voltage THD of 4% mainly due to fifth and seventh harmonic components contained in the voltage error caused by the dead time. Fig. 15(b) is the waveform of two-level ACM. Comparing with that in Fig. 15(a), the converter voltage had a sinusoidal

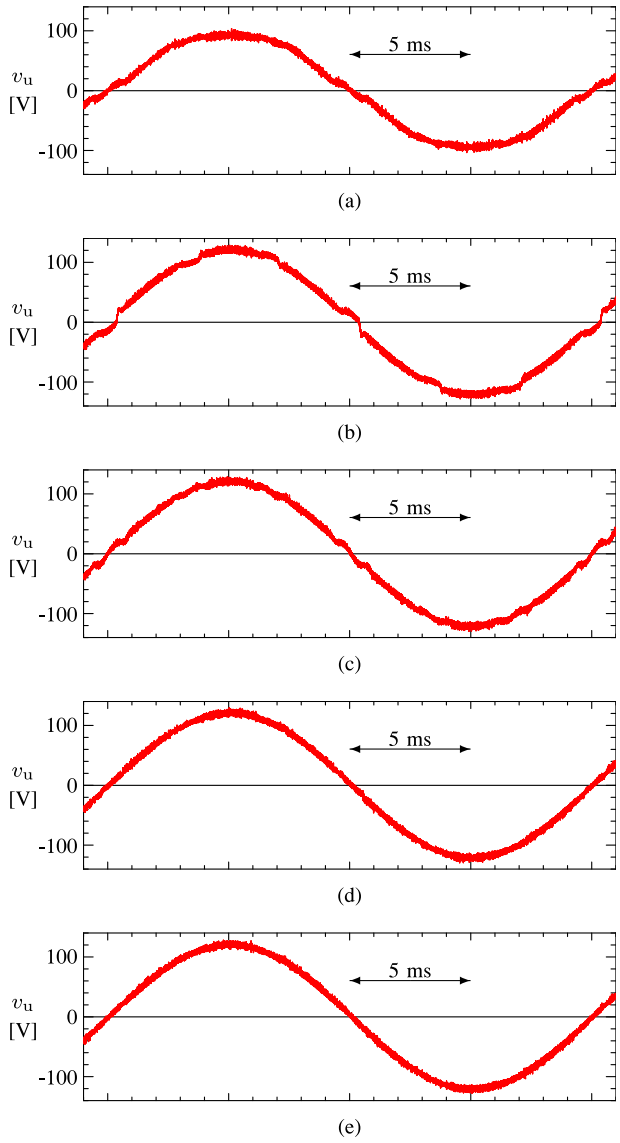

Fig. 15. Experimental voltage waveforms of the resistive load (a) without compensation, (b) with a two-level ACM, (c) with a linear ACM, (d) with a three-level ACM, and (e) with TTCM.

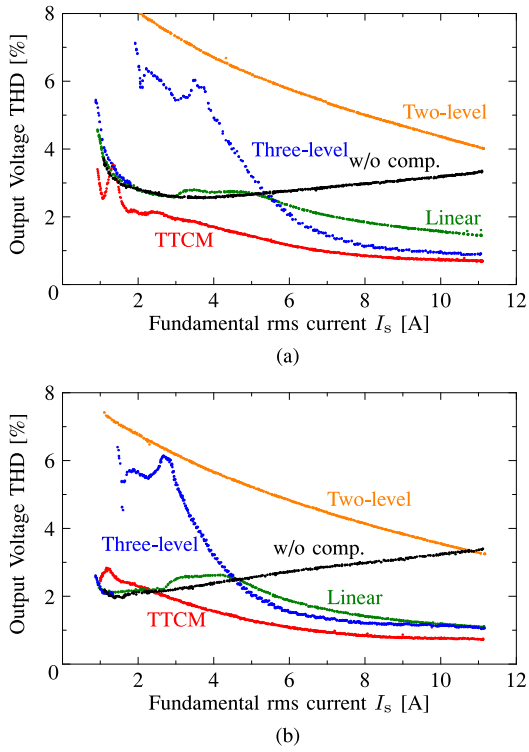

Fig. 16. Measured voltage THDs under a three-phase resistive load condition (a) without additional output capacitors and (b) with additional output capacitors of 4.7 nF.

waveform. However, considerable distortion still appeared around the zero-crossing and the peak voltage as shown in Fig. 15(b). Thus, the voltage THD was as high as 5%. Fig. 15(c) is the waveform of linear ACM. The voltage distortion was reduced to 2% in THD. Fig. 15(d) is the waveform of three-level ACM. The converter voltage included a less voltage distortion than the two-level and linear ACMs. The waveform became close to a sinusoidal waveform with a THD of 0.5%. Fig. 15(e) shows the measured waveform with TTCM developed in this paper. This method uses the analytical result of the voltage error in (26) as the compensating voltage ΔV. The voltage waveform was a sinusoidal waveform which had a very low THD of 0.4% as well as that in the three-level ACM.

Fig. 16 shows the experimental voltage THDs measured using the IGBT module under a three-phase resistive load condition. In the following experiments, the voltage reference was fixed at 150 V in line-to-line rms voltage, and the load current was adjusted by the three-phase resistive load. The threshold currents $i_{\rm th}$ were set to be $i_{\rm th} = 4.1$ A for the linear ACM and $i_{\rm th} = 2.5$ A for the three-level ACM in Fig. 16(a), and $i_{\rm th} = 3.7$ A for the linear ACM and $i_{\rm th} = 1.9$ A for the three-level ACM in Fig. 16(b). These threshold currents was adjusted and decided to minimize the voltage THD at a load current of 11 A in each compensation method. The current THD was also calculated from the harmonic components up to 50th order in the u-phase load current waveform.

The voltage THD of the two-level ACM is higher than that without compensation because excess compensation occurred around a current zero-crossing and a significant voltage distortion appeared in this experimental system having the small ac inductors. The three-level ACM is more effective in suppressing the voltage harmonics than the linear ACM in Fig. 16(a) because of a large current ripple with $i_{\rm ripple}/I_{\rm C} = 16$ in this system. On the other hand, the three-level ACM can suppress the voltage harmonics as much as the linear ACM in Fig. 16(b) because of $i_{\rm ripple}/I_{\rm C} = 5.5$ in this system. The snubber capacitor shrinks and shifts the curves of the linear ACM and the three-level ACM. As a result, the voltage THDs of the linear and three-level ACMs were the same at $I_{\rm s} = 5.5$ A in Fig. 16(a), while their plots crossed at $I_{\rm s} = 4.5$ A as shown in Fig. 16(b). The three-level ACM exhibited a relatively high voltage THD in a current range smaller than the crossover which caused by the fixed threshold current $i_{\rm th}$. The result implies that the threshold current $i_{\rm th}$ should be set to an appropriate value. Furthermore, the voltage THD without compensation is less than that in the three conventional compensation methods when the load current

is smaller than the crossover point. In this case, the load current is smaller than the current ripple amplitude of $I_{\rm ripple} = 3.6$ A, and thus, almost no voltage error occurs as shown in Fig. 3. The voltage THD of the linear ACM is as small as that without compensation in a current range smaller than $i_{\rm ripple}$. Most effective compensation performance is obtained by the TTCM in all over the measured current range.

VI. Conclusion

This paper has analyzed the detailed the voltage error caused by the dead time in voltage-source PWM converters and discussed various compensation methods from the theoretical and experimental point of view. Considering the output capacitances of switching devices, the average voltage error in a switching cycle has been derived from the theoretical analysis of the converter voltage during the dead time. The analytical result has revealed that the average voltage error can be obtained as the function of the turn-off current. The current ripple analysis of three-phase PWM converters has also been conducted to estimate the turn-off currents of each switching device. It is clarified that a simple multiply-accumulate operation makes it possible to calculate the turn-off current from detected currents by a synchronous sampling or from the reference values for the grid current. Furthermore, the compensation method based on the analytical result has been developed and compared with the conventional compensating methods. As a result, compensating performance of conventional compensation methods have been quantitatively clarified. The two-level and linear ACMs are suitable for systems having relatively small current ripples. On the other hand, the three-level ACM would exhibit a better compensating performance in applications with a large current ripple. It has also been clarified that an appropriate adjustment of the threshold current is required to obtain a effective compensation performance in the linear and three-level ACMs.

References

[1] J. Millan, P. Godignon, X. Perpinya, A. Perez-Tomas, and J. Rebollo, "A survey of wide band gap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[2] T. Friedli, S. D. Round, D. Hassler, and J. W. Kolar, "Design and performance of a 200-kHz all-SiC JFET current DC-link back-to-back converter," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1868–1878, Sep./Oct. 2009.

[3] T. Reiter, D. Polenov, H. Proöbstle, and H.-G. Herzog, "PWM dead time optimization method for automotive multiphase DC/DC-converters," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1604–1614, Jun. 2010.

[4] A.C. Oliveira, C.B. Jacobina, and A.M.N. Lima, "Improved dead-time compensation for sinusoidal PWM inverters operating at high switching frequencies," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2295–2304, Aug. 2007.

[5] J. Muhlethaler, M. Schweizer, R. Blattmann, J. W. Kolar, and A. Ecklebe, "Optimal design of LCL harmonic filters for three-phase PFC rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3114–3125, Jul. 2013.

[6] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an LCL-filter-based three-phase active rectifier," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1281–1291, Sep./Oct. 2005.

[7] L. Ben-Brahim, "On the compensation of dead time and zero-current crossing for a PWM-inverter-controlled AC servo drive," *IEEE Trans. Ind. Electron.*, vol. 51, no. 5, pp. 1113–1117, Oct. 2004.

[8] S. Bolognani, L. Peretti, and M. Zigliotto, "Repetitive-control-based self-commissioning procedure for inverter nonidealities compensation," *IEEE Trans. Ind. Appl.*, vol. 44, no. 5, pp. 1587–1596, Sep./Oct. 2008.

[9] M. Nagao and K. Harada, "Effects on commutation elements in inductor commutation soft-switched PWM inverter and its design equations," *IEEE Trans. Power Electron.*, vol. 16, no. 6, pp. 858–865, Nov. 2001.

[10] S. Jeong and M. Park, "The analysis and compensation of dead-time effects in PWM inverters," *IEEE Trans. Ind. Electron.*, vol. 38, no. 2 , pp. 108–114, Apr. 1991.

[11] Seon-Hwan Hwang and Jang-Mok Kim, "Dead time compensation method for voltage-fed PWM inverter," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 1–10, Mar. 2010.

[12] A. C. Oliveira, C. B. Jacobina, A. M. N. Lima, and E. R. C. da Silva, "Dead-time compensation in the zero-crossing current region,"in *Proc. IEEE 34th Annu. Power Electron. Spec. Conf.*, 2003, vol. 4, pp. 1937–1942.

[13] Z. Guo and F. Kurokawa, "Control and PWM modulation scheme for dead-time compensation of CVCF inverters," in *Proc. IEEE 31st Int. Telecommun. Energy Conf.*, 2009, pp. 1–6.

[14] J. M. Schellekens, R. A. M. Bierbooms, and J. L. Duarte, "Dead-time compensation for PWM amplifiers using simple feed-forward techniques," in *Proc. IEEE Int. Conf. Elect. Mach.*, 2010, pp. 1–6.

[15] M. A. Herrán, J. R. Fischer, S. A. González, M. G. Judewicz, and D. O. Carrica, "Adaptive dead-time compensation for grid-connected PWM inverters of single-stage PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2816–2825, Jun. 2013.

[16] M. Miyazaki, Y. Hayashi, and T. Fukumoto, "An estimation of voltage control error in PWM inverter taking instantaneous phase current value into account," (in Japanese), in *Proc. IEEJ IASC*, 2011, pp. 1–26.

[17] M. Ogawa, S. Ogasawara, and M. Takemoto, "A feedback-type dead-time compensation method for high-frequency PWM inverter –Delay and pulse width characteristics–," in *Proc. IEEE Appl. Power Electron. Conf.*, 2012, pp. 100–105.

[18] P. Jintakosonwit, H. Fujita, and H. Akagi, "Control and performance of a fully-digital-controlled shunt active filter for installation on a power distribution system," *IEEE Trans. Power Electron.*, vol. 17, no. 1, pp. 132–140, Jan. 2002.

Tomoyuki Mannen (S'13) received the B.S. and M.S. degrees in electrical engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2012 and 2014, respectively. He is currently working toward the Ph.D. degree at the Tokyo Institute of Technology.

His research interests include grid-connection converters, active power filters, and its control methods.

Mr. Mannen received the 2013 Institute of Electrical Engineers of Japan Industry Application Society Conference Paper Presentation Award.

Hideaki Fujita (M'91–SM'10) received the B.S. and M.S. degrees from the Nagaoka University of Technology, Niigata, Japan, in 1988 and 1990, respectively, and the Dr. Eng. degree from the Tokyo institute of Technology, Tokyo, Japan, in 2000, all in electrical engineering.

He joined Okayama University, Okayama, Japan, in 1991, as a Research Associate. Since 2002, he has been an Associate Professor in the Department of Electrical Engineering, Tokyo Institute of Technology. His research interests include high-frequency inverters for industrial induction heating, power converters for solar and wind power generations, and multilevel converters.

Dr. Fujita received four Committee Prize Paper Awards from the IEEE Industry Applications Society Industrial Power Converter Committee in 1990, 1995, 1998, and 2003, and a Society Prize Paper Award from the IEEE Industry Applications Society in 2009. He was the recipient of the 2005 Isao Takahashi Power Electronics Award presented by the Institute of Electrical Engineers of Japan (IEEJ) at the International Power Electronics Conference (IPEC-Niigata 2005). He was awarded the IEEJ Distinguished Paper Award in 2008, and the IEEJ Industry Applications Society Distinguished Transaction Paper Award in 2010. He was the Chair of the IEEE IAS Japan Chapter 2008–2009. He is an Associate Editor for the IEEE Transactions on Industry Applications and the IEEE Transactions Power Electronics, and the *IEEJ Journal of Industry Applications*.