Analysis and Mitigation of Inverter Output Impedance Impacts for Distributed Energy Resource Interface

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***Abstract*—In order to provide reliable electric power, the interfacing voltage source inverters in distributed generation often rely on autonomous droop control method integrated with virtual impedance and inner voltage and current control loops. In general, the droop-controlled inverters can be modeled as a controllable voltage source in series with output impedance. However, stability, dynamic performance, and load adaptability in islanding mode are sensitive to the inverter output impedance. In this paper, the detailed impacts of the inverter output impedance are investigated in different operation modes. Furthermore, an inverter current feedforward control scheme is proposed to mitigate the effects. With the implementation of the proposed control scheme, system reliability and load adaptability in islanding mode are enhanced without additional control complexity and extra sensors. Moreover, a voltage magnitude control loop is added to improve the control accuracy of reactive power flow in grid-connected mode. Finally, the proposed strategy is validated with simulation and experiments based on a 15-kVA prototype.**

***Index Terms*—Distributed generation, droop control, inverter current feedforward, inverter output impedance, voltage source inverters (VSIs).**

I. Introduction

With increasing concerns about environmental problems of conventional energy and security of the centralized power generation, distributed generation (DG) and renewable energy sources, e.g., wind and solar energy, are widely applied recently [1]–[3]. By integrating the DG units, a power-electronics-interfaced microgrid can be formed [2]–[4]. Moreover, voltage source inverters (VSI) are often applied as the power electronics interface.

In order to offer reliable electrical power supply, the microgrid should be able to operate in both grid-connected (GC) mode and islanding (IS) mode [4]–[6]. Therefore, the droop control method has been widely applied for power sharing among parallel inverters in IS mode and between DG and utility in GC mode [5]–[12]. Seamless transition from GC mode to IS mode can be realized while grid synchronization measures are necessary for transition from IS mode to GC mode [10], [12], [13].

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The droop-controlled inverters can be modeled as a controllable voltage source in series with output impedance [5], [7], [14]–[16]. Impedance-based stability criterion is proposed for GC inverters in [14]. Nevertheless, the impacts of inverter output impedance in both operation modes, especially upon stability and dynamic performance, are seldom analyzed. Actually, virtual impedance insertion can be efficient to enhance system stability while the dynamic response is sacrificed [5], [7], [9], [11], [12], [15]. Moreover, load adaptability (note that the transient during load switching and voltage quality under nonlinear and unbalanced loads are named the load adaptability in this paper) in IS mode may also be influenced by virtual impedance [15]. In addition, inadequate accuracy of reactive power flow control in GC mode is also a disadvantage for droop-controlled inverters [5], [8], [11], [17]–[21]. Pure integrators can be applied in the droop control method to improve the control accuracy of power sharing in GC mode [11]. Nevertheless, total loads may not coincide with the total injected power in IS mode. The voltage of point of common coupling (PCC) is introduced while extra sensors are needed [8], [20]. Meanwhile, it may be not practical to measure PCC voltage since DG units are distributed in different locations.

When the VSI-based microgrid is disconnected from the grid, severe voltage quality problems may be caused due to the presence of nonlinear or unbalanced loads. Essentially, voltage quality problems in IS mode can be regarded as the disturbance of load current which is introduced by the inverter output impedance. Suppression of the harmonic distortion and compensation of the voltage unbalance have been investigated in [15], [17], [22]–[26]. Liu *et al.* [15] utilizes a proportional-integral (PI) plus multiresonant controller and modified virtual impedance to enhance the voltage quality in IS mode. In [23], the direct change of the voltage reference is proposed to compensate for voltage unbalance, which requires the positive- and negative-sequence extraction in advance. The stability is also influenced by the unbalance compensation gain. Harmonic droop control strategy with one harmonic droop controller for each individual harmonic component is developed in [24], while computational burden is the restriction. [25] makes use of the proportional plus multiresonant controller for inner voltage regulation loop in the stationary *abc*-frame. However, the system stability is degraded, and a lead-lag compensator is needed. In addition, load current feedforward control is proposed to suppress harmonics while extra sensors for load current are required [26].

The dynamic performance during load switching in IS mode is mainly determined by the bandwidth of the voltage loop and

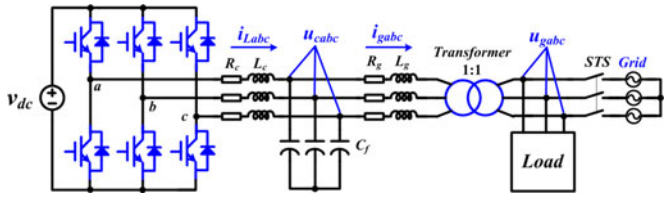

Fig. 1. Schematic diagram of the three-phase VSI with *LCL* filter.

inverter output impedance. Particularly, during load switching from full load to no load in IS mode, spike of the inverter's output voltage may induce saturation of the isolation transformer and damage the critical loads. Unfortunately, the bandwidth of the voltage loop is usually limited especially under high-power circumstance with lower switching frequency, which fails to respond rapidly to the load switching in IS mode. As a result, inverter output impedance is the key factor to improve the dynamic performance during load switching.

Considering the significant influence of inverter output impedance, the impacts of the inverter output impedance on stability, dynamic performance, and load adaptability in IS mode are further investigated in this paper through the small-signal analysis in different operation modes. Furthermore, the inverter current feedforward control (ICFC) scheme is proposed to mitigate the impacts of inverter output impedance. The proposed ICFC scheme is integrated into the conventional control strategy which includes the droop controller, virtual impedance, and inner voltage and current loop. With the implementation of the proposed control scheme, system reliability and load adaptability in IS mode are enhanced without additional control complexity and extra current sensors. Meanwhile, a voltage magnitude control loop is added to improve the accuracy of reactive power sharing in GC mode. Finally, the proposed strategy is validated with simulation and experiments based on a 15-kVA prototype.

This paper is organized as follows. Modeling of the conventional control strategy is introduced in Section II. Impacts of inverter output impedance are analyzed with the small-signal models in Section III. The ICFC scheme is introduced to mitigate the impacts of inverter output impedance, and the detailed performance analysis is presented in Section IV. Validation of simulation and experiment results is given in Section V. The last section summarizes the investigation.

II. Modeling of Conventional Control Strategy

In general, VSIs are applied as the interface to connect DG units to the grid. Fig. 1 shows the three-phase VSI with *LCL* filter considered as the interface in this paper. L_c is the inverter-side filter inductor, and R_c is the equivalent series resistor (ESR). C_f is the filter capacitor. L_g consists of the grid-side inductor of the *LCL* filter, the leakage inductor of the isolation transformer and the feeder inductance, and R_g is the ESR. i_{Labc}, u_{cabc}, i_{gabc}, and u_{gabc} are the inverter-side current, the voltage of the filter capacitor, the grid-side current, and the grid voltage in GC mode or load voltage in IS mode. Transition between GC mode and IS mode is realized through the static transfer switch. In addition, different load conditions, e.g., unbalanced loads and nonlinear loads, may be dealt with in IS mode.

As shown in Fig. 2, conventional control strategy [5] is discussed in the synchronous reference frame (SRF), and the main control loops are explained as follows.

A. Droop Control Loops

In order to avoid communication wires while obtaining good power sharing, the droop control method is often utilized. The conventional active power–frequency and reactive power–voltage magnitude droop control are shown in Fig. 2 as

$$\omega = \omega_0 + k_p(P_0 - P) \tag{1}$$

$$E = E_0 + k_q(Q_0 - Q) \tag{2}$$

where ω and E are the frequency and amplitude of the output voltage reference, ω_0 and E_0 are the nominal frequency and amplitude, P and Q are the active and reactive power, P_0 and Q_0 are their references, and k_p and k_q are the droop coefficients, respectively. Note that compensation networks in droop loops may be needed to guarantee the system stability, which may damp the system dynamic response simultaneously [11].

In addition, the instantaneous fundamental positive sequence power can be calculated as

$$P = \frac{\omega_f}{s+\omega_f}(u_{cd}i_{Ld} + u_{cq}i_{Lq}) \tag{3}$$

$$Q = \frac{\omega_f}{s+\omega_f}(u_{cq}i_{Ld} - u_{cd}i_{Lq}) \tag{4}$$

where ω_f is the cutoff frequency of the first-order low-pass filter (LPF), and u_{cdq} and i_{Ldq} are the three-phase instantaneous output voltage and inverter current when transformed to the SRF, respectively.

B. Virtual Impedance Loop

The system oscillation is damped, and stability is enhanced with the addition of virtual resistance. Furthermore, virtual inductance is considered to make the output impedance more inductive to improve the decoupling of the active and reactive power [5], [9], [23]. However, even though the system is well damped with virtual impedance, the dynamic response is degraded.

The voltage drops across the virtual impedance in SRF shown in Fig. 2 can be expressed as

$$u_{vd} = (R_v + sL_v)i_{gd} - \omega L_v i_{gq} \tag{5}$$

$$u_{vq} = (R_v + sL_v)i_{gq} + \omega L_v i_{gd} \tag{6}$$

where R_v and L_v are the virtual resistance and inductance, and i_{gdq} is the injected grid current when in GC mode or the load current when in IS mode in SRF, respectively. Considering about the low bandwidth of droop controller, the derivative term sL_v has a little impact on stability and dynamic performance. Moreover, the impacts of the derivative term sL_v on low-frequency performance can also be ignored. In this paper, when implemented in simulation and experiments, the derivative term sL_v

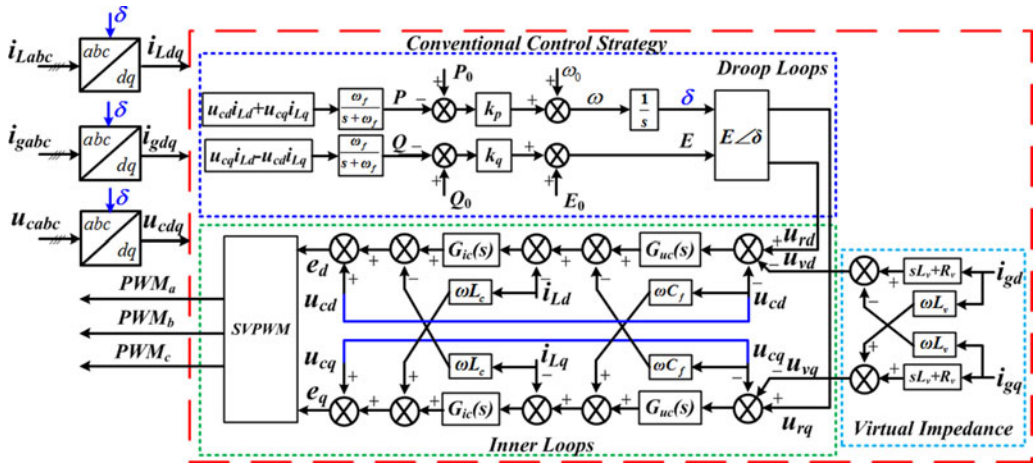

Fig. 2. Block diagram of conventional control strategy [5].

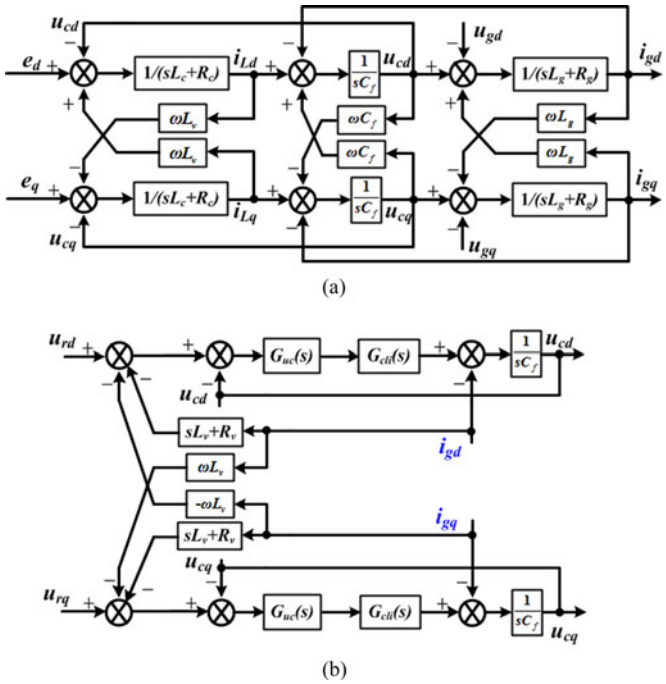

Fig. 3. Inner voltage and current control loops: (a) model of the VSI with *LCL* filter in SRF, (b) simplified model of the inner loops.

is neglected to avoid introducing high-frequency noise. However, it is included in theoretical analysis to thoroughly research the impacts.

C. Inner Voltage and Current Control Loops

According to the inner voltage and current loops with PI controller in Fig. 2 and the model of the VSI in Fig. 3(a), the simplified model of the inner loops is derived in Fig. 3(b) [15].

The closed-loop transfer function of the current loop and voltage loop in Fig. 3(b) can be derived as

$$G_{cli}(s) = \frac{G_{ic}(s) \cdot \dfrac{1}{sL_c + R_c}}{1 + G_{ic}(s) \cdot \dfrac{1}{sL_c + R_c}} \tag{7}$$

$$G_{clu}(s) = \frac{\frac{1}{sC_f} G_{uc}(s) G_{cli}(s)}{1 + \dfrac{1}{sC_f} G_{uc}(s) G_{cli}(s)} \tag{8}$$

$$\begin{bmatrix} u_{cd} \\ u_{cq} \end{bmatrix} = G_{clu}(s) \begin{bmatrix} u_{rd} \\ u_{rq} \end{bmatrix} - \begin{bmatrix} Z_o(s) + Z_v(s) & -G_{clu}(s)\omega L_v \\ G_{clu}(s)\omega L_v & Z_o(s) + Z_v(s) \end{bmatrix} \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} \tag{9}$$

where $G_{ic}(s) = k_{pi} + k_{ii}/s$, $G_{uc}(s) = k_{pv} + k_{iv}/s$, u_{rdq} is the output voltage reference, $\boldsymbol{Z_o(s)}$ is the inverter output impedance, $Z_v(s)$ is the virtual impedance, and

$$Z_o(s) = \frac{\frac{1}{sC_f}}{1 + \frac{1}{sC_f} G_{uc}(s) G_{cli}(s)} \tag{10}$$

$$Z_v(s) = G_{clu}(s)(R_v + sL_v). \tag{11}$$

In addition, (12) can be obtained from Fig. 3(a) as

$$\begin{bmatrix} u_{gd} \\ u_{gq} \end{bmatrix} = \begin{bmatrix} u_{cd} \\ u_{cq} \end{bmatrix} - \begin{bmatrix} Z_g(s) & -\omega L_g \\ \omega L_g & Z_g(s) \end{bmatrix} \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}. \tag{12}$$

Substituting (12) into (9), it can be manipulated that

$$\begin{bmatrix} u_{gd} \\ u_{gq} \end{bmatrix} = G_{clu}(s) \begin{bmatrix} u_{rd} \\ u_{rq} \end{bmatrix} - \begin{bmatrix} Z_o(s) + Z_v(s) + Z_g(s) & -\omega L_v G_{clu}(s) - \omega L_g \\ \omega L_v G_{clu}(s) + \omega L_g & Z_o(s) + Z_v(s) + Z_g(s) \end{bmatrix} \times \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} \tag{13}$$

where $Z_g(s) = R_g + sL_g$ and u_{gdq} is the grid voltage in SRF when in GC mode or the load voltage in SRF when in IS mode.

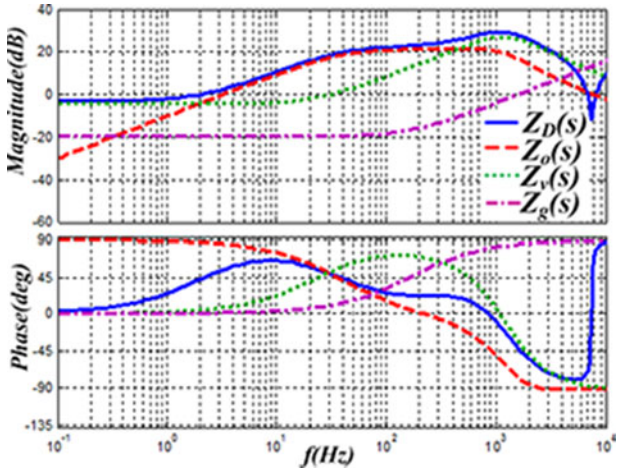

Fig. 4. Bode diagram of the total output impedance.

In addition, the total output impedance including inverter output impedance, virtual impedance, and feeder impedance is defined as

$$Z_D(s) = Z_o(s) + Z_v(s) + Z_g(s). \tag{14}$$

Therefore, it can be illustrated with (13) that:

1) When in IS mode, the impacts of loads on the output voltage can be seen as the perturbation of load current. The disturbance is introduced through the total output impedance. Therefore, the voltage quality in IS mode can be improved with proper design of the total output impedance [15].
2) The load voltage swell or sag happens during load switching, which may lead to saturation of the isolation transformer and damage the critical loads. Since u_{rdq} is determined by the droop loop which is too slow to track the load transient and the bandwidth of the inner voltage loop is limited by the bandwidth of current loop and switching frequency, the total output impedance is the key factor to suppress the voltage swell and sag.
3) Since inverter output impedance is the main part of the total output impedance as verified later in Section III, load adaptability in IS mode is significantly influenced by inverter output impedance.

In addition, as verified later in Section III, stability and dynamic performance are also influenced by the inverter output impedance, and conventional control strategy presents poor reliability which confines the adjustable range in energy management [27].

III. Analysis of the Inverter Output Impedance Impacts

As it can be seen in (14), the total output impedance consists of the virtual impedance $Z_v(s)$, feeder impedance $Z_g(s)$, and the inverter output impedance $Z_o(s)$. In order to explicitly illustrate the relationship among the above impedances, bode diagram of the total output impedance is shown in Fig. 4 with the parameters listed in Tables I and II.

As shown in Fig. 4, the inverter output impedance $Z_o(s)$ approaches to zero in low frequency while close to $Z_D(s)$ in the frequency range from 3 to 1 kHz. Therefore, the dynamic performance is significantly influenced by $Z_o(s)$, while the steady-state performance at fundamental frequency hardly depends on $Z_o(s)$. As analyzed in [15] in IS mode, voltage harmonics are mainly influenced by the impedance at 300 and 600 Hz, and voltage unbalance is primarily determined by the impedance at 100 Hz. In addition, the disturbance of load switching is also introduced by $Z_D(s)$. Since $Z_o(s)$ is the main part of $Z_D(s)$ from 3 Hz to 1 kHz, load adaptability in IS mode is significantly influenced by the inverter output impedance $Z_o(s)$.

TABLE I
Power Stage Parameters

Parameter	Symbol	Value
DC Voltage	v_{dc}	650 V
Grid Frequency	ω_0	$2\pi \cdot 50$ rad/s
Grid Voltage (Line–Line RMS)	E_0	380 V
Initial phase angle	δ_0	0.087 rad/s
Inverter-side Filter Inductor	L_c, R_c	1.6 mH, 0.06 Ω
Filter Capacitor	C_f	20 μF
Grid-side Inductor	L_g, R_g	0.1 mH, 0.104 Ω
Switching Frequency	f_s	10 kHz

In order to investigate the impacts of $Z_o(s)$ on stability and dynamic performance, small-signal analysis in both GC mode and IS mode is further researched.

A. Stability and Dynamic Performance in GC Mode

From Fig. 2, we obtain

$$\delta = \frac{1}{s}[\omega_0 + k_p(P_0 - P)] \tag{15}$$

$$u_{rd} = E = E_0 + k_q(Q_0 - Q) \tag{16}$$

$$u_{rq} = 0 \tag{17}$$

where δ is the phase angle between reference voltage u_{rdq} and grid voltage u_{gdq}.

According to the small-signal model in Appendix A, the active power–frequency droop and reactive power–voltage magnitude droop closed-loop transfer functions can be manipulated as

$$G_{pc}(s) = \left.\frac{\Delta P}{\Delta P_0}\right|_{\Delta Q_0 = 0} = \frac{k_p B_2 E_0 + k_p k_q E_0 (B_2^2 + B_1^2)}{(1 + k_q B_2)s + k_p B_2 E_0 + k_p k_q E_0 (B_2^2 + B_1^2)} \tag{18}$$

$$G_{qc}(s) = \left.\frac{\Delta Q}{\Delta Q_0}\right|_{\Delta P_0 = 0} = \frac{k_q B_2 s + k_p k_q E_0 (B_2^2 + B_1^2)}{(1 + k_q B_2)s + k_p B_2 E_0 + k_p k_q E_0 (B_2^2 + B_1^2)}. \tag{19}$$

As shown in Fig. 5, a resonance peak appears in the closed-loop transfer functions of conventional control strategy, which possibly causes instability. To mitigate the resonance peak,

TABLE II
CONTROL PARAMETERS

Parameter	Symbol	Value
Droop Coefficients	k_p , k_q	2.09×10^{-4} rad/(W·s), 0.0076 V/Var
Voltage Magnitude Control Integral Gain	k_v	4
Cutoff Frequency of Power Calculation LPF	ω_f	$2\pi \cdot 10$ rad/s
Cutoff Frequency of LPF_1	ω_c	$2\pi \cdot 1000$ rad/s
Feedforward Gain	k_c	1
Voltage Loop PI	k_{pv} , k_{iv}	0.09, 20
Current Loop PI	k_{pi} , k_{ii}	14, 400
Virtual Impedance	R_v , L_v	0.6 Ω, 4 mH

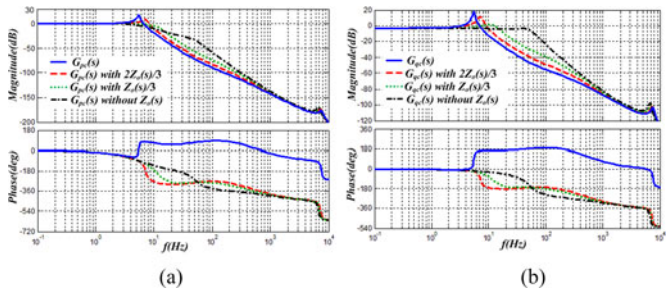

Fig. 5. Bode diagrams of closed-loop transfer function of the droop loops for conventional control strategy in GC mode: (a) frequency droop loop, (b) voltage magnitude droop loop.

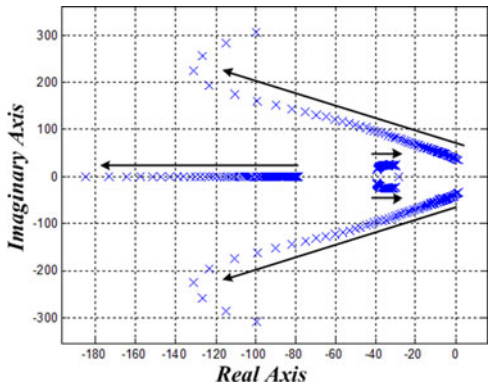

Fig. 6. Root locus diagram of dominant eigenvalues when inverter output impedance decreases from $Z_o(s)$ to 0 in GC mode.

compensation networks can be added to the droop loop. However, the dynamic performance is thus degraded. In addition, $G_{qc}(s)$ is a little lower than 1 in low frequency, which means inaccuracy during the control of the reactive power flow.

As shown, the resonance peak appears between 1 and 10 Hz, and $Z_o(s)$ is the main part of $Z_D(s)$ in this frequency range. Therefore, it can be deduced that stability and dynamic performance are mainly influenced by the inverter output impedance. In order to consider the impacts of inverter output impedance in detail, the closed-loop characteristics under different inverter output impedance are also given in Fig. 5. Note that the different inverter output impedances are obtained by changing the item $Z_o(s)$ in (13). In practice, the inverter output impedance can be modified through changing the feedforward gain when introducing output current feedforward [26], [28]. As shown, the resonance peak is mitigated when inverter output impedance decreases. In addition, the root locus of conventional control strategy with different inverter output impedance in GC mode is shown in Fig. 6. As shown, dominant low frequency eigenvalues move from right to left which represents enhanced stability and dynamic performance. However, too small inverter output impedance may also degrade the dynamic performance as seen that the conjugate poles move from left to right when the inverter output impedance continues to decrease.

Consequently, stability and dynamic performance in GC mode is improved with reduced inverter output impedance, and low frequency part of the inverter output impedance is the dominating factor that influences stability and dynamic performance.

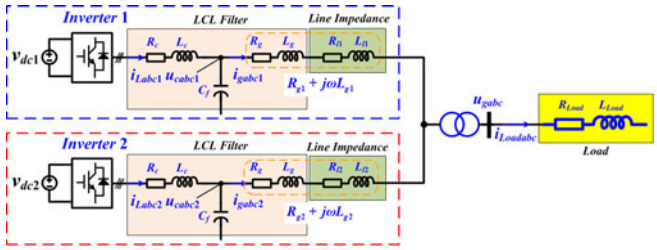

Fig. 7. Simplified circuit for parallel inverters in IS mode.

B. Stability and Dynamic Performance in IS Mode

The dynamic model of the conventional droop-controlled system in IS mode has been extensively discussed in [28]–[30]. In this paper, the small-signal dynamic model is derived for the conventional control strategy according to [28]. According to the small-signal model in IS mode provided in Appendix B, the complete system model can be obtained as

$$\begin{bmatrix} \Delta \dot{\boldsymbol{X}}_{inv1} \\ \Delta \dot{\boldsymbol{X}}_{inv2} \\ \Delta \dot{i}_{\mathrm{Load}\ DQ} \end{bmatrix} = \boldsymbol{A}_{\mathrm{sys}} \begin{bmatrix} \Delta \boldsymbol{X}_{inv1} \\ \Delta \boldsymbol{X}_{inv2} \\ \Delta i_{\mathrm{Load}\ DQ} \end{bmatrix}. \tag{20}$$

According to the model, the root locus of dominant eigenvalues with different inverter output impedance in IS mode can be obtained as shown in Fig. 8. Similar to the root locus in GC mode as shown in Fig. 6, dominant low frequency eigenvalues move from right to left, and stability and dynamic performance in

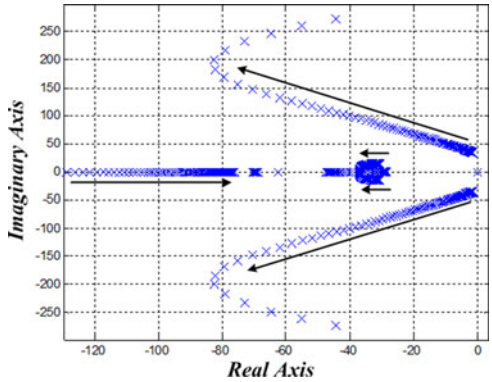

Fig. 8. Root locus diagram of dominant eigenvalues when inverter output impedance decreases from $Z_o(s)$ to 0 in IS mode.

IS mode are improved with reduced inverter output impedance. However, too low inverter output impedance may also degrade the dynamic performance.

IV. Proposed ICFC Scheme

According to the analysis in Section III, inverter output impedance has a significant impact on the performance of inverter. Therefore, measures need to be taken to mitigate the effects. As presented in [26], inverter output impedance is eliminated when load current feedforward scheme is introduced in IS mode. Similarly, grid current feedforward control scheme can be applied in this paper. Nevertheless, extra sensors for grid current i_{gabc} are necessary. Meanwhile, grid current is usually not sensed in small power inverter applications. In addition, the control accuracy of reactive power and voltage magnitude in GC mode cannot be guaranteed with conventional control strategy.

In order to mitigate the impacts of inverter output impedance and improve the control accuracy of reactive power and voltage magnitude in GC mode, the ICFC scheme without additional control complexity and extra sensors as presented in Fig. 9 is proposed in this section. The difference between conventional control strategy in Fig. 2 and ICFC scheme in Fig. 9 is the modified droop loops and the enhanced inner loops with inverter current feedforward.

As shown in Fig. 9, a voltage magnitude control is added to the droop loops to enhance the control accuracy of the voltage magnitude and reactive power flow in GC mode. Thus, (2) is modified as

$$E = E_0 + \frac{k_v}{s}\left[E_0 + k_q(Q_0 - Q) - \sqrt{u_{cd}^2 + u_{cq}^2}\right] \tag{21}$$

where k_v is integral gain of the voltage magnitude control. In GC mode, the voltage magnitude is precisely controlled to track with the grid voltage with voltage magnitude control loop in the proposed ICFC scheme. Therefore, the accuracy of tracking the instruction of reactive power Q_0 can be improved under a less fluctuating grid according to (21). Nevertheless, steady-state errors exist in voltage magnitude control with conventional control strategy, and accurate tracking of Q_0 cannot be guaranteed. Additionally, in IS mode, the sharing of reactive power is mainly influenced by the line impedance. Therefore, the impacts of voltage magnitude control loop on the control accuracy of reactive power sharing are not obvious in IS mode.

In addition, the inverter current i_{Ldq} with a first-order low-pass filter LPF_1 is added in inner loops as the feedforward element, and k_c is the feedforward gain. Meanwhile, virtual impedance is also introduced through i_{Ldq} with a first-order low-pass filter LPF_1.

The detailed performance analysis of the proposed ICFC scheme is introduced as follows.

A. Inverter Output Impedance

According to Fig. 9, voltage drop of the virtual impedance is changed as

$$\begin{bmatrix} u_{vd} \\ u_{vq} \end{bmatrix} = \begin{bmatrix} R_v + sL_v & -\omega L_v \\ \omega L_v & R_v + sL_v \end{bmatrix} \frac{\omega_c}{s+\omega_c} \begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix}. \tag{22}$$

The closed-loop characteristics of inner loops can be expressed as

$$\begin{bmatrix} u_{cd} \\ u_{cq} \end{bmatrix} = G_{clu}(s) \begin{bmatrix} u_{rd} \\ u_{rq} \end{bmatrix} + \begin{bmatrix} Z_{DLdd}(s) & Z_{DLdq}(s) \\ -Z_{DLdq}(s) & Z_{DLdd}(s) \end{bmatrix} \times \begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} - Z_o(s) \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}. \tag{23}$$

The detailed expressions of $Z_{DLdd}(s)$ and $Z_{DLdq}(s)$ are shown as follows:

$$Z_{DLdd}(s) = \frac{\frac{1}{sC_f}\frac{\omega_c}{s+\omega_c}k_c G_{cli}(s)}{1 + G_{uc}(s)G_{cli}(s)\frac{1}{sC_f}} - G_{clu}(s)(R_v + sL_v) \times \frac{\omega_c}{s+\omega_c} \tag{24}$$

$$Z_{DLdq}(s) = G_{clu}(s)(\omega L_v)\frac{\omega_c}{s+\omega_c}. \tag{25}$$

According to the inverter model in Fig. 3(a), it can be derived that

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{bmatrix} sC_f & -\omega C_f \\ \omega C_f & sC_f \end{bmatrix} \begin{bmatrix} u_{cd} \\ u_{cq} \end{bmatrix} + \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix}. \tag{26}$$

Substituting (12) and (26) into (23), it can be derived as

$$\begin{bmatrix} u_{gd} \\ u_{gq} \end{bmatrix} = G_{clu}(s)Y(s) \begin{bmatrix} u_{rd} \\ u_{rq} \end{bmatrix} - \begin{bmatrix} Z_{Di}(s) & -Z_{Ci}(s) \\ Z_{Ci}(s) & Z_{Di}(s) \end{bmatrix} \times \begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} \tag{27}$$

$$Y(s) = \frac{1}{[1-\omega C_f Z_{DLdq}(s)]^2 + [\omega C_f Z_{DLdd}(s)]^2} \begin{bmatrix} 1-\omega C_f Z_{DLdq}(s) & -\omega C_f Z_{DLdd}(s) \\ \omega C_f Z_{DLdd}(s) & 1-\omega C_f Z_{DLdq}(s) \end{bmatrix} \tag{28}$$

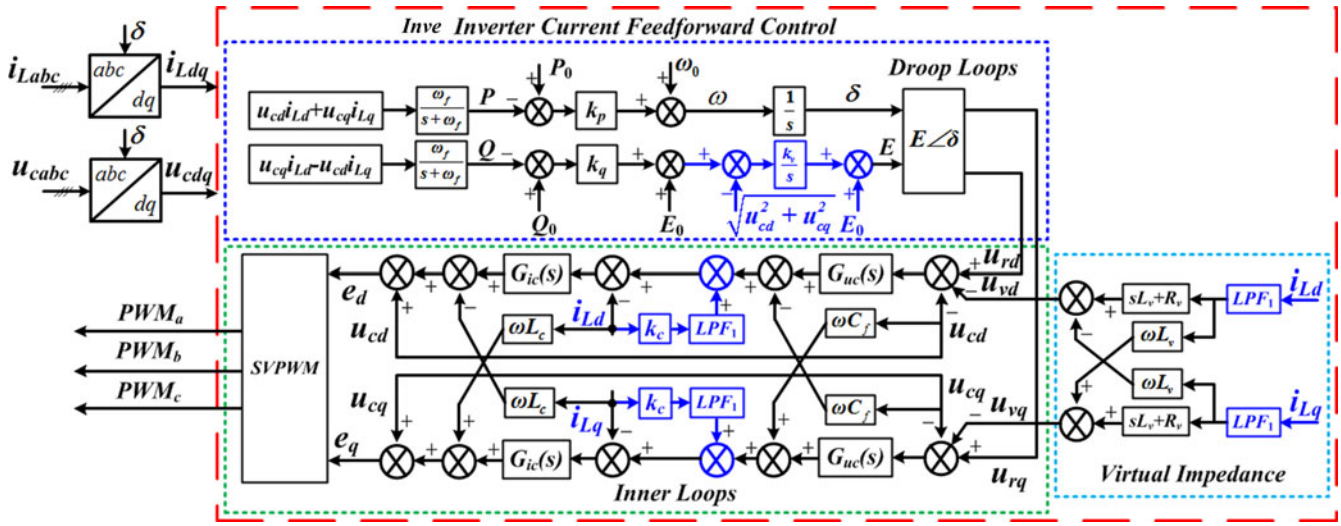

Fig. 9. Block diagram of the proposed ICFC scheme.

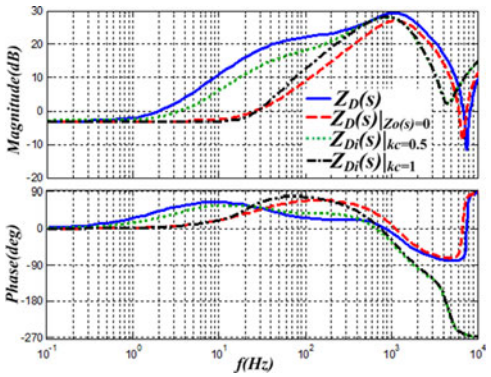

Fig. 10. Bode diagram of the total output impedance.

where $Y(s)$, $Z_{Di}(s)$, and $Z_{Ci}(s)$ are as equation (28) shown at the bottom of the previous page, and, (29) and (30) as shown at the bottom of the this page.

As shown in Fig. 10, below 30 Hz, the total output impedance $Z_{Di}(s)$ when $k_c = 1$ basically coincides with $Z_D(s)$ when $Z_o(s) = 0$. As shown in Fig. 5, the resonance peak in the closed-loop transfer functions of droop loops appears between 1 and 10 Hz. Moreover, stability and dynamic performance are influenced by the resonance peak. Therefore, stability and dynamic performance are mainly determined by the impedance between 1 and 10 Hz. Since inverter output impedance is the main part of total output impedance from 3 to 100 Hz as displayed in Fig. 4, the impacts of inverter output impedance on stability and dynamic performance are mitigated with the proposed ICFC scheme.

Meanwhile, compared with the conventional strategy, the value of $Z_{Di}(s)$ when $k_c = 1$ at 100 Hz is greatly reduced, which means that voltage unbalance in IS mode can be effectively compensated with the ICFC scheme. Moreover, $Z_{Di}(s)$ at 300 Hz (which represents fifth and seventh harmonic in SRF) is also diminished, while $Z_{Di}(s)$ is close to $Z_D(s)$ in high frequency. Therefore, harmonic impedance is reduced to enhance harmonic compensation with proposed ICFC scheme. Since the total output impedance is diminished, voltage swell or sag during load switching in IS mode is also mitigated. Nevertheless, the grid current in GC mode has more harmonic distortions with a slightly distorted grid voltage. Therefore, the impacts of inverter output impedance on load adaptability in IS mode are suppressed with the ICFC scheme.

In addition, taking into account the impacts of inverter output impedance, k_c is set to 1in this paper.

B. Stability and Dynamic Performance

According to the modeling method introduced in Section III, the small-signal model of the proposed ICFC scheme can be obtained. The comparison of closed-loop characteristics in GC mode between conventional control strategy and the proposed ICFC scheme is shown in Fig. 11. As shown, the resonance peak in $G_{pc}(s)$ and $G_{qc}(s)$ is efficiently mitigated in $G_{pi}(s)$ and

$$Z_{Di}(s) = \frac{[Z_o(s) - Z_{DLdd}(s)][1 - \omega C_f Z_{DLdq}(s)] - \omega C_f Z_{DLdd}(s) Z_{DLdq}(s)}{[1 - \omega C_f Z_{DLdq}(s)]^2 + [\omega C_f Z_{DLdd}(s)]^2} + Z_g(s) \tag{29}$$

$$Z_{Ci}(s) = \frac{\omega C_f Z_{DLdd}(s)[Z_o(s) - Z_{DLdd}(s)] + Z_{DLdq}(s)[1 - \omega C_f Z_{DLdq}(s)]}{[1 - \omega C_f Z_{DLdq}(s)]^2 + [\omega C_f Z_{DLdd}(s)]^2} + \omega L_g \tag{30}$$

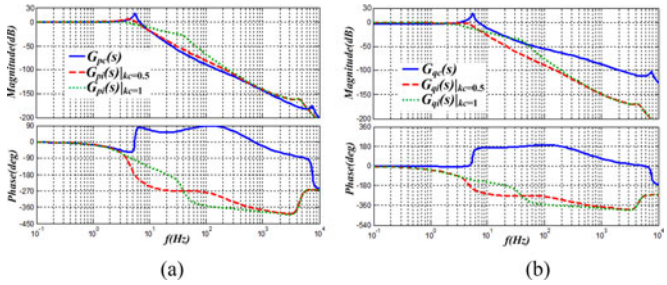

Fig. 11. Comparison of closed-loop transfer functions of the droop loops between conventional control scheme and proposed ICFC scheme in GC mode: (a) frequency droop loop, (b) voltage magnitude droop loop. ($G_{pi}(s)$ and $G_{qi}(s)$ are the closed-loop transfer functions in GC mode for ICFC scheme.).

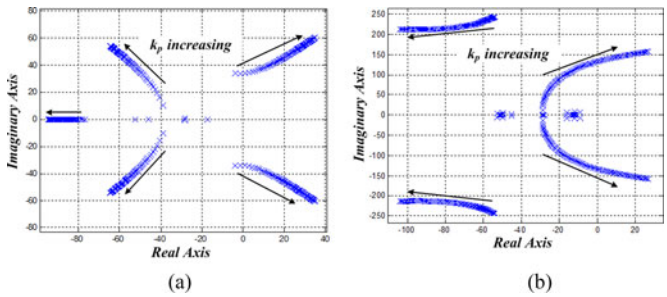

Fig. 12. Root locus diagrams of the low-frequency dominant eigenvalues for $1.045 \times 10^{-4} \leq k_p \leq 4.18 \times 10^{-3}$, while the other control parameters keep the same as Table II in GC mode: (a) conventional control strategy, (b) proposed ICFC scheme.

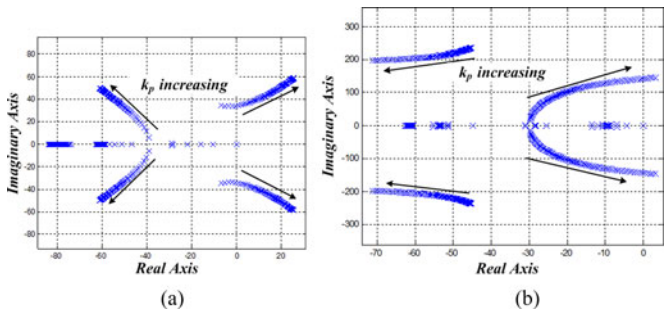

Fig. 13. Root locus diagrams of the low-frequency dominant eigenvalues for $1.045 \times 10^{-4} \leq k_p \leq 4.18 \times 10^{-3}$, while the other control parameters keep the same as Table II in IS mode: (a) conventional control strategy, (b) proposed ICFC scheme.

$G_{qi}(s)$ when $k_c = 1$, respectively. Hence, stability and dynamic performance in GC mode is enhanced with the proposed ICFC scheme. In addition, the control accuracy of reactive power flow is also improved since the low frequency gain of $G_{qi}(s)$ is 1. Nevertheless, bandwidth of $G_{qi}(s)$ is reduced when increasing feedforward gain k_c from 0.5 to 1. It means that dynamic performance of reactive power flow is reduced when increasing k_c.

In order to better understand the stability and dynamic performance with the proposed ICFC scheme in different modes, the trajectory of the low-frequency dominant eigenvalues for variation of k_p is shown in Figs. 12 and 13. It can be obtained that:

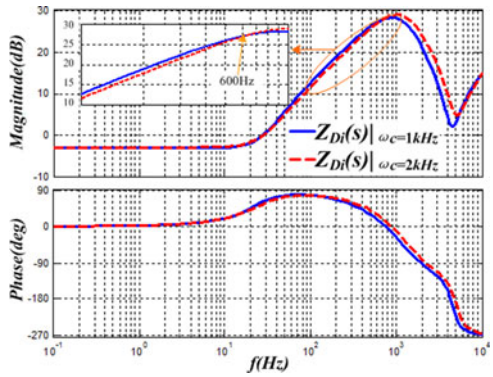

Fig. 14. Bode diagram of $Z_{Di}(s)$ with different cutoff frequencies of LPF_1.

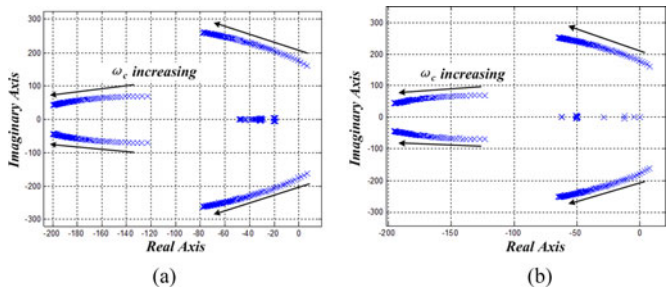

Fig. 15. Trajectory of the low-frequency dominant eigenvalues for $2\pi \cdot 200\ \mathrm{rad/s} \leq \omega_c \leq 2\pi \cdot 2000\ \mathrm{rad/s}$ with the proposed ICFC scheme.

1) Since the dominant eigenvalues are very close to the imaginary axis, stability margin of the conventional control strategy is very low. Moreover, the system is even unstable when in a low droop gain k_p as shown in Figs. 12(a) and 13(a).
2) Stability and dynamic performance are obviously enhanced with the proposed ICFC scheme in both modes. Even with a high droop gain k_p, the system still keeps stable as shown in Figs. 12(b) and 13(b).
3) Since the coefficient k_p when dominant poles move to the right plane in IS mode is much larger than in GC mode, stability margin in IS mode is much better than in GC mode with the ICFC scheme.

C. Impacts of LPF_1

Referring to the derivation in Section IV-A, the performance of the proposed ICFC scheme is also influenced by the low-pass filter LPF_1. As shown in Fig. 14, when ω_c increases, the magnitude of $Z_{Di}(s)$ below 600 Hz, which mainly determines the capability of compensating voltage unbalance and suppressing harmonics, decreases. Therefore, in the context of eliminating the impacts of ripple in inverter current, a high cutoff frequency ω_c is helpful to improve the voltage quality in IS mode. However, THD of grid current in GC mode is slightly increased.

In addition, stability of the proposed scheme is also influenced by the low-pass filter LPF_1 of the inverter current. As shown in Fig. 15, stability and dynamic performance are improved as ω_c increases in both modes because the dominant poles move

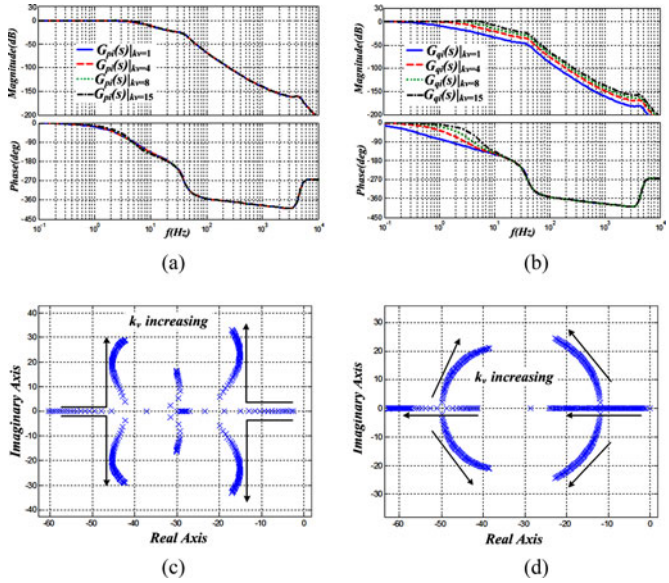

Fig. 16. Closed-loop characteristics of droop loops for variation of k_v in GC mode: (a) $G_{pi}(s)$, (b) $G_{qi}(s)$, and dominant eigenvalues for $1 \leq k_v \leq 20$: (c) in GC mode, (d) in IS mode.

from right to left. In this paper, the cutoff frequency ω_c is set to 1 kHz.

D. Effects of the Voltage Magnitude Control Loop

As shown in Fig. 11(b), control accuracy of reactive power flow in GC mode is enhanced with voltage magnitude control loop in the proposed ICFC scheme. However, the dynamic response of the reactive power flow is also influenced. The closed-loop characteristics of droop loops for variation of k_v in GC mode are given in Fig. 16(a)–(b). When k_v increases, the crossover frequency of $G_{qi}(s)$ is enhanced while $G_{pi}(s)$ hardly alters. Consequently, the dynamic response of reactive power flow is improved when k_v increases. Moreover, performance of active power flow is independent of k_v. In addition, because the dominant poles keep in the left plane, stability is independent of k_v in different operation modes as shown in Fig. 16(c)–(d). However, dynamic response is enhanced as k_v increases since the dominant poles move from right to left. In this paper, k_v is set as 4.

E. Influence of LCL Filter Parameter Variations

In practice, due to the tolerance and aging of the filter components and the parasitic parameters of the system, the *LCL* filter parameter mismatch might happen. To investigate the impacts of *LCL* filter parameter variations on the proposed algorithm, bode diagram of $Z_{Di}(s)$ with different *LCL* filter parameters is presented in Fig. 17. As shown, the impedance below 600 Hz is immune to the *LCL* filter parameter variations, and the effect on the impedance at high frequency is also limited. Therefore, under the *LCL* filter parameter variations, the proposed ICFC scheme is still feasible and effective.

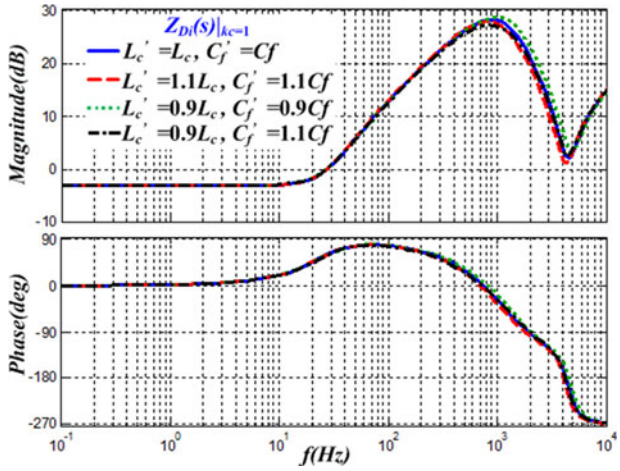

Fig. 17. Bode diagram of $Z_{Di}(s)$ with different *LCL* filter parameters.

V. Simulation and Experimental Validation

In order to verify the correctness of the analysis above, simulation and experiment results with both conventional strategy and proposed ICFC scheme are obtained based on a 15-kVA VSI prototype. The algorithms are implemented with a TI DSP TMS320F28335 in the experiments. Therefore, the computation delay is inevitably introduced with digital control, which may degrade the stability margin. In this paper, control frequency is increased to twice the switching frequency when implemented in experiments, and the delay can be largely reduced (note that the computation is implemented twice per switching period with sampling frequency ten times higher than the switching frequency). In addition, the effects of the delay are mainly at high frequency [31]. Since inner loops are designed with high phase margin, high frequency stability is guaranteed. Consequently, the effects of time discretization of digital control are well restricted. The power stage parameters and control parameters of the prototype are listed in Tables I and II, respectively.

A. Stability and Dynamic Performance

In order to validate the impacts of inverter output impedance on stability and dynamic performance, simulation and experiments in both GC mode and IS mode are implemented.

1) Simulation Results: As shown in Fig. 18(a)–(b), when a step of the power instructions P_0 or Q_0 happens at $t = 0.1$ s in GC mode, the proposed ICFC scheme presents better dynamic performance than conventional control strategy. Meanwhile, control accuracy of reactive power is also enhanced with the ICFC scheme, while tracking error exists on the reactive power control with conventional control strategy as displayed in Fig. 18(b). In addition, the system turns to be unstable with conventional strategy when k_p increases to 2.09×10^{-4} in Fig. 18(c). However, the system keeps stable with the proposed ICFC scheme even though k_p increases to 2.09×10^{-3} as presented in Fig. 18(d). Therefore, stability, dynamic performance, and control accuracy of reactive power in GC mode are improved with the proposed ICFC scheme.

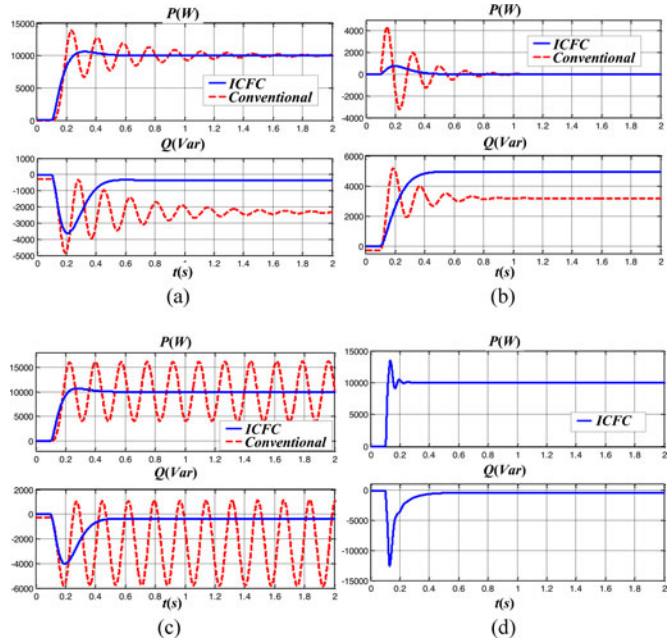

Fig. 18. Simulation waveforms of active power and reactive power in GC mode, respectively: (a) P_0 increases from 0 to 10 kW at $t = 0.1$ s when $k_p = 1.672 \times 10^{-4}$, (b) Q_0 increases from 0 to 5 kVar at $t = 0.1$ s when $k_p = 1.672 \times 10^{-4}$, (c) P_0 increases from 0 to 10 kW at $t = 0.1$ s when $k_p = 2.09 \times 10^{-4}$, (d) P_0 increases from 0 to 10 kW at $t = 0.1$ s when $k_p = 2.09 \times 10^{-3}$.

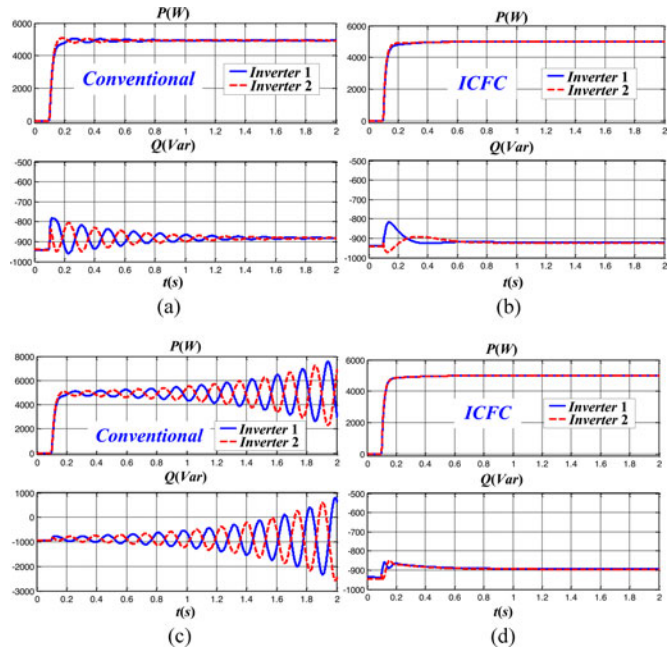

Fig. 19. Simulation waveforms of active power and reactive power in IS mode, respectively, when 10-kW load is put into operation at $t = 0.1$: (a) and (b) $k_p = 2.09 \times 10^{-4}$, (c) $k_p = 2.926 \times 10^{-4}$, and (d) $k_p = 2.09 \times 10^{-3}$.

In IS mode, the prototype is shown in Fig. 7. The parameters are the same as Tables I and II, except that $R_{g1} = 0.164\ \Omega$ and $L_{g2} = 0.45$ mH. As shown in Fig. 19(b), when 10-kW load is switched ON, stability and dynamic performance in IS mode are guaranteed with the proposed ICFC scheme. Moreover, when k_p increases to 2.09×10^{-3}, stability is still sustained, and better dynamic response is achieved as displayed in Fig. 19(d). Nevertheless, dynamic response with conventional control strategy presents damped oscillation when $k_p = 2.09 \times 10^{-4}$ as presented in Fig. 19(a), and the system becomes unstable when k_p increases to 2.926×10^{-4} as displayed in Fig. 19(c).

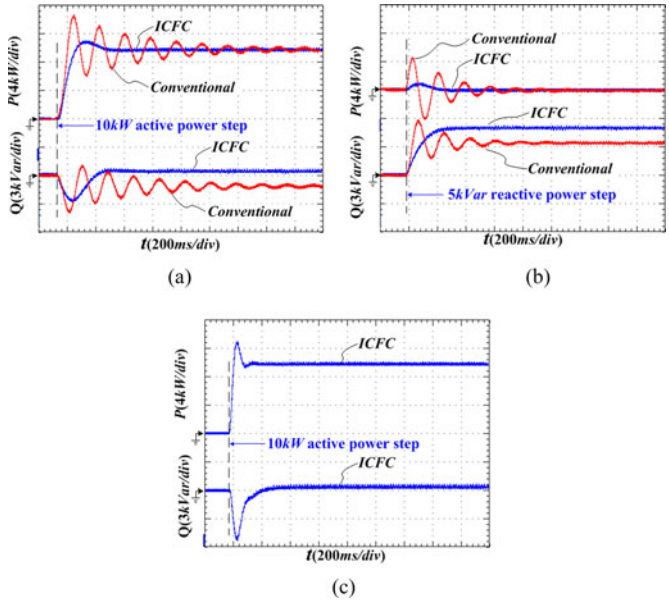

Fig. 20. Experimental waveforms of active power P and reactive power Q in GC mode, respectively: (a) P_0 increases from 0 to 10 kW when $k_p = 1.672 \times 10^{-4}$, (b) Q_0 increases from 0 to 5 kVar when $k_p = 1.672 \times 10^{-4}$, (c) P_0 increases from 0 to 10 W when $k_p = 8.36 \times 10^{-4}$.

2) Experiment Validation: As shown in Fig. 20, the stability and dynamic performance in GC mode are enhanced with the proposed scheme which coordinates with the simulation. When $k_p = 8.36 \times 10^{-4}$, the system is still stable, and a fast dynamic response is achieved as presented in Fig. 20(c). Unfortunately, with the conventional control strategy, power oscillation happens, and stability is degraded even in a lower droop coefficient k_p as shown in Fig. 20(a). In addition, control accuracy of reactive power flow is also enhanced with the proposed ICFC scheme as displayed in Fig. 20(b).

In IS mode, damped power oscillation in a small k_p with conventional strategy is presented in Fig. 21(a) while power oscillation happens when k_p increases to 2.508×10^{-4}, and the system stays critical stable state as shown in Fig. 21(d). Therefore, stability is greatly degraded when k_p increases, and stability margin is very limited with conventional control strategy. However, compared with conventional strategy, dynamic performance is enhanced with proposed ICFC scheme as shown in Fig. 21(b). Moreover, stability and dynamic performance are still guaranteed even when k_p increases to 8.36×10^{-4} as displayed in Fig. 21(c).

B. Load Adaptability in IS Mode (Experiment Validation)

As analyzed previously, voltage quality under unbalanced loads and nonlinear loads and dynamic response during load switching in IS mode are significantly influenced by inverter output impedance. In order to verify the analysis about load adaptability in IS mode, experiments are carried out in IS mode.

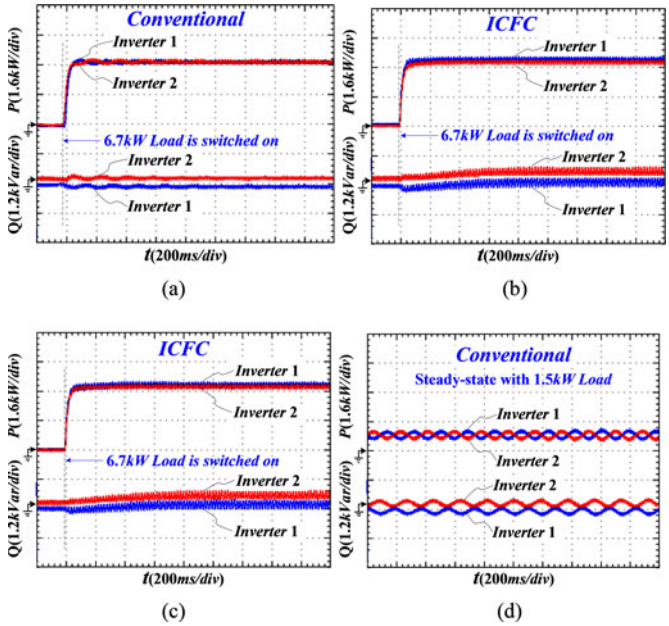

Fig. 21. Experiment waveforms of active and reactive power in IS mode, respectively, when 6.7 kW load is switched ON: (a) and (b) $k_p = 2.09 \times 10^{-4}$ and (c) $k_p = 8.36 \times 10^{-4}$, (d) steady-state waveforms with 1.5-kW load when $k_p = 2.508 \times 10^{-4}$.

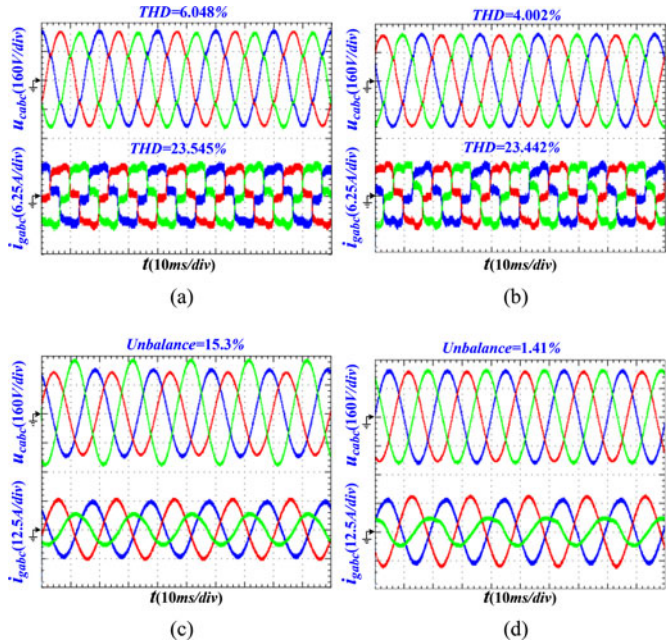

Fig. 22. Experimental results under nonlinear load (a three-phase rectifier load 77 Ω): (a) with conventional strategy, (b) with the proposed ICFC scheme, and unbalanced load (16-Ω load in phase A and 16-Ω load in phase B): (c) with conventional strategy, (d) with proposed ICFC scheme.

The rated phase voltage in IS mode is set to 180 V instead of 220 V to avoid the saturation of isolation transformer during load switching with the conventional control strategy. The other parameters are the same as Tables I and II. The experiment results under unbalanced and nonlinear loads and during load switching are presented in Figs. 22 and 23.

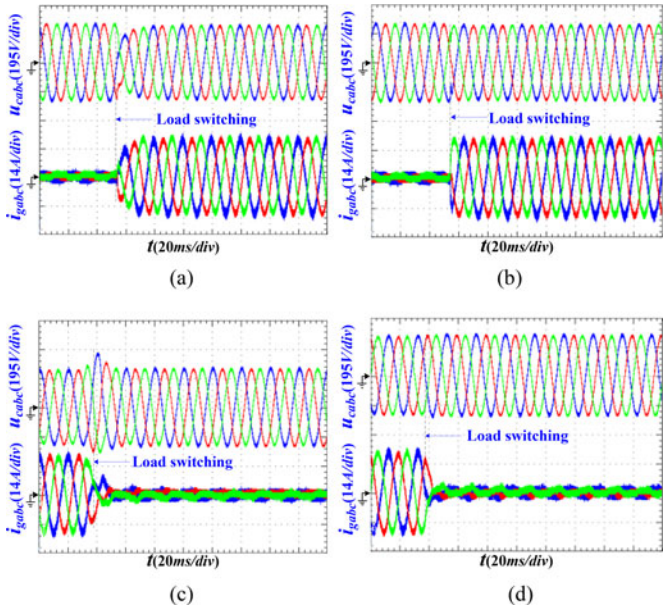

Fig. 23. Experimental results during switching from no load to 6.7 kW: (a) with conventional strategy, (b) with the proposed ICFC scheme and from 6.7 kW to no load: (c) with conventional strategy, (d) with the proposed ICFC scheme.

As shown in Fig. 22(a), under nonlinear load, the voltage THD is up to 6.048% with the conventional control strategy. Nevertheless, voltage THD is reduced to 4.002% with the proposed scheme, which can be seen in Fig. 22(b). Hence, voltage harmonics are partly compensated with the proposed ICFC scheme.

Voltage unbalance which can be calculated according to symmetrical components method [32], is effectively compensated with the proposed ICFC scheme as displayed in Fig. 22(c)–(d). As shown, voltage unbalance is reduced from 15.3% to 1.41% with the proposed ICFC scheme. Note that the current in phase C is not zero, because neutral line in the secondary side of the transformer is connected with the neutral line in load.

As shown in Fig. 23(a)–(b), during load switching from no load to 6.7 kW, the proposed scheme performs fast dynamic response, and the voltage sag recovers instantly. Nevertheless, conventional strategy presents slow dynamic response when the load is switched ON.

The results during load switching from 6.7 kW to no load are displayed in Fig. 23(c)–(d). As seen, the voltage swells to 380 V during load switching in the conventional control strategy, which possibly induces the saturation of the isolation transformer. Nevertheless, with the proposed ICFC scheme, the voltage spike is effectively mitigated.

Based on the experiment results, it can be concluded that load adaptability in IS mode is effectively enhanced with proposed ICFC scheme. Consequently, the impacts of inverter output impedance on load adaptability in IS mode are mitigated with proposed ICFC scheme since the problems are essentially introduced through inverter output impedance.

VI. Conclusion

In this paper, the impacts of inverter output impedance on stability, dynamic performance, and load adaptability are investigated in detail. Moreover, small-signal models in both operation modes are analyzed. The inverter output impedance causes limited stability margin, poor dynamic performance, and deficient load adaptability in IS mode with conventional control strategy. Therefore, the ICFC scheme is proposed to mitigate the effects of the inverter output impedance. The ICFC scheme consists of an inverter current feedforward scheme to mitigate the impacts of inverter output impedance and a voltage magnitude control loop to enhance the control accuracy of reactive power flow in GC mode. The detailed performance analysis and comparison with conventional control strategy are also discussed.

The proposed ICFC scheme has been validated through simulation and experiments. The obtained results show that by utilizing the proposed ICFC scheme, stability and dynamic performance are well improved in both operation modes, control accuracy of reactive power flow in GC mode is raised, voltage unbalance and harmonics in IS mode are compensated, and transient performance during load switching in IS mode is also enhanced.

Appendix A
Small-Signal Model in GC Mode

In GC mode, since the grid-side impedance is very small, u_{cdq} can be approximated to u_{gdq}, and u_{gdq} satisfies

$$\begin{bmatrix} u_{gd} \\ u_{gq} \end{bmatrix} = E_0 \begin{bmatrix} \cos\delta \\ -\sin\delta \end{bmatrix}. \tag{A1}$$

To substitute i_{gdq} into (3) and (4), (13) is transformed to (A2) first

$$\begin{bmatrix} i_{gd} \\ i_{gq} \end{bmatrix} = G_{clu}(s) \begin{bmatrix} G_1 & G_2 \\ -G_2 & G_1 \end{bmatrix} \begin{bmatrix} u_{rd} \\ u_{rq} \end{bmatrix} - \begin{bmatrix} G_1 & G_2 \\ -G_2 & G_1 \end{bmatrix} \begin{bmatrix} u_{gd} \\ u_{gq} \end{bmatrix} \tag{A2}$$

where

$$G_1 = \frac{Z_D(s)}{[Z_D(s)]^2 + [\omega L_v G_{clu}(s) + \omega L_g]^2}$$
$$G_2 = \frac{\omega L_v G_{clu}(s) + \omega L_g}{[Z_D(s)]^2 + [\omega L_v G_{clu}(s) + \omega L_g]^2}. \tag{A3}$$

Instantaneous active power calculated with inverter current is basically equal to the active power calculated with grid current. However, reactive power calculated with inverter current is the sum of reactive power calculated with grid current and reactive power of filter capacitor. Therefore, by substituting (A1) and (A2) into (3) and (4), and facilitating the result with $u_{rd} = E$ and $u_{rq} = 0$, it can be obtained that

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \frac{\omega_f}{s+\omega_f} E_0 \left(G_{clu}(s) \begin{bmatrix} G_1 \cos\delta + G_2 \sin\delta \\ -G_1 \sin\delta + G_2 \cos\delta \end{bmatrix} E - E_0 \begin{bmatrix} G_1 \\ G_2 \end{bmatrix} + E_0 \begin{bmatrix} 0 \\ \omega C_f \end{bmatrix} \right). \tag{A4}$$

By linearizing (A4), (15), and (16), the following small-signal representations are achieved:

$$\begin{bmatrix} \Delta E \\ \Delta\delta \end{bmatrix} = \begin{bmatrix} k_q & 0 \\ 0 & k_p \frac{1}{s} \end{bmatrix} \left(\begin{bmatrix} \Delta Q_0 \\ \Delta P_0 \end{bmatrix} - \begin{bmatrix} \Delta Q \\ \Delta P \end{bmatrix} \right) \tag{A5}$$

$$\begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} = \begin{bmatrix} B_1 & B_2 E_0 \\ B_2 & -B_1 E_0 \end{bmatrix} \begin{bmatrix} \Delta E \\ \Delta\delta \end{bmatrix} \tag{A6}$$

where Δ denotes the perturbed value, δ_0 is the initial phase angle and B_1 and B_2 are

$$B_1 = \frac{\omega_f}{s+\omega_f} E_0 G_{clu}(s)(G_1 \cos\delta_0 + G_2 \sin\delta_0)$$
$$B_2 = \frac{\omega_f}{s+\omega_f} E_0 G_{clu}(s)(-G_1 \sin\delta_0 + G_2 \cos\delta_0). \tag{A7}$$

Substituting (A5) into (A6), (A8) can be obtained:

$$\begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} = \begin{bmatrix} k_p \frac{1}{s} B_2 E_0 & k_q B_1 \\ -k_p \frac{1}{s} B_1 E_0 & k_q B_2 \end{bmatrix} \left(\begin{bmatrix} \Delta P_0 \\ \Delta Q_0 \end{bmatrix} - \begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} \right). \tag{A8}$$

Finally, the active power–frequency droop and reactive power–voltage magnitude droop closed-loop transfer functions can be manipulated as

$$G_{pc}(s) = \left. \frac{\Delta P}{\Delta P_0} \right|_{\Delta Q_0 = 0} = \frac{k_p B_2 E_0 + k_p k_q E_0 (B_2^2 + B_1^2)}{(1 + k_q B_2)s + k_p B_2 E_0 + k_p k_q E_0 (B_2^2 + B_1^2)} \tag{A9}$$

$$G_{qc}(s) = \left. \frac{\Delta Q}{\Delta Q_0} \right|_{\Delta P_0 = 0} = \frac{k_q B_2 s + k_p k_q E_0 (B_2^2 + B_1^2)}{(1 + k_q B_2)s + k_p B_2 E_0 + k_p k_q E_0 (B_2^2 + B_1^2)}. \tag{A10}$$

Appendix B
Small-Signal Model in IS Mode

The state variables are defined as

$$\boldsymbol{X}_{\boldsymbol{inv}} = [\,\delta \quad P \quad Q \quad \phi_{dq} \quad \gamma_{dq} \quad i_{Ldq} \quad u_{cdq} \quad i_{gdq}\,]^T \tag{A11}$$

where i^*_{Ldq} is the reference of inner current loop and

$$\frac{d\phi_{dq}}{dt} = u_{rdq} - u_{vdq} - u_{cdq}$$
$$\frac{d\gamma_{dq}}{dt} = i^*_{Ldq} - i_{Ldq}. \tag{A12}$$

And according to [28], the state-space model for each inverter can be obtained

$$\Delta \dot{\boldsymbol{X}}_{\mathrm{inv}} = \boldsymbol{A}_{\mathrm{inv}} \Delta \boldsymbol{X}_{\mathrm{inv}} + \boldsymbol{B}_{\mathrm{inv}} \Delta u_{gDQ} + \boldsymbol{C}_{\mathrm{inv}} \Delta \omega_{\mathrm{PCC}} \tag{A13}$$

where Δu_{gDQ} denotes the deviation of the PCC voltage in the common reference frame, and $\Delta\omega_{\mathrm{PCC}}$ denotes the frequency deviation of the common reference frame.

The load model can be obtained as (A14) according to Fig. 7 (Note that the power stage parameters are basically the same as Table I except that $R_{g1} = 0.164\ \Omega$ and $L_{g1} = 0.45$ mH.)

$$\Delta \dot{i}_{\mathrm{Load}DQ} = \boldsymbol{H} I_{\mathrm{Load}} \Delta i_{\mathrm{Load}DQ} + \boldsymbol{F} I_{\mathrm{Load}} \Delta u_{gDQ} + \boldsymbol{C}_{\mathrm{Load}} \Delta \omega_{\mathrm{PCC}} \quad \text{(A14)}$$

where $\Delta i_{\mathrm{Load}DQ}$ denotes deviation of the load current in the common reference frame, I_{gDQ1} and I_{gDQ2} denote the steady-state value of grid-side current in inverter 1 and inverter 2, R_{Load} and L_{Load} are the load and

$$\boldsymbol{H} I_{\mathrm{Load}} = \begin{bmatrix} -R_{\mathrm{Load}}/L_{\mathrm{Load}} & \omega_0 \\ -\omega_0 & -R_{\mathrm{Load}}/L_{\mathrm{Load}} \end{bmatrix},$$

$$\boldsymbol{F} I_{\mathrm{Load}} = \frac{1}{L_{\mathrm{Load}}}, \boldsymbol{C}_{\mathrm{Load}} = \begin{bmatrix} I_{gQ1} + I_{gQ2} \\ -I_{gD1} - I_{gD2} \end{bmatrix}. \quad \text{(A15)}$$

Finally, following the modeling approach in [28], the complete system model can be obtained:

$$\begin{bmatrix} \Delta \dot{\boldsymbol{X}}_{\mathrm{inv1}} \\ \Delta \dot{\boldsymbol{X}}_{\mathrm{inv2}} \\ \Delta \dot{i}_{\mathrm{Load}DQ} \end{bmatrix} = \boldsymbol{A}_{\mathrm{sys}} \begin{bmatrix} \Delta \boldsymbol{X}_{\mathrm{inv1}} \\ \Delta \boldsymbol{X}_{\mathrm{inv2}} \\ \Delta i_{\mathrm{Load}DQ} \end{bmatrix}. \quad \text{(A16)}$$

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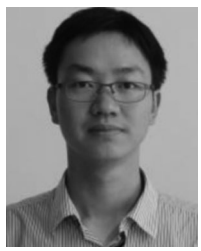

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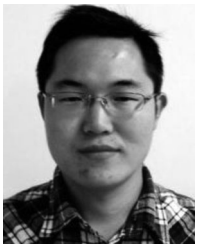

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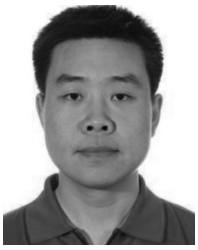

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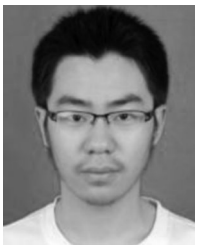

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