A High-Efficiency Fast-Transient-Response Buck Converter with Analog-Voltage-Dynamic-Estimation Techniques

Yuh-Shyan Hwang, *Senior Member, IEEE*, An Liu, Yuan-Bo Chang, and Jiann-Jong Chen, *Senior Member, IEEE*

***Abstract*—A fast-transient-response buck converter utilizing analog-voltage-dynamic-estimation (AVDE) techniques is proposed in this paper. The responses of the proposed buck converter are very fast when load changes between heavy load and light load. The switching frequency of the proposed buck converter is 1 MHz for nominal 3.3 V input and 1.0–2.5 V output range application. Experimental results prove that the proposed scheme improves the transient response to within 2 μs and that its maximum power efficiency can be up to 95%. The maximum load current is 300 mA. The proposed AVDE buck converter has been fabricated with a commercial 0.35 μm CMOS 2P4M process, the total chip area is about $1.5\ \mathrm{mm} \times 1.5\ \mathrm{mm}$, including PADs.**

***Index Terms*—Buck converter, derivative output ripple voltage (DORV), pulsewidth modulation (PWM), transient response.**

I. Introduction

With the growing demand for portable electronic devices and the development of semiconductor manufacturing technology, conversion efficiency, power consumption, and component size become the most important design criteria of power supply [1]–[4]. Switching converters are used because of their higher conversion efficiencies. Fast dynamic response is required when the system status changes between idle and active modes or vice versa, and the tasks to extend battery life and to improve power conversion efficiency constantly challenge the designers. Since the recurrent load switching demands fast load transient response with recovery times in the order of microseconds, the switching frequency of the converter should be in the megahertz range [5].

Although the transient response of a hysteresis voltage-mode control converter that manipulates output voltage directly may be acceptable, the variable switching frequency of the hysteresis-control scheme leads to a wide noise spectrum and serious electromagnetic interference (EMI) shielding problems [6]. The transient response of a current-mode control switching converter may also be acceptable because of the inductor current that is fed forward to the PWM generator; a complicated integrated current sensor is needed. To solve this problem, the V^2 control converter [7]–[9] is introduced, where the inductor current is sensed by the equivalent series resistor (R_{ESR}) of the output capacitor. The output voltage ripple of a V^2 control converter is produced by the inductor current through impedance, which consists of three components: R_{ESR}, equivalent series inductance (L_{ESL}), and the pure capacitor C_L impedance [10]. Because the phase delay increases as the C_L value decreases, and the output ripple is dominated by the $\Delta I_L \times R_{\mathrm{ESR}}$ term, a large $R_{\mathrm{ESR}} \times C_L$ value is generally required to detect the inductor current, whereas the values of L_{ESL} and $1/j\omega C_L$ should be small enough to be ignored [11], [12]. Like the peak current-mode control, V^2 control also suffers from subharmonic oscillations [5].

In order to alleviate the influence of a large R_{ESR} value, a derivative output ripple voltage (DORV) technique is proposed [12]–[14] to detect the inductor current through the differential output voltage. The waveforms of DORV and inductor current under steady state are basically the same except for their dc levels. However, there are nearly identical but opposite pulsations or changes in the waveforms of DORV and inductor current at the instant of load change. Such characteristic is exploited in this study. The current signals, which are of no use by themselves in transient states, are extracted and introduced to the control circuitry. Such control scheme does not affect the steady state, but it will reduce the transient time when a load change occurs. However, its inherent characteristics make it difficult for DORV control to detect dc components accurately and to deal with the influence of L_{ESL} effectively.

Therefore, a new analog-voltage-dynamic-estimation (AVDE) technique, which is based on DORV and usage of filters, is proposed in this study. The transient response of the proposed AVDE buck converter is faster than a conventional buck converter. The EMI problems are minor, and no slope compensation is required as in peak current-mode control. Furthermore, the circuit is very simple to implement. A buck converter applying the proposed AVDE technique can achieve peak efficiency of 95% and has transient response time of only 2 μs. There are two reasons why the efficiency of the proposed converter may be further improved. First, the voltage control circuit is intrinsically simple. Second, the losses of the power MOSs are reduced. The area ratio of the power PMOS and power NMOS ($\mathrm{Area}_{(\mathrm{PMOS})}/\mathrm{Area}_{(\mathrm{NMOS})}$) is 2.6:1 instead of

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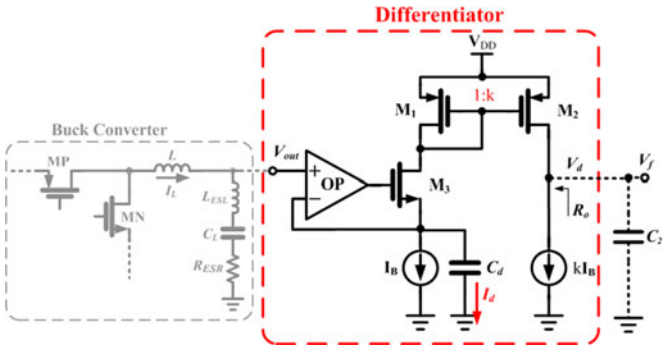


Fig. 1. Differentiator implemented by a VCCS circuit.

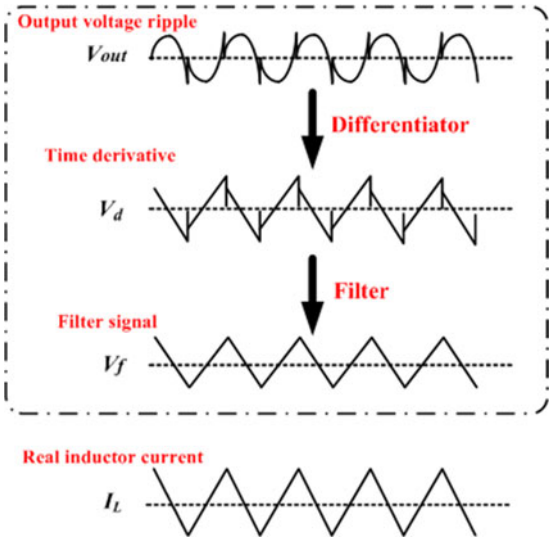


Fig. 2. Concept of the DORV under steady load.

the conventional value of 3:1. Such design leads to less power MOSs losses and is discussed further later in this paper.

The proposed AVDE control technique will be introduced in Section II, and the circuit descriptions of the proposed AVDE buck converter is described in Section III. The experimental results are shown in Section IV to verify the design and performance as claimed. Finally, conclusions are made in Section V.

II. Proposed AVDE Buck Converter

A. Concept of AVDE

The problems of DORV are discussed first. The differentiator is implemented by a voltage-control current-source (VCCS) circuit [12] as shown in Fig. 1 where $V_{\rm out}$ is the output voltage of a buck converter. The OP amplifier and the NMOS switch M_3 form a negative feedback circuit to generate the differential current I_d with capacitor C_d. The current I_d is then mirrored and amplified k times by M_1 and M_2 to produce the output voltage V_d, which can be expressed as follows:

$$\boldsymbol{V}_d = \boldsymbol{k}\boldsymbol{R}_o\boldsymbol{I}_d \tag{1}$$

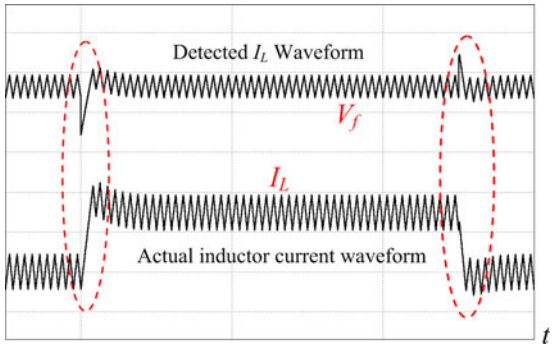


Fig. 3. Waveforms of V_f and I_L when the load changes instantaneously from light to heavy load and from heavy to light load. From top to bottom, vertical scale: 2 V/div, 500 mA/div; horizontal scale: 20 μs/div.

where R_o is the equivalent output resistance of the VCCS circuit.

If we neglect the effect of $L_{\rm ESL}$ for the moment and consider only $R_{\rm ESR}$ and C_L, we get

$$\boldsymbol{V}_d = \boldsymbol{k}\boldsymbol{C}_d\boldsymbol{R}_o\left(\frac{\boldsymbol{dV}_{\rm out}}{\boldsymbol{dt}}\right) = \boldsymbol{k}\boldsymbol{C}_d\boldsymbol{R}_o\left(\boldsymbol{R}_{\rm ESR}\frac{\boldsymbol{dI}_L}{\boldsymbol{dt}} + \frac{\boldsymbol{I}_L}{\boldsymbol{C}_L}\right). \tag{2}$$

As can be seen from (2), V_d contains the information of the inductor current I_L even with small $R_{\rm ESR}$. By contrast, a large $R_{\rm ESR}$ is needed by a conventional V^2 control.

If the influence of $L_{\rm ESL}$ is considered, V_d can be expressed as follows:

$$\begin{aligned}\boldsymbol{V}_d &= \boldsymbol{k}\boldsymbol{C}_d\boldsymbol{R}_o\left(\frac{\boldsymbol{dV}_{\rm out}}{\boldsymbol{dt}}\right)\\ &= \boldsymbol{k}\boldsymbol{C}_d\boldsymbol{R}_o\left(\boldsymbol{R}_{\rm ESR}\frac{\boldsymbol{dI}_L}{\boldsymbol{dt}} + \boldsymbol{L}_{\rm ESL}\frac{\boldsymbol{d}^2\boldsymbol{I}_L}{\boldsymbol{dt}^2} + \frac{\boldsymbol{I}_L}{\boldsymbol{C}_L}\right).\end{aligned} \tag{3}$$

A typical waveform of V_d under steady load is shown in Fig. 2. Because of the high-frequency components associated with $L_{\rm ESL}$ and $R_{\rm ESR}$, the waveform of V_d does not resemble the waveform of the inductor current I_L. Such waveform distortion is the first inherent problem or limitation of the DORV. The high-frequency components in the waveform of V_d can be filtered out by adding a capacitor in the differential circuit [1] to obtain a signal V_f, the detected I_L or the pseudo current, whose waveform is almost identical to that of I_L as shown in Fig. 2.

The waveforms of V_f and I_L when the load changes instantaneously from light to heavy load and from heavy to light load are shown in Fig. 3, where the upper waveform is the waveform of V_f or the sensed waveform, and the lower waveform is the actual waveform of I_L. While both waveforms are almost identical as in the steady state mentioned earlier, their dc levels are not the same. Such inability to track the dc level of I_L is the second limitation of the DORV. The waveform of V_f can never follow I_L exactly.

However, notice that there are sudden pulsations or changes of V_f that are almost exactly the same but opposite to those of I_L as highlighted by the dashed circles in Fig. 3. Therefore, it can be concluded that:

1) The waveforms of V_f and I_L under steady state are almost the same except for their dc levels.

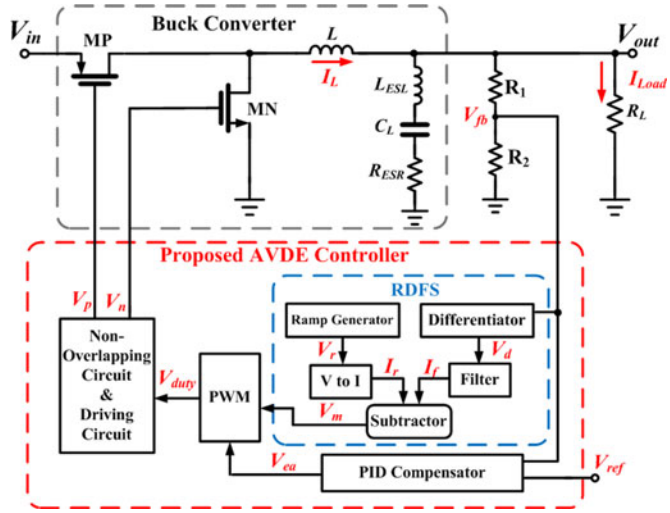


Fig. 4. Block diagram of the proposed AVDE buck converter.

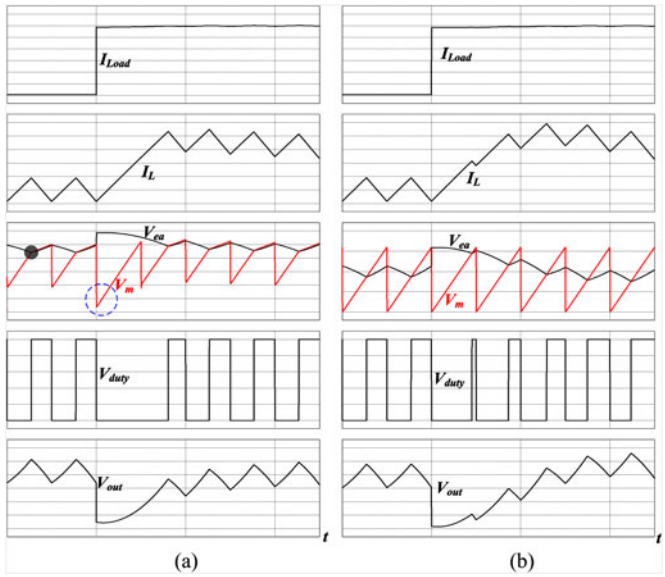


Fig. 5. Converters responses when load current changes from light to heavy: (a) with AVDE; (b) without AVDE. From top to bottom, vertical scale: 50 mA/div, 100 mA/div, 200 mV/div, 200 mV/div, 10 mV/div; horizontal scale: 2 μs/div.

2) There are almost same but opposite pulsations or changes in the waveforms of V_f and I_L at the instant of load change.

More detail follows.

The dc level is denoted as $\boldsymbol{V}_{dc\text{-}C_L}$. The output voltage $V_{\rm out}$ can be rewritten as (4) with the effect of $L_{\rm ESL}$ included

$$\boldsymbol{V}_{\rm out} = \boldsymbol{L}_{\rm ESL}\frac{\boldsymbol{dI}_L}{\boldsymbol{dt}} + \boldsymbol{R}_{\rm ESR}\boldsymbol{I}_L + \frac{1}{\boldsymbol{C}_L}\int \boldsymbol{I}_L\boldsymbol{dt} + \boldsymbol{V}_{dc\text{-}C_L} \tag{4}$$

and V_d can be expressed as follows:

$$\begin{aligned}\boldsymbol{V}_d &= \frac{\boldsymbol{dV}_{\rm out}}{\boldsymbol{dt}} \\ &= \boldsymbol{kC}_d\boldsymbol{R}_o\left(\boldsymbol{L}_{\rm ESL}\frac{\boldsymbol{d}^2\boldsymbol{I}_L}{\boldsymbol{dt}^2} + \boldsymbol{R}_{\rm ESR}\frac{\boldsymbol{dI}_L}{\boldsymbol{dt}} \right. \\ &\quad \left. + \frac{\boldsymbol{I}_L}{\boldsymbol{C}_L} + \frac{\boldsymbol{dV}_{dc-C_L}}{\boldsymbol{dt}}\right).\end{aligned} \tag{5}$$

A capacitor is used as a high-frequency filter to eliminate the $R_{\rm ESR}$ and $L_{\rm ESL}$ terms. The effectiveness of the filter is shown in Fig. 2, and the signal V_f can be expressed as follows:

$$\boldsymbol{V}_f \approx \boldsymbol{kC}_d\boldsymbol{R}_o\left(\frac{\boldsymbol{I}_L}{\boldsymbol{C}_L} + \frac{\boldsymbol{dV}_{dc-C_L}}{\boldsymbol{dt}}\right). \tag{6}$$

The $\boldsymbol{V}_{dc-C_L}$ term is eliminated by the differentiator and only information of I_L remains under constant load. On the other hand, the dV_{dc-C_L}/dt term contains important information of load changes, and can be integrated into the PWM sawtooth wave. This is why the proposed AVDE controller can improve the transient response time when load changes and has no adverse effect on the steady state.

The development of the AVDE control circuit and the implementation of the proposed AVDE buck converter with fast transient response are described later.

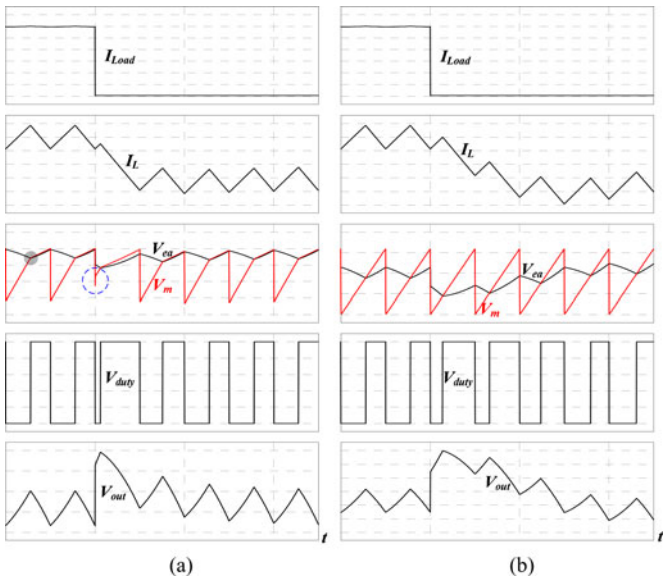


Fig. 6. Converters responses when load current changes from heavy to light: (a) with AVDE; (b) without AVDE. From top to bottom, vertical scale: 50 mA/div, 100 mA/div, 200 mV/div, 200 mV/div, 10 mV/div; horizontal scale: 2 μs/div.

B. Proposed AVDE Controller

The block diagram of the proposed AVDE buck converter is shown in Fig. 4. It is composed of a buck converter that contains two MOS power switches and a second-order *LC* filter [15], a nonoverlapping circuit and driving circuit, a pulsewidth modulator (PWM), a PID compensator, and a ramp and differentiator-filter subtractor (RDFS) circuit, which consists of a ramp generator, a voltage-to-current converter (*V* to *I*), a differentiator,

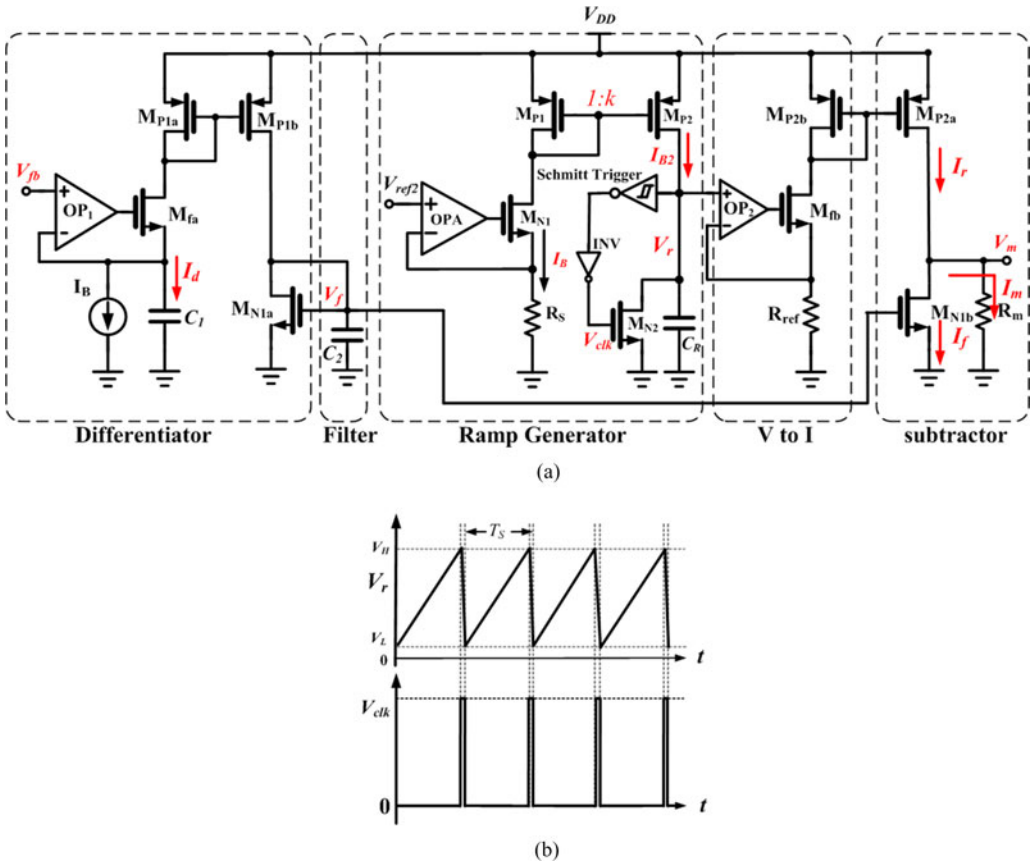


Fig. 7. (a) RDFS circuit and (b) the ramp generator waveforms.

a filter, and a subtractor. The C_L, R_1, R_2, R_L, and L are the external components.

There are two subintervals in each operating cycle of the buck converter. During the first subinterval, the power switch $M_{\rm MP}$ is ON and $M_{\rm MN}$ is OFF, $V_{\rm in}$ passes through the *LC* low-pass filter and output to the load R_L. In the second subinterval, the power switch $M_{\rm MN}$ is ON and $M_{\rm MP}$ is OFF, and the energy is released from the inductor L to the load R_L.

In contrast, a conventional buck converter has only a ramp generator instead of the complete RDFS circuit. This makes a conventional buck converter responds slower because its V_m signal is simply a periodic ramp signal, which does not respond to load changes.

As can be seen in Fig. 4, the divided output voltage V_{fb} and the reference voltage $V_{\rm ref}$ are fed to the PID compensator to generate V_{ea}. The signal V_{fb} is also fed to the RDFS to generate a differentiator-filter signal I_f, which is subtracted from the ramp signal I_r to produce the RDFS output signal V_m. The signals V_{ea} and V_m are then fed into the PWM to generate the duty cycle signal $V_{\rm duty}$, which is fed to the nonoverlapping circuit and driving circuit to generate the control signals V_p and V_n to control the MOS switches in the buck converter.

The operations of the proposed AVDE buck converter and a conventional buck converter under steady load and under load changes are analyzed and compared in detail later.

The responses of the converters under steady load and when load changes from light load to heavy load are shown in Fig. 5. In order to demonstrate the effectiveness of the proposed AVDE controller, the responses of identical load changes from light load to heavy load with the AVDE function enabled and disabled are shown in Fig. 5(a) and (b), respectively.

For the proposed AVDE buck converter under steady state or when $I_{\rm Load}$ is constant, I_r and I_f are mixed (subtracted) to generate V_m, which changed from a ramp wave to a quadrilateral waveform and its vertex points are where the duty changes. The intersections of the waveforms of V_m and V_{ea} always occur at these vertices to generate the required control duty, and this is the same as conventional PWM control. When the load suddenly changes from light to heavy, both $V_{\rm out}$ and I_f drop abruptly, which causes a sudden drop in V_m as highlighted by the dashed circle in Fig. 5(a). This sudden drop in V_m leads to the desired correction of the $V_{\rm duty}$ to quicken the recovery of $V_{\rm out}$ as shown in Fig. 5(a). The response of a conventional converter is shown in Fig. 5(b) for comparison.

The responses of the converters under steady load and when load changes from heavy load to light load are shown in Fig. 6. In order to demonstrate the effectiveness of the proposed AVDE controller, the responses of identical load changes from heavy load to light load with the AVDE function enabled and disabled are shown in Fig. 6(a) and (b), respectively. When the load suddenly changes from heavy to light, both $V_{\rm out}$ and I_f rise

abruptly, which causes a sudden increase in V_m as highlighted by the dashed circle in Fig. 6(a). This sudden increase in V_m also leads to the desired correction of the $V_{\rm duty}$ to quicken the recovery of $V_{\rm out}$ as shown in Fig. 6(a). The response of a conventional converter is shown in Fig. 6(b) for comparison.

It should be noted that slope compensation is not needed because the proposed AVDE buck converter is operated in voltage control mode rather than in peak current control mode.

It is clear that the proposed AVDE technique, which utilizes the RDFS signal V_m, can detect the load changes correctly and improve the transient response significantly. The circuit implementation of the proposed AVDE converter is described in the next section.

III. Circuit Descriptions

A. RDFS Circuit

Fig. 7(a) shows the RDFS, which consists of a differentiator, a filter [12], a ramp generator, a voltage-to-current converter (*V* to *I*), and a subtractor.

The input voltage V_{fb} comes from the voltage divider circuit of the converter output voltage $V_{\rm out}$ and contains information of the inductor current. As mentioned in Section II, $V_{fb}(= k_{fb}V_{\rm out})$ is composed of four components: $\boldsymbol{L}_{\rm ESL}(\boldsymbol{dI/dt})$, $\boldsymbol{R}_{\rm ESR}\boldsymbol{I}$, $(1/C_L)\int \boldsymbol{I}dt$, and $\boldsymbol{V}_{dc-C_L}$. The V_{fb} passes through a differentiator, composed by $\rm OP_1$, C_1, and $M_{\rm fa}$, to obtain differential signal I_d, which is mirrored by $M_{\rm P1a}$ and $M_{\rm P1b}$ and then filtered by a 5 pF capacitor C_2 to eliminate the high-frequency components related to $\boldsymbol{L}_{\rm ESL}(\boldsymbol{d^2I/dt^2})$ and $\boldsymbol{R}_{\rm ESR}(\boldsymbol{dI/dt})$. As a result, the final output voltage V_f and thus the current I_f derived by $M_{\rm N1b}$ is free from the influence of $R_{\rm ESR}$ and $L_{\rm ESL}$ and retains only terms proportional to I/C_L (information of inductor current) and dV_{dc-C_L}/dt (information of load variation).

The ramp generator generates a ramp signal using the basic PWM technique [17] [see Fig. 7(a)]. The reference voltage $V_{\rm ref2}$ is inputted to the OP amplifier to generate I_B, which is mirrored by $M_{\rm P1}$ and $M_{\rm P2}$ to obtain a constant current $I_{B2}(= kI_B)$. The path of I_{B2} and thus the charging or discharging of C_R depends on the ON/OFF state of switch $M_{\rm N2}$, which, in turn, depends on the output voltage V_{clk} of the INV-Schmitt trigger [16], which, in turn, depends on the output ramp voltage V_r. When V_r is low, V_{clk} is low (logic 0), $M_{\rm N2}$ is OFF, C_R is charged by I_{B2}, and V_r rises linearly with time. When V_r reaches V_H, the Schmitt trigger changes its state, V_{clk} is HIGH (logic 1), $M_{\rm N2}$ is ON, I_{B2} flows through $M_{\rm N2}$, C_R is discharged through $M_{\rm N2}$ to ground, and V_r drops very quickly toward ground level. When V_r reaches V_L, the Schmitt trigger changes its state again, and the earlier process repeats itself all over again. The waveforms V_r and V_{clk} are shown in Fig. 7(b).

The ramp frequency f_r can be expressed as (7) and is set to 1 MHz in the proposed AVDE buck converter

$$\boldsymbol{f}_r = \frac{\boldsymbol{I}_{B2}}{\boldsymbol{C}_R \times \Delta \boldsymbol{V}}. \tag{7}$$

The ramp voltage V_r is inputted to the voltage-to-current converter (*V* to *I*) to obtain a ramp current I_r in the same way I_{B2} is obtained from external power supply $V_{\rm ref2}$.

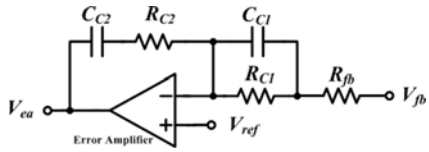


Fig. 8. PID compensator.

TABLE I
Component Parameters of the PID Compensator

Resistor and Capacitor	Value
R_{C2}	300 kΩ
R_{C1}	1 kΩ
R_{fb}	10 kΩ
C_{C2}	10 nF
C_{C1}	1 nF

Finally, the current $I_m = I_r - I_f$ is obtained and flows through the resistor R_m in the subtractor to produce the RDFS output signal V_m, which can be expressed as follows:

$$\boldsymbol{V}_m = \underbrace{\boldsymbol{V}_r - \boldsymbol{kC}_1\boldsymbol{R}_o\left(\frac{\boldsymbol{I}}{\boldsymbol{C_L}}\right)}_{\text{Vramp - pseudo current}} \underbrace{-\boldsymbol{kC}_1\boldsymbol{R}_o\left(\frac{\boldsymbol{dV}_{\rm dc-c_L}}{\boldsymbol{dt}}\right)}_{\text{dynamic detection}}. \tag{8}$$

The Vramp-pseudocurrent term is concealed in the ramp and does not affect the correct duty cycle switching times. The dynamic detection term is the main contribution factor for the fast transient response.

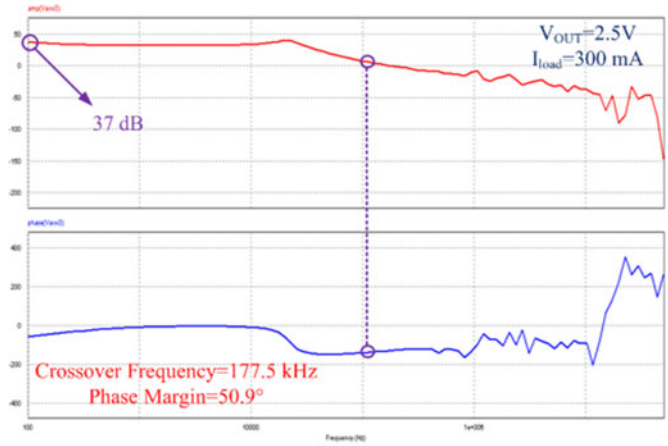
B. PID Compensator Circuit

The PID compensator circuit is shown in Fig. 8 where V_{fb} is the converter output voltage derived from the voltage divider circuit, V_{ea} is the output voltage of the PID compensator, and $V_{\rm ref}$ is the external reference voltage. The C_{C_2}, R_{C_2}, C_{C_1}, R_{C_1}, and R_{fb} are the external components. The PID compensator can extend the crossover frequency and increase the phase margin and loop gain to improve the stability of the proposed converter [18].

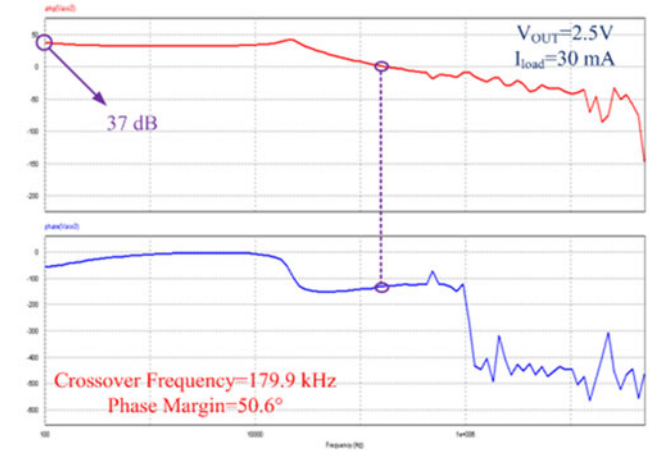
The transfer function of the PID compensator can be described as

$$\frac{V_{ea}}{V_{fb}} = \frac{R_{C_2}}{R_{fb}}\frac{(S + (1/C_{C_1}R_{C_1}))\,(S + (1/C_{C_2}R_{C_2}))}{S\,(S + (1/C_{C_1}R_{fb}))}. \tag{9}$$

The component parameters of the PID compensator are listed in Table I. The simulation result of the closed-loop gains of the buck converter at 2.5 V output voltage and 1 MHz switching frequency when the load currents are 300 and 30 mA are shown in Fig. 9(a) and (b), respectively. The result shows that the low frequency gain is about 37 dB, the crossover frequency is about 177.5 kHz (about 1/5–1/10 of main switching frequency), and the phase margin is 50.9°. The simulation result shows that the proposed buck converter is very stable.



(a)



(b)

Fig. 9. Open-loop gain at $V_{\rm out} = 2.5$V and switching frequency = 1 MHz. (a) $I_{\rm Load} = 300$ mA. (b) $I_{\rm Load} = 30$ mA.

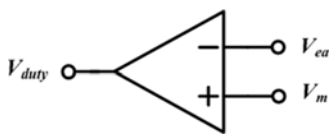


Fig. 10. PWM Symbol

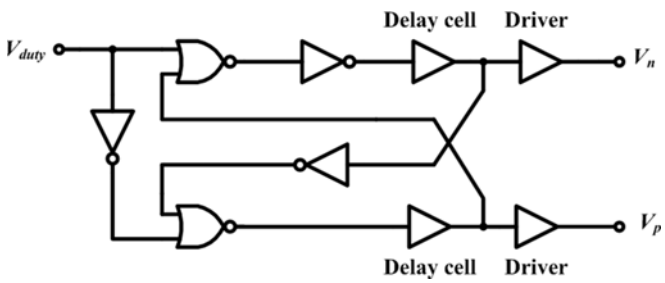


Fig. 11. Nonoverlapping circuit and driving circuit and its typical timing diagram.

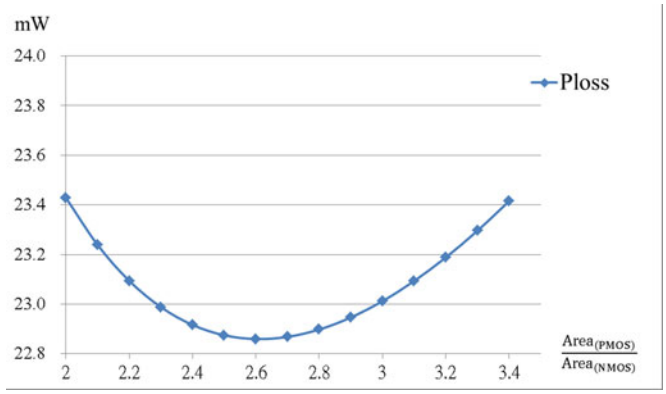


Fig. 12. Power loss versus area ratio ($\text{Area}_{\text{power\_PMOS}}/\text{Area}_{\text{power\_NMOS}}$).

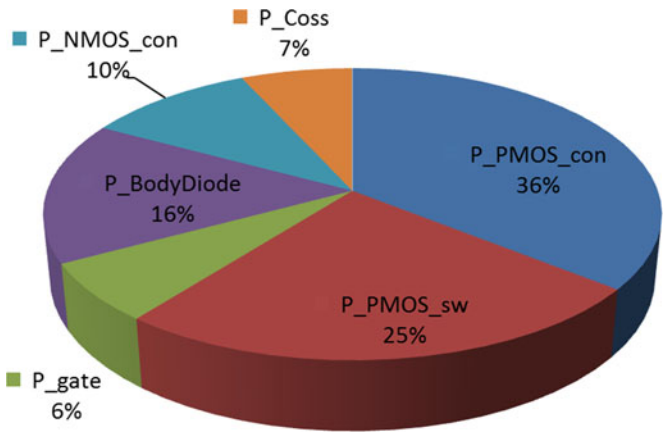


Fig. 13. Percentages of total power MOS loss of individual losses.

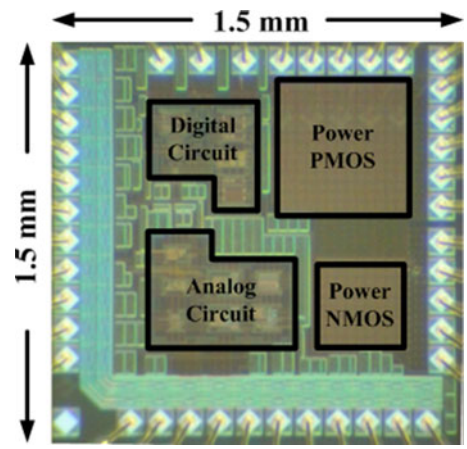
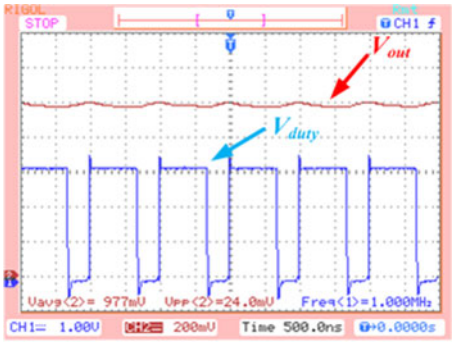


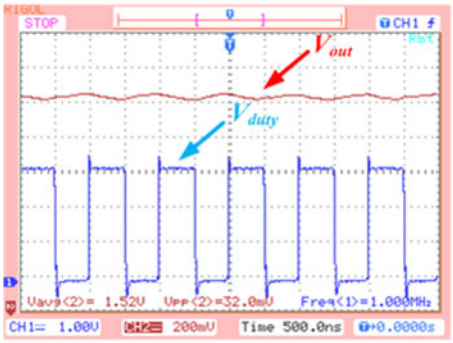
Fig. 14. Chip microphotograph and configuration of the proposed AVDE buck converter.

C. Pulsewidth Modulator

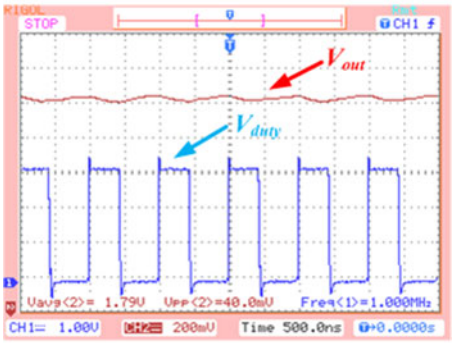
The PWM circuit is basically a comparator as shown in Fig. 10. The RDFS signal V_m and the PID compensator signal V_{ea} are inputted to generate the duty cycle signal $V_{\rm duty}$.



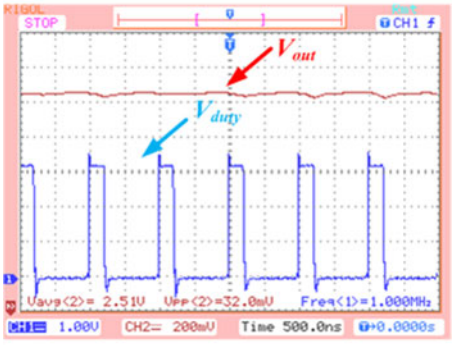
(a)



(b)

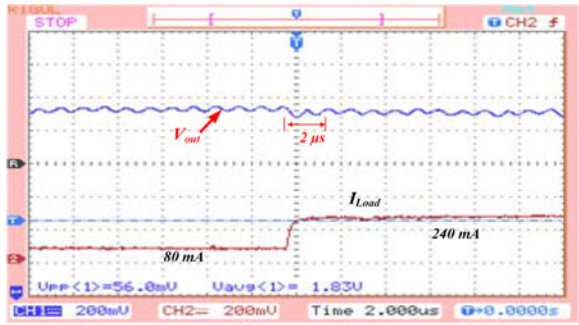


(c)

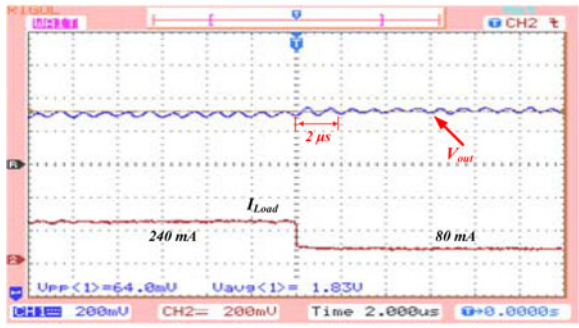


(d)

Fig. 15. Steady-state responses of the proposed AVDE buck converter at $V_{\rm in} = 3.3$ V and $I_{\rm Load} = 50$ mA. (a) $V_{\rm out} = 1$ V and $D = 30.3\%$. (b) $V_{\rm out} = 1.5$ V and $D = 45.4\%$. (c) $V_{\rm out} = 1.8$ V and $D = 54.5\%$. (d) $V_{\rm out} = 2.5$ V and $D = 75.8\%$.

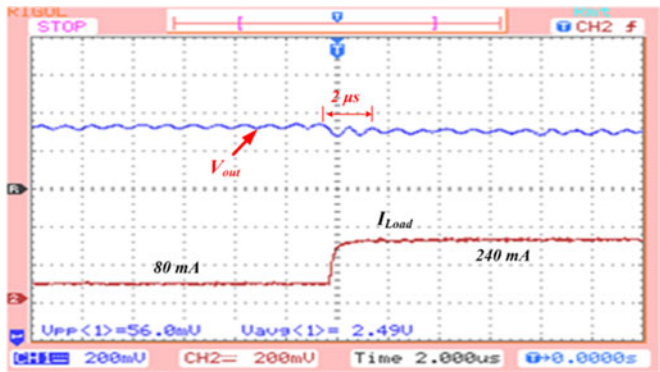


(a)

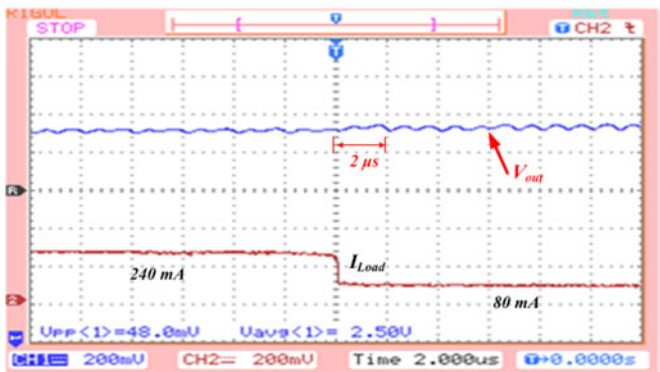


(b)

Fig. 16. Transient responses of the proposed AVDE buck converter at $V_{\rm in} = 3.3$ V and $V_{\rm out} = 1.8$ V. (a) $I_{\rm Load}$ changes from 80 to 240 mA. (b) $I_{\rm Load}$ changes from 240 to 80 mA.

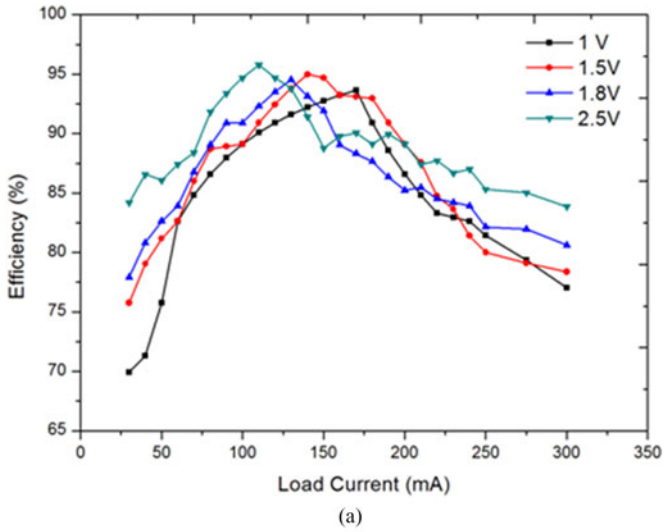


(a)



(b)

Fig. 17. Transient responses of the proposed AVDE buck converter at $V_{\rm in} = 3.3$ V and $V_{\rm out} = 2.5$ V. (a) $I_{\rm Load}$ changes from 80 to 240 mA. (b) $I_{\rm Load}$ changes from 240 to 80 mA.



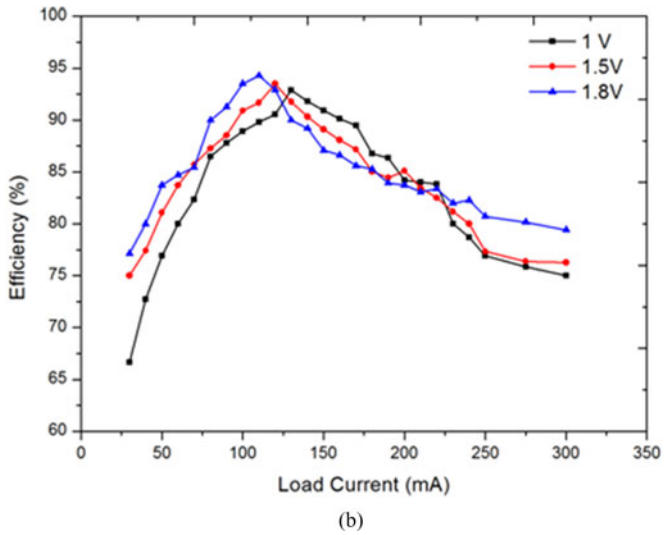


Fig. 18. Power efficiencies of the proposed AVDE buck converter. (a) $V_{\rm in} = 3.3$ V. (b) $V_{\rm in} = 2.5$ V.

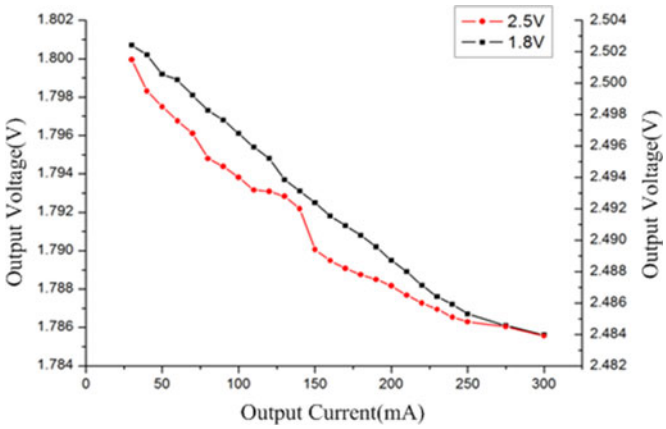


Fig. 19. Voltage regulations of the proposed AVDE buck converter with input voltage $V_{\rm in} = 3.3$ V (line with squares (black): $V_{\rm out} = 1.8$ V; line with circles (red): $V_{\rm out} = 2.5$ V).

TABLE II
SUMMARY OF SPECIFICATIONS AND PERFORMANCE

Technology		0.35 μm 2P4M 3.3/5 V
Input voltage		1.8–3.6 V (3.3 V nominal)
Output voltage range		1.0–2.5 V
Max. load current		300 mA
Max. output ripple		40 mV
Inductor (L) (off-chip)		4.7 μH
Output capacitor (C_L) (off-chip)		10 μF(R_{ESR} $\approx$150 mΩ)
Transient response	Rise (80 mA $\rightarrow$ 240 mA)	2 μs
	Fall (240 mA $\rightarrow$ 80 mA)	2 μs
Load regulation		25.25 ppm/mA
Line regulation		0.88%/V at $V_{\rm out} = 2.5$ V, $I_{\rm Load} = 150$ mA
Peak power efficiency		95% at $V_{out} = 2.5$ V, $I_{\rm Load} = 110$ mA
Switching frequency		1 MHz
Chip area (with PADs)		1.5 mm $\times$1.5 mm

D. Nonoverlapping Circuit and Driving Circuit

The nonoverlapping circuit and driving circuit [19] is shown in Fig. 11. It receives the duty cycle signal $V_{\rm duty}$ from the PWM to generate the control signals V_p and V_n, which does not only control the PMOS and NMOS power switches but also prevent them from being turned ON at the same time. If the two power switches conduct at the same time, the supply voltage $V_{\rm DD}$ is shorted to ground and large currents occur. This not only wastes energy and generates heat but may also overheat or even damage the circuit. Since large transistor gate areas means large capacitances, driver circuits are needed to boost the driving capacity to make the rising edges and the falling edges of the waveforms as steep as possible so that the control signals V_p and V_n are as close to ideal square waves as possible.

E. Power Dissipation Analysis

There are three major power losses in a buck converter: control circuit loss, power MOS loss and inductor conduction loss (core loss and winding loss). If only the control circuit, the power consumption of the subcircuits is about 0.74% of the total buck converter power consumption. Power MOS loss composes about 80% of the total loss, whereas control circuit loss and inductor conduction loss compose about 20% of the total loss. The power loss related to power MOSs in a buck converter comprises conduction loss and switching loss. Conduction loss is dependent on the *W*/*L* ratio. Switching loss consists of PMOS switching loss, NMOS switching loss, gate drive loss, NMOS body diode loss, and MOS output capacitance loss. Switching loss is also dependent on the *W*/*L* ratio. In general, the area of power PMOS is about three times that of power NMOS due to hole–electron mobility ratio considerations.

Software Hspice is used in this study to extract the simulation parameters to perform the power loss simulation for the proposed buck converter at normal $V_{\rm in} = 3.3$ V and $V_{\rm out} = 2.5$ V, with the area ratio of power PMOS to power NMOS ($\text{Area}_{(\rm PMOS)}/\text{Area}_{(\rm NMOS)}$) ranging from 2 to 3.4, and the results are shown in Fig. 12. The power MOS

TABLE III
COMPARISON OF RECENTLY PUBLISHED CMOS BUCK CONVERTERS

	2008 [12]	**2009 [13]**	**2009 [20]**	**2012 [21]**	**2013 [22]**	**2014[23]**	**This Work**
Technology	0.35 μm	0.35 μm	65 nm	0.35 μm	0.18 μm	0.18 μm	0.35 μm
Inductor	N/A	4.7 μH	4.7 μH	22 μH	4.7 μH	78 nH	4.7 μH
Output capacitor	10 μF	4.7 μF	4.7 μF	22 μF	47 μF	0.94 μF	10 μF
Input voltage	2.4 V	2.8–3.6 V	3.3 V	2.6–3.6 V	0.9–1.5 V	3.3 V	1.8–3.6 V (3.3 V nominal)
Output voltage	1.8 V	2 V	1.2 V	0.6–2.1 V	0.3–0.9 V	0.7–2.5 V	1.0–2.5 V
Max. load current	500 mA	500 mA	500 mA	N/A	320 mA	6000 mA	300 mA
Switching frequency	500 kHz	800 kHz	800 kHz	1 MHz	1 MHz	40 MHz	1 MHz
Transient response (step load change)	**10 μs at 450 mA**	**10 μs at 300 mA**	**8 μs at 200 mA**	**9 μs at 450 mA**	**5 μs at 320 mA**	**5 ns at 5000 mA**	**2 μs at 160 mA**
Load regulation (ppm/mA)	N/A	16.5	22.2	N/A	83	N/A	25.25
Peak efficiency	**N/A**	**93%**	**92%**	**90%**	**91.5%**	**86.1%**	**95.78%**
Chip area (with PADs)	1.8 mm × 1 mm	1.88 mm × 1.54 mm	1.12 mm × 0.88 mm	1.6 mm × 1.9 mm	1.34 mm × 1.23 mm	2.5 mm × 3.1 mm	1.5 mm × 1.5 mm
FOM_a [1]	N/A	0.0358	0.0435	0.0222	0.0171	0.000053	0.0131
FOM_b [2]	44.44	66.67	80.00	N/A	48.83	0.0077	41.67
FOM[3]	**N/A**	**71.68**	**86.96**	**N/A**	**53.36**	**0.0089**	**43.50**

[1] $\mathrm{FOM_a} = \frac{\mathrm{Transient\,Response\,Time\ (\mu s)/Step\,Load\,Change\ (mA)}}{\mathrm{Peak\,Efficiency\ (\%)}}$.
[2] $\mathrm{FOM_b} = \frac{\mathrm{Transient\,Response\,Time\ (\mu s)/Step\,Load\,Change\ (mA)}}{\mathrm{Max.Load\,Current\ (mA)}} \times 10^6$.
[3] $\mathrm{FOM} = \frac{\mathrm{Transient\,Response\,Time\ (\mu s)/Step\,Load\,Change\ (mA)}}{\mathrm{Peak\,Efficiency\ (\%)} \times \mathrm{Max.Load\,Current(mA)}} \times 10^6$.

loss is composed of PMOS conduction loss (P_PMOS_con), PMOS switching loss (P_PMOS_sw), gate drive loss (P_gate), body diode loss (P_BodyDiode), NMOS conduction loss (P_NMOS_con), and MOSs output capacitance loss (P_Coss). The percentages of total power MOS loss of these individual losses are shown in Fig. 13. Since the simulation results show that the power loss is minimal when the area ratio ($\mathrm{Area_{power\_PMOS}/Area_{power\_NMOS}}$) is 2.6:1, the area ratio in the physical IC chip microphotograph implementation of the proposed converter is therefore determined to be 2.6:1 accordingly, as shown in Fig. 14.

IV. EXPERIMENT RESULTS

The proposed AVDE buck converter has been fabricated with a commercial 0.35 μm CMOS 2P4M processes. The nominal input voltage of the proposed AVDE buck converter is 3.3 V and ranges from 1.8–3.6 V. The maximum load current is 300 mA, and the converter output voltage can be regulated from 1.0 to 2.5 V. The total chip area is 1.5 mm × 1.5 mm, PADs included. The micrograph and configuration of the proposed AVDE buck converter is shown in Fig. 14. The PMOS to NMOS area ratio of 2.6:1 is realized to achieve higher efficiency. The switching frequency is 1 MHz and its maximum output ripple is less than 40 mV, and the off-chip inductor and output capacitor are 4.7 μH and 10 μF, respectively.

Fig. 15 shows the steady-state responses of the proposed converter at $V_{\mathrm{in}} = 3.3$ V and $I_{\mathrm{Load}} = 50$ mA. When the duty cycles (D) are 30.3%, 45.4%, 54.5%, and 75.8%, the output voltages V_{out} are 1, 1.5, 1.8, and 2.5 V, respectively.

Fig. 16 shows the transient responses of the proposed buck converter at $V_{\mathrm{out}} = 1.8$ V. Fig. 16(a) shows the transient response as I_{Load} changes from 80 to 240 mA. Fig. 16(b) shows the transient response as I_{Load} changes from 240 to 80 mA. Fig. 17 shows the transient response of the proposed buck converter at $V_{\mathrm{out}} = 2.5$ V. Fig. 17(a) shows the transient response as I_{Load} changes from 80 to 240 mA. Fig. 17(b) shows the transient response as I_{Load} changes from 240 to 80 mA. The transient response times are about 2 μs in each experiment, which agree well with the theory that fast load transient response.

The power efficiencies of the proposed converter at $V_{\mathrm{in}} = 3.3$ V and $V_{\mathrm{in}} = 2.5$ V are shown in Fig. 18. When $V_{\mathrm{in}} = 3.3$ V, the peak efficiency is 95% at $V_{\mathrm{out}} = 2.5$ V and $I_{\mathrm{Load}} = 110$ mA as shown in Fig. 18(a). When $V_{\mathrm{in}} = 2.5$ V, the peak efficiency is 94% at $V_{\mathrm{out}} = 1.8$ V and $I_{\mathrm{Load}} = 110$ mA as shown in Fig. 18(b).

The output voltage regulations with $V_{\mathrm{in}} = 3.3$ V when $V_{\mathrm{out}} = 1.8$ and 2.5 V at various load currents are shown in Fig. 19. The voltage regulations are all within 25.25 ppm/mA.

The specifications and the performance of the proposed AVDE buck converter are summarized in Table II. The comparisons of the performances of the proposed AVDE buck converter and some of the previous works are summarized in Table III. The figure of merit (FOM) takes parameters such as transient response time/step load change, peak efficiency and maximum load current into account. The smaller the FOM is, the better the converter performs. Such conclusion may also be drawn from the comparisons of the simplified $\mathrm{FOM_a}$ and $\mathrm{FOM_b}$. In Table III, the study by Song *et al.* [23] is excellent. Because the switching frequency is as high as 40 MHz, the transient response is 230 ns at 5 A. However, the disadvantage of such a high frequency is that the peak efficiency is only 86.1%. Furthermore, the variable switching frequency control of the hysteresis control scheme probably causes not only wide noise spectrum but also serious EMI shielding problems. As Table III shows, the proposed design has not only faster transient response but also higher efficiency compared to prior researches.

V. Conclusion

A buck converter applying a novel AVDE technique is proposed in this paper. Its performance is not affected by the R_{ESR} and the L_{ESL}, and it can achieve fast and stable transient responses within 2 μs. Its design is simple and it has been fabricated with a commercial 0.35 μm CMOS 2P4M process. The power PMOS to power NMOS area ratio in the physical IC implementation is 2.6:1 for minimum power loss. Results of experiments confirm that the proposed converter operates excellently as expected. With its excellent performance and peak efficiency of 95%, the proposed AVDE buck converter is suitable for applications in portable devices.

Acknowledgment

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