A Fully Integrated and Battery-Free Interface for Low-Voltage Electromagnetic Energy Harvesters

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***Abstract*—This paper presents a fully integrated and battery-free 90 nm interface circuit for ac/dc conversion and step up of low-voltage ac signals generated by electromagnetic (EM) energy harvesters. The circuit is composed of two stages: The rectifier in the first stage utilizes an improved ac/dc doubler structure with active diodes internally powered by a passive ac/dc doubler and custom-designed comparators to minimize the voltage drops. With this, the efficiency is enhanced to 67% while providing 0.61 V to 40 μA load. The second stage is a dc/dc converter utilizing a low-voltage charge pump with an on-chip ring oscillator for further voltage step up. The rectifier stage is functional down to 125 mV input peak voltage, and the full interface circuit can maintain more than 1 V dc at 1 MΩ load for input peak voltages higher than 0.4 V. The circuit delivers 2.48 V to a 4.4 MΩ load, when interfaced to an in-house EM harvester, operating under 10 Hz, 0.5*g* vibration.**

***Index Terms*—Electromagnetic (EM) power generation, fully integrated interface electronics, low-voltage ac/dc conversion, self-powered rectifier, vibration-based energy harvesting.**

I. Introduction

PORTABLE microelectronics enable contemporary smart systems with many applications such as communications, defense, environmental, structural, and biomedical monitoring. The weight and volume constraints limit temporary storage capacity to small batteries, leading to shorter lifetime, and added cost in replacement and recycling. Energy harvesting from ambient sources, which helps to increase the lifespan of the micropowered wireless sensor networks (WSNs), has thus attracted attention during the last decade [1], [2]. Vibration is especially attractive [3]–[5] due to its abundance; however, power and amplitude of the harvested signal highly depend on the vibration conditions. The kinetic energy in the vibrations can be harvested by electrostatic (ES), piezoelectric (PZT), or electromagnetic (EM) transducers [6]–[8]. PZT and EM harvesters yield relatively higher power density [9]. Interface electronics for PZT energy harvesters [10]–[12] benefit from high ac voltage. However, the high output impedance of the PZT interface necessitates the use of an additional impedance matching network, which increases the complexity and power losses. EM energy harvesters are more suitable for low frequency ($<$10 Hz) ambient vibrations due to the existence of a permanent magnet, which naturally acts as a seismic mass. Moreover, they have lower output impedance ($<$ few kΩ) compared to PZT and ES energy harvesters, which facilitates the processing of generated voltage. On the other hand, the generated ac power level is low, making the design of the interface circuit between the EM harvester and the dc load challenging.

The low-voltage profile of the EM energy harvesters at low frequency and acceleration conditions provides interface design challenges, due to voltage drops across the rectifying diodes. The maximum output dc voltage from the passive boot-strap rectifier (BSR) introduced in [13] and gate cross-coupled rectifier (GCCR) in [14] was limited to the peak value of the input signal. GCCR used two cross-coupled NMOS transistors at input stage, which caused poor performance due to threshold drops across the diode-connected devices. The ac/dc doubler structure in [15] produced rectified voltages at the input peak-to-peak voltage level, but an external supply was required to charge the front-end electronics. Although the rectifier efficiency in [16] was high, the minimum input voltage was limited due to the use of off-the-shelf components. A fully self-powered system by our group generated a dc voltage level at approximately input peak-to-peak value in [17], but use of discrete components limited the efficiency and increased the cost. Many previously reported designs either failed in achieving low input voltage [18], [19] or low cost and size [9], [19]–[21] due to the use of off-the-shelf (e.g., magnetic) components.

In this paper, a fully integrated and battery-free interface is presented for low-voltage EM energy harvesters. An active ac/dc doubler circuit efficiently rectifies the harvested voltage with power provided by an auxiliary passive ac/dc doubler. A dc/dc converter on the same chip boosts the rectified voltage sufficiently to drive a practical load. The multistage circuit has been designed in TSMC 90 nm CMOS technology, implemented, and validated under realistic conditions, using an in-house EM energy harvester module.

The next section contains the design and simulation based verification of the interface circuit. Experimental results from the 90 nm test chip are provided in Section III. Finally, Section IV concludes the paper.

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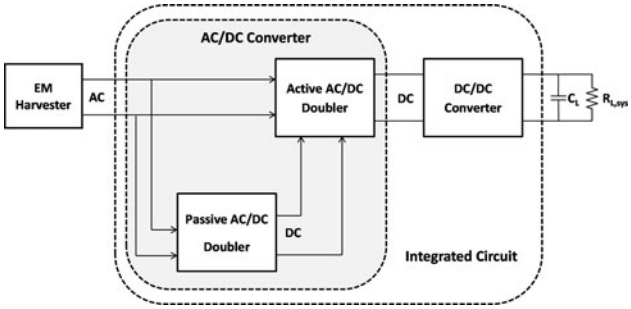

Fig. 1. Proposed interface circuit for power extraction from EM energy harvesters.

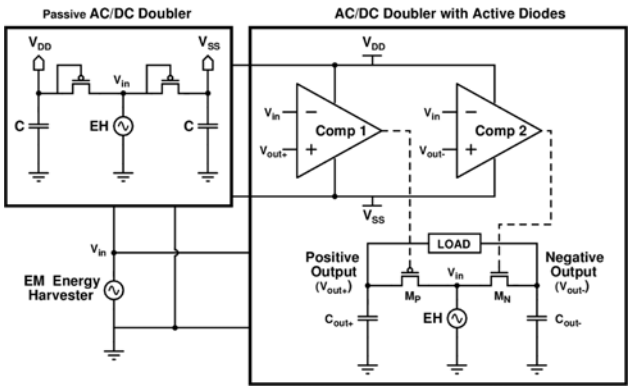

Fig. 2. Autonomous ac/dc converter with passive and active ac/dc doublers.

II. Interface Electronics Design

The interface circuit architecture between the EM transducer and the load is depicted in Fig. 1. The ac/dc converter at the first stage consists of a passive ac/dc doubler built from diode-connected transistors and an active ac/dc doubler employing active diodes [22]. The passive doubler supplies power to the active doubler. This design enables the operation of the efficient active rectifier without an auxiliary supply. The dc signal level at the output of the active rectifier cannot be higher than the input ac peak-to-peak voltage and is not therefore sufficient to power most low-power sensors from natural vibrations. Thus, a dc/dc converter in the second stage boosts the voltage to the desired level for the load.

A. Self-Powered Rectifier Circuit

Fig. 2 depicts the block diagram of the circuit to convert the ac signal, generated from vibrations of the EM harvester, into dc. The problem of rectifier voltage drop is alleviated using active diodes instead of the diode-connected transistors on the power delivery path to the load in order to increase the overall interface efficiency. Furthermore, active diodes can drive higher loads compared to the passive diodes. The ac/dc doubler is constructed with two active diodes consisting of two-pass transistors (M_P, M_N) and two comparators (Comp1, Comp2). Since the comparators require much less power than the power delivered to the load, the inefficiency of passive rectifier circuit as their power supply is not of concern.

When the input is higher than positive output, the comparator on the left side (Comp1) in Fig. 2 turns the PMOS pass transistor ON, and the positive output ($V_{\mathrm{out}+}$) is charged. As the input falls below the positive output, the pass transistor turns OFF, and positive charge is stored on the capacitor ($C_{\mathrm{out}+}$). Similarly, when the input drops below the voltage at the negative output node, the right-hand comparator (Comp 2) turns the NMOS pass transistor ON, which charges the negative output ($V_{\mathrm{out}-}$). The charge is stored on the capacitor ($C_{\mathrm{out}-}$) by turning the NMOS transistor OFF.

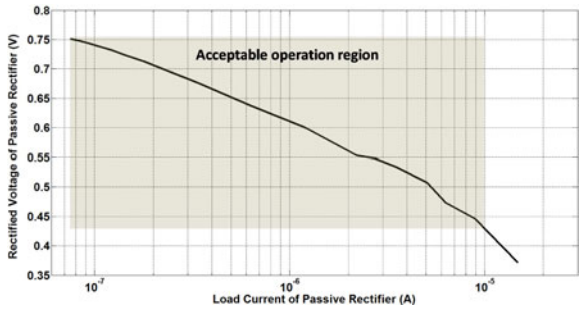

Fig. 3. Load line of passive rectifier.

The diode-connected MOSFETs in the passive rectifier of the first stage are sized based on optimization between their drain-to-source resistance R_{ds} and signal attenuation due to their parasitic capacitance.

The design of the comparators is dictated by the tradeoff between high gain required to sustain fast switching of the pass transistors, which increases the power dissipation, and the power available from the passive rectifier. The gain of the comparator is proportional to the transconductance of the input transistors by

$$A_V = g_{m\_\mathrm{in}} \times R_{\mathrm{out}} \tag{1}$$

where g_{m_in} is the transconductance of the input transistors and R_{out} is the output resistance of the comparator. Current consumption of the comparator increases proportionally with the transconductance according to the following equation:

$$g_m = \frac{kI_D}{V_T} \tag{2}$$

where k stands for the gate coupling coefficient, I_D is the current through the MOSFETs, and V_T is the thermal voltage (26 mV at room temperature). Hence, the higher gain for the comparator is simply achieved at the cost of higher power consumption.

The power consumption is also critical for another reason: Any excessive current consumption at the comparator augments the voltage drop across the passive rectifier. The effect of the current consumed by the comparators on the output voltage of the passive ac/dc doubler is shown in Fig. 3 for $V_{\mathrm{IN,peak}} = 0.5$ V and rectifier load, $R_L = 10$ kΩ. It can be inferred that the current consumption of the comparator should be less than 10 μA in order to ensure the availability of sufficient voltage for the comparators.

Fig. 4(a) shows the circuit used to verify the effect of comparator gain on the quality of rectification in ac/dc doubler circuit, which is simulated using load $R_L = 10$ kΩ, $C_L = 100$ μF, $V_{\mathrm{in_{peak}}} = 0.3$ V, and $f_{\mathrm{in}} = 10$ Hz. The rectified output voltage is plotted against the comparator gain in Fig. 4(b). According to the figure, the voltage gain of more than $A_v = 12$ will not increase

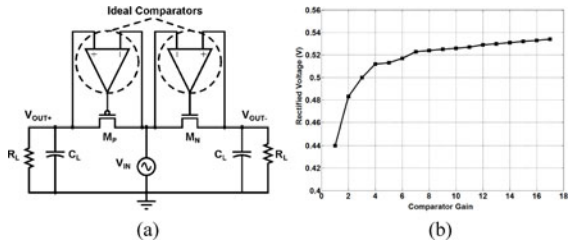

Fig. 4. AC/DC doubler performance dependence on comparator gain: (a) circuit under study and (b) output voltage versus comparator gain.

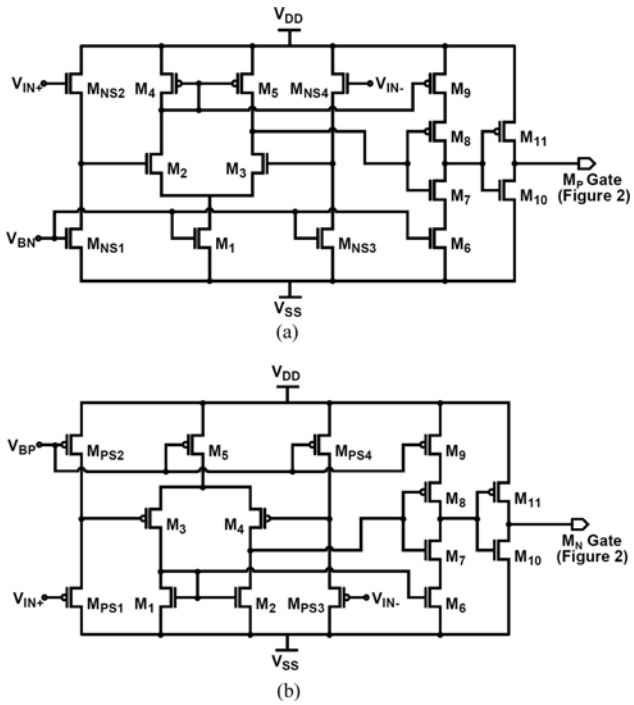

Fig. 5. Schematic of the comparator circuits used at (a) positive and (b) negative output terminals of the active ac/dc doubler circuit.

the magnitude of the rectified voltage considerably. However, $A_v = 16$ has been chosen in the design in order to preserve margin to compensate for parasitic elements in the nonideal circuit and to allow for lower rail to rail supply voltage derived from the input ac signal. Comparator MOSFETs are thus sized based on the gain target and the desired input gate capacitance (<30 fF).

B. Custom Comparators

Two circuit design techniques have been used at the comparator input stage to maximize the performance of the active rectifier by accurate sensing of the input voltage across the full rails: 1) source follower level shifters, and 2) customized input stage for the negative and positive output signal phase.

1) Source Follower Level Shifters: The voltage levels at the inputs of the comparators exceed their supply voltage, due to the higher voltage drop across the diode-connected transistors of the passive ac/dc doubler compared to the voltage drop across the active diodes. Source follower level shifters ($M_{\rm PS1}$–$M_{\rm PS4}$, $M_{\rm NS1}$–$M_{\rm NS4}$ in Fig. 5) pull the inputs to the common mode range to increase the sensitivity of the comparators to the voltage difference at the source and drain terminals of the pass transistors. Fig. 6(a) shows that the comparator without the level shifter is not able to preserve its low output when its negative input (ac voltage) is higher than its positive input (rectified voltage), since the input voltage is higher than the supply. On the other hand, the comparator with the level shifter stage retains the low output during the phase that its positive input is higher than the negative input. Fig. 6(b) indicates more current is delivered as a result to the load, and the output dc voltage improves [see Fig. 6(c)] with the level shifters.

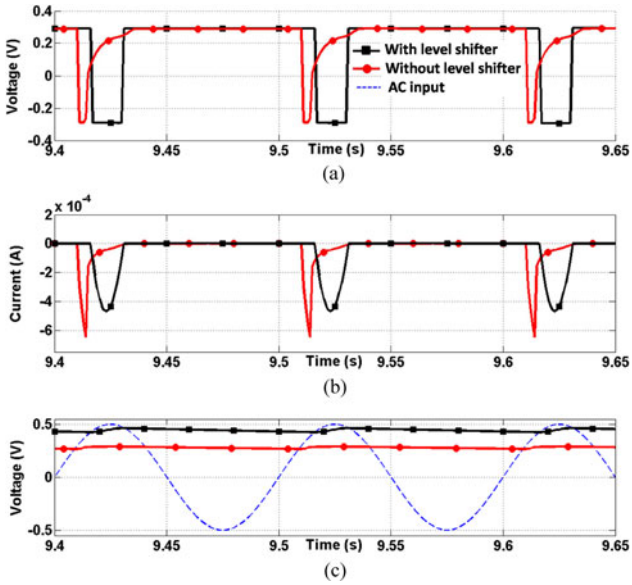

Fig. 6. (a) Output of the comparators; (b) the current through the pass transistors at active ac/dc doubler, and (c) the output voltage of ac/dc doubler rectifier, with and without the level shifter.

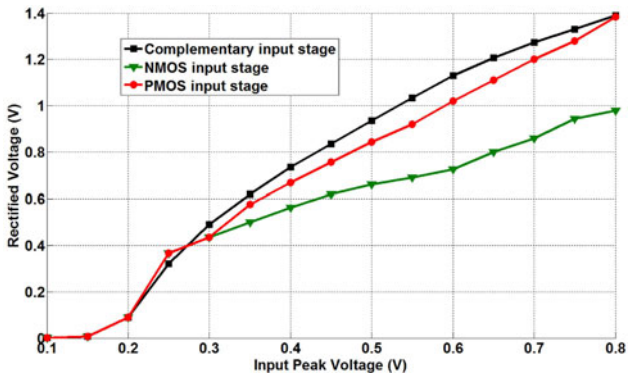

Fig. 7. Comparison of the active rectifier performance with different comparator input stage design approaches.

2) Input Stage Customized to Signal Phase: The input stage of each comparator is customized to best serve the phase of the ac input it is processing: P-type and N-type input MOSFETs are utilized for the generation of negative and positive outputs, respectively, as depicted in Fig. 5. The input common-mode range (ICMR) of the comparator with N-type MOSFETs is close to the positive supply ($V_{\rm DD}$), while the circuit with P-type MOSFETs has an ICMR closer to the negative supply. As depicted in the simulation (see Fig. 7) of the ac/dc doubler structure for different MOSFET options, the complementary design in Fig. 5

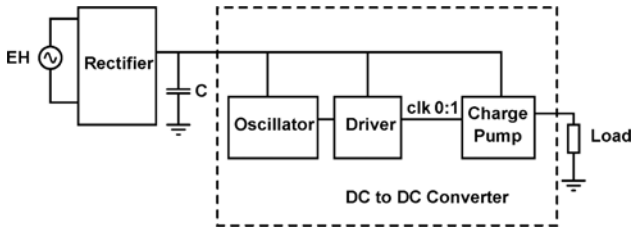

Fig. 8. Interface block diagram with dc–dc converter detail.

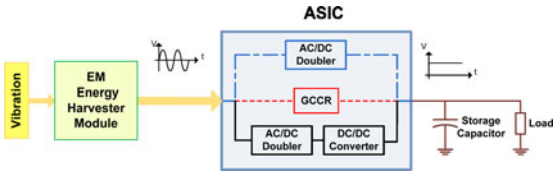

Fig. 9. Block diagram of the prepared test structure for the designed interface circuit.

achieves higher rectified voltages when compared to common comparator design with either NMOS or PMOS input stage for both phases of the input.

The comparators need two external voltages ($V_{\rm BP}$ and $V_{\rm BN}$) to be biased in current-starved configuration for low-power dissipation. A subthreshold voltage reference circuit from [23] has been adapted for generating the bias under low-voltage conditions with tolerance to supply and temperature variations.

C. DC-to-DC Converter

The rectified output is equal to the peak-to-peak value of the input ac voltage. This dc voltage (200–400 mV) may not be enough for powering typical microsystems. A state-of-the-art dc/dc converter has hence been designed for boosting the output voltage level of the rectifier to a higher dc level.

Fig. 8 shows the block diagram of the dc/dc converter, which is composed of an oscillator, a driver stage, and a charge pump. The current-starved ring oscillator is used to provide two complementary clocks for the charge pump circuits [24]. Addition of a driver stage is beneficial since it prevents extra loading of the oscillator and reduces the rise and fall time of the clocks, enhancing the charge pump boosting performance. A three-stage charge pump circuit constructed by cross-connected NMOS cells [25] has been utilized. The step-up ratio of the dc/dc converter depends on the input voltage and is more than 3 provided that the minimum input voltage of 0.3 V is available from the rectifier. Ripple can be minimized at the output voltage by utilizing a proper off-chip capacitor at the load side.

III. Test Results

A. Interface Circuit Test Structure

Fig. 9 illustrates the block diagram of the test system, which consists of an EM energy harvester module, the interface (IC) test chip, an external storage capacitor, and a resistive load. The EM energy harvester generates an ac signal from vibrations, which is fed to the test chip. The output capacitor can be fed from one of: 1) proposed ac/dc doubler circuit, 2) state-of-the-art GCCR [14], and 3) serially connected ac/dc doubler and dc/dc converter for full system characterization with boosted output voltage, which are all placed on the same test chip to enable detailed characterization and comparison.

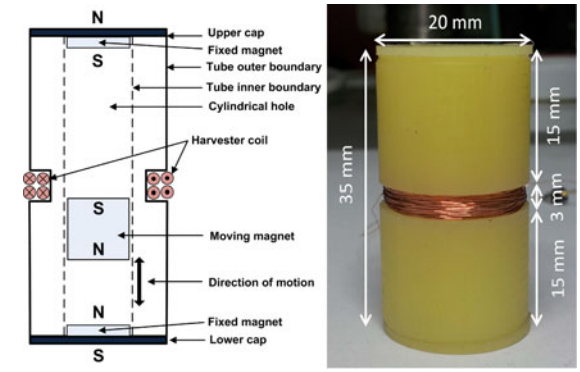

Fig. 10. Fabricated EM energy harvester prototype.

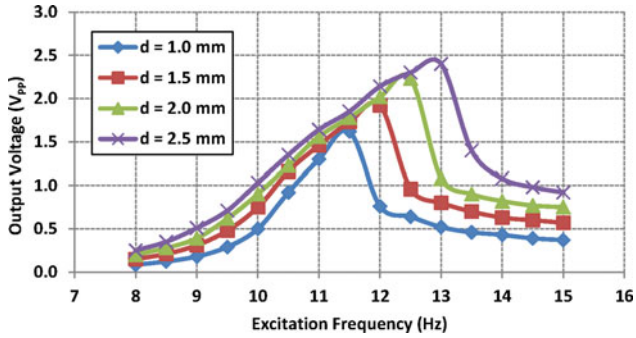

Fig. 11. Peak-to-peak value of the harvested ac voltage versus the vibration frequency at different peak-to-peak vibration displacements.

B. Electromagnetic Energy Harvester Module

A modified version of a low-cost EM energy harvester module [17] has been designed and fabricated, as depicted in Fig. 10. The cylindrical package contains two fixed magnets (5.3 mm $\times$ 5.3 mm $\times$ 0.5 mm) at upper and bottom caps, and a magnet (7.5 mm $\times$ 7.5 mm $\times$ 7.5 mm) suspended in the air inside the tube with the magnetic field developed by the fixed magnets. A pick-up coil is wound around the designated cavity on the tube. When vibration is applied along the tube axis, the fixed magnet moves and induces voltage across the coil according to Faraday's law. The energy harvester has 5.5 and 20 mm inner and outer diameters, respectively. Length of the prototype is 35 mm. The harvester coil wounded around the tube has 500 turns and has 180 Ω internal resistance. The overall volume of the harvester is roughly 1.5 times that of an AA battery.

Fig. 11 presents the peak-to-peak output voltage of the fabricated in-house EM energy harvester at different vibration amplitudes, within a frequency range of 8–15 Hz, at open-load conditions. The results show that resonant frequency changes between 11.5 and 13 Hz for 1–2.5 mm peak-to-peak vibration amplitudes. The vibration frequency has been chosen as 10 Hz for the rest of the tests to observe the low-voltage and low-vibration performance of the circuit.

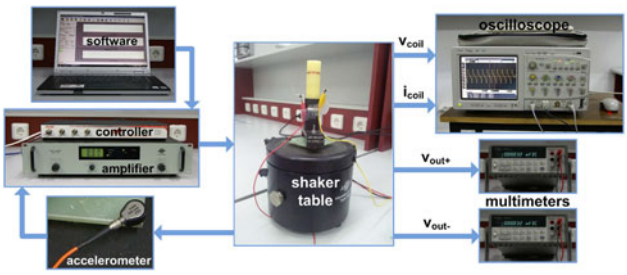

Fig. 12. Test setup and equipment.

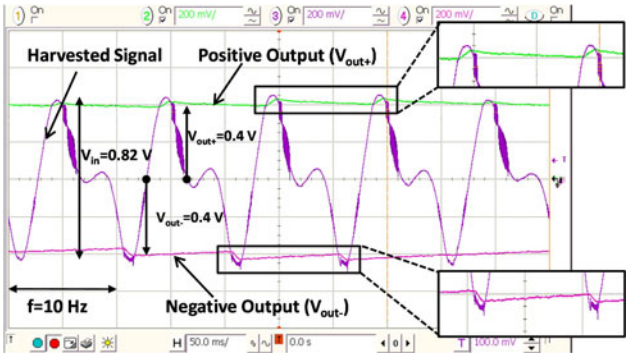

Fig. 13. Input ac voltage coming from the EM energy harvester for 0.5 g peak acceleration, the positive and negative output dc voltages of the ac/dc doubler.

C. Test Results of the Interface Electronics

The energy harvester module was excited in the acceleration range of 0.4 g to 0.6 g and at 10 Hz vibration frequency. The experimental setup is depicted in Fig. 12. The shaker table vibrates using a closed-loop accelerometer control. Instantaneous ac input voltage $V_{\rm in}\,(t)$ (output of the EM harvester) to the circuit was measured with an oscilloscope, and a sense resistor and an amplifier were used to monitor the ac input current $I_{\rm in}(t)$. The expression of the input power is given by

$$P_{\rm in} = \frac{1}{T}\int_0^T V_{\rm in}(t) I_{\rm in}(t) dt \tag{3}$$

where $T(=1/f)$ is one period of input voltage and t is the time. The dual-rail output voltage of the rectifier was measured with two multimeters. The load current and the output power were calculated according to (4) and (5), respectively

$$I_{\rm out} = \frac{V_{\rm out}}{R_L} = \frac{V_{\rm out+} - V_{\rm out-}}{R_L} \tag{4}$$

$$P_{\rm out} = I_{\rm out} \times V_{\rm out} = I_{\rm out} \times (V_{\rm out+} - V_{\rm out-}). \tag{5}$$

The power conversion efficiency η was defined as the ratio of the output power to the harvested input power

$$\eta\ (\%) = \frac{P_{\rm out}}{P_{\rm in}} \times 100. \tag{6}$$

Fig. 13 shows the EM energy harvester output and the rectified voltages of the active rectifier circuit for 10 Hz vibration frequency with 2.5 mm peak-to-peak amplitude corresponding to 0.5g peak acceleration. The output storage capacitors were chosen as 47 μF. The circuit generates a dc output ($V_{\rm out+} - V_{\rm out-}$) close to the peak-to-peak value of the input. The harvested peak-to-peak voltage of 0.82 V results in a rectified output voltage of 0.80 V. The voltage drop of about 20 mV is considerably lower than what can be achieved in traditional designs using passive diodes.

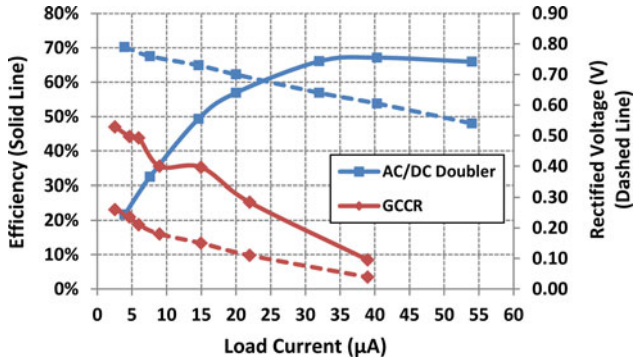

Fig. 14. Output dc voltage and efficiency of the ac/dc doubler and the GCCR circuits versus the load current for 10 Hz input frequency, 2.5 mm peak-to-peak vibration amplitude, and 0.5g external acceleration profile.

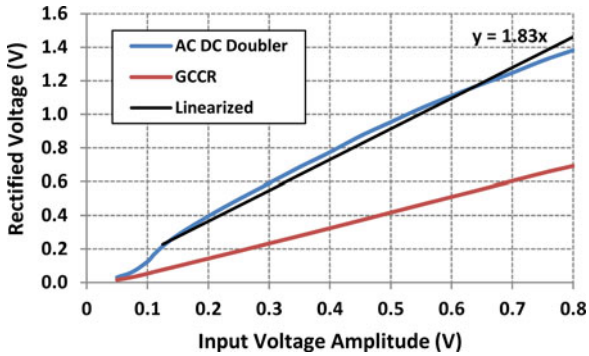

Fig. 15. Output dc voltage versus the input voltage peak at 10 Hz input frequency and open-load condition. The circuit is functional for input peak voltages higher than 125 mV.

The peak value of the harvested ac voltage is different from the one presented at Fig. 11. The difference at the peak value of the harvested voltage is a result of the difference in the resistance seen by the harvester for different experiments. The harvested voltage presented in Fig. 11 is measured by using an oscilloscope, which has an input resistance of 2.2 MΩ. However, in the results presented in this section, the energy harvester is connected to the interface circuit where the input resistance is around 4 kΩ, which leads to a decrease in the peak-to-peak value of the measured ac waveform of the harvested voltage.

Fig. 14 presents the efficiency and the output voltage comparisons of the ac/dc doubler and GCCR circuits with varying load. The output voltage of the ac/dc doubler is three times larger than that of the GCCR for the same harvester prototype excited with the same vibration conditions as mentioned earlier. Although the GCCR circuit has higher efficiency at small loads, the ac/dc doubler has significant advantage for applications with a higher output current demand and has more than two times better efficiency for load currents larger than 20 μA.

The input was next fed from a signal generator for the precise control of the ac amplitude. As depicted in Fig. 15, with 10 Hz input frequency, the ac/dc doubler provides about two times larger dc output compared to GCCR circuit at open-load

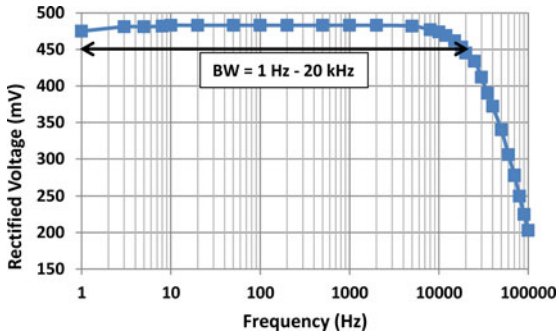

Fig. 16. Change of the rectified dc voltage of the proposed ac/dc doubler circuit with respect to the excitation frequency for 0.25 V input peak voltage.

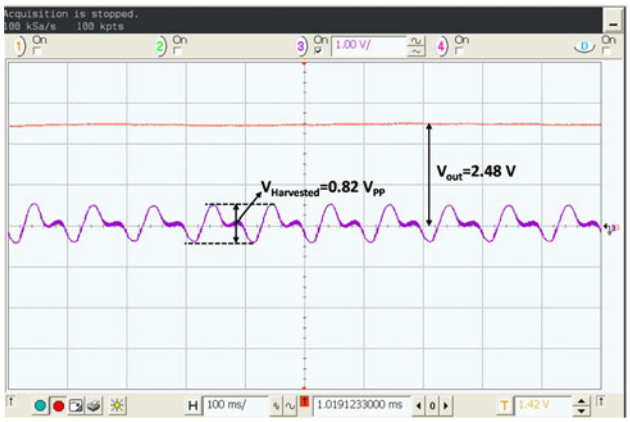

Fig. 17. Harvested ac voltage and output of the unregulated system for 10 Hz frequency, 2.5 mm peak-to-peak vibration amplitude, and 0.5 g acceleration.

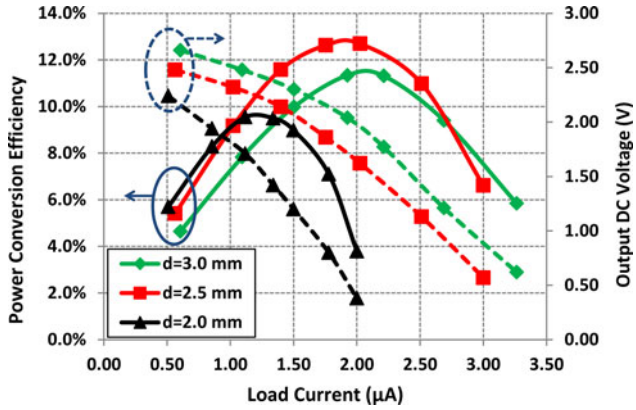

Fig. 18. Output dc voltage and power conversion efficiency of the overall circuit versus the load current for 10 Hz input frequency and 2, 2.5, and 3 mm peak-to-peak vibration amplitudes.

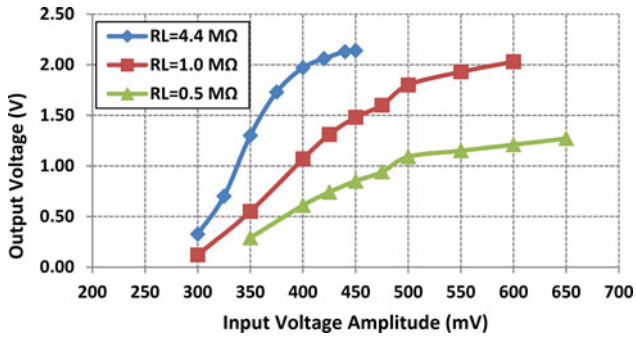

Fig. 19. Output dc voltage of the designed interface circuit versus the input peak voltage for 10 Hz input frequency and 0.5, 1, and 4.4 MΩ load resistance conditions.

conditions. Furthermore, it is observed that the ac/dc doubler is functional for input peak voltages as low as 125 mV, which is nearly impossible to obtain with traditional passive structures. The circuit functionality threshold is defined as the minimum input peak voltage for which a step-up ratio more than 1.70 is observed at the output. The step-up ratio of the circuit is obtained as 1.83, when the output is line fitted for input voltages between 125 and 800 mV.

Fig. 16 shows the change in the rectified dc voltage of the proposed ac/dc doubler with respect to the excitation frequency for 0.25 V input peak voltage and 47 μF storage capacitor. The output voltage starts to decrease after 5 kHz, and drops by about 10% at 20 kHz due to the limited bandwidth of the low-power comparators in the active rectifier.

Fig. 17 shows the harvested ac signal and output of the full interface, including the dc–dc step up, for 10 Hz frequency, 2.5 mm peak-to-peak vibration amplitude and 0.5g acceleration condition. The circuit generates 2.48 V dc output for 4.4 MΩ load resistance and 1 μF load capacitance. Voltage drop at the rectifier circuit, dc/dc charge-pump losses, and the finite-load resistance result in an output voltage lower than the ideal value of 3.3 V for 0.82 V ac input. Fig. 18 depicts the output voltage and the efficiency of the interface circuit for varying load current at 10 Hz vibration frequency and peak-to-peak vibration amplitudes of 2 mm (0.4g acceleration), 2.5 mm (0.5 g), and 3 mm (0.6 g). The storage capacitors of the rectifier circuit have been chosen as 47 μF, and 1 μF storage capacitor has been utilized at the interface output.

The circuit generates more than 1 V output voltage for load currents lower than 1.7, 2.6, and 2.9 μA with peak-to-peak vibration amplitudes of 2, 2.5, and 3 mm, respectively. The maximum efficiency of the circuit for the same vibration conditions is about 10%, 13%, and 11.5%, respectively. The maximum efficiency has been observed as designed, at 0.4 V input peak voltage, which occurs at 2.5 mm peak-to-peak vibration. Although efficiency of the overall system seems low around 12%, it is in the expected range for circuits with no magnetic components, considering low input voltage and high step-up ratio.

Fig. 19 presents change of the output dc voltage of the circuit for varying input peak voltages and different load resistances. A signal generator was used for these tests to precisely control the input signal. For input peak voltages larger than 0.4 V the circuit achieves more than 1 μW output power with 1 V dc voltage, showing that the circuit can be used as an interface for EM harvesters to power microsystems such as wireless temperature sensors. Variety of on-chip temperature sensors are presented in literature, which have power dissipation lower than 1 μW [26]–[28]. By integrating an ultra-low-power temperature sensor, a totally integrated and self-powered WSN can be implemented for environmental temperature monitoring.

Fig. 20 depicts the test chip layout micrograph. Table I shows the system specifications of the EM energy harvester prototype and the interface electronics. Table II presents the comparison

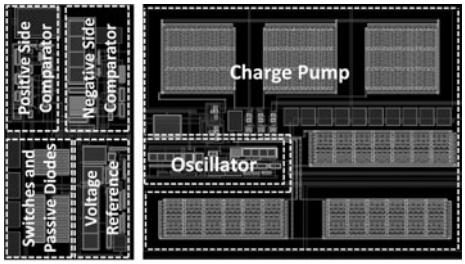

Fig. 20. Layout micrograph of the (a) ac/dc doubler and (b) dc/dc converter circuits.

TABLE I
PERFORMANCE SPECIFICATIONS OF THE DESIGNED SYSTEM

Moving magnet dimension		7.5 mm × 7.5 mm × 7.5 mm
Fixed magnets dimension		5.3 mm × 5.3 mm × 0.5 mm
Saturation magnetization		1.2 T
Number of coil turns		500
Coil resistance		180 Ω
IC technology		TSMC 90 nm CMOS
Vibration conditions		2.5 mm peak to peak,10 Hz, 0.5g
Harvested ac voltage		820 m$V_{\mathrm{peak\ to\ peak}}$
Rectifier stage	Max. DC output voltage	0.8 V at no load
	Max. power conversion efficiency	67% at 0.61 V, 40 μA load
	Min. operation voltage	125 mV peak
Overall interface circuit	Max. dc output voltage	2.48 V at no load
	Min. operation voltage (to reach 1 V output)	400 mV peak (at 1 MΩ load)

of the circuit with the state-of-the-art interface electronics for vibration-based energy harvesters.

IV. CONCLUSION

In this paper, a fully integrated and battery-free interface circuit for low-voltage and low-power EM energy harvesters has been presented. The designed interface circuit includes a novel and efficient active rectifier design and a fully integrated dc/dc converter that boosts the rectified voltage. The active rectifier uses an ac/dc doubler structure to benefit from the full cycle of the input signal. The comparators utilized at the active diodes are powered internally by another passive rectifier, and external power requirement is thus eliminated. Performance of the rectifier has been further improved by custom-designed comparators. The interface electronics has been designed and implemented using TSMC 90 nm CMOS technology and tested with an in-house EM energy harvester module operating at low input vibration frequencies (<10 Hz).

The rectifier stage operates with 67% efficiency while providing 0.61 V for 40 μA load. For the same conditions, the efficiency and the output voltage of the GCCR is lower than 10% and 0.1 V, respectively. The ac/dc doubler circuit functionally operates for input voltages higher than 125 mV peak, within a bandwidth of 1 Hz–20 kHz. When the rectifier stage is combined with the dc/dc converter block, the output voltage of the circuit is 2.48 V at 4.4 MΩ load resistance, when operated with an in-house EM harvester subjected to vibrations at 10 Hz, 2.5 mm peak-to-peak displacement with 0.5g acceleration. The circuit generates more than 1 V output voltage with 1 MΩ load resistance for input peak voltages higher than 0.4 V. The interface circuit can be used with low-frequency energy harvesters to supply 1 μW to a 1 V sensor.

TABLE II
COMPARISON OF THE PRESENTED WORK WITH THE STATE OF THE ART

Ref.	Circuit	Energy Harvester	Min V_{in} [V_{peak}]	$\mathrm{PCE}_{\mathrm{max}}{}^{*}$ [%]	Integration Level	IC Tech.
[16]	Rectifier	EM**	0.350	90	Off-the-shelf components	–
[17]		EM	0.200	81	IC + discrete components	0.35 μm
[18]	Rectifier + DC/DC converter	PZT	1.1	80	Off-the-shelf components	–
[20]		EM	1.5	–	Off-chip inductor	0.25 μm
[19]		EM	1	60	Off-chip inductor	0.5 μm
This work	Rectifier	EM	0.125	67	Fully integrated	90 nm
	Overall		0.400	13		

*Maximum power conversion efficiency.
**Electromagnetic.

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