A Cell-to-Cell Battery Equalizer With Zero-Current Switching and Zero-Voltage Gap Based on Quasi-Resonant *LC* Converter and Boost Converter

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***Abstract*—In conventional equalizers, the facts of bulky size and high cost are widespread. Particularly, the zero-switching loss and zero-voltage gap (ZVG) between cells are difficult to implement due to the high-frequency hard switching and the voltage drop across power devices. To overcome these difficulties, a direct cell-to-cell battery equalizer based on quasi-resonant *LC* converter (QRLCC) and boost dc–dc converter (BDDC) is proposed. The QRLCC is employed to gain zero-current switching, leading to a reduction of power losses. The BDDC is employed to enhance the equalization voltage gap for large balancing current and ZVG between cells. Moreover, through controlling the duty cycle of the BDDC, the topology can online adaptively regulate the equalization current according to the voltage difference, which not only effectively prevents overequalization but also abridges the overall balancing time. Instead of a dedicated equalizer for each cell, only one balancing converter is employed and shared by all cells, reducing the size and implementation cost. Simulation and experimental results show the proposed scheme exhibits outstanding balancing performance, and the energy conversion efficiency is higher than 98%. The validity of the proposed equalizer is further verified by a quantitative and systematic comparison with the existing active balancing methods.**

***Index Terms*—Battery management systems (BMSs), dc–dc power converters, electric vehicles (EVs), equalizers, lithium-ion batteries, zero-current switching (ZCS).**

I. INTRODUCTION

DUE to high energy density, low self-discharge rate, and no memory effect, lithium-ion batteries play important roles in high-power battery applications such as electric vehicles (EVs) and hybrid electric vehicles (HEVs). However, since one single cell has limited voltage and capacity, it is required to construct battery packs with hundreds or thousands of single cells connected in parallel and/or in series to meet the power and energy requirements of EVs or HEVs [1]–[6]. For example, the power battery pack in BMW's MINI E is composed of 5088 single cells (48 cells in parallel and 106 cells in series) [7]. Unfortunately, series-connected lithium-ion cells bring a key technical issue: Serious imbalance between cell voltages or state of charge (SOCs) is generated due to manufacturing inconsistencies and unique performance characteristics of individual cells in a typical pack. Furthermore, after a number of charge/discharge cycles, the imbalance tends to grow over time. This reduces enormously the available capacity of the battery pack and even leads to premature cells degradation and safety hazards (e.g., explosion or fire, etc.) due to the overcharge or overdischarge of cells. Consequently, equalization for series-connected batteries is essential to prevent these phenomena and to extend the life time of the battery pack. Obviously, as one key technology of the battery management system (BMS), the battery equalization for series-connected lithium-ion batteries has become a research focus.

Numerous balancing methods have been proposed and well summarized in [8]–[10]. As described in Fig. 1, these equalization methods can be classified into three main groups: the dissipative methods [8], [11]–[14], the nondissipative methods [15]–[41], and battery selection method [42], [43]. Furthermore, each group can be further divided into several categories. The tree trunk, the tree large branches, the tree branches, and the tree leaves in Fig. 1 represent the classification process of the equalization methods from coarse to fine. The ground represents the balancing strategies, which include the voltage-based, SOC-based, and pack capacity-based strategies [44], [45].

A review of the literature shows that the conventional equalizers are not suitable for lithium-ion batteries due to the following facts:

1) The size of the conventional equalizers is prone to be bulky because large amounts of transformers, MOSFETs, and floating drive circuits are necessary.
2) Lithium-ion battery offers a relatively flat open-circuit voltage (OCV) across a broad range of SOC from 20% to 80% [11], [36]. In other words, even though the SOC difference between cells is large, the corresponding voltage difference still remains small. Consequently, the equalization current of the conventional equalizers is very small. Particularly, the power devices would not conduct normally when the voltage difference between cells is less than the voltage drop across power devices.
3) Zero-voltage gap (ZVG) between cells cannot be achieved due to the voltage drop across the power devices.

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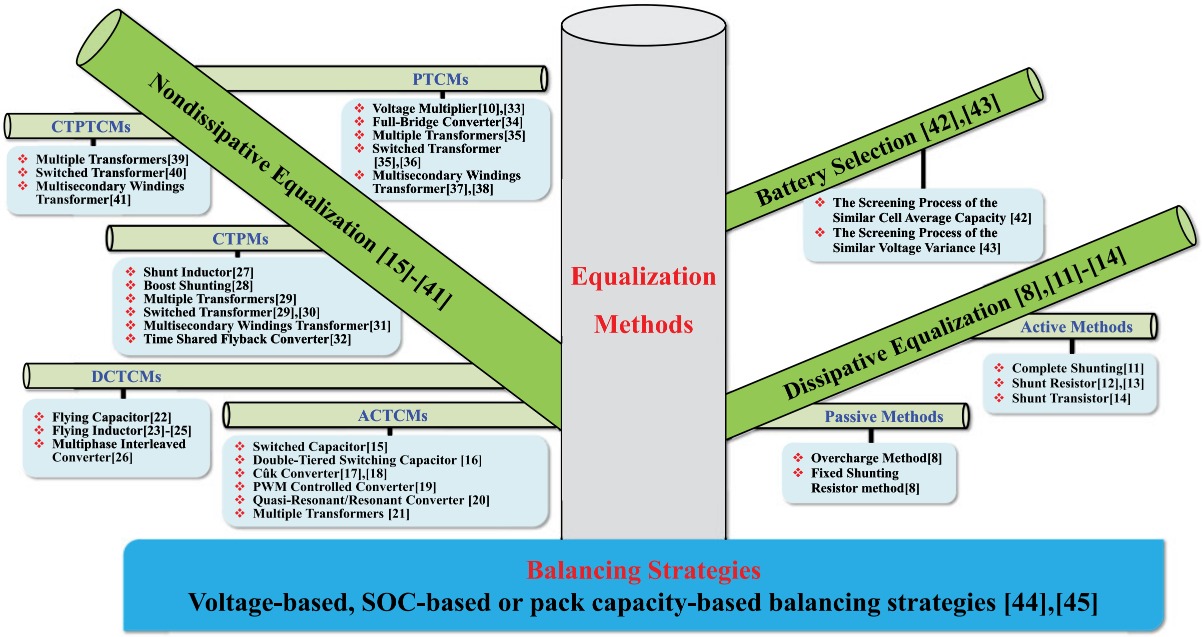


Fig. 1. Conceptual tree of equalization methods.

4) The switching loss is very high because the switches are conducted in high-frequency hard switching mode.

5) The equalization current, which depends on the voltage difference between cells, is difficult to regulate as needed, leading to a long equalization time or overequalization.

To solve these problems, a direct cell-to-cell equalizer based on quasi-resonant *LC* converter (QRLCC) and boost dc–dc converter (BDDC) is proposed. The QRLCC is employed to achieve ZCS, which results in a reduction of power losses and electromagnetic interference. The BDDC is employed to enhance the maximum cell voltage gap so that large equalization current and ZVG between cells can be achieved. Through controlling the duty cycle of the BDDC, the equalizer can online adaptively regulate the equalization current according to the cell voltage difference, which effectively prevents overequalization and abbreviates the overall balancing time. Moreover, this topology is able to transfer energy directly from the source cell at any position to the target one at any position in the pack, resulting in a great improvement of equalization speed and efficiency. In addition, since there are few MOSFETs, a small number of floating drive circuits and no transformers, and all the cells in the battery pack share one *LC* converter and one BDDC, the presented solution promises to solve the dilemma of bulky size and high cost.

This paper is organized as follows. State of the art in battery balancing methods is reviewed in Section II. In Section III, the design concept and the operation principle of the proposed system are analyzed, and a numerical approach for enhancing the equalization speed is proposed. Simulation and experimental results are presented in Sections IV and V, respectively. The comparative studies with the conventional equalizers are presented in Section VI.

II. REVIEW OF BATTERY-BALANCING METHODS

A. *Dissipative Equalization*

The dissipative equalization, also known as cell bypass method (CBM), employs a dissipative element connected as a shunt to bypass or drain extra energy from one cell. The dissipative equalization methods can be further divided into two categories, i.e., passive methods (no active control is used to balance) and active methods (external circuitry with active control is used to balance). The passive equalization methods include the overcharge method and the fixed shunting resistor method [8]. The active equalization methods include the complete shunting method [11], the shunt resistor method [12], [13], and the shunt transistor method [14]. Fig. 2(a) shows the charge and discharge processes of three cells connected in series with the dissipative balancing methods, where the three cells' initial SOCs and capacities are randomly given obeying the normal distribution. The cell voltage equalization with these methods is achieved by consuming the excess energy from the cells with higher voltage. Therefore, the available capacity of the battery pack in series with the dissipative methods is expressed as

$$C_{Bp} = \min_{j=0,1,\ldots,n-1} \{C_{B_j}\} \tag{1}$$

where C_{Bp} is the battery pack capacity in Ah. C_{B_j} is the cell capacity of the jth cell B_j in Ah, and *n* is the number of cells connected in series. The dissipative equalization is the cheapest one, and it is easily to be modularized and controlled. Owing to the individual shunt for each cell, it only takes one switching cycle to equalize the cell voltages to a same voltage level, showing excellent equalization speed. However, the excess energy is converted into heat rather than be stored, which leads to

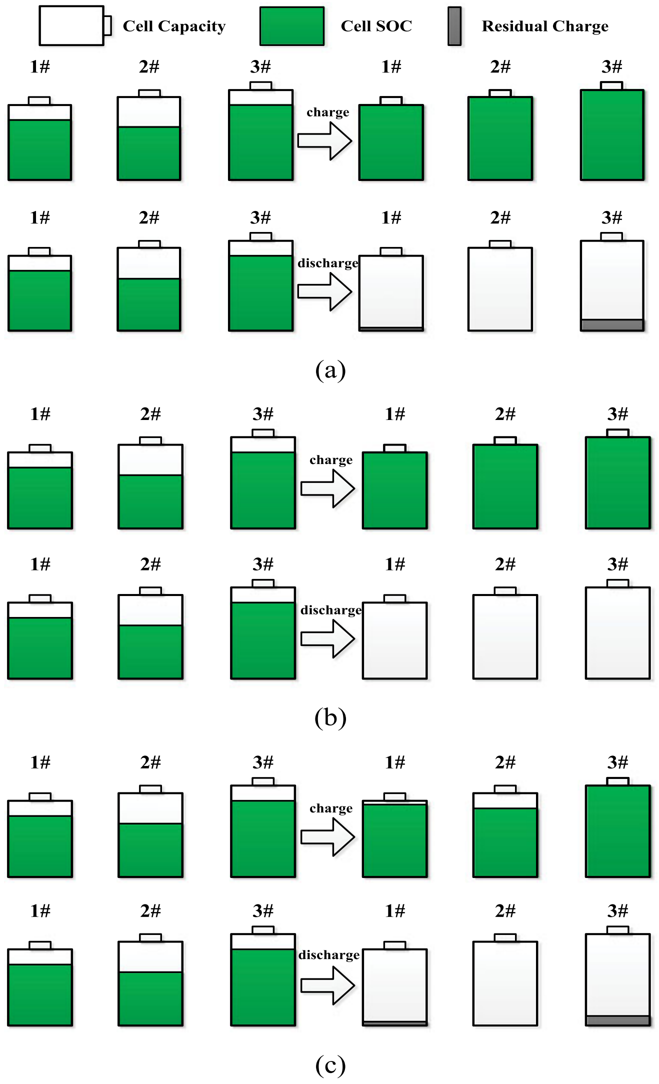


Fig. 2. Charge and discharge processes of three cells connected in series with different balancing methods. (a) Dissipative balancing methods. (b) Nondissipative balancing methods. (c) Battery selection method.

the energy waste and thermal management issues and reduces greatly the available capacity of battery packs.

B. Nondissipative Equalization

Nondissipative balancing methods employ nondissipative charge-shuttling elements or voltage/current converters to move energy from one cell to another or from one cell to the pack or from the pack to one cell. According to the energy flow, nondissipative balancing methods can be further classified into five groups as follows.

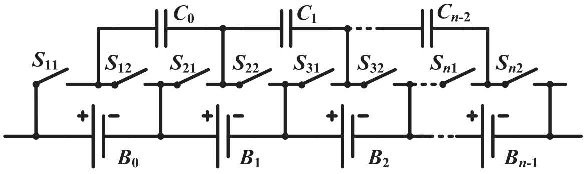


Fig. 3. Switched capacitor method.

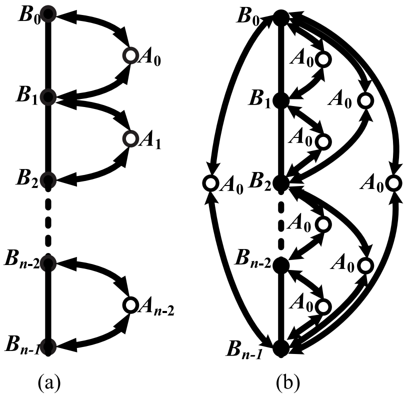


Fig. 4. Directed graph topologies of cell-to-cell balancing methods. (a) ACTCMs. (b) DCTCMs.

1) Adjacent Cell-to-Cell Methods (ACTCMs): As the name suggests, the charge is transferred between two adjacent cells with this method. The ACTCMs consist of five methods: the switched capacitor [15], the double-tiered switching capacitor [16], the cûk converter [17], [18], the pulse width modulation (PWM)-controlled converter [19], the quasi-resonant/resonant converter [20], and the multiple transformers [21]. Fig. 3 shows a typical ACTCM, i.e., the switched capacitor method, where one switched capacitor is implemented in every two adjacent cells and the equalizing path is controlled by the complementary switches S_{i1} and S_{i2} ($i = 1, 2, \ldots, n$). For example, when S_{11} and S_{21} are turned ON, while S_{12} and S_{22} are turned OFF, the capacitor C_0 is connected in parallel with B_0. On the contrary, when S_{11} and S_{21} are turned OFF, while S_{12} and S_{22} are turned ON, the capacitor C_0 is connected in parallel with B_1. Through these two states constantly switching, the energy exchange between any two adjacent cells is achieved. Fig. 4(a) further shows the directed graph topology of the ACTCMs, where A_0–A_{n-2} represent the individual cell equalizers, e.g., the switched capacitors C_i ($i = 0, 1, \ldots, n-2$) in Fig. 3. The charge is only transferred from one cell to an adjacent one through an individual cell equalizer with this method. It would take a large amount of time to transport charge from the source cell to the target one, particularly when they are on opposite ends of the pack. In addition, the charge would have to travel through all the cells and individual cell equalizers, and this results in a penalty for the balancing efficiency. Moreover, the ZVG between cells is difficult to obtain due to the voltage drop across the power devices. The outstanding advantages of this system are the modular design, the extremely low voltage stress, and the easy control.

2) Direct Cell-to-Cell Methods (DCTCMs): To overcome the disadvantages of the ACTCM, a DCTCM using a common equalizer is introduced. By using a common equalizer such as a capacitor, this method achieves the direct cell-to-cell charge transportation between any two cells in the battery stack. The DCTCMs consist of three methods: the flying capacitor [22], the flying inductor [23]–[25], and the multiphase interleaved

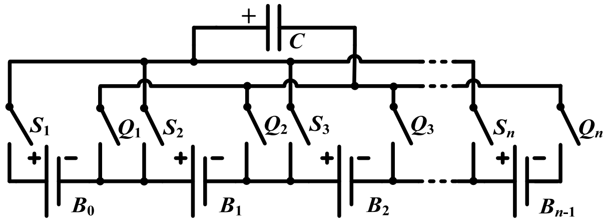


Fig. 5. Flying capacitor method.

converter [26]. Fig. 5 shows the flying capacitor method, where only one switched capacitor is shared by all cells and the equalizing path is controlled by n pairs of switches S_i and Q_i ($i =$ 1,2,. . . ,n). For example, when S_1 and Q_1 are turned ON, and others are turned OFF, the capacitor C is connected in parallel with B_0. When S_3 and Q_3 are turned ON, and others are turned OFF, the capacitor C is connected in parallel with B_2. Thus, the energy exchange between any cells at any position in the pack can be achieved. Fig. 4(b) further shows the directed graph topology of the DCTCMs, where A_0 represents the common cell equalizer, e.g., the switched capacitor C in Fig. 5. The charge can be transferred directly from the source cell at any position to the target one at any position in the pack with this method. Consequently, high efficiency can be obtained for high-power applications. Overequalization is prevented as the equalizing current is proportional to the voltage difference between the source cell and the target one, but this also leads to a slow balance. In addition, this method cannot obtain ZVG between cells due to the voltage drop across the power devices.

3) Cell-to-Pack Methods (CTPMs): The charge is transferred from the most charged cell to the pack. The CTPMs consist of six methods: the shunt inductor [27], the boost shunting [28], the multiple transformers [29], the switched transformer [29], [30], the multisecondary windings transformer [31], and the time-shared flyback converter [32]. When one cell is more charged than the other cells, and the other cells are balanced in a same voltage level, the CTPM has the best equalization performance. It only takes one switching cycle to complete the charge transportation. When one cell is less charged than the others while the others are balanced, this is the worst case for this method, which needs $n - 1$ switching cycles to complete the charge transportation. Therefore, the average switching cycle is n/2, showing poor equalization speed. When the target cell is balanced by the mean of discharge with this method, the cell also will be simultaneously charged through the battery pack. Therefore, the average conversion efficiency with this method is slightly lower than the one conversion efficiency when n is large. In addition, this method can obtain ZVG between cells but suffers from overequalization and high switching losses.

4) Pack-to-Cell Methods (PTCMs): The charge is transferred from the pack to the least charged cell in the battery pack. The PTCMs consist of five methods: the voltage multiplier [10], [33], the full-bridge converter [34], the multiple transformers [35], the switched transformer [35], [36], and the multisecondary windings transformer [37], [38]. When one cell is less charged than the other cells, and the other cells are balanced in a same voltage level, the PTCM has the best equalization performance. It only takes one switching cycle to complete the charge transportation. When one cell is more charged than the others while the others are balanced, this is the worst case for this method, which needs $n - 1$ switching cycles to complete the charge transportation. Therefore, the average switching cycle is n/2. The PTCMs have the same advantages and disadvantages as the CTPMs.

5) Cell-to-Pack-to-Cell Methods (CTPTCMs): These methods allow the cell-to-pack equalization in case a cell has a higher voltage than the others in the battery pack, and the pack-to-cell equalization in case a cell has a lower voltage than the others. The CTPTCMs consist of three methods: the bidirectional multiple transformers [39], the bidirectional switched transformer [40], and the bidirectional multisecondary windings transformer [41]. Compared with the CTPMs and the PTCMs, the CTPTCMs have higher equalization speed and average conversion efficiency at the cost of control complexity.

Obviously, nondissipative balancing methods are all active equalization ones. Fig. 2(b) shows the charge and discharge processes of three cells connected in series with the nondissipative methods. These methods seek to transfer efficiently energy from the strongest cell to the weakest one via different approaches until the cell voltages are equalized to a same level. Therefore, the available capacity of the battery pack in series with nondissipative balancing methods can be expressed as

$$C_{Bp} = \underset{j=0,1,\ldots,n-1}{\text{mean}} \{C_{B_j}\}. \tag{2}$$

C. Battery Selection

The battery selection, which builds up the battery pack by selecting the cells with similar properties, can be divided into two different screening processes to select the similar cells. In the first screening process [42], the cells with similar average capacity are selected by discharging at different current regimes. The second one [43] is applied to select the cells from the first process with the similar voltage variance under the pulse discharging/charging currents at different SOC points. By using the battery selection method, the series-connected battery string is not enough to remain balanced because the self-discharges of cells vary differently along their lifetime. It can only be useful in the case of complementing a balancing system. Fig. 2(c) shows the charge and discharge processes of three cells connected in series with this method. It can be observed that the battery pack capacity with this method is limited by the barrel theory also known as Liebig's law of the minimum [46]. Therefore, the available capacity of the battery pack in series with battery selection can be expressed as

$$\begin{aligned} C_{Bp} = \; & \min_{j=0,1,\ldots,n-1} \{Cr_{B_j}\} + \\ & \min_{j=0,1,\ldots,n-1} \{(1 - \mathrm{SOC_j}) * Cr_{B_j}\} \end{aligned} \tag{3}$$

where Cr_{B_j} and SOC_j are, respectively, the remaining cell capacity in Ah and the SOC of the $j\mathrm{th}$ cell B_j.

It can be summarized from the above discussion that the nondissipative equalization has higher available battery pack capacity and higher efficiency than the dissipative equalization

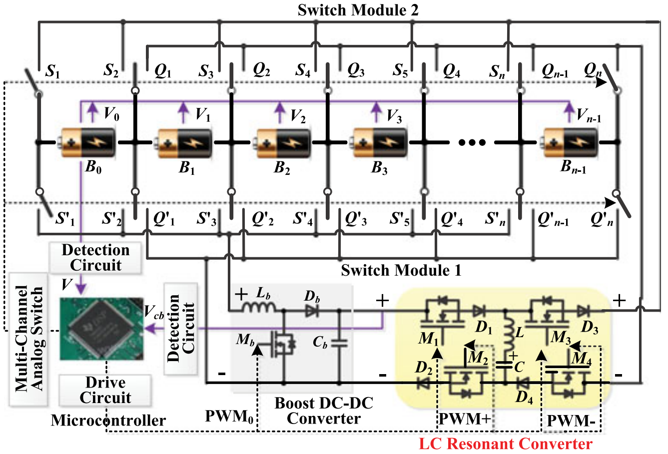
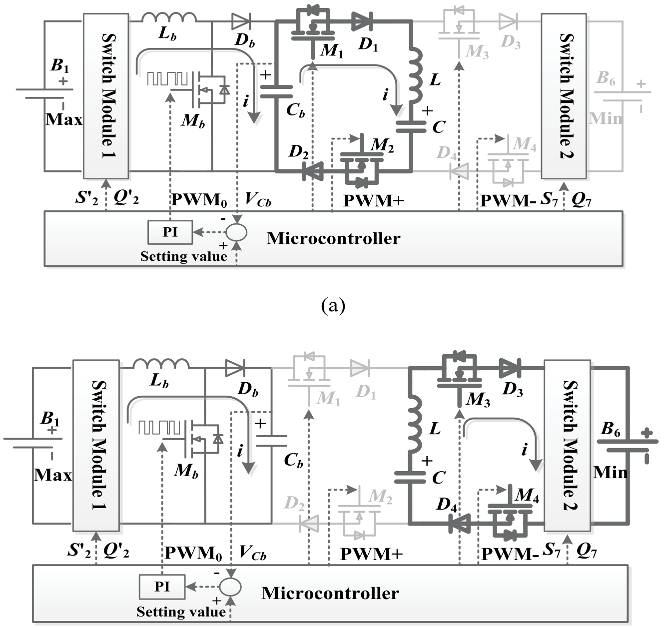


Fig. 6. System configuration of the proposed equalizer for n cells based on QRLCC and BDDC.



(a)

(b)

Fig. 7. Two consecutive working states of the proposed equalizer. (a) Working state I. (b) Working state II.

and the battery selection. Nevertheless, the existing nondissipative equalization methods feature bulky size and high implementation cost ubiquitously, because large amounts of transformers, capacitors, inductances, MOSFETs, and floating drive circuits are necessary. What is more, they also suffer from some other problems e.g., long equalization time, high switching loss, overequalization, etc. Therefore, a high-efficiency battery equalizer with ZCS and ZVG is highly desired for enhancing the available capacity and life cycle of the battery packs.

III. PROPOSED EQUALIZER SCHEME

A. Concept of the Proposed Equalizer

Fig. 6 shows the system configuration of the proposed equalizer for n battery cells, which consists of three parts, i.e., the QRLCC, the BDDC, and the selection switch modules. The QRLCC, as the core of the proposed equalizer, is made up of one *LC* converter, four MOSFET switches, and four diodes. The MOSFET switches are divided into two pairs (i.e., M_1, M_2 and M_3, M_4). They are controlled by a pair of complementary PWM pulses, enabling the QRLCC to operate alternatively between the state of charging and the state of discharging. The diodes are employed to isolate the cells to be equalized from the battery pack. The major role of the QRLCC is to achieve the energy transportation with ZCS. The BDDC, which is simply implemented by using a boost converter, can regulate the voltage of the source cell to a higher value in order to obtain large equalization current and ZVG between cells. Moreover, through controlling the duty cycle of the BDDC, the equalizer can online adaptively regulate the equalization current according to the cell voltage difference, which effectively prevents overequalization. The selection switch modules consist of $2n$ pairs of relays, through which the energy can be transferred from the cell with the highest voltage at any position to the one with the lowest voltage at any position in the stack, resulting in an improvement of the equalization speed and efficiency.

B. Operational Principle

In this paper, the equalization is achieved by directly interchanging energy between the source cell with the highest voltage and the target one with the lowest voltage in a battery pack. To realize this, a microcontroller with a voltage monitoring integrated circuit is employed. The microcontroller collects the voltage data to find out the source and target cells in real time. Then, the microcontroller drives the selection switch modules to connect the BDDC with the source cell and to link the QRLCC with the target cell. A PI controller is employed to control the output voltage of the BDDC so that the equalization current can be regulated according to the cell voltage difference for fast equalization and preventing overequalization. The equalization with two consecutive working states is shown in Fig. 7(a) and (b), respectively. Before describing the two states, the second battery B_1 is assumed to be overcharged, and the seventh battery B_6 is undercharged. Thus, the cell selection switches S'_2, Q'_2 and S_7, Q_7 are first turned ON before the operation of the BDDC. In the balancing process, the cell selection switches S'_2, Q'_2 and S_7, Q_7 are kept ON until the new generation of the source and target cells. The four MOSFET switches in the QRLCC are controlled by a pair of complementary PWM pulses, i.e., PWM+ and PWM−. To be specific, M_1 and M_2 are turned ON simultaneously in the first half of a switching cycle, while M_3 and M_4 are turned ON in the second half-cycle. Particularly, ZCS is achieved when the resonant frequency of the QRLCC is an integer multiple of the switching frequency. The multiple cycles of the oscillation in one switching cycle will lead to a small average equalization current. Thus, it is optimum to set the switching frequency equal to the resonant frequency.

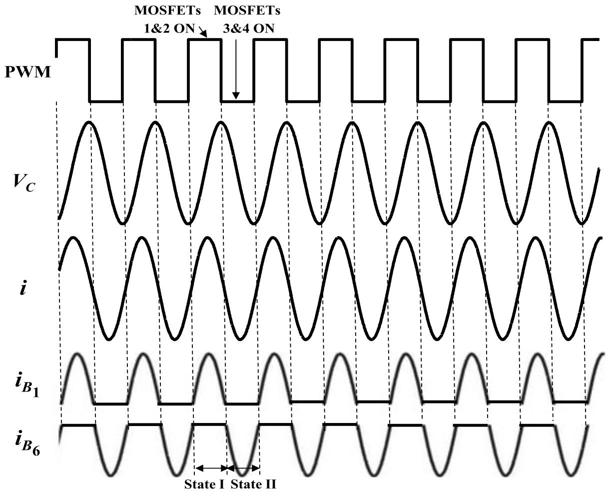


Fig. 8. Timing diagram representing energy transfer from B_1 to B_6. It is specified that the current flowing out of a cell is positive, and vice is negative.

1) Working state I: M_1, M_2 are turned ON, and M_3, M_4 are turned OFF. The QRLCC is connected in parallel with the BDDC through M_1, D_1 and M_2, D_2, as shown in Fig. 7(a). C_b, *L*, and *C* form a resonant loop, and the current path from B_1 is constructed. The capacitor *C* is charged by C_b. Then, the voltage across *C* V_c begins to increase. Since the output voltage of the BDDC is always regulated to a constant value and C_b is considerably larger than *C*, the output voltage of the BDDC can be seen as an ideal voltage source in a very short time. Thus, the current flowing into the QRLCC is equal to that flowing out of the cell B_1. Meanwhile, because of M_3 and M_4 maintaining OFF, B_6 acts as an open path, thus the charge current into B_6 is zero (see the state I in Fig. 8).

2) Working state II: M_1, M_2 are turned OFF, and M_3, M_4 are turned ON. The QRLCC is connected in parallel with B_6 through M_3, D_3 and M_4, D_4, as shown in Fig. 7(b). *L*, *C*, and B_6 form a resonant loop. The current path from the QRLCC into B_6 is constructed. B_6 is charged by the capacitor *C*. Then, V_c begins to decrease. Simultaneously, the BDDC acts as an open path, so the discharge current out of B_1 is zero (see the state II in Fig. 8).

C. Circuit Analysis

For a sake of simplicity, it is assumed that the equalization is carried out in the battery pack with two cells. The output voltage of the BDDC is regulated to a constant value, and the voltages of the pack cells can also be viewed as constant values in a very short time. Therefore, the proposed equalization circuit can be simplified as shown in Fig. 9, and the following notations are to be used.

1) R: the equivalent resistance of the QRLCC. For the working state I as shown in Fig. 7(a), R is the sum of the internal resistances of the *LC* converter and the on-resistances of MOSFETs M_1 and M_2. In terms of the working state II as shown in Fig. 7(b), R is the sum of the internal resistances of the *LC* converter and the on-resistances of MOSFETs M_3 and M_4. Generally speaking, the on-resistances of MOSFETs M_1–M_4 are considered to be equal. Therefore, the resistance *R* in Fig. 9 can be expressed as

$$R = R_{LC} + 2R_{\mathrm{DS(on)}} \tag{4}$$

where R_{LC} is the internal resistance of the *LC* converter. $R_{\mathrm{DS(on)}}$ is the static drain–source on resistance of a MOSFET switch.

2) T: the switching period of the MOSFET switches, satisfying

$$T = 2\pi\sqrt{LC}. \tag{5}$$

3) ω_0: the characteristic angular frequency, satisfying

$$\omega_0 = \frac{2\pi}{T} = \frac{1}{\sqrt{LC}}. \tag{6}$$

4) m: the harmonic number, and

$$m = \frac{\omega}{\omega_0} \tag{7}$$

where ω is the angular frequency.

5) $V_{\max}(t)$: the maximum cell voltage.

6) $V_{\min}(t)$: the minimum cell voltage, which can be approximate to a constant value in a switching period T.

7) V_{boost}: the output voltage of the BDDC, satisfying

$$V_{\mathrm{boost}} > V_{\max}(t). \tag{8}$$

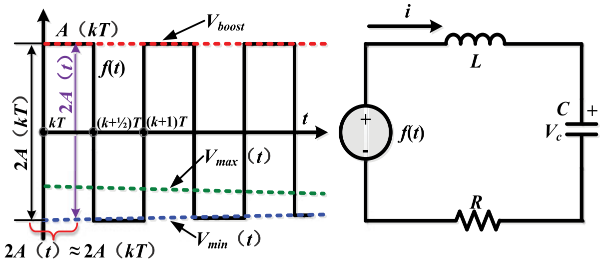


Fig. 9. Series resonant equivalent circuit of the proposed topology with the ac square wave power source.

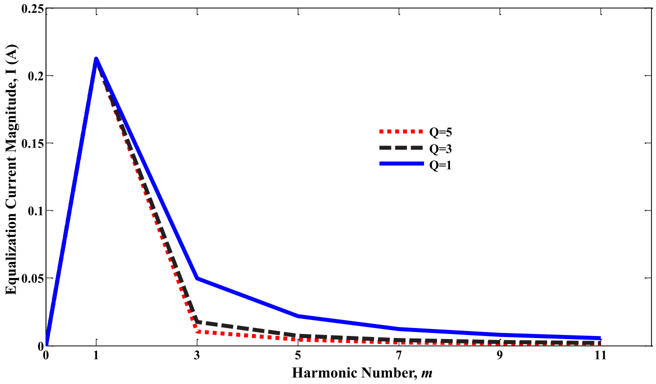


Fig. 10. Output current magnitudes of series-resonant circuit with different harmonic order m under the assumptions of $R = 0.3\ \Omega$ and $A(kT) = 0.1$ V.

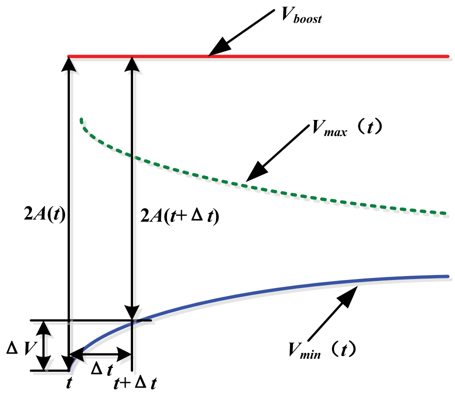


Fig. 11. Balancing process schematic diagram.

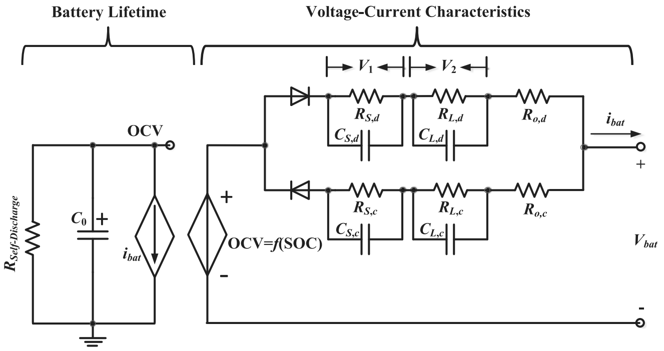


Fig. 12. Two-order *RC* equivalent circuit model of a battery cell. The *d* index is used for discharge, and *c* is used for charge.

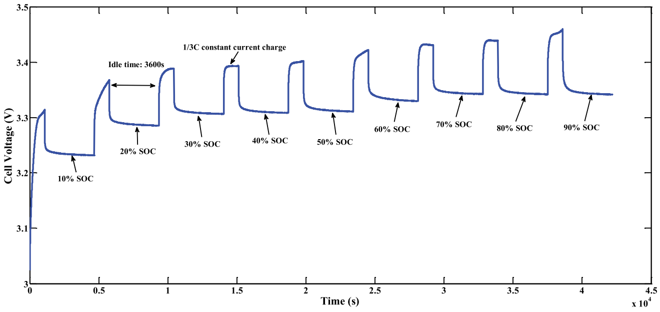
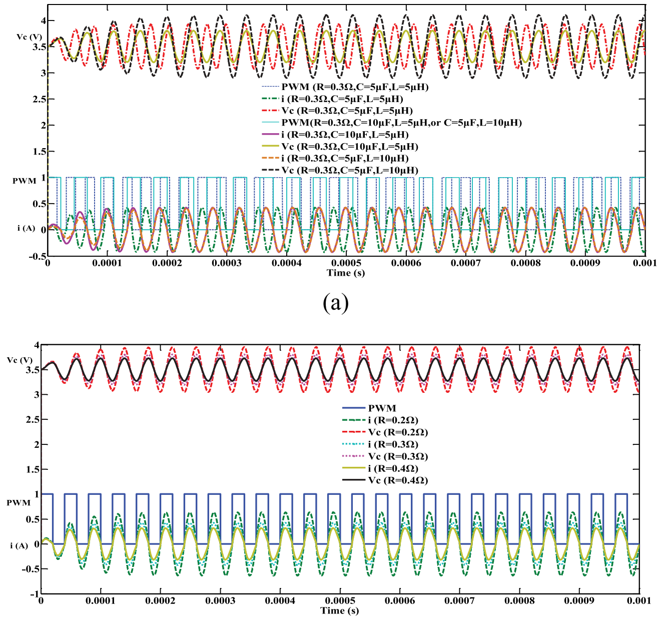


Fig. 13. Typical voltage response curve with pulse charge.

8) $f(t)$: The ac square wave input of the QRLCC, whose amplitude is denoted by $A(t)$. In our process, $f(t)$ can be expressed as

$$f(t) = \begin{cases} \dfrac{V_{\text{boost}} - V_{\min}(t)}{2} = A(t), \\ t \in \left(kT, \ \left(k + \frac{1}{2}\right) T\right) \\ \dfrac{V_{\min}(t) - V_{\text{boost}}}{2} = -A(t), \\ t \in \left(\left(k + \frac{1}{2}\right) T, (k+1)T\right) \end{cases} \tag{9}$$



(a)

(b)

Fig. 14. Simulation results of resonant currents and capacitor voltages under resonant state. (a) Simulation waveforms with $R = 0.3\ \Omega$ and different L, C values. (b) Simulation waveforms with $L = 5\ \mu$H, $C = 10\ \mu$F, and different R values.

where $k=[\frac{t}{T}]$ and $[\cdot]$ is a Gaussian function. The Fourier transform of $f(t)$ can be expressed as

$$\begin{aligned} f(t) = \ & a_0 + \sum_{m=1}^{\infty} a_m \cos\left(\frac{2\pi mt}{T}\right) \\ & + \sum_{m=1}^{\infty} b_m \sin\left(\frac{2\pi mt}{T}\right) \end{aligned} \tag{10}$$

where a_0, a_m, and b_m are determined by

$$a_0 = \frac{1}{T}\int_0^T f(t)dt \tag{11}$$

$$a_m = \frac{2}{T}\int_0^T f(t)\cos\frac{2\pi mt}{T}dt, \quad m = 1, 2, 3, \ldots \tag{12}$$

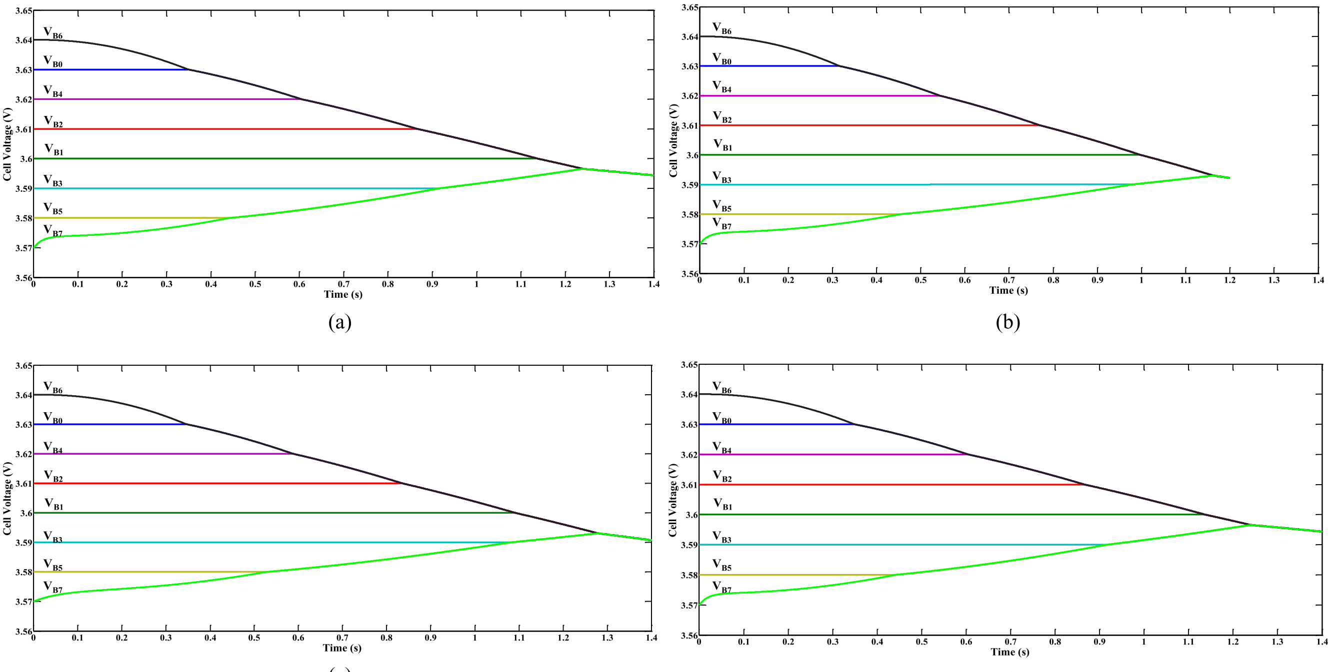
and

$$b_m = \frac{2}{T}\int_0^T f(t)\sin\frac{2\pi mt}{T}dt, \quad m = 0, 1, 2, \ldots. \tag{13}$$

As the period T in our process is very small, $A(t), t\in(kT,(k+\frac{1}{2})T))\cup((k+\frac{1}{2})T,(k+1)T)$ can be simplified as $A(kT)$ for a sake of simple calculation. With this knowledge in hard, the Fourier coefficient can be calculated as

$$a_m = 0, \quad m = 0, 1, 2, \ldots \tag{14}$$

$$b_m = (1^m - (-1)^m)\frac{2A(kT)}{m\pi}, \quad m = 0, 1, 2\ldots. \tag{15}$$



(a) (b)

(c) (d)

Fig. 15. Balancing simulation results of the proposed scheme for eight battery cells with different $V_{\rm boost}$, C, L, and R. (a) $V_{\rm boost} = 7.5$ V, $R = 0.01\ \Omega$, $C = 10\ \mu$F, and $L = 10\ \mu$H. (b) $V_{\rm boost} = 15$ V, $R = 0.01\ \Omega$, $C = 10\ \mu$F, and $L = 10\ \mu$H. (c) $V_{\rm boost} = 15$ V, $R = 0.1\ \Omega$, $C = 10\ \mu$F, and $L = 10\ \mu$H. (d) $V_{\rm boost} = 7.5$ V, $R = 0.01\ \Omega$, $C = 20\ \mu$F, and $L = 5\ \mu$H.

After determining all coefficients of (10), the series of *f*(*t*) $(kT < t < (k+1)T, t \neq (k+\frac{1}{2})T)$ can be rewritten as

$$f(t) \approx \frac{4A(kT)}{\pi}\left(\sin(\omega_0 t) + \frac{\sin(3\omega_0 t)}{3} + \frac{\sin(5\omega_0 t)}{5} + \ldots\right). \tag{16}$$

The input ac impedance of the series-resonant circuit shown in Fig. 9 can be expressed as

$$Z = R + j(\omega L - 1/\omega C) \tag{17}$$

From (16) and (17), the mth harmonic wave amplitude in the resonance current is shown as

$$I_m = \frac{4A(kT)}{m\pi R\sqrt{1+Q^2\left(m-\frac{1}{m}\right)^2}} \tag{18}$$

where *Q* is the quality factor, and

$$Q = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 C R}. \tag{19}$$

With (18), one can get the maximum of I_m, $m \in N$, i.e.,

$$I_1 = \frac{4A(kT)}{\pi R}. \tag{20}$$

It can be seen from (20) that I_1 is proportional to $A(kT)$, while is inversely proportional to the equivalent resistance R, but has no relationship with L or C values.

Under the reasonable assumptions of $R = 0.3\ \Omega$ and $A(kT) = 0.1$ V, I_m in (18) is represented in Fig. 10 for $Q = 1$, 3, and 5, respectively. Comparing I_1 with I_m ($m \neq 1$), if *Q* is large enough, the harmonic component in i is far less than the fundamental component with the increase of the harmonic order m. It follows that the current i in the QRLCC is very close to a sine wave and can be approximatively represented by

$$i \approx \frac{4A(t)}{\pi R}\sin\omega_0 t. \tag{21}$$

A reasonable simplification on the transferred charge Δq_T from one cell to another in one switching cycle can be obtained from (21), given by the following equation:

$$\Delta q_T \approx \int_0^{\frac{T}{2}} \frac{4A(t)}{\pi R}\sin\omega_0 t dt \approx \frac{8A(kT)\sqrt{LC}}{\pi R}. \tag{22}$$

Through dividing (22) by *T*, the transferred charge in unit time can be derived from

$$\frac{\Delta q}{\Delta t} = \frac{\Delta q_T}{T} = \frac{4A(kT)}{\pi^2 R} = \frac{I_1}{\pi} \tag{23}$$

where Δq is the transferred charge in the time period Δt. Equation (23) shows that the amplitude of the resonance current decides the balancing speed, which is not affected by L or C values.

The relationship between the cell voltage and SOC is piecewise linear [15], which can be given by the following equation:

$$\Delta V = \lambda \Delta \mathrm{SOC} = \lambda \frac{\Delta q}{C_{B,C}} = \frac{4\lambda A(kT)}{\pi^2 R \cdot C_{B,C}}\Delta t \tag{24}$$

where ΔV is the variation of the cell voltage according to the SOC variation ΔSOC within the time period Δt. λ is the proportionality coefficient between the voltage and SOC in one approximate linear segment, and λ can be viewed as a constant in the balancing process for relatively small SOC variation. $C_{B,C}$

represents the whole charge stored in the battery by converting nominal battery capacity in Ah to charge in Coulomb, and its value is defined as

$$C_{B,C} = 3600 \cdot C_{B,\text{Ah}} \cdot f_1(\text{Cyc}) \cdot f_2(\text{Temp}) \qquad (25)$$

where $C_{B,\text{Ah}}$ is the nominal capacity in Ah. f_1(Cyc) and f_2(Temp) are cycle number-dependent and temperature-dependent correction factors. In general, the cycle number can be viewed as a constant in the balancing process, and a thermostat is used to keep the battery temperature constant, so all battery parameters are independent of the cycle number and temperature, i.e., f_1(Cyc) and f_2(Temp) are set to 1.

Fig. 11 shows the balancing process schematic diagram. It can be seen that the variation of the minimum cell voltage ΔV in the time period Δt can be represented as

$$\begin{aligned} \Delta V &= 2A(t) - 2A(t+\Delta t) = -2\Delta A(t) \\ &= \frac{4\lambda A(t)}{\pi^2 R \cdot C_{B,C}} \Delta t \end{aligned} \qquad (26)$$

where $\Delta A(t)$ is the variation of ac square wave amplitude in the time period Δt.

By solving (26), the relationship between $A(t)$ and the equalization time t can be obtained as

$$A(t) = A(0) e^{-\frac{2\lambda}{\pi^2 R \cdot C_{B,C}} t} \qquad (27)$$

where $A(0)$ is the amplitude of ac square wave at the beginning of the balancing process.

From (27), the expression of the equalization time t can be represented as

$$\begin{aligned} t &= \frac{\pi^2 R \cdot C_{B,C}}{2\lambda} \ln \frac{A(0)}{A(t)} \\ &= \frac{\pi^2 R \cdot C_{B,C}}{2\lambda} \ln \frac{V_{\text{boost}} - V_{\min}(0)}{V_{\text{boost}} - V_{\min}(t)} \end{aligned} \qquad (28)$$

where $V_{\min}(0)$ is the initial value of the minimum cell voltage at the beginning of the balancing process.

As can be seen from (28), the equalization time t is proportional to R and $C_{B,C}$, and is inversely proportional to V_{boost} and λ, having no relationship with L or C values. The larger the value of R, the longer the equalization time t. Therefore, the components, such as MOSFET switches, diodes, inductances, and capacitances with low equivalent resistances, can be selected accordingly to satisfy the equalizer fine requirement.

IV. SIMULATION RESULT

A. Battery-Equivalent Circuit Model

Using the equivalent circuit model with two *RC* time constants shown in Fig. 12 is the best tradeoff between accuracy and complexity [47]. Therefore, this paper adopts the two-order *RC* circuit model for the proposed equalization system. This model comprises three parts: usable capacity (C_B), OCV, and transient response (*RC* networks) [48]–[51].

1) Usable Capacity: The battery usable capacity can be modeled by a large capacitor C_0 and a self-discharge resistor $R_{\text{Self-Discharge}}$. The self-discharge resistor is used to characterize the self-discharge energy losses when the battery is stored for a long time. Theoretically, $R_{\text{Self-Discharge}}$ is a function of SOC, temperature, and cycle number. However, it can be simplified as a large resistor, or even ignored in practical application.

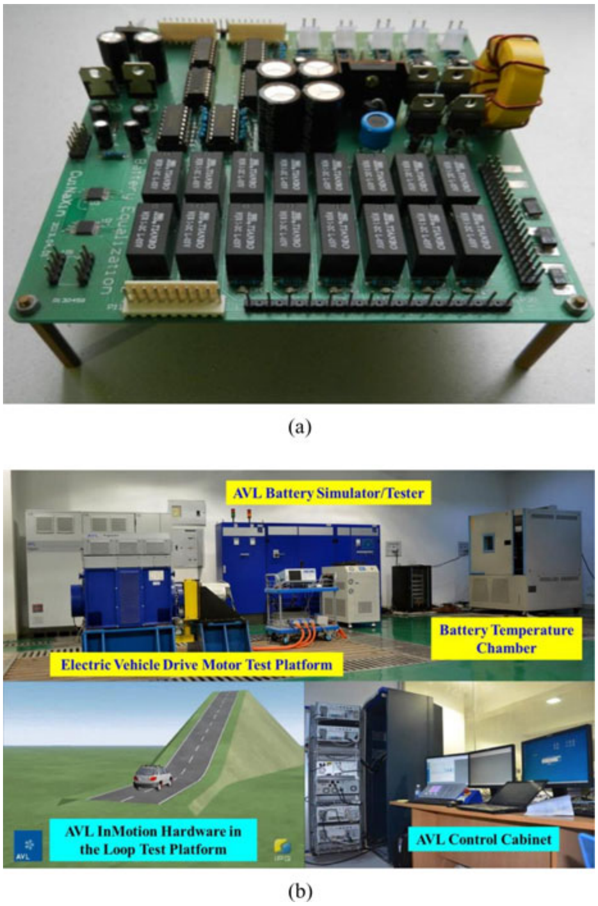


Fig. 16. Proposed eight-cell balancing system and experimental platforms. (a) Photograph of the implemented prototype. (b) Test platforms.

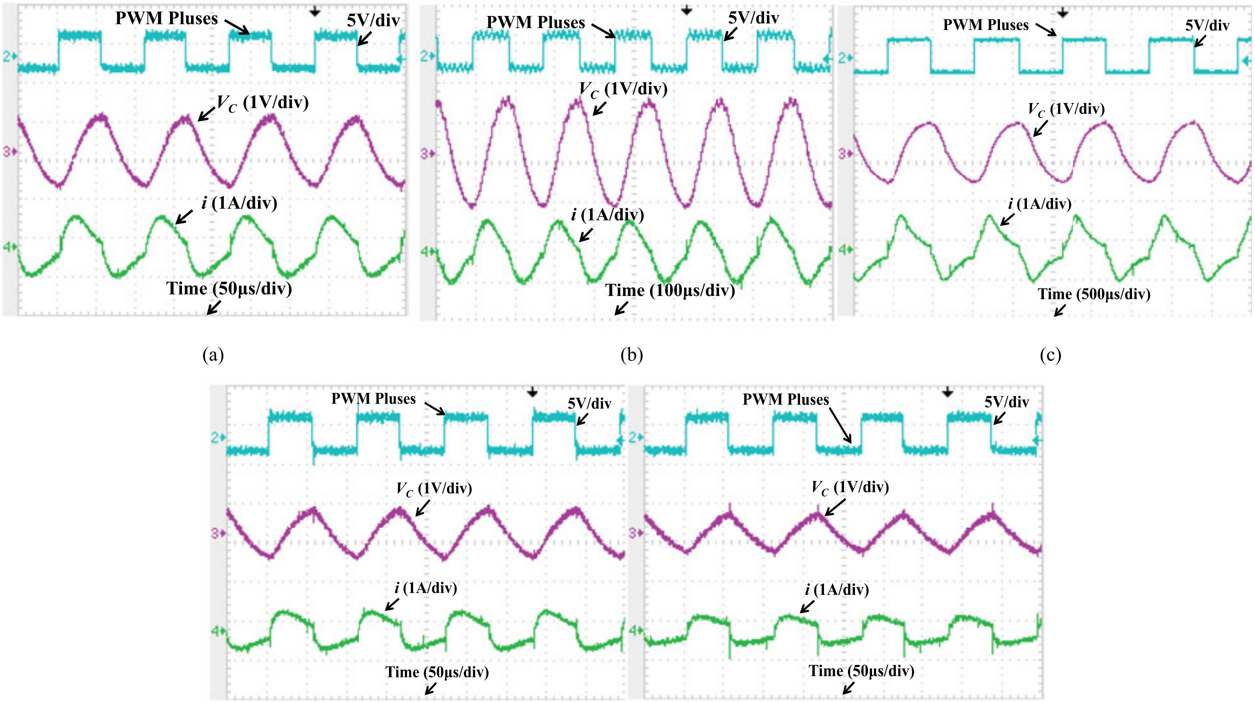
2) Open-Circuit Voltage: OCV, which changes depending on different capacity levels (SOCs), represents the potential difference between the two electrodes of battery in an open circuit. The nonlinear relationship between OCV and SOC, which can be represented by the voltage-controlled voltage source OCV = *f*(SOC), as shown in Fig. 12, is important to be included in the second-order *RC* circuit model. The OCVs at different SOCs can be obtained by measuring the battery terminal voltage after a long standing time. Through fitting the measured OCVs and the SOCs using a nonlinear function or lookup table, the nonlinear relationship between OCV and SOC is achieved for the second-order *RC* circuit model.

3) Transient Response: The electrical network consists of series resistor R_o and two *RC* parallel networks, which are composed of $R_{S,c}$, $C_{S,c}$ and $R_{L,c}$, $C_{L,c}$ for charge, and $R_{S,d}$, $C_{S,d}$ and $R_{L,d}$, $C_{L,d}$ for discharge. R_o determines the instantaneous voltage drop of the step response and the ohmic losses related to the physical nature of the electrodes and the electrolyte. The two *RC* networks determine the short-time and long-time constants

TABLE I
COMPONENT VALUES USED FOR THE PROTOTYPE

Parameters			Value
Equalizer	The BDDC	MOSFET, M_b	80NF70, $R^1_{\mathrm{DS(on)}}$ ≤0.0098 Ω
		Diode, D_b	IN5819, $V_F^2 = 0.6$ V
		Inductance, L_b	100 μH
		Capacitance, C_b	4700 μF
	The QRLCC	MOSFETs, M_1–M_4	80NF70, $R^1_{\mathrm{DS(on)}} \leq 0.0098\Omega$
		Diodes, D_1–D_4	IN5819, $V_F^2 = 0.6$ V
		Inductances, L	(9.5 μH, 0.010 Ω), (50.3 μH, 0.088 Ω), (200.8 μH, 0.040 Ω)
		Capacitances, C	(10.9 μF, 0.288 Ω), (51.2 μF, 0.106 Ω), (93.6 μF, 0.158 Ω)
	The Switch Module	(S_1, Q_1)–(S_n, Q_n), (S'_1, Q'_1)–(S'_n, Q'_n)	HJR 1-2C L-05V
Battery Pack	B_0–B_{n-1}		$LiFePO_4$, IFR26650, 6.2 Ah

1 $R_{\mathrm{DS(on)}}$. Static drain–source on resistance.
2 V_F. Forward voltage.



(a) (b) (c)

(d) (e)

Fig. 17. Experimental waveforms of resonant current i and capacitor voltage V_C with various L, C, and R values. (a) $C = 10.9$ μF, $L = 9.5$ μH, and $R = 0.317$ Ω. (b) $C = 9.5$ μF, $L = 50.3$ μH, and $R = 0.395$ Ω. (c) $C = 93.6$ μF, $L = 200.8$ μH, and $R = 0.217$ Ω. (d) $C = 10.9$ μF, $L = 9.5$ μH, and $R = 1.397$ Ω. (e) $C = 10.9$ μF, $L = 9.5$ μH, and $R = 2.407$ Ω.

of the step response, which represents the effects of the double-layer capacity and the diffusion phenomenon in the electrolyte, respectively.

To extract all the parameters in the second-order *RC* model at various SOC points, two experimental procedures, i.e., the pulse charge shown in Fig. 13 and the pulse discharge, need to be designed to measure the voltages and currents of cells at various SOC points. By using the measured data, the parameters of the second-order *RC* circuit model can be identified based on the nonlinear least-squares method, which can minimize the error between the experimental results and the model outputs.

B. Simulation Analyses

In order to facilitate analyses, a PSpice simulation of the QRLCC is performed for a battery stack with two cells, whose initial voltages are set as 3.6 and 3.4 V, respectively. The switching period for the QRLCC is determined by (5), and the duty ratio is set as 0.5.

Fig. 14 show the simulation results of resonant currents and capacitor voltages with different L, C, and R values. We observe that the resonant current i is sinusoidal. The capacitor voltage V_c is also a sinusoidal waveform lagging 90° phase from the resonant current i, and the peak value of V_c will occur at zero-crossing point of the resonant current. The MOSFETs are switched at the near-zero-current state, thus reducing switching losses.

Fig. 14(a) shows the simulation results of resonant currents and capacitor voltages under the conditions of $R = 0.3\ \Omega$ and different L, C values, which are set as $L = 5\ \mu$H, $C = 5\ \mu$F, or $L = 5\ \mu$H, $C = 10\ \mu$F, or L=10 μH, $C = 10\ \mu$F, respectively. We can observe that the resonant current magnitude remains invariant even though L and C values are changed. This verifies (20) in which the magnitude of the resonant current is not affected by L or C values. However, the capacitor voltage oscillation amplitude increases with L/C ratio increasing.

Fig. 14(b) shows the simulation waveforms with $L = 5\ \mu$H, $C = 10\ \mu$F, and different R values, which are set as 0.2, 0.3, or 0.4 Ω, respectively. We can observe that when the equivalent resistance R changes from 0.2 to 0.3 Ω and then to 0.4 Ω, the oscillation amplitudes of the resonant current and capacitor voltage become smaller every time. This fact is in accord with (20) in which the magnitude of the resonant current is inversely proportional to the equivalent resistance R. Consequently, the choice of MOSFET switches, diodes, inductances, and capacitances with different equivalent resistances will affect the balancing settling time.

Fig. 15 shows the balancing simulation results of the proposed scheme for eight battery cells with different V_{boost}, C, L, and R values. The initial voltages of the eight battery cells are set as 3.63, 3.60, 3.61, 3.59, 3.62, 3.58, 3.64, and 3.57 V, respectively. Fig. 15(a) and(b) shows that the equalization time gets shorter with a higher V_{boost}. Fig. 15(b) and (c) shows that the larger R results in a longer equalization time. Fig. 15(a) and (d) shows that the variations of L and C value have less effect on the equalization time when R and V_{boost} remain the same.

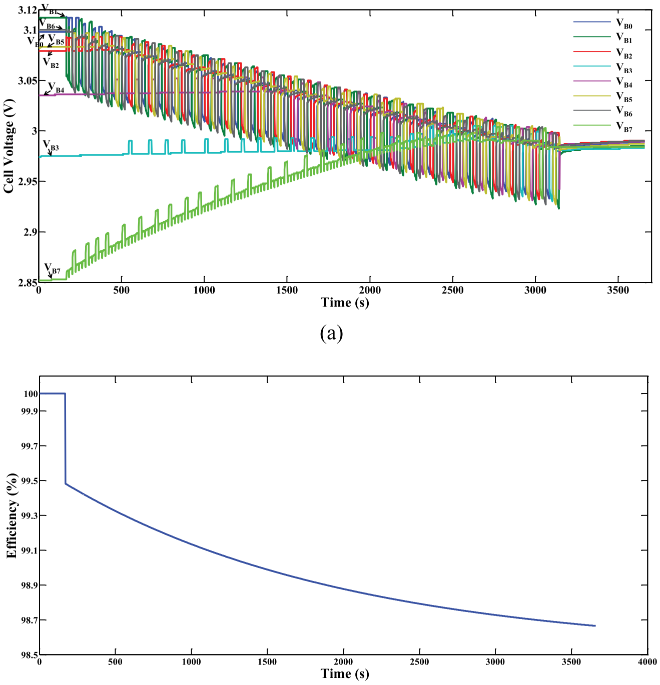
V. Experimental Results

In order to verify the operation principles and to show the balancing performance of the proposed equalizer, a prototype of eight lithium-ion cells, as shown in Fig. 16(a), is implemented and tested. The battery tests, e.g., the constant-current charge/discharge and Urban Dynamometer Driving Schedule (UDDS) test cycles, can be achieved with the AVL test platforms, as shown in Fig. 16(b). It mainly includes the AVL battery simulator/tester, the EV drive motor test platform, and the AVL InMotion hardware in the loop test platform. The InMotion hardware in the loop test platform can simulate well enough the characteristics of EVs and the real-road conditions.

Table I summarizes the parameters of the QRLCC, the BDDC, and the selection switch modules in Fig. 6. The inductances, capacitances, and resistances in Table I are measured by an Agilent 4263B LCR Meter. The cell voltages are monitored by LTC6802-1 (made by Linear Technology) and are recorded every second.

A. Experimental Waveforms of Resonant Current and Capacitor Voltage

Fig. 17 shows the experimental waveforms of resonant current i and capacitor voltage V_c with various L, C, and R values, where the minimum cell voltage $V_{\min}$ and the output voltage of the BDDC V_{boost} are set to 3.343 and 7.5 V, respectively. We can observe clearly from the results that the resonant current i and the capacitor voltage V_c are sinusoidal, and the peak value of the capacitor voltage V_c occurs at zero-crossing point of the resonant current. The MOSFET switches are turned ON and OFF at near zero current state, thus effectively reducing the switching losses. We can observe from Fig. 17(a)–(c) that if the influence of different L, C values resulting in different equivalent resistances can be ignored, the amplitudes of the resonant current can be considered to be essentially consensus, and this verifies that the balancing current amplitude has no relationship with L or C values. Fig. 17(a), (d), and (e) shows that when the equivalent resistor R in the resonant converter is changed from 0.317 to 1.397 Ω and then to 2.407 Ω, the magnitude of the resonant current changes from 0.86 to 0.64 A and then to 0.48 A. This demonstates the balancing current amplitude is inversely proportional to the equivalent resistance R. Therefore, the experimental results are the same as the theoretical analyses and simulations.



(a)

(b)

Fig. 18. Static equalization for eight lithium-ion cells during an idle period. (a) Eight-cell voltage trajectories. (b) Energy conversion efficiency during an idle period.

B. Static Equalization

In order to evaluate the consistency of the cells, the consistency coefficient ρ is introduced by

$$\rho = \sigma / \overline{V} \tag{29}$$

where $\overline{V}$ and σ are the average value and the standard deviation of cell voltages, respectively.

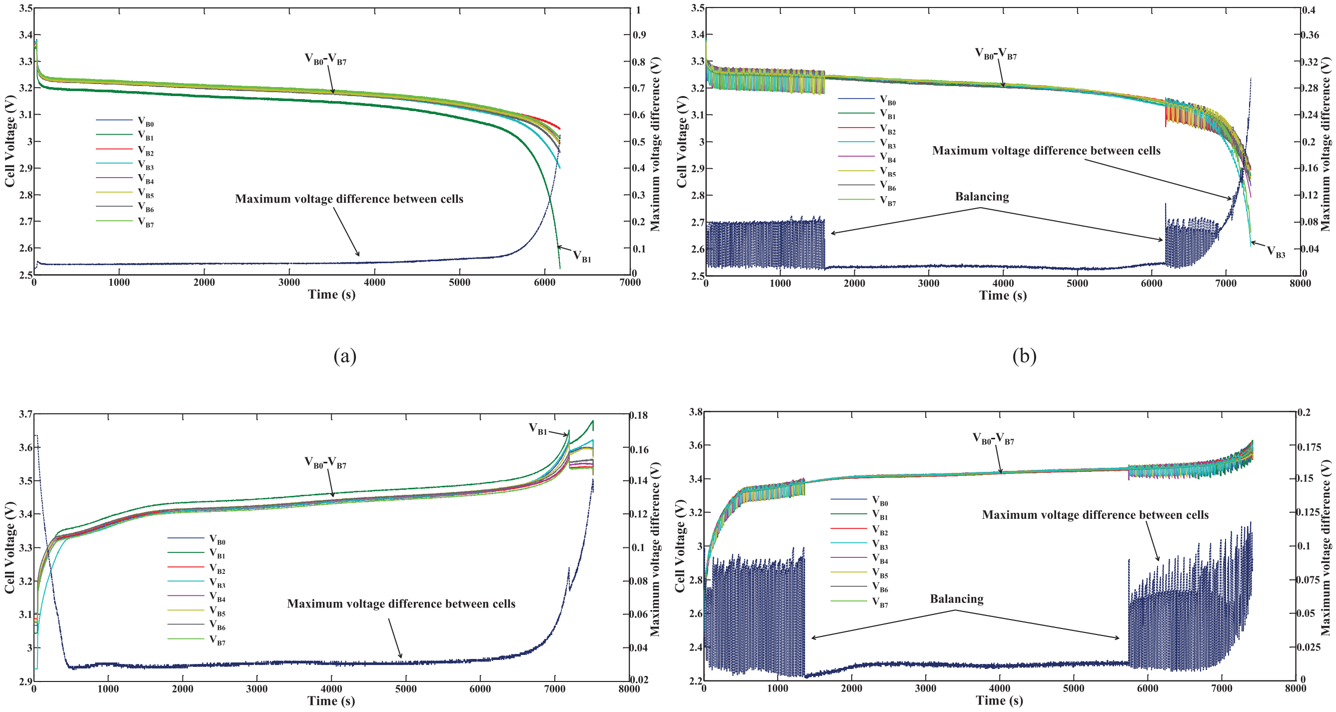


Fig. 19. Dynamic equalization during discharge and charge at a constant current of 0.5 C. (a) Discharge without voltage balancing. (b) Discharge with the proposed balancing. (c) Charge without voltage balancing. (d) Charge with the proposed balancing.

TABLE II
COMPARISON OF THE CONSISTENCY COEFFICIENT AND AVAILABLE PACK CAPACITY BETWEEN WITH AND WITHOUT BALANCING DURING CONSTANT-CURRENT DISCHARGE AND CHARGE

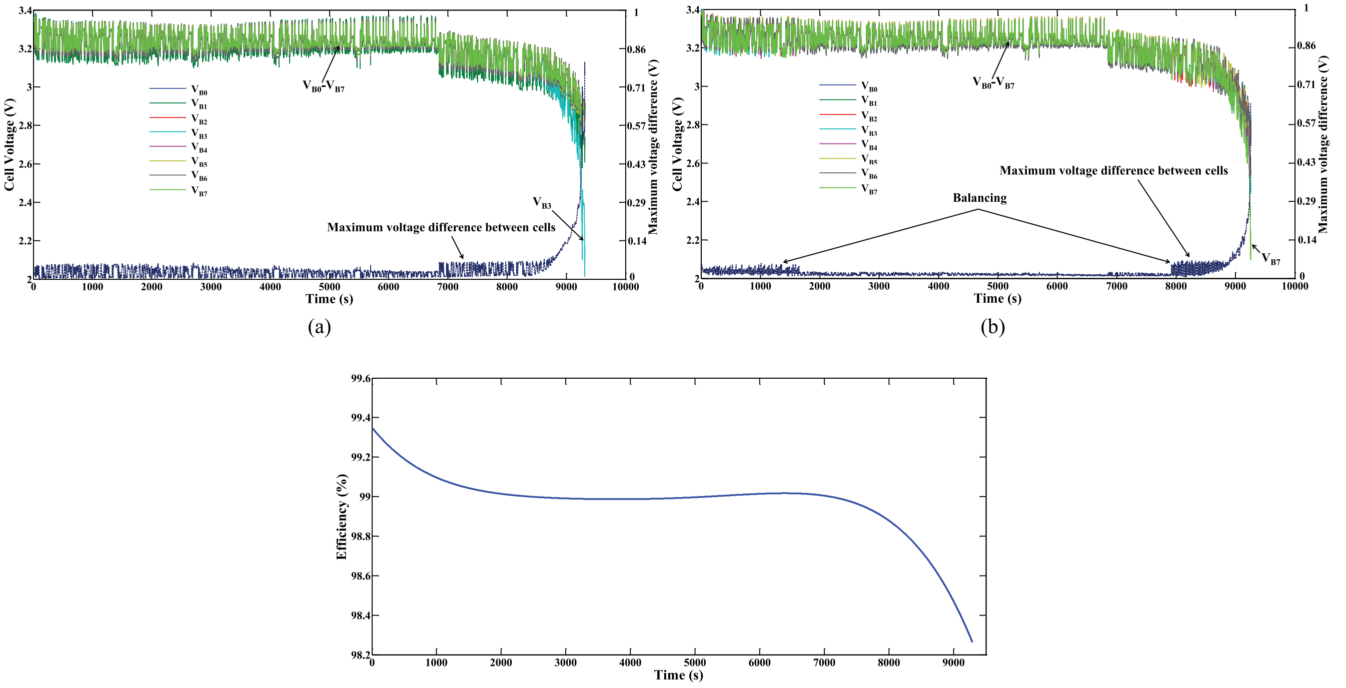
	Constant-Current Discharge		Constant-Current Charge	
Performance Indicators	Without Balancing	With Balancing	Without Balancing	With Balancing
ρ at 30% SOC	0.0156	0.0013	0.0024	0.0005
ρ at 70% SOC	0.0122	0.0014	0.0025	0.0013
Available Capacity	5.3 Ah	6.0 Ah	6.0 Ah	6.3 Ah

Fig. 18 presents the voltage equalization results of eight lithium-ion cells during an idle period with the initial voltages of $V_{B0} = 3.098$ V, $V_{B1} = 3.112$ V, $V_{B2} = 3.079$ V, $V_{B3} = 2.975$ V, $V_{B4} = 3.036$ V, $V_{B5} = 3.083$ V, $V_{B6} = 3.1$ V, and $V_{B7} = 2.853$ V. We can observe from Fig. 18(a) that the most undercharged cell and the most overcharged voltage cell are B_7 and B_1, respectively. The maximum voltage difference between them is 0.259 V. From (29), the initial consistency coefficient of the battery stack can be obtained as 0.0884. At about 3200 s, ZVG between cells is achieved, and the consistency coefficient is greatly reduced to approximately 0. As shown in Fig. 18(b), during the balancing process, the energy conversion efficiency varies from 99.5% to 98.6%, keeping at a high level.

C. Dynamic Equalization

The equalization during the charge or discharge process of battery, i.e., the dynamic equalization, is more complex but necessary than that during the idle period. This is due to the serious imbalance in cell voltages that is usually generated during the fast charge or discharge process of battery. Furthermore, the cell voltage should not go below the discharge cut-off voltage ($\sim$2 V) in order to prevent overdischarge, and the cell voltage cannot exceed the end-of-charge voltage ($\sim$3.65 V) in order to prevent overcharge. Once one cell voltage in the battery string either exceeds the end-of-charge voltage or reaches the discharge cut-off voltage, the charge or discharge process will have to stop. This fact reduces enormously the available capacity of the battery pack. Consequently, the dynamic equalization performance is a significant issue need to verify.

The lithium-ion battery offers a relatively flat OCV within a broad range of SOC from 20% to 80%. In other words, even though the SOC difference between cells is large, the corresponding voltage difference still remains small. Moreover, in practice the resolution limit of the analog-to-digital converter is about 0.001–0.002 V. Therefore, it would be counterproductive to carry out the voltage-based equalization during the SOC range of 20–80% because this may enlarge the cell inconsistency due to the voltage measurement errors. Thus, in order to improve the balancing performance, it is optimum to carry out the voltage-based equalization across the SOC range of 0–20% or 80–100%. Fig. 19 shows the experimental results during the constant current discharging and charging without the equalization



(a) (b)

(c)

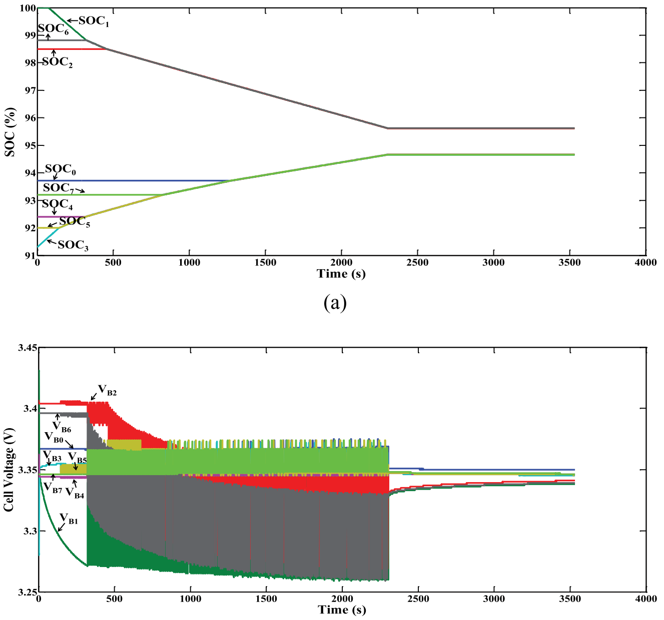
Fig. 20. Dynamic equalization during UDDS test cycles. (a) Cells' voltages and maximum voltage difference between cells without equalization. (b) Cells' voltages and maximum voltage difference between cells with the proposed equalization. (c) Energy conversion efficiency during UDDS test cycles.

[see Fig. 19(a) and(c)] and with the equalization [see Fig. 19(b) and (d)].

As shown in Fig. 19(a), the discharging process without equalization has to stop when the cell B_1 reaches the discharge cutoff voltage, although the other cells still have energy left. The maximum voltage difference between cells from 80% SOC to 20% SOC is more than 0.05 V. As shown in Fig. 19(b), the maximum voltage difference between cells from 80% SOC to 20% SOC is less than 0.02 V, showing a good consistency of the cell voltages with the proposed equalization. Almost the whole energy (i.e., 6.0 Ah) in the battery stack is used and is significantly larger than that (i.e., 5.3 Ah) without the equalization. The available capacity of the battery stack with the proposed equalizer is increased by 13.2% compared with that without equalization.

As shown in Fig. 19(c) and (d), a similar situation occurs when this battery stack is charged. Table II summarizes the consistency coefficients and the available capacities of the battery pack with and without equalization. We can observe that the consistency and the available capacity of the battery stack are greatly improved by the proposed equalization scheme.

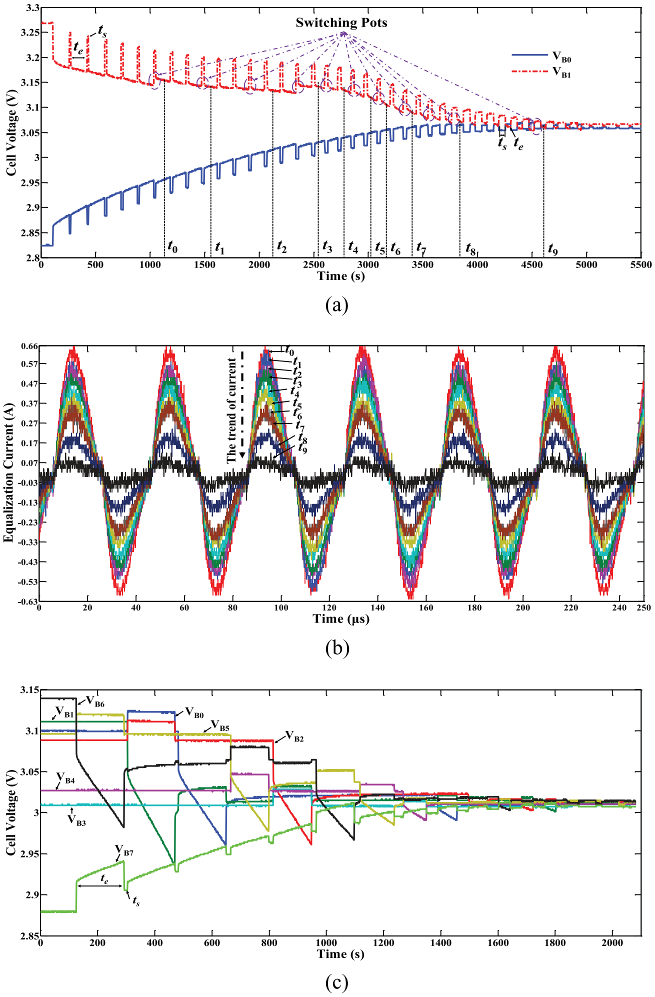
In order to further prove the validity of the proposed scheme in terms of the dynamic equalization, Fig. 20 further presents the test results under UDDS test cycles. As shown in Fig. 20(a), the discharging process without equalization has to stop when the cell B_3 reaches the discharge cutoff voltage, and the maximum voltage difference is over 0.8 V. As shown in Fig. 20(b), all the cells are almost identically discharged with the proposed equalization, and the maximum voltage difference is about 0.6 V when the cell B_7 reaches the discharge cutoff voltage. Fig. 20(c) presents the energy conversion efficiency varies from 99.3% to 98.2% during UDDS test cycles, showing a high dynamic equalization efficiency of the proposed equalizer. Hence, the proposed equalizer is also appropriate for UDDS test cycles.



(a)

(b)

Fig. 21. SOC-based balancing for eight lithium-ion cells during an idle period. (a) Eight-cell SOC trajectories. (b)Eight-cell voltage trajectories.



(a)

(b)

(c)

Fig. 22. Balancing results with the FLC. (a) Balancing results for two cells. (b) Equalizing currents during the two-cell balancing process. (c) Balancing results for eight cells.

D. SOC-Based Equalization

Voltage-based equalization, which targets the consistent cell voltages, is the most feasible to realize due to the direct measured cell voltages. But the voltage-based equalization is more challenging because of the relatively flat OCV. To solve this dilemma, an SOC-based equalization algorithm is proposed and shown in Fig. 21. SOC-based equalization targets the consistent cell SOCs rather than the cell voltages; hence, this method is not limited to the SOC range of 20–80%.

The initial SOCs of the battery cells are established from a lookup table, which consists of the OCVs and the corresponding SOC information. The ampere-hour integration approach is used to count how many coulombs of charge being pumped into or out of a battery cell, which provides higher accuracy than most other SOC estimation methods [51]–[54], since it computes directly the integral of the current with respect to time.

In the proposed method, the SOC-based balancing test is operated in an idle battery pack. As shown in Fig. 21, the balancing test begins with the initial SOCs of $\mathrm{SOC}_0 = 93.7\%$, $\mathrm{SOC}_1 = 100\%$, $\mathrm{SOC}_2 = 98.5\%$, $\mathrm{SOC}_3 = 91.3\%$, $\mathrm{SOC}_4 = 92.4\%$, $\mathrm{SOC}_5 = 92\%$, $\mathrm{SOC}_6 = 98.8\%$, and $\mathrm{SOC}_7 = 93.2\%$, whose corresponding initial voltages are $V_{B0} = 3.348$ V, $V_{B1} = 3.425$ V, $V_{B2} = 3.407$ V, $V_{B3} = 3.280$ V, $V_{B4} = 3.363$ V, $V_{B5} = 3.346$ V, $V_{B6} = 3.396$ V, and $V_{B7} = 3.346$ V, respectively. We can observe from Fig. 21, that after about 2400 s, the proposed equalizer reduces the maximum SOC difference from 8.7% to 0.9% and the corresponding maximum voltage difference from 0.145 to 0.012 V, which proves the validity of SOC-based equalization of the proposed scheme.

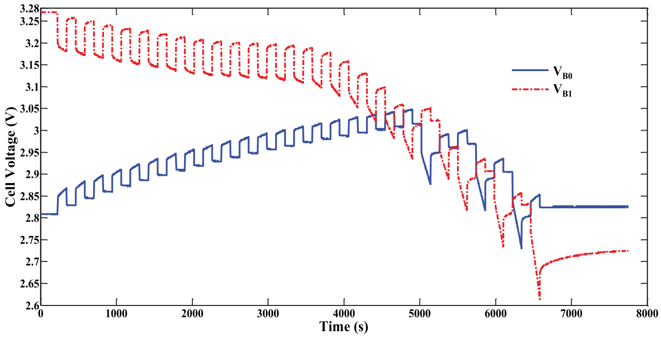


Fig. 23. Overequalization for two cells without the FLC.

TABLE III
COMPARISON OF THE PROPOSED EQUALIZER WITH THE EXISTING TYPICAL SOLUTIONS IN TERMS OF THE EQUALIZATION SPEED AND EFFICIENCY

Topology References	Type	Equalization Speed I_E	Equalization Speed Cyc_{ave}	Equalization Efficiency η	Equalization Efficiency η_{ave}
[12], [13]	CBM	0.7 A	$\frac{n}{2}$	0%	0%
[15]	ACTCM	0.18 A	$\frac{n+1}{3}$	98%	$(98\%)^{\frac{n+1}{3}}$
[22]	DCTCM	0.8 A	1	90%	90%
[32]	CTPM	0.3 A	$\frac{n}{2}$	88%	$88\% - \frac{1}{n}$
[36]	PTCM	0.49 A	$\frac{n}{2}$	61.5%	$61.5\% \frac{n-1}{n}$
[40]	CTPTC	1.96 A	$\frac{4}{3}$	81.6%	$(81.6\%)^{\frac{4}{3}}$
Proposed Topology	DCTCM	0.86 A	1	98%	98%

n: the number of cells connected in series in a battery pack.
I_E : the maximum equalization current.
Cyc_{ave}: the average switching cycle to complete the charge transportation.
η: the conversion efficiency in one equalization cycle.
η_{ave}: the average conversion efficiency.

E. Overequalization Prevention

The energy in the proposed topology is transferred in real time from the cell with the highest voltage at any position to the one with the lowest voltage at any position in the stack. Therefore, an appropriate equalization switching period and equalization current are important for the consistency of the battery pack. The equalization switching period is composed of the equalization time t_e and the standing time t_s, as shown in Fig. 22(a). A long equalization time or a large equalization current is ample in equalization capability but might lead to overequalization, while a short equalization time or a small equalization current can efficiently prevent overequalization but leads to a long infant stage and high switching frequency. Hence, a fuzzy logic controller (FLC) is employed to regulate the equalization switching period (t_e and t_s) and the equalization current of the proposed

TABLE IV
COMPARISON BETWEEN THE PROPOSED EQUALIZER AND THE EXISTING TYPICAL SOLUTIONS IN TERMS OF THE COMPONENT NUMBER AND THE WORK PERFORMANCE

Topology		Components							Performance Indicators						
References	Type	M	RE	L	C	D	T	R	P_1	P_2	P_3	P_4	P_5	P_6	P_7
[12], [13]	CBM	n	0	0	0	0	0	n	+	+	+	−	−	+	−
[15]	ACTCM	$2n$	0	$n-1$	$n-1$	0	0	0	−	−	−	−	+	+	+
[22]	DCTCM	$4n$	0	0	1	0	0	0	=	=	+	+	−	−	+
[32]	CTPM	$n+1$	0	0	0	$2n-1$	1	0	−	−	−	=	−	+	−
[36]	PTCM	$2n+9$	0	0	9	9	9	0	−	−	−	−	−	+	−
[40]	CTPTC	$2n+2$	11	0	2	2	2	0	−	−	+	=	−	+	−
Proposed Topology	DCTCM	5	$2n$	2	2	5	0	0	=	=	+	+	+	+	+

Components. M (MOSFETs), RE (Relays), L (Inductors), C (Capacitors), D (Diodes), R (Resistors).
P_1. Cost (−: expensive, +: cheap).
P_2. Size (−: big, +: small).
P_3. Speed (−: low, +: high).
P_4. Efficiency (−: low, +: high).
P_5. Whether be ZCS or not? (−: no, +: yes).
P_6. Whether be ZVG or not? (−: no, +: yes).
P_7. Whether can prevent overequalization or not? (−: no, +: yes).

equalization scheme. The input of the FLC is the maximum voltage difference between cells in the battery pack, and the output are the equalization switching period and the duty cycle of the BDDC. It can be seen from (20) that the amplitude of the equalization current is proportional to the difference between the BDDC output voltage and the minimum cell voltage. Hence, the proposed equalizer can regulate the equalization current by directly controlling the duty cycle of the BDDC.

Fig. 22 shows the experimental results with the FLC. As shown in Fig. 22(a), the equalizing time t_e and the standing time t_s are adjusted according to the voltage difference between the two cells [see the switching pots in Fig. 22(a)]. The larger the voltage difference, the longer the equalizing time t_e, and the shorter the standing time t_s. Fig. 22(b) presents the changing process of the equalizing currents at the times t_0–t_9 marked in Fig. 22(a). It can be observed that the equalizing current is online adaptively regulated according to the voltage difference. The proposed equalizer with the FLC effectively prevents overequalization compared with the balancing result without the FLC in Fig. 23, where overequalization happens due to the constant equalization switching period and the fixed duty cycle of the BDDC. Fig. 22(c) further shows the eight-cell voltage trajectories with the FLC, whose initial voltages are the same as that in Fig. 18. We can observe that the total equalization time is abbreviated about 50% compared with the experimental result without the FLC in Fig. 18.

VI. COMPARISON WITH CONVENTIONAL EQUALIZERS

In this section, the proposed equalizer is compared with the typical solutions of each traditional balancing method. In order to make a systematic evaluation of the proposed scheme, it is assumed that the battery pack consists of n cells connected in series.

Equalization speed is one of the major design parameters for a battery-balancing scheme because the serious imbalance in cell voltages is usually generated during the fast charge or discharge of battery, which reduces enormously the available capacity of the battery pack. In general, the equalization speed is determined by the maximum equalization current and the average switching cycle. The maximum equalization current decides the transferred power among the cells in one switching cycle, and the average switching cycle to complete the charge transportation from the source cell to the target one decides the equalization speed and efficiency.

Table III gives a quantitative comparison of the proposed equalizer with the existing typical solutions in terms of the maximum equalization current I_E, the average switching cycle $\mathrm{Cyc}_{\mathrm{ave}}$, and the average energy conversion efficiency η_{ave}. Since the proposed scheme belongs to DCTCM, the energy can be transferred directly from the source cell at any position to the target one at any position in the stack. Theoretically, it only takes one switching cycle to complete the charge transportation, which makes the cell balancing faster and more effective. As shown in Table III, the presented topology offers a 0.86-A equalization current, which is comparable to many existing solutions. In conclusion, the proposed equalizer offers a better equalization speed.

In terms of the circuit size, weight, and cost, the presented solution has also some advantages compared with the typical solutions due to the absence of transformers and a small number of MOSFETs. In the proposed topology, MOSFET switches M_1, M_2, M_3, and M_4 require a single floating drive circuit, whereas the drive circuits of the relays (S_1, Q_1)–(S_n, Q_n), (S_1', Q_1')–(S_n', Q_n') are powered by a common power source. Therefore, the drive circuitries of this topology are simpler. Moreover, only one *LC* converter and one BDDC are shared by all cells, leading to great size and cost reduction for the circuit.

Based on the above analyses, Table IV further gives a systematically comparative study in terms of component, cost, size, speed, efficiency, ZCS, ZVG, and overequalization. "Components" defines what components are utilized and the number of them. A fuzzy scale is employed to evaluate each parameter, for which "−" is the minimum value, "+" is the maximum one, and

"=" is the mean one between "+" and "−." It can be concluded from Table IV that the proposed topology has the advantages of low cost, low size, high efficiency, high speed, ZCS, and ZVG, which give the proposed topology very good implementation possibility for a long series-connected battery string.

VII. CONCLUSION

In this paper, a novel direct cell-to-cell equalizer based on QRLCC and BDDC is proposed. The operation principle, the equalization time prediction, the cell-balancing performance, and the comparative studies with previous contributions are presented. The proposed scheme obtains ZCS due to the QRLCC and achieves ZVG between cells because of the BDDC. Moreover, by sharing connection of the QRLCC and the cell selection switches, the proposed equalizer solves the dilemma of equalization implementation with small size and low cost for a long series-connected battery string. On the one hand, the outstanding equalization performance (e.g., ZCS, ZVG between cells, overequalization prevention, good equalization speed, and high equalization efficiency) of the proposed equalizer is certified by the experimental results with eight lithium-ion battery cells. On the other hand, a systematic and quantitative comparison for n cells has been presented to further show the superiorities of the proposed topology in terms of circuit size, weight, and cost compared with the existing ones. As a future work, this topology will be extended for the battery pack with more than hundred cells to be used in EVs or HEVs.

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