Ultrahigh Step-Down Converter

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***Abstract*—In this paper, an ultrahigh step-down converter is presented, which combines one coupled inductor and one energy-transferring capacitor. The corresponding voltage conversion ratio is much lower than that of the traditional synchronously rectified (SR) buck converter, and the proposed converter can achieve extremely low output voltage with an appropriate duty ratio. Moreover, there are three major merits in the proposed converter. One merit is that the voltage conversion ratio of the proposed converter is linear, thereby making control quite easy. Another merit is that if one of the switches fails or is abnormally controlled, a high voltage does not appear in the output terminal, so the output load can be protected. The other merit is that the proposed converter can be driven using the existing SR buck pulse-width modulation control integrated circuit. In this study, brief theoretical deductions and some experimental results are given to verify the feasibility and effectiveness of the proposed converter.**

***Index Terms*—Buck converter, coupled inductor, energy-transferring capacitor, step-down converter.**

I. Introduction

As GENERALLY recognized, the step-down converter is widely used in many applications, where the loads need lower input voltages, such as digital circuits. In general, a 48-V voltage source generated from the ac–dc converter is used for communication systems in the network communication room. Traditionally, the buck converter is used to step down the high voltage to a lower voltage. However, for the device that needs an input voltage of 3.3 V or less, an extremely low duty cycle is necessary for the buck converter if the input voltage is 48 V, thereby causing the control design to be tough and the accompanying power loss to be relatively high. Up to now, the two-stage step-down structure has been widely employed in the applications, which need much lower voltage conversion ratio. For example, in order to power the CPU, the DRAM, and the hard disk, the first stage transfers 48–12 V to power the point of load (POL), and then, the POL, called the second stage, transfers 12 to 3.3, 2.5, 1.8, 1.5, 1.2 or 1 V.

The methods described in [1]–[4] are based on the two-stage buck converter. But these methods need relatively many active switches and components, pulse-width modulation (PWM) gate driving circuits, and signals, etc. Obviously, its overall efficiency is the product of the efficiencies of two stages. Hence, the two-stage buck converter is not suitable for low-power applications. In [5], a high-efficiency open-loop bus converter is presented. In this converter, the input voltage of 48-V voltage is first stepped down to 12 V, which is converted into a lower output voltage of 3.3 V or less to supply the load via a second stage, named POL. Basically, this topology belongs to a two-stage converter. But, this bus converter and the POL need six active switches and three magnetic devices, along with individual control integrated circuits (ICs). The methods described in [6]–[10] are based on multiple voltage regulators connected in parallel and coupled inductors, and accordingly by using interleaved PWM signals, the ratio of output voltage to input voltage can be enhanced. As compared to the traditional buck converter, under the condition of the same input and output voltages, this converter can operate under a relatively large duty cycle, thereby reducing the problem in a relatively small duty cycle. However, the aforementioned structure needs at least two phases operating simultaneously, so it is suitable for high output current applications. The methods described in [7], and [11]–[18] are based on coupled inductors so as to achieve high step-down voltage conversion ratios. Even though these circuits are simple, the leakage inductances of the coupled inductors would cause high voltage spikes to tend to break down the switches, and hence, additional passive snubbers are required to protect the switches from being destroyed, thereby tending to reduce the corresponding efficiency. Although the active snubbers presented in the literatures [18]–[20] can recycle the energy stored in leakage inductances, the accompanying circuits are too complex. In [6], [12], and [21]–[24], too many switches and magnetic devices are needed, resulting in high cost and complex structures; hence, they are not suitable for low- or middle-power applications. In [25], in order to achieve the fast transient response, the switching capacitor along with the transformer is employed to transfer the energy to the output terminal. In [7], [10], [12], [17], [19], [21], [22], and [26], the switches require floating gate drivers instead of low-cost half-bridge gate drivers. In this case, if the pulse transformer is adopted, the PCB space will become relatively large, leading to difficulty in applications. The method described in [4] possesses the floating output, which limits the applications. The method described in [8], [11]–[13], [15], [19], [20], and [27]–[29] possesses nonlinearity in voltage conversion ratio, thereby making the controller design difficult. The method described in [30] needs many inductors, capacitors, and diode arrays, leading to too many components used and relatively low efficiency.

Based on the aforementioned, a novel ultrahigh step-down converter is presented, which utilizes one coupled inductor, one additional grounded switch, and one additional capacitor with small capacitance and can be driven using existing buck PWM control ICs. Furthermore, the voltage conversion ratio of this converter does not have nonlinearity characteristics, and if one of the switches fails or is abnormally controlled, the high voltage

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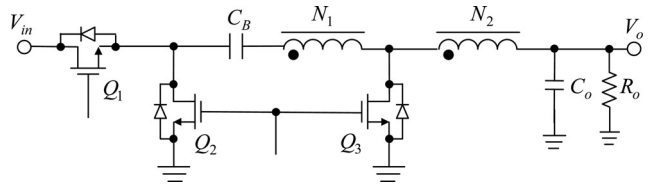

Fig. 1. Proposed step-down converter.

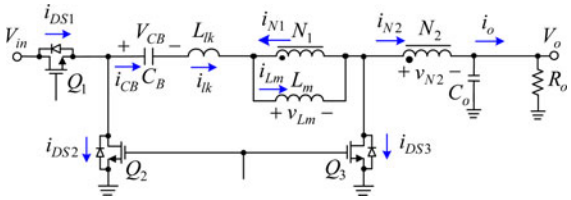

Fig. 2. Equivalent circuit model of the proposed converter.

does not appear in the output terminal, so the output load can be protected.

II. Overall System Configuration

Fig. 1 shows the proposed converter, which contains three switches Q_1, Q_2, and Q_3, one energy-transferring capacitor C_B and one output capacitor C_o, and one coupled inductor composed of the primary winding N_1 and the secondary winding N_2. Moreover, Q_2 and Q_3 are driven simultaneously with both gates connected together, and hence, although there are three switches in this circuit, only one half-gate driver is needed to drive them. In addition, the input voltage is denoted by V_i, the output voltage is signified by V_o, and the output resistor is represented by R_o.

In addition, how this improved converter is derived from the traditional buck converter is to be described as following. As generally acknowledged, for the traditional buck converter, its output inductor is directly connected to the input during the turn-on period of the main switch. Therefore, if a high step-down voltage gain is needed, then the corresponding duty cycle is quite small. By doing so, the control design tends to be difficult and the accompanying power loss tends to be relatively high. Accordingly, to get a high step-down voltage gain under a suitable duty cycle is necessary. In general, the most direct method is by inserting a voltage source between the input voltage and the output inductor. Therefore, in order to achieve this goal, the energy-transferring capacitor C_B takes such an important role, and the voltage across C_B is determined by the coupled inductor. And, as the switch Q_1 is turned ON, the capacitor C_B is charged, whereas as the switch Q_3 is turned OFF, the capacitor C_B is discharged. By doing so, the amp-second balance of the capacitor C_B is held. It is noted that the switch Q_3 is used as a synchronously rectified (SR) switch, similar to the low-side switch of the traditional SR buck converter.

III. Basic Operating Principles

The equivalent circuit of the proposed converter is shown in Fig. 2. The coupled inductor is modeled as an ideal transformer

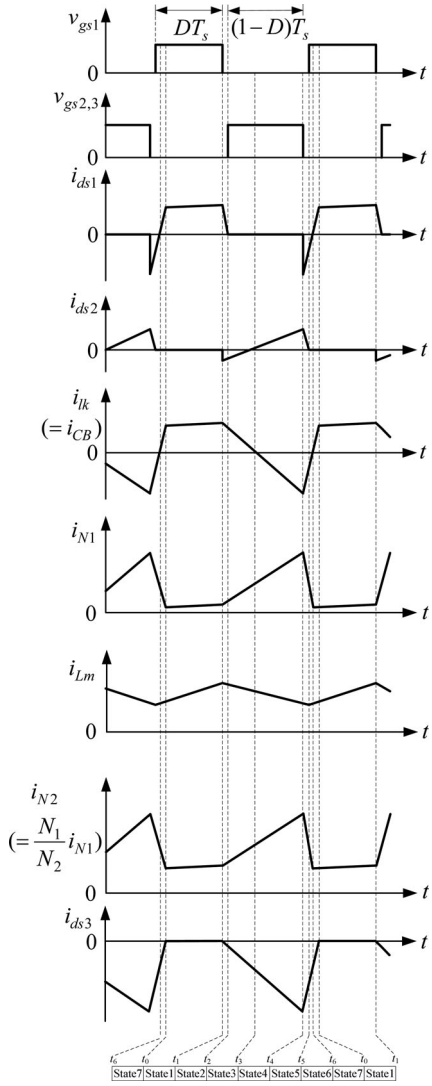

Fig. 3. Illustrated waveforms for the proposed converter.

with primary winding N_1 and secondary winding N_2, a magnetizing inductor L_m connected in parallel with N_1, and a leakage inductor L_{lk}. Besides, in order to make the analysis of the proposed converter easier, there are some assumptions to be made as follows.

1) The proposed converter operates in the positive current region. That is, the current flowing through the magnetizing inductor L_m is always positive.
2) All the switches and diodes are assumed to be ideal components.
3) The values of all the capacitors are large enough such that the voltages across them are kept constant at some values.

The following analysis contains the operating principles, voltage gain, boundary condition for magnetizing inductor, influence of leakage inductance of the coupled inductor, performance comparison, and small-signal modeling. In addition, the input current is denoted by $i_{\rm DS1}$, the currents flowing through Q_2, Q_3, C_B, L_{lk}, N_1, N_2, L_m, and R_o are signified by $i_{\rm DS2}$, $i_{\rm DS3}$, i_{CB}, i_{lk}, i_{N_1}, i_{N_2}, i_{Lm}, and i_o, respectively. Furthermore, the

voltage across L_m or the voltage across the N_1 winding is signified by v_{Lm}, the voltage across the N_2 winding is represented by v_{N_2}, the voltage across C_B is indicated by V_{CB}, and the voltage across C_o or R_o is denoted by V_o.

A. Basic Operating Principles of the Proposed Converter

For the proposed converter operating in the positive current region, there are seven operating states, to be described as follows. Fig. 3 shows the illustrated waveforms over one switching period.

1) *State 1 [t_0, t_1]:* As shown in Fig. 4(a), the switch Q_1 is turned ON, but the switches Q_2 and Q_3 are turned OFF. During this state, a positive voltage is imposed on the magnetizing inductor L_m and the leakage inductor L_{lk}, making L_m, and L_{lk} magnetized. In the meantime, the capacitor C_B is being charged, and the currents in the windings N_1 and N_2, i.e., i_{N_1} and i_{N_2}, are increasing slowly

$$i_{\mathrm{DS1}} = i_{CB} = i_{lk} = i_{Lm} - i_{N1} = i_{N2} = \frac{N_1}{N_2} i_{N1} \tag{1}$$

$$\frac{di_{Lm}}{dt} = \frac{v_{Lm}}{L_m} \approx \frac{(V_{\mathrm{in}} - V_{CB} - V_o) \cdot \left(\dfrac{N_1}{N_1 + N_2}\right)}{L_m}. \tag{2}$$

2) *State 2 [t_1, t_2]:* As shown in Fig. 4(b), the switch Q_1 is turned OFF, and the switches Q_2 and Q_3 are still turned OFF. During this blanking time period, the body diodes of the switches Q_2 and Q_3 are forward-biased by the leakage inductance current i_{lk}. Meanwhile, the voltage $-V_o \times N_1/N_2$ is imposed on L_m, causing L_m to be demagnetized, and i_{lk} is declining

$$-i_{\mathrm{DS2}} = i_{CB} = i_{lk} \tag{3}$$

$$-i_{\mathrm{DS3}} = i_{N2} - i_{CB} \tag{4}$$

$$i_{Lm} = i_{lk} + i_{N1} = i_{CB} + i_{N2} \cdot \frac{N_2}{N_1} \tag{5}$$

$$\frac{di_{Lm}}{dt} = \frac{v_{Lm}}{L_m} \approx \frac{-V_o \cdot \left(\frac{N_1}{N_2}\right)}{L_m}. \tag{6}$$

3) *State 3 [t_2, t_3]:* As shown in Fig. 4(c), the switch Q_1 still keeps turned OFF. Before the state 3 begins, there are currents flowing through the body diodes of Q_2 and Q_3. Hence, if Q_2 and Q_3 are turned ON during this state, then the zero-voltage switching (ZVS) will occur. Also, L_m is still demagnetized as shown in (6). Once the leakage inductance current i_{lk} falls to zero, state 3 comes to an end. The corresponding equations are the same as those mentioned in state 2.

4) *State 4 [t_3, t_4]:* As shown in Fig. 4(d), the switch Q_1 is still turned off, but the switches Q_2 and Q_3 keep turned ON. During this state, the energy-transferring capacitor

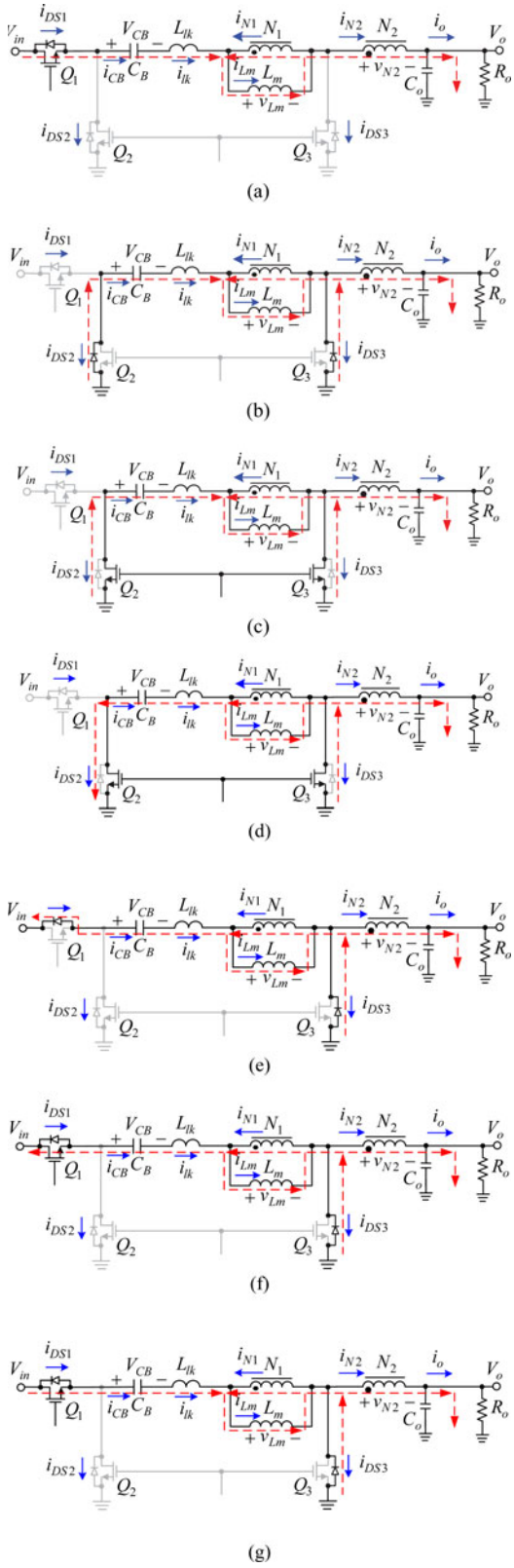

Fig. 4. Power flow paths over one switching period in the positive current region: (a) state 1; (b) state 2; (c) state 3; (d) state 4; (e) state 5; (f) state 6; (g) state 7.

C_B is discharging the energy, and this energy is released to the output resistor R_o by C_B via the primary winding N_1 and the secondary winding N_2. Hence, the currents in the windings N_1 and N_2, i.e., i_{N_1} and i_{N_2}, are increasing gradually. Also, L_m is still demagnetized as shown in (6)

$$i_{\mathrm{DS2}} = -i_{CB} = -i_{lk} \tag{7}$$

$$-i_{\mathrm{DS3}} = -i_{CB} + i_{N2} \tag{8}$$

$$i_{Lm} = i_{N1} - (-i_{CB}) = i_{N2} \cdot \frac{N_2}{N_1} + i_{CB}. \tag{9}$$

5) *State 5 [t_4, t_5]:* As shown in Fig. 4(e), the switch Q_1 is still turned OFF, and the switches Q_2 and Q_3 are turned OFF. Since this state is the other blanking time over one PWM cycle, and the currents in the coupled inductor keep continuous, the body diodes of the switches Q_1 and Q_3 are forward biased. Also, L_m is demagnetized as shown in (6)

$$-i_{\mathrm{DS1}} = -i_{CB} = -i_{lk} \tag{10}$$

$$i_{Lm} = i_{N1} - (-i_{CB}) = i_{N1} - (-i_{\mathrm{DS1}}) = i_{N2} \cdot \frac{N_2}{N_1} + i_{\mathrm{DS1}}. \tag{11}$$

6) *State 6 [t_5, t_6]:* As shown in Fig. 4(f), the switches Q_2 and Q_3 are still turned OFF. Before the state 6 begins, there is a current flowing through the body diode of Q_1. At this time, Q_1 can be turned ON with ZVS. The corresponding equations are the same as those in state 5.

7) *State 7 [t_6, t_0]:* As shown in Fig. 4(g), the switch Q_1 is turned ON, but the switches Q_2 and Q_3 are still turned OFF. During this state, the input voltage V_{in} charges the energy-transferring capacitor C_B. At the same time, the current i_{lk} is smaller than the current in the winding N_2, i.e., i_{N_2}, the body diode of the switch Q_3 is still forward biased. As soon as the current i_{lk} is equal to the current i_{N_2}, the current in the body of the switch Q_3 stops flowing, the operating state goes back to state 1, and the next cycle is repeated

$$i_{\mathrm{DS1}} = i_{CB} = i_{lk} \tag{12}$$

$$i_{Lm} = i_{CB} + i_{N1} = i_{CB} + i_{N2} \cdot \frac{N_2}{N_1} \tag{13}$$

$$-i_{\mathrm{DS3}} = i_{N2} - i_{CB}. \tag{14}$$

B. Voltage Gain of the Proposed Converter

To get the voltage gain and the voltage across C_B, only states 1, 3, and 4 are considered herein with the blacking times and the leakage inductance L_{lk} ignored. From state 3 or state 4, v_{Lm} can be found to be

$$v_{Lm} = -V_{CB} = -V_o \cdot \left(\frac{N_1}{N_2}\right). \tag{15}$$

From state 1, the following equation can be obtained to be

$$v_{Lm} = (V_{\mathrm{in}} - V_{CB} - V_o) \cdot \left(\frac{N_1}{N_1 + N_2}\right). \tag{16}$$

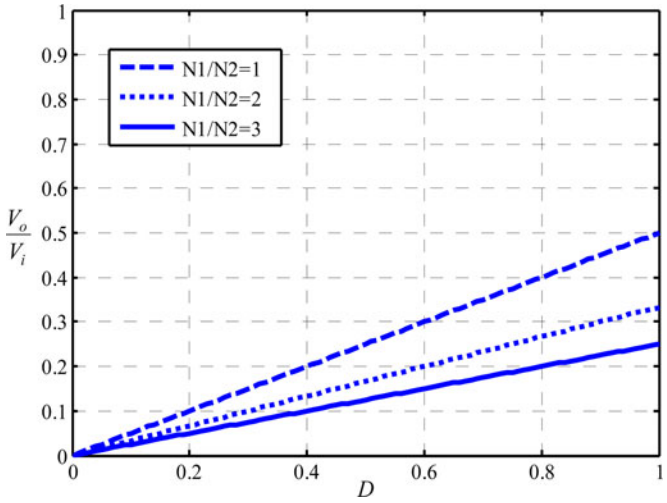

Fig. 5. Curves of voltage gain versus duty cycle for the proposed converter with different values of turns ratio.

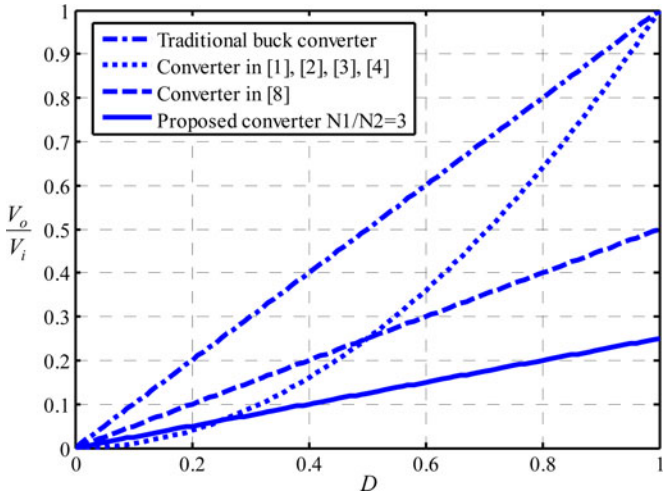

Fig. 6. Comparison of voltage gain versus duty cycle for four types of converters.

By applying the voltage-second balance principle to L_m over one switching period, the following equation can be obtained:

$$D \cdot (V_{\mathrm{in}} - V_{CB} - V_o) \cdot \left(\frac{N_1}{N_1+N_2}\right) = (1-D) \cdot V_o \cdot \left(\frac{N_1}{N_2}\right). \tag{17}$$

Next, based on (15) and the aforementioned equation, the corresponding voltage gain can be expressed to be

$$\frac{V_o}{V_{\mathrm{in}}} = D \cdot \left(\frac{N_2}{N_1 + N_2}\right). \tag{18}$$

From (18), it can be seen that the voltage gain of the proposed converter can be adjusted not only by the duty cycle but also by the primary and secondary turns. Fig. 5 shows the curves of voltage gain versus duty cycle of the proposed converter, considering different values of turns ratio. Fig. 6 illustrates the

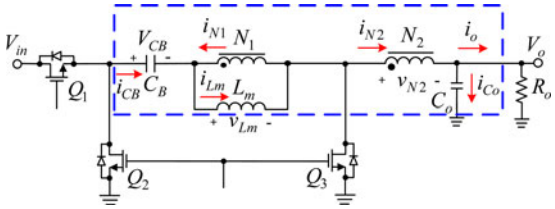

Fig. 7. Marked area in the proposed converter used to explain the relationship between I_{Lm} and I_o.

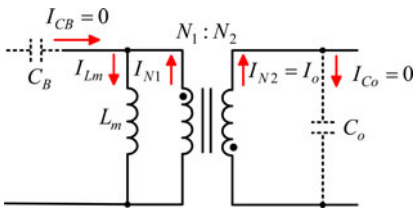

Fig. 8. Equivalent model for the dc analysis of the coupled inductor.

voltage gain of the proposed converter with $N_1/N_2 = 3$ versus duty cycle, compared with the traditional buck converter and the converters in [1]–[4] and [8].

C. Boundary Condition for Magnetizing Inductor

The condition for the magnetizing inductor L_m operating in what region will be described as follows:

$$\begin{cases} 2I_{Lm} \geq \Delta i_{Lm}, & \text{for all current values in the positive current region} \\ 2I_{Lm} < \Delta i_{Lm}, & \text{for part of current values in the negative current region.} \end{cases} \tag{19}$$

where I_{Lm} and Δi_{Lm} are the dc and ac components of i_{Lm}, respectively.

The expression of I_{Lm} can be obtained from (20) and (21). For analysis convenience, it is assumed that the input power is equal to the output power. According to the voltage-second balance for the inductor and the ampere-second balance for the capacitor, the dc component of the inductor voltage and the dc component of the capacitor current are zero. Therefore, as shown in Fig. 7, the dc component of i_{N_2}, i.e., I_{N_2}, is equal to I_o, which is the dc component of the output current i_o; likewise, as shown in Fig. 8, the dc component of current i_{Lm}, i.e., I_{Lm}, is equal to the dc component of i_{N_1}, i.e., I_{N_1}. Therefore

$$I_{N1} = \frac{N_2}{N_1} I_{N2} = \frac{N_2}{N_1} I_o \tag{20}$$

$$I_{Lm} = I_{N1} = \frac{N_2}{N_1} I_o. \tag{21}$$

In Fig. 8, I_o can be expressed as V_o/R_o. Substituting V_o/R_o into I_o in (21) yields the following equation:

$$I_{Lm} = I_{N1} = \frac{N_2}{N_1} \times \frac{V_o}{R_o}. \tag{22}$$

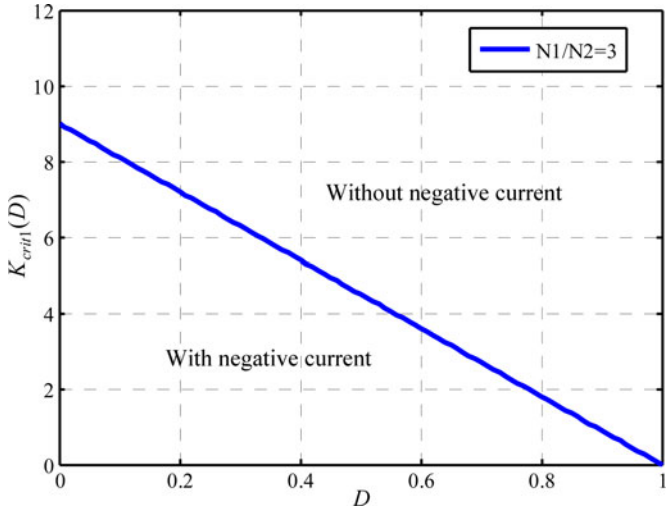

Fig. 9. Boundary condition for magnetizing inductor L_m.

Also, Δi_{Lm} can be represented by

$$\begin{aligned} \Delta i_{Lm} &= \frac{v_{Lm}\Delta t}{L_m} = \frac{\frac{N_1}{N_2} \times V_o \times (1-D)T_s}{L_m} \\ &= \frac{\frac{N_1}{N_1+N_2} \times V_{\text{in}} \times D(1-D)T_s}{L_m}. \end{aligned} \tag{23}$$

As $2I_{Lm} \geq \Delta i_{Lm}$, L_m operates in the positive current region. Moreover, the further deduction is shown as follows:

$$\begin{aligned} & 2I_{Lm} \geq \Delta i_{Lm} \\ & \Rightarrow 2 \times \frac{N_2}{N_1} \times \frac{V_o}{R_o} \geq \frac{\frac{N_1}{N_1+N_2} V_{\text{in}} \times D(1-D)T_s}{L_m} \\ & \Rightarrow \frac{2L_m}{R_o T_s} \geq \left(\frac{N_1}{N_2}\right)^2 (1-D) \\ & \Rightarrow K_1 \geq K_{\text{crit1}}(D) \end{aligned} \tag{24}$$

where $K_1 = \frac{2L_m}{R_o T_s}$ and $K_{\text{crit1}}(D) = \left(\frac{N_1}{N_2}\right)^2 (1-D)$.

From (24), the relationship between $K_{\text{crit1}}(D)$ and D is shown in Fig. 9 under the condition that N_1/N_2 is set at three. From Fig. 9, it can be seen that if K_1 is larger than $K_{\text{crit1}}(D)$, L_m will operate in the positive current region; otherwise, part of i_{Lm} will enter into the negative current region.

D. Influence of the Leakage Inductance

From state 3 shown in Fig. 4, the voltage across C_B, V_{CB}, with the leakage inductance considered can be found as follows:

$$\begin{aligned} V_{CB} &= -\left(v_{lk}^{(3)} + v_{Lm}^{(3)}\right) = -\left[L_{lk}\frac{di_{lk}^{(3)}}{dt} + \frac{N_1}{N_2} \times (-V_o)\right] \\ &= \frac{N_1}{N_2} \times V_o - L_{lk}\frac{di_{lk}^{(3)}}{dt} \end{aligned} \tag{25}$$

where $v_{lk}^{(3)}$, $v_{Lm}^{(3)}$, and $i_{lk}^{(3)}$ are the leakage inductance voltage, magnetizing inductance voltage, and primary-side current in state 3, respectively.

TABLE I
COMPARISON OF TWO STEP-DOWN-TYPE CONVERTERS

Converter	[31]	Proposed
Voltage gain	$D \cdot \left(\frac{N_2}{N_1}\right)$	$D \cdot \left(\frac{N_2}{N_1+N_2}\right)$
Switch voltage stress	$V_{\rm ds1} = V_{\rm ds2} = V_{\rm ds3} = V_{\rm in}$	$V_{\rm ds1} = V_{\rm ds2}$: (44) $V_{\rm ds3}$: (45)
Number of switches	3	3
Number of coupled inductor	1	1
Number of capacitors	2	2

From (25), it can be seen that the leakage inductance will determine the leakage current slew rate. Moreover, if the leakage inductance is ignored, (25) will be equal to (15).

E. Performance Comparison

The novel high step-down converters presented within three years are the circuits shown in [5], [25], [26], and [31]. In [5], a resonant voltage divider is comprised of four switches, one resonant inductor and one resonant capacitor. Such a circuit utilizes *LC* resonance to step down the input voltage. In [25], an isolated step-down converter is presented. In [26], three types of novel nonisolated *LLC* resonant converters are proposed. In [31], a nonisolated flyback switching capacitor voltage regulator is presented. As shown in Table I, where (44) and (45) are to be mentioned in Section IV-D, the proposed converter is compared with the converter in [31]. This is because these two converters have the same number of components and possess nonisolation without resonance used. Furthermore, under the same duty cycle and turns ratio, the voltage gain of the proposed converter has a higher step-down value and the switch voltage stress of Q_3 is smaller than the input voltage, thereby allowing the low on-resistance MOSFET switch to be chosen for Q_3.

F. Small-Signal Modeling

In order to simplify the analysis of small-signal modeling of the proposed converter, the leakage inductance is ignored herein. Therefore, the operating states are briefly classified from seven states shown in Fig. 4 into the following two states shown in Fig. 10. Moreover, in the following deduction, the turns ratio *n* is defined to be N_2/N_1.

In state 1 shown in Fig. 10(a), the resulting differential equations are as follows:

$$\begin{cases} L_m \dfrac{di_{Lm}}{dt} = v_{Lm} = (v_{\rm in} - v_{CB} - v_o) \cdot \dfrac{1}{1+n} \\ C_B \dfrac{dv_{CB}}{dt} = i_{CB} = i_{N2} \\ C_o \dfrac{dv_o}{dt} = i_{N2} - \dfrac{v_o}{R_o} \\ i_{\rm DS1} = i_{Lm} - i_{N1} = i_{Lm} - i_{N2} \cdot n = i_{N2}. \end{cases} \tag{26}$$

From the above $i_{\rm DS1}$ equation, the following equation can be obtained:

$$i_{N2} = i_{Lm} \cdot \frac{1}{1+n}. \tag{27}$$

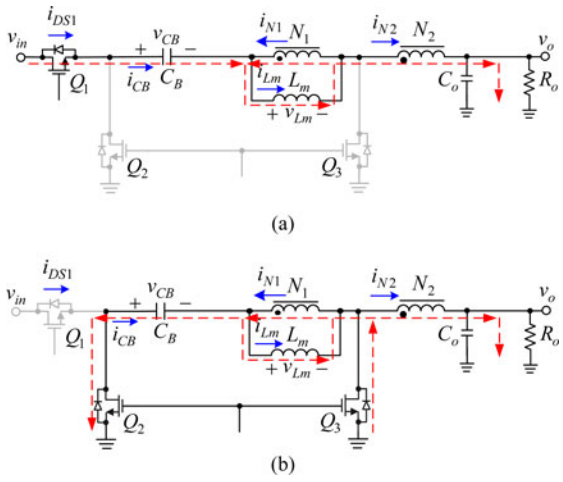

Fig. 10. Equivalent circuits of the proposed converter for small-signal modeling: (a) state 1; (b) state 2.

In state 2 shown in Fig. 10(b), the corresponding differential equations are as follows:

$$\begin{cases} L_m \dfrac{di_{Lm}}{dt} = v_{Lm} = -\dfrac{v_o}{n} = -v_{CB} \\ C_B \dfrac{dv_{CB}}{dt} = -i_{CB} \\ C_o \dfrac{dv_o}{dt} = i_{N2} - \dfrac{v_o}{R_o} = \dfrac{i_{Lm} - i_{CB}}{n} - \dfrac{v_o}{R_o} \\ i_{\rm DS1} = 0. \end{cases} \tag{28}$$

From state 2, the voltage across C_B, v_{CB}, can be obtained as

$$v_{CB} = \frac{v_o}{n}. \tag{29}$$

Next, by inserting (27) and (29) into (26), the following equations can be obtained:

$$\begin{cases} L_m \dfrac{di_{Lm}}{dt} = v_{Lm} = (v_{\rm in} - \dfrac{v_o}{n} - v_o) \cdot \dfrac{1}{1+n} \\ C_B \dfrac{dv_{CB}}{dt} = i_{Lm} \cdot \dfrac{1}{1+n} \\ C_o \dfrac{dv_o}{dt} = i_{Lm} \cdot \dfrac{1}{1+n} - \dfrac{v_o}{R_o} \\ i_{\rm DS1} = i_{Lm} \cdot \dfrac{1}{1+n}. \end{cases} \tag{30}$$

The next step is to remove the switching ripples. Therefore, the averaging method is employed herein. The mathematical operator is defined as (31), where $\langle x \rangle$ denotes the average of *x*, which can be voltage or current, over one switching period

$$\langle x \rangle = \frac{1}{T_s} \int_0^{T_s} x d\tau. \tag{31}$$

Based on (28), (30), and (31), the averaged equations can be obtained

$$\begin{cases} L_m \frac{d\langle i_{Lm}\rangle}{dt} = \left[(\langle v_{\rm in}\rangle - \frac{\langle v_o\rangle}{n} - \langle v_o\rangle)\cdot\frac{1}{1+n}\right]\times d \\ \qquad\qquad -\frac{\langle v_o\rangle}{n}\times(1-d) \\ C_B \frac{d\langle v_{CB}\rangle}{dt} = \left(\langle i_{Lm}\rangle\cdot\frac{1}{1+n}\right)\times d - \langle i_{CB}\rangle\times(1-d) \\ C_o \frac{d\langle v_o\rangle}{dt} = \left(\langle i_{Lm}\rangle\cdot\frac{1}{1+n} - \frac{\langle v_o\rangle}{R_o}\right)\times d \\ \qquad\qquad + \left(\frac{\langle i_{Lm}\rangle - \langle i_{CB}\rangle}{n} - \frac{\langle v_o\rangle}{R_o}\right)\times(1-d) \\ \langle i_{DS1}\rangle = \left(\langle i_{Lm}\rangle\cdot\frac{1}{1+n}\right)\times d. \end{cases} \tag{32}$$

It is assumed that the value of C_B is large enough, and hence, the voltage v_{CB} is a constant value. Therefore, from (32), one can find the relationship between $\langle i_{CB}\rangle$ and $\langle i_{Lm}\rangle$ as follows:

$$\langle i_{CB}\rangle = \frac{d}{1-d}\cdot\frac{1}{1+n}\cdot\langle i_{Lm}\rangle. \tag{33}$$

By inserting (33) into (32), the following equations can be obtained:

$$\begin{cases} L_m \frac{d\langle i_{Lm}\rangle}{dt} = \frac{d}{1+n}\cdot\langle v_{\rm in}\rangle - \frac{1}{n}\cdot\langle v_o\rangle \\ C_o \frac{d\langle v_o\rangle}{dt} = \frac{1}{n}\cdot\langle i_{Lm}\rangle - \frac{\langle v_o\rangle}{R_o} \\ \langle i_{\rm DS1}\rangle = \frac{d}{1+n}\cdot\langle i_{Lm}\rangle. \end{cases} \tag{34}$$

After that, to construct a small-signal model at a quiescent operating point from (34), $\langle x\rangle$ is represented as the corresponding dc quiescent value X plus the superimposed small ac variation $\hat{x}$, with the assumptions that the ac variation is much smaller than the dc quiescent value in magnitude. Let

$$\begin{cases} \langle v_{\rm in}\rangle = V_{\rm in} + \hat{v}_{\rm in}, \\ d = D + \hat{d}, \\ \langle i_{Lm}\rangle = I_{Lm} + \hat{i}_{Lm}, \\ \langle v_o\rangle = V_o + \hat{v}_o, \\ \langle i_{\rm DS1}\rangle = I_{\rm DS1} + \hat{i}_{\rm DS1}, \end{cases} \quad \text{with} \quad \begin{cases} |\hat{v}_{\rm in}| << V_{\rm in} \\ \left|\hat{d}\right| << D \\ \left|\hat{i}_{Lm}\right| << I_{Lm} \\ |\hat{v}_o| << V_o \\ \left|\hat{i}_{\rm DS1}\right| << I_{\rm DS1}. \end{cases} \tag{35}$$

Next, by inserting (35) into (34), the following equations are obtained:

$$\begin{cases} L_m \frac{d(I_{Lm}+\hat{i}_{Lm})}{dt} = \frac{(D+\hat{d})}{1+n}\cdot(V_{\rm in}+\hat{v}_{\rm in}) - \frac{1}{n}\cdot(V_o+\hat{v}_o) \\ C_o \frac{d(V_o+\hat{v}_o)}{dt} = \frac{1}{n}\cdot(I_{Lm}+\hat{i}_{Lm}) - \frac{(V_o+\hat{v}_o)}{R_o} \\ I_{\rm DS1}+\hat{i}_{\rm DS1} = \frac{(D+\hat{d})}{1+n}\cdot(I_{Lm}+\hat{i}_{Lm}). \end{cases} \tag{36}$$

By multiplying out (36) and neglecting dc terms and second-order ac terms, one can obtain the following equations:

$$\begin{cases} L_m \frac{d\left\langle \hat{i}_{Lm}\right\rangle}{dt} = \frac{V_{\rm in}}{1+n}\cdot\hat{d} + \frac{D}{1+n}\cdot\hat{v}_{\rm in} - \frac{\hat{v}_o}{n} \\ C_o \frac{d\left\langle \hat{v}_o\right\rangle}{dt} = \frac{1}{n}\cdot\hat{i}_{Lm} - \frac{\hat{v}_o}{R_o} \\ \left\langle \hat{i}_{\rm DS1}\right\rangle = \frac{I_{Lm}}{1+n}\cdot\hat{d} + \frac{D}{1+n}\cdot\hat{i}_{Lm}. \end{cases} \tag{37}$$

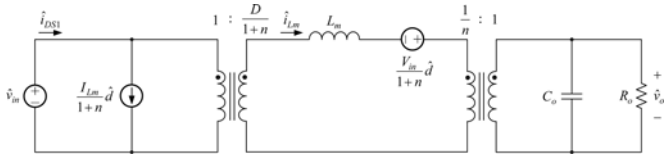

Fig. 11. Small-signal model for the proposed converter.

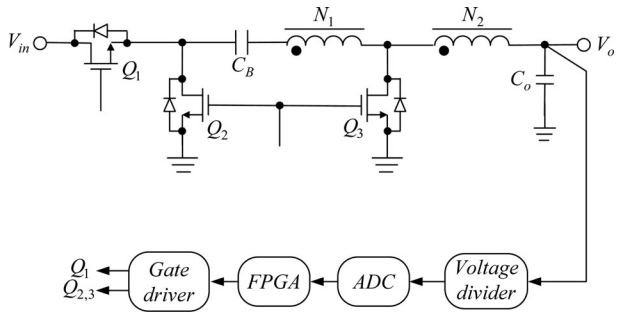

Fig. 12. Proposed overall system block diagram.

Finally, from (37), the resulting small-signal model is illustrated in Fig. 11.

From Fig. 11, the control-to-output function $G_{vd}(s)$ and line-to-output transfer function $G_{vg}(s)$ of the proposed converter can be found to be

$$G_{vd}(s) = \left(\frac{nV_{\rm in}}{1+n}\right)\frac{1}{s^2(n^2L_mC_o) + s\left(\frac{n^2L_m}{R}\right)+1} \tag{38}$$

$$G_{vg}(s) = \left(\frac{nD}{1+n}\right)\frac{1}{s^2(n^2L_mC_o) + s\left(\frac{n^2L_m}{R}\right)+1}. \tag{39}$$

From (38), $G_{vd}(s)$ has no right half-plane zero, and hence, the behavior of the proposed converter is similar to the traditional buck converter. Also, from (39), if s is set to zero, the voltage gain is $nD/(1+n)$, where $n = N_2/N_1$, corresponding to (18).

IV. Control Method Applied With Design Considerations

Fig. 12 shows the overall system block diagram. First of all, the voltage divider transfers the output voltage to a desired lower value, which is fed to the analog-to-digital converter (ADC) to create a corresponding digital signal. After this, this digital signal is sent to the field programmable gate array (FPGA), which is the control kernel, containing one serial peripheral interface (SPI), one proportional-integral (PI) controller, and one digital PWM (DPWM) generator. Eventually, the FPGA processes this digital signal, and accordingly produces two gate driving signals to drive the MOSFET switches. The system specifications and used component names of the proposed converter are shown in Tables II and III, respectively. In addition, there are two steps to tune the parameters of the proportional gain k_p and integral gain k_i in the PI controller as follows.

1) *Step 1:* Starting with $k_p \neq 0$ and $k_i = 0$, and trimming k_p until a small residual error is received.

TABLE II
SYSTEM SPECIFICATIONS OF THE PROPOSED CONVERTER

System parameters	Specifications
Operating current region	Positive
Input voltage (V_i)	48 V
Rated output voltage (V_o)	3.3 V
Rated output current ($I_{o_{\rm rated}}$)/power ($P_{o_{\rm rated}}$)	15A/49.5 W
Minimum output current ($I_{o_{\rm min}}$)/power ($P_{o_{\rm min}}$)	1.5A/4.95 W
Switching frequency (f_s)	100 kHz

TABLE III
COMPONENTS USED IN THE PROPOSED CONVERTER

Components		Product name
MOSFET switches	Q_1, Q_2	PHB34NQ10T
	Q_3	PHD96NQ03LT
Energy-transferring capacitor C_B		Two 10 μF/50 V MLCC capacitors connected in parallel
Output capacitor C_o		One 1800 μF/16 V Rubycon capacitor
Coupled inductor		Core: T106-M125, $N_1 : N_2 = 3 : 1$, $L_m = 86$ μH, $L_{lk} = 1.5$ μH
FPGA		EP1C3T100
Gate driver		HIP2101
ADC		ADC7476

2) *Step 2:* Increasing k_i until the system reaches an almost zero final error.

The design procedure of the magnetizing inductor L_m, the energy-transferring capacitor C_B and the voltage stresses on the active components is shown as follows.

A. Determination of Duty Cycle and Turns Ratio

In this study, the voltage conversion ratio is set at $3.3/48 = 0.06875$. Therefore, according to (18), there are many different possibilities of choosing the duty cycle *D* and turns ratio. If $N_1/N_2 = 1$, *D* will be 13.75%, which is too small and not a suitable duty cycle. If $N_1/N_2 = 4$, *D* will be 34.38%. However, this turns ratio will increase the volume of the coupled inductor and enlarge the leakage inductance. Eventually, the combination of $N_1/N_2 = 3$ and $D = 27.5\%$ will be a preferred choice.

B. Magnetizing Inductor Design

What current region the proposed converter operates in is determined by the current flowing through the magnetizing inductor L_m. To make sure that L_m always operates in the positive current region, the required equation is as follows:

$$I_{Lm,\min} = \frac{N_2}{N_1} \times I_{o,\min} = \frac{1}{3} \times 1.5 = 0.5 \text{ A} \tag{40}$$

$$\begin{aligned} L_m &\geq \frac{v_{Lm}\Delta t}{\Delta i_{Lm}} = \frac{\frac{N_1}{N_2} \times V_o \times (1-D)T_s}{2 \times I_{Lm,\min}} \\ &= \frac{3 \times 3.3 \times (1-0.275) \times 10\mu}{2 \times 0.5} \\ &\approx 72\,\mu\text{H} \end{aligned} \tag{41}$$

where $I_{Lm_{\rm min}}$ is the minimum dc current in L_m. And finally, the value of L_m is set to 86 μH.

Next, based on (42) and the parameters shown in Table II, it can be seen that if the output current I_o is higher than 1.25 A, the converter will always operate in the positive current region. In the proposed converter with the value of L_m set to 86 μH, the corresponding output current at minimum load is set at 10% of the rated load current, i.e., 1.5 A. Therefore, the proposed converter always operates in the positive current region. Also, (42) is described as follows:

$$\begin{aligned} &\frac{2L_m}{R_o T_s} \geq \left(\frac{N_1}{N_2}\right)^2 (1-D) \\ &\Rightarrow \frac{1}{R_o} \geq \left(\frac{N_1}{N_2}\right)^2 (1-D)\left(\frac{T_s}{2L_m}\right) \\ &\Rightarrow I_o \geq \left(\frac{N_1}{N_2}\right)^2 (1-D)\left(\frac{T_s}{2L_m}\right) V_o \\ &\Rightarrow I_o \geq 3^2 \times (1-0.275) \times \left(\frac{10\mu}{2 \times 86\mu}\right) \times 3.3 \\ &\Rightarrow I_o \geq 1.25\,\text{A}. \end{aligned} \tag{42}$$

C. Energy-Transferring Capacitor Design

The capacitor C_B is used to transfer the energy from the input to the output. Thus, the capacitance of C_B can be estimated by using the following equation:

$$C_B \geq \frac{2 \cdot P_{o,\text{rated}}}{V_{CB}^2 \cdot f_s} = \frac{2 \cdot 49.5}{(9.9)^2 \cdot 100 \cdot 10^3} \approx 10\,\mu\text{F}. \tag{43}$$

In practice, the actual capacitance decreases with the frequency. The actual capacitance is smaller than its rated capacitance when operated at a high switching frequency. Hence, the capacitance should be selected to be larger than the theoretical value. Also, based on (15) and Tables II and III, the voltage across C_B, named V_{CB}, is 9.9 V. Eventually, two 10 μF/50 V MLCC capacitors in parallel are selected for C_B.

D. Switch Voltage Stress Design

The voltage stresses across Q_1, Q_2, and Q_3 can be obtained from the following equations:

$$V_{\text{ds1}} = V_{\text{ds2}} = V_{\text{in}} = 48\,\text{V} \tag{44}$$

$$\begin{aligned} V_{\text{ds3}} &= V_o + (V_{\text{in}} - V_{CB} - V_o) \cdot \left(\frac{N_2}{N_1 + N_2}\right) \\ &= 3.3 + (48 - 9.9 - 3.3) \cdot \frac{1}{4} = 9.53\ \text{V}. \end{aligned} \tag{45}$$

Practically, considering the effect of noises and the voltage spikes caused by the parasitic and leakage inductances, the specifications of the drain–source voltage rating of the MOSFET, used as the switch, should be appropriately chosen to ensure that the MOSEFET can operate without being damaged. The voltage rating of the MOSFET should be higher than its theoretical values. Finally, two PHB34NQ10T MOSFETs with a drain–source voltage rating of 100 V are selected for Q_1 and Q_2, and one PHD96NQ03LT MOSFET with a drain–source voltage rating of 25 V is chosen for Q_3.

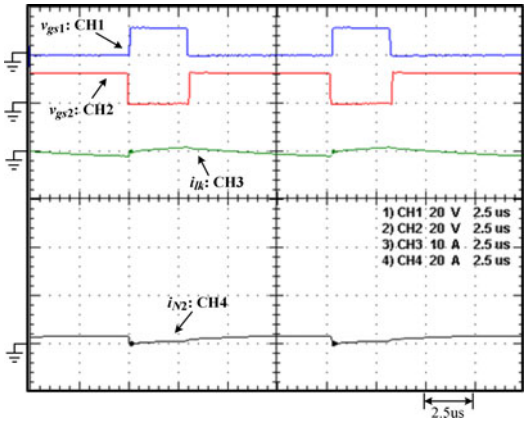

Fig. 13. Waveforms at minimum load: (1) $v_{\rm gs1}$ [20 V/div]; (2) $v_{\rm gs2}$ [20 V/div]; (3) i_{lk} [10 A/div]; (4) i_{N_2} [20 A/div].

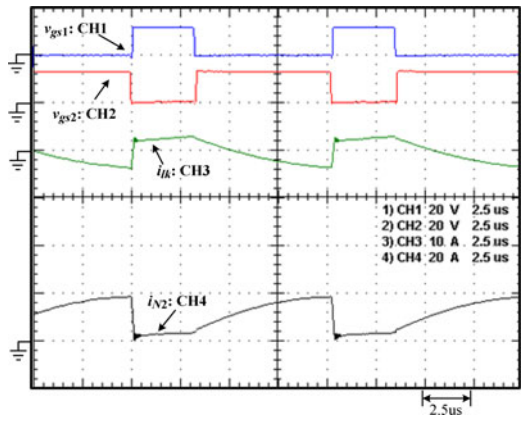

Fig. 14. Waveforms at half load: (1) $v_{\rm gs1}$ [20 V/div]; (2) $v_{\rm gs2}$ [20 V/div]; (3) i_{lk} [10 A/div]; (4) i_{N_2} [20 A/div].

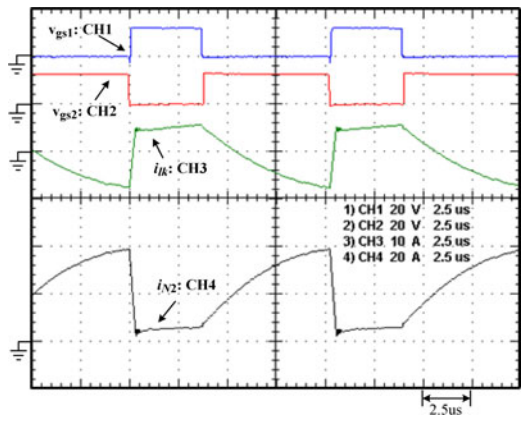

Fig. 15. Waveforms at rated load: (1) $v_{\rm gs1}$ [20 V/div]; (2) $v_{\rm gs2}$ [20 V/div]; (3) i_{lk} [10 A/div]; (4) i_{N_2} [20 A/div].

V. Experimental Results

Figs. 13–15 show the gate driving signals $v_{\rm gs1}$ and $v_{\rm gs2}$ for the switches Q_1 and Q_2, respectively, the primary-side current i_{lk}, and the secondary-side current i_{N_2}, at minimum, half and rated load, respectively. It is noted that the switch Q_3 is synchronized

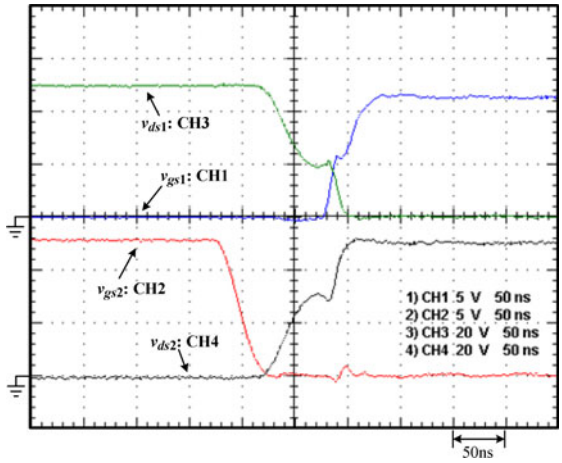

Fig. 16. Waveforms at minimum load due to rising edge of $v_{\rm gs1}$: (1) $v_{\rm gs1}$ [5 V/div]; (2) $v_{\rm gs2}$ [5 V/div]; (3) $v_{\rm ds1}$ [20 V/div]; (4) $v_{\rm ds2}$ [20 V/div].

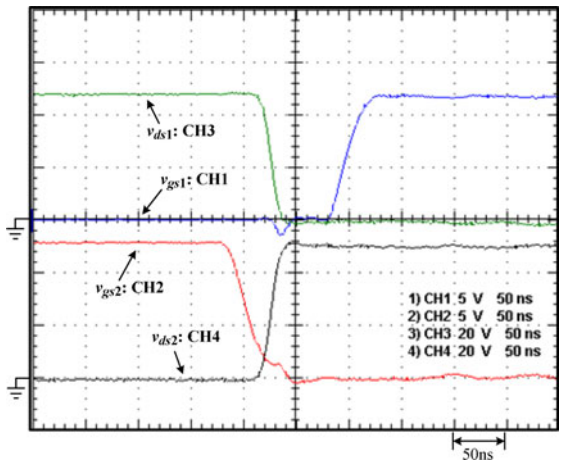

Fig. 17. Waveforms at half load due to rising edge of $v_{\rm gs1}$: (1) $v_{\rm gs1}$ [5 V/div]; (2) v_{gs2} [5 V/div]; (3) $v_{\rm ds1}$ [20 V/div]; (4) $v_{\rm ds2}$ [20 V/div].

with the switch Q_2. Figs. 16–18 show the rising edge of $v_{\rm gs1}$ and the voltage across Q_1, $v_{\rm ds1}$, the falling edge of $v_{\rm gs2}$, and the voltage across Q_2, $v_{\rm ds2}$, at minimum, half and rated load, respectively. Figs. 19–21 show the falling edge of $v_{\rm gs1}$, the voltage across Q_1, $v_{\rm ds1}$, the rising edge of $v_{\rm gs2}$, and the voltage across Q_2, $v_{\rm ds2}$, at minimum, half and rated load, respectively. Figs. 22–24 show the rising edge of $v_{\rm gs3}$ and the voltage across Q_3, $v_{\rm ds3}$, at minimum, half and rated load, respectively. From these aforementioned figures, it can be seen that the proposed converter can operate well to some extent and the switches Q_1, Q_2, and Q_3 possess ZVS or near ZVS turn-on.

On the other hand, the following waveforms are the measured phase margins (PMs) and gain margins (GMs) based on a phase sensitive multimeter, named PSM2200 QuanteQ. Fig. 25 displays the Bode plot at half load, whereas–Fig. 26 displays the Bode plot at rated load. From Figs. 25 and 26, it is obvious that both the PMs are larger than 45 degrees, thereby making sure that this circuit is stable from the industrial point of view. Fig. 27 shows the load transient responses due to step load change from

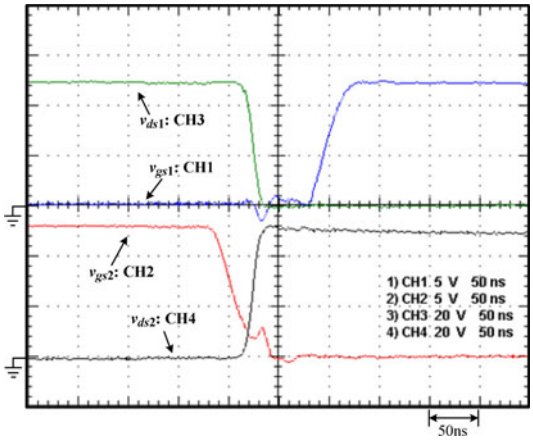

Fig. 18. Waveforms at rated load due to rising edge of v_{gs1}: (1) v_{gs1} [5 V/div]; (2) v_{gs2} [5 V/div]; (3) v_{ds1} [20 V/div]; (4) v_{ds2} [20 V/div].

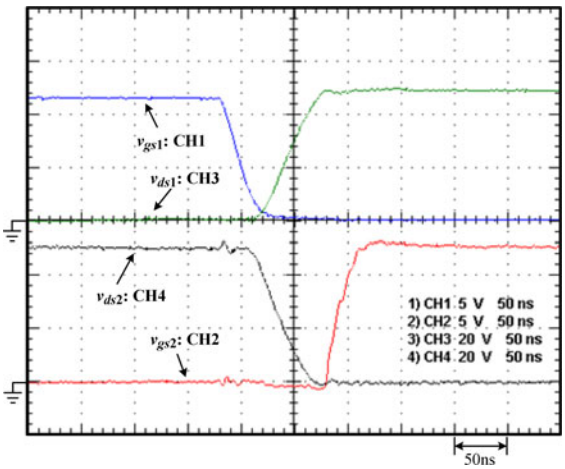

Fig. 19. Waveforms at minimum load due to rising edge of v_{gs2}: (1) v_{gs1} [5V/div]; (2) v_{gs2} [5 V/div]; (3) v_{ds1} [20 V/div]; (4) v_{ds2} [20 V/div].

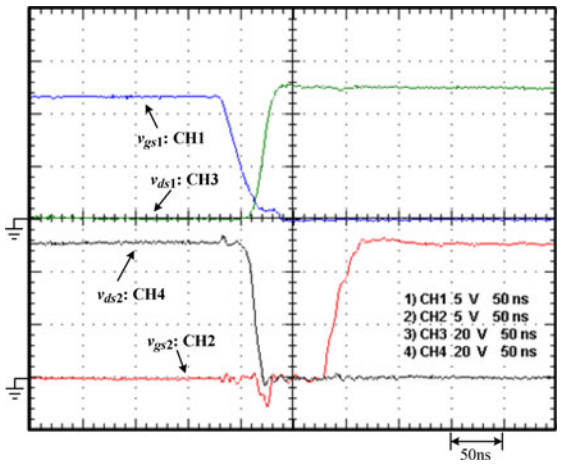

Fig. 20. Waveforms at half load due to rising edge of v_{gs2}: (1) v_{gs1} [5 V/div]; (2) v_{gs2} [5 V/div]; (3) v_{ds1} [20 V/div]; (4) v_{ds2} [20 V/div].

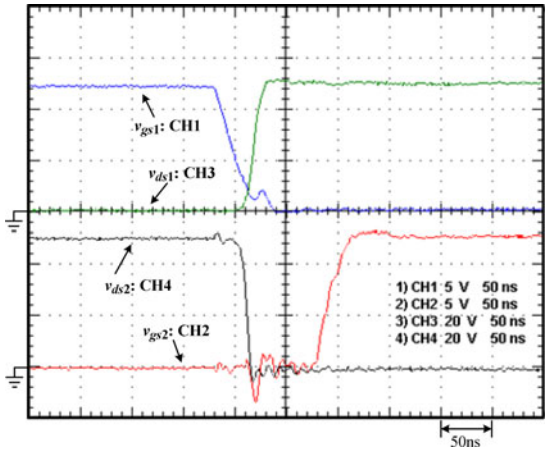

Fig. 21. Waveforms at rated load due to rising edge of v_{gs2}: (1) v_{gs1} [5 V/div]; (2) v_{gs2} [5 V/div]; (3) v_{ds1} [20 V/div]; (4) v_{ds2} [20 V/div].

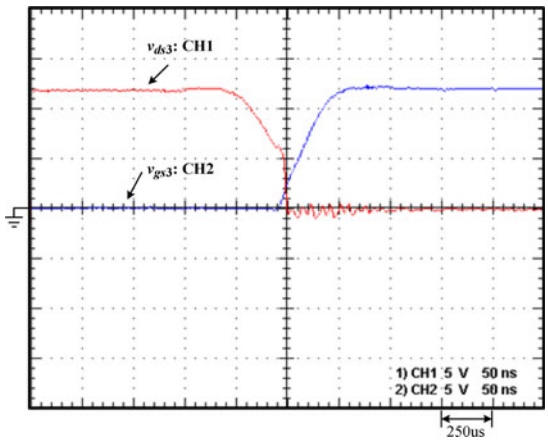

Fig. 22. Waveforms at minimum load due to rising edge of v_{gs3}: (1) v_{gs3} [5V/div]; (2) v_{ds3} [5 V/div].

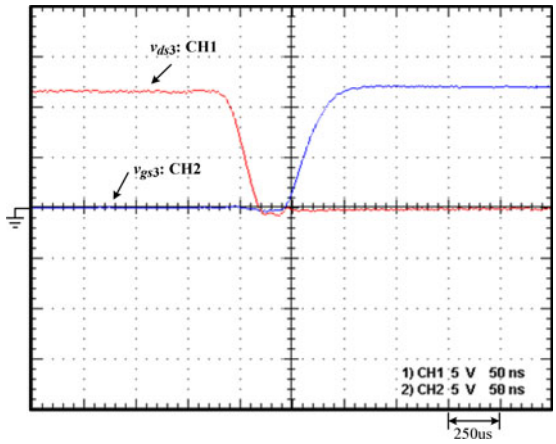

Fig. 23. Waveforms at half load due to rising edge of v_{gs3}: (1) v_{gs3} [5 V/div]; (2) v_{ds3} [5 V/div].

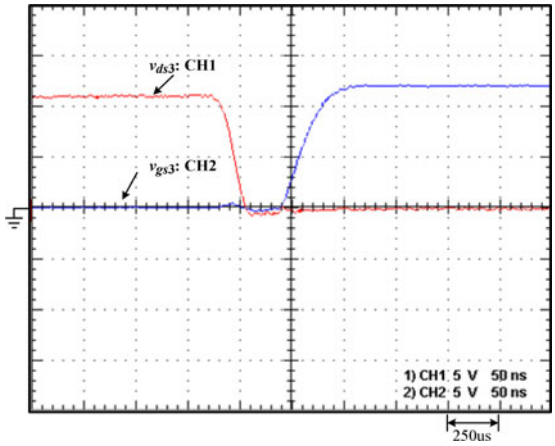

Fig. 24. Waveforms at rated load due to rising edge of $v_{\rm gs3}$: (1) $v_{\rm gs3}$ [5 V/div]; (2) $v_{\rm ds3}$ [5 V/div].

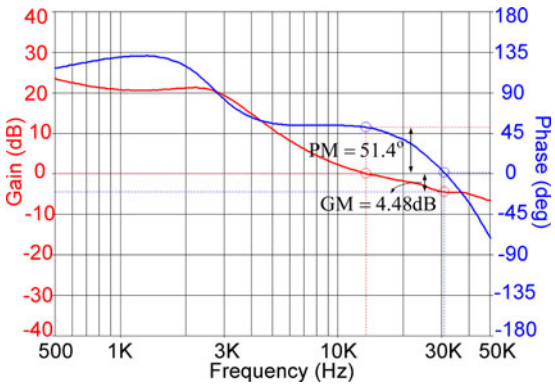

Fig. 25. Bode plot at half load with PM of 51.4° and GM of 4.48 dB.

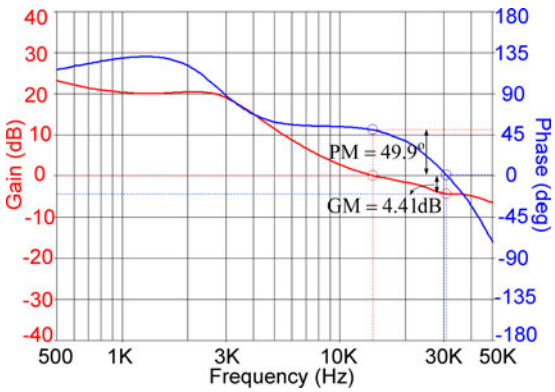

Fig. 26. Bode plot at rated load with PM of 49.9° and GM of 4.41 dB.

50% to 100% load, whereas Fig. 28 shows the load transient responses due to step load change from 100% to 50% load. From Figs. 27 and 28, it can be seen that the corresponding undershoot or overshoot is about 320 mV within the recovery time of 500 μs.

Furthermore, if the proposed converter operates at no load, the current in L_m will work both in the positive current region and in the negative current region, different from the design

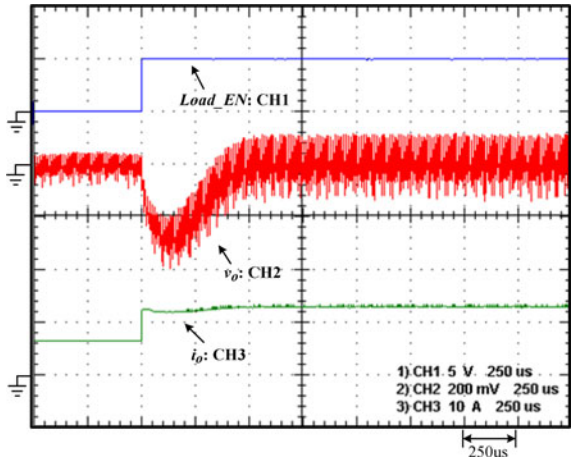

Fig. 27. Load transient responses due to step load change from 50% to 100% load: (1) *Load_EN*; (2) v_o; (3) i_o.

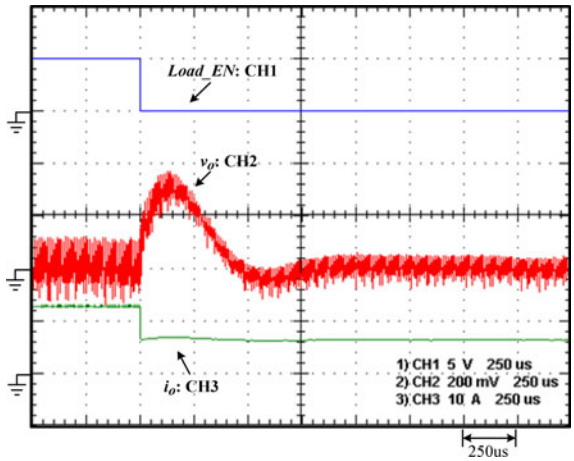

Fig. 28. Load transient responses due to step load change from 50% to 100% load: (1) *Load_EN*; (2) v_o; (3) i_o.

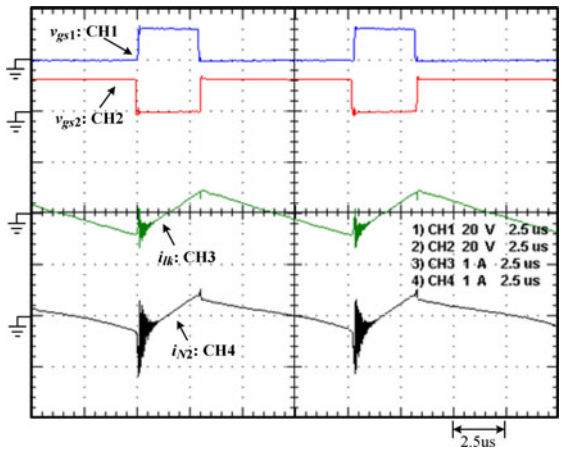

Fig. 29. Waveforms at no load: (1) $v_{\rm gs1}$ [20 V/div]; (2) $v_{\rm gs2}$ [20V/div]; (3) i_{lk} [1 A/div]; (4) i_{N_2} [1 A/div].

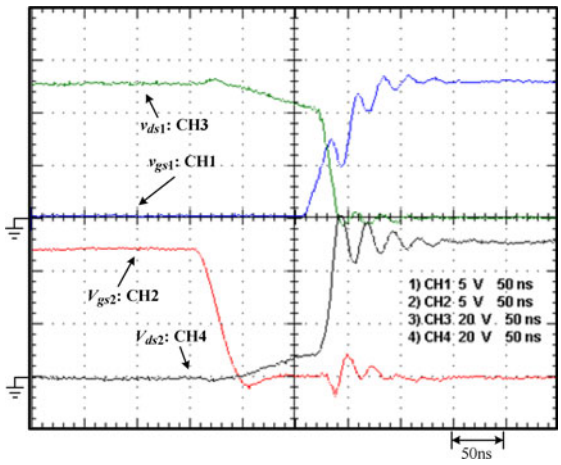

Fig. 30. Waveforms at no load due to rising edge of $v_{\rm gs1}$: (1) $v_{\rm gs1}$ [5 V/div]; (2) $v_{\rm gs2}$ [5 V/div]; (3) $v_{\rm ds1}$ [20V/div]; (4) $v_{\rm ds2}$ [20 V/div].

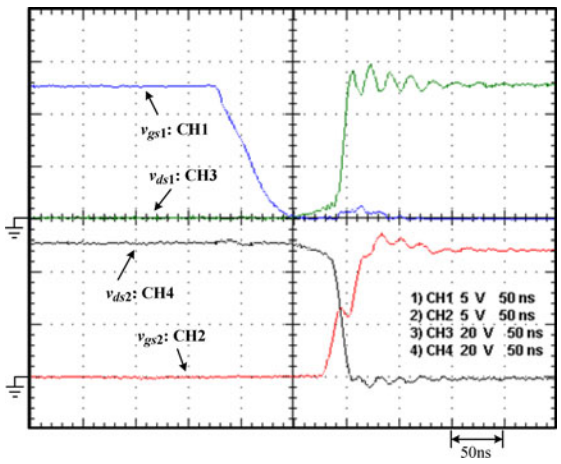

Fig. 31. Waveforms at no load due to rising edge of $v_{\rm gs2}$: (1) $v_{\rm gs1}$ [5 V/div]; (2) $v_{\rm gs2}$ [5 V/div]; (3) $v_{\rm ds1}$ [20 V/div]; (4) $v_{\rm ds2}$ [20 V/div].

condition that the converter always operates in the positive current region above minimum load as shown in Figs. 13–15. Since in practice, the current in L_m, named i_{Lm}, cannot be measured, only the current into the primary winding N_1, named i_{lk}, can be measured. Accordingly, the following waveforms relevant to no load condition are shown in Figs. 29–32. From Fig. 2, it can be seen that $i_{Lm} = i_{lk} + i_{N1} = i_{lk} + i_{N2} \times N_2/N_1 = i_{lk} + i_{N2}/3$. Hence, from Fig. 29, it can be seen that i_{lk} and i_{N_2} both have positive and negative values, implying that i_{Lm} has positive and negative values, and hence, the converter operates both in the positive current region and in the negative current region. Also, from Figs. 30–32, it can be seen that Q_1, Q_2, and Q_3 possess near ZVS turn-on to some extent.

In addition, if the input voltage variation percentage is $\pm 25\%$, then three input voltage levels of 36, 48, and 60 V are imposed on the converter. Fig. 33 shows the curves of efficiency versus load current under these three input voltage levels, whereas Fig. 34 shows the curves of output voltage versus load current under these three input voltage levels. From Fig. 33, it can be seen that the maximum efficiency is 96.1%, occurring at the input voltage of 36 V, whereas the efficiency at the rated load current

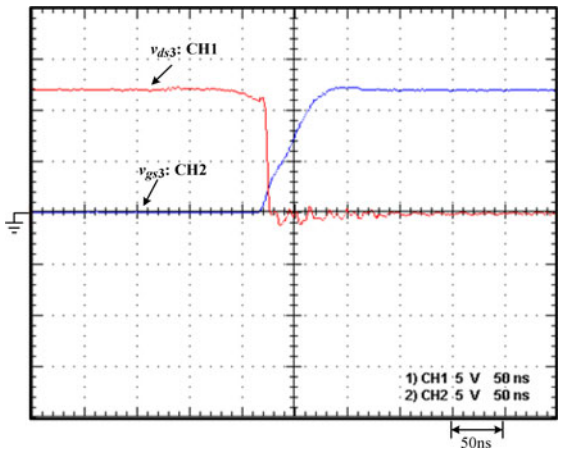

Fig. 32. Waveforms at no load due to rising edge of $v_{\rm gs3}$: (1) $v_{\rm ds3}$ [5 V/div]; (2) $v_{\rm gs3}$ [5 V/div].

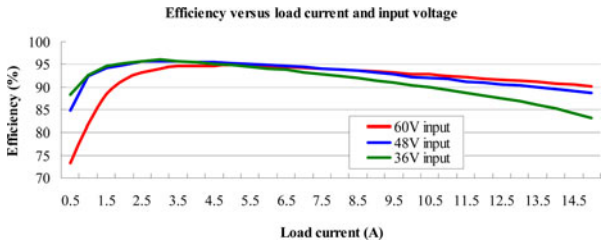

Fig. 33. Efficiency versus load current under three input voltage levels.

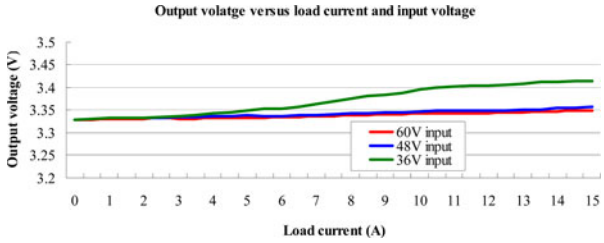

Fig. 34. Load regulation.

can be up to 90.2%, occurring at the input voltage of 60 V. In addition, from Fig. 34, it can be seen that the corresponding load regulations for three input voltage levels of 36, 48, and 60 V are 3.5%, 1.8%, and 1.5%, respectively.

VI. Conclusion

An ultrahigh step-down converter is presented herein. By combining one coupled inductor and one energy-transferring capacitor, the corresponding voltage conversion ratio can be much lower than that of the traditional buck converter. There are three merits in this converter as following: 1) the voltage conversion ratio of this converter does not have nonlinearity characteristics; 2) if one of the switches fails or is abnormally controlled, and in the meantime, any other two switches are made turned ON, then the high voltage does not appear in the output terminal, so the output load can be protected; and 3) the

proposed converter can be driven using existing SR buck PWM control ICs. To sum up, the structure of the proposed converter is quite simple and very suitable for industrial applications.

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