# Three-Level Single-Phase Bridgeless PFC Rectifiers

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***Abstract*—This paper presents new three-level unidirectional single-phase PFC rectifier topologies well suited for applications targeting high efficiency and/or high power density. The characteristics of a selected novel rectifier topology including its principles of operation, modulation strategy, feedback control scheme, and a power circuit design related analysis are presented. Finally, a 220-V/3-kW laboratory prototype is constructed and used in order to verify the characteristics of the new converter, which include remarkably low switching losses and single ac-side boost inductor, that allow for a 98.6% peak efficiency with a switching frequency of 140 kHz.**

***Index Terms*—AC–DC converter, high efficiency rectifier, multilevel converter, power factor correction, PWM modulation, PWM rectifier.**

## I. Introduction

An unidirectional high power factor single-phase ac–dc system assembled by cascading a single-phase diode bridge and a boost dc–dc converter is shown in Fig. 1(a). This converter system, known as conventional single-phase power factor correction (PFC) boost-type rectifier, has many interesting features that justify its extensive use in industry for power conversion below 1 kW, namely, it requires only one fast-switched diode $D_b$, it employs a single switch $S_b$, the gate signal of $S_b$, and the measurement circuits for the input/output voltages can be referenced to the same potential, i.e., the negative output voltage terminal; the inductor $L_b$ current can be measured with a shunt resistor also referenced to the negative output voltage terminal; it can be operated with relatively low complexity modulation and control strategies, where low cost dedicated analog integrated circuits can be employed, it displays relatively low common mode (CM) emission levels. As a result, this ac–dc converter typically features low production cost. Unfortunately, the current across $L_b$ is carried through three semiconductor devices in every operation stage, causing relatively high conduction losses. Additionally, in order to achieve high power density and/or low input current total harmonic distortion (THD), this circuit needs to operate at high switching frequencies, which can lead to unacceptably high switching losses since the switch and diode must commutate the full dc-link voltage.

Unidirectional single-phase PFC rectifier topologies featuring low conduction losses were proposed in [1]–[18]. Comparison among this type of topologies was performed in [19]–[22], while appropriate control techniques and electromagnetic compatibility solutions to this type of converters were discussed in [23]–[27] and [28]–[31], respectively. Some of the mentioned low conduction losses PFC rectifiers are presented in Fig. 1(b)–(h). These ac–dc topologies, which are examples of the bridgeless rectifier technology, have only two devices conducting current in at least one of their current conduction states. This characteristic can expressively enhance the conduction loss performance in such systems especially for power conversion levels above 1 kW. The circuits shown in Fig. 1(b)–(g) present a similar operating principle, indeed the main difference is found in the implementation of the bidirectional four quadrant switch, i.e., the active switches $S_{i,A}$ and $S_{i,N}$ with $i = 1$ or 2 in Fig. 1(b)–(d) are implemented with a single switch $S_1$ in Fig. 1(e)–(g). The converter concepts illustrated in Fig. 1(h) is recommended when aiming for high power density. This circuit can be modulated in such a way that the current ripple across the boost inductor displays twice the frequency of the one achieved with the conventional circuit shown in Fig. 1(a) [3] for a given switching frequency. Hence, the required inductance to fulfill a maximum current ripple design criteria for a given switching frequency will be half the value of the one necessary for the conventional system [18].

In this context, bridgeless PFC rectifiers are appropriate solutions regarding conduction losses. However, the power semiconductor devices in these converters must typically withstand and commutate the full dc-link voltage and, thus, present appreciable switching losses. To improve this characteristic and enable the use of higher switching frequencies, multilevel converters can be employed to build PFC rectifier topologies. With this, the switched voltage steps are reduced and also the resulting switching losses.

This paper presents new three-level unidirectional single-phase high power factor rectifier topologies that combine many features of the bridgeless rectifiers shown in Fig. 1. The proposed converter topologies are shown in Fig. 2(d)–(i). The topologies shown in Fig. 2 present three distinct dc voltage levels per converter arm for controlling the input current, which not only leads to a substantial volume reduction of the boost inductor, but also to lower switching losses when compared to the conventional two-level PFC rectifiers depicted in Fig. 1. In addition, the proposed converters can also achieve lower conduction losses than the conventional system [see Fig. 1(a)], as in some conduction states only two semiconductor devices carry the inductor current and some of the semiconductors are rated for one-half of the

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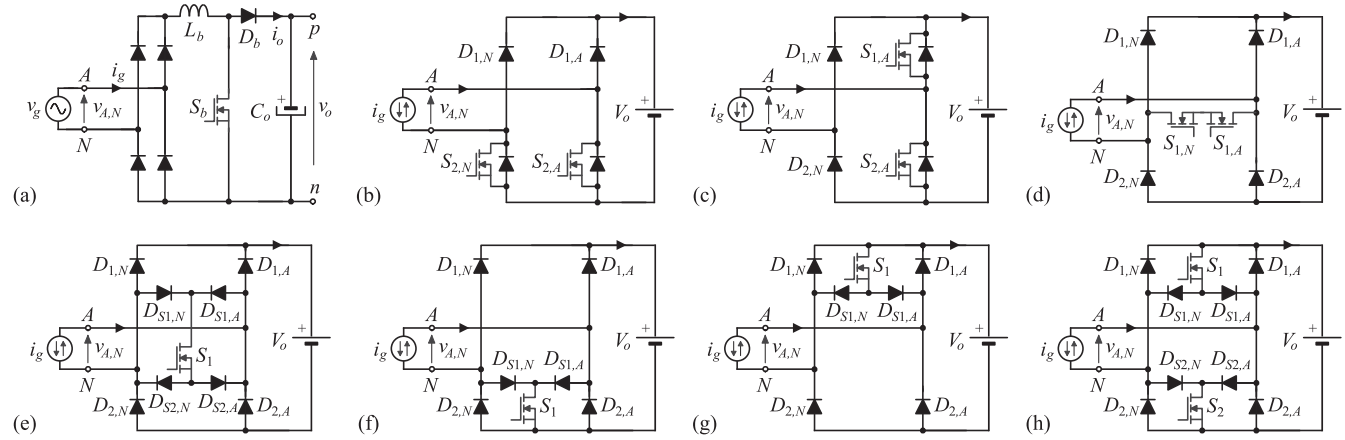


Fig. 1. Single-phase unidirectional PFC rectifiers: (a) conventional system; and bridgeless technology rectifiers: (b) and (c) standard version; (d)–(g) employing bidirectional four quadrant switch; and, (h) multiplying the effective switching frequency across the input inductor.

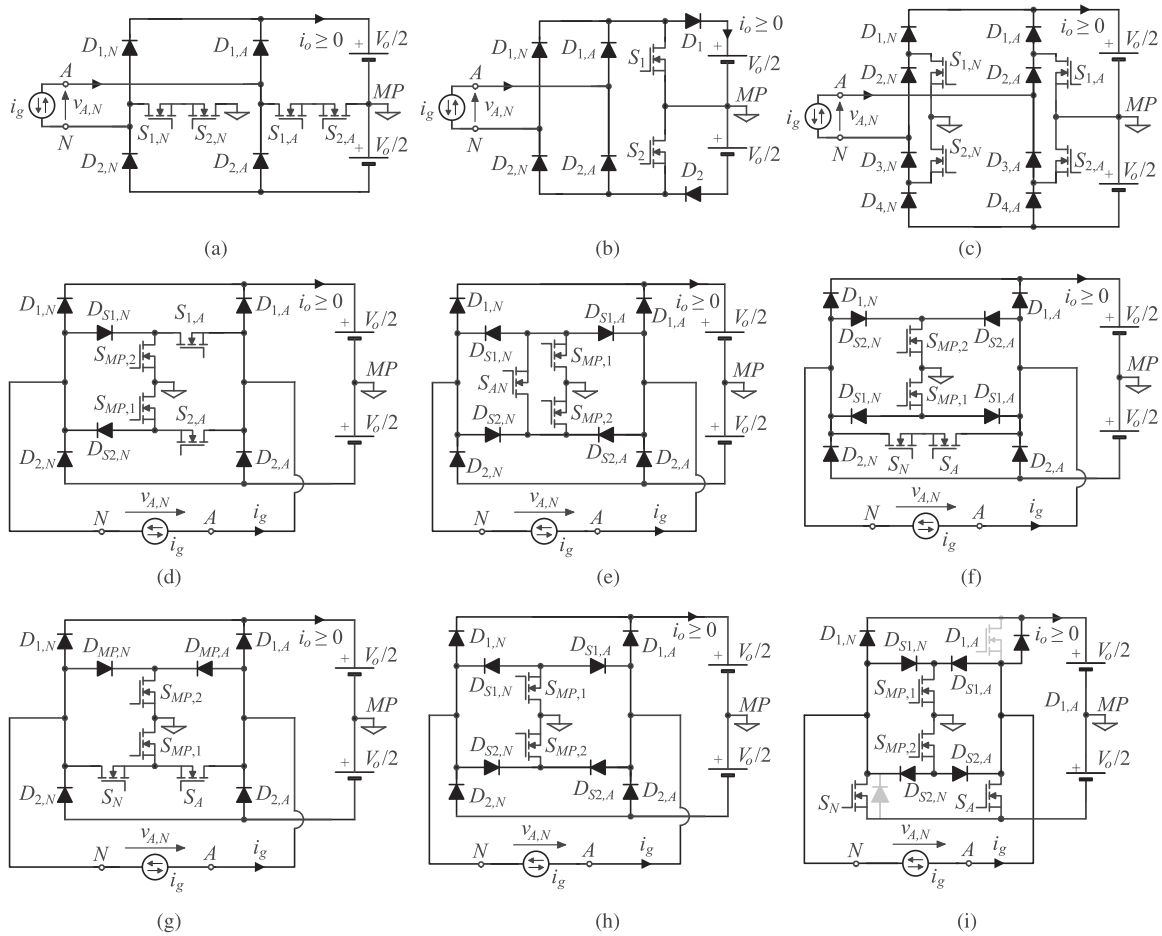


Fig. 2. Single-phase three-level boost-type PFC rectifiers: (a)–(c) conventional circuits; and (d)–(i) new topologies.

dc-link voltage. These characteristics make the new rectifiers well suited for applications aiming for high efficiency and/or high power density.

This paper is organized as follows. Initially, new multilevel unidirectional single-phase PFC rectifiers are introduced in Section II and compared with other well-known systems. Additionally, the explanation of the structural characteristics of a remarkable converter, including a suitable modulation strategy and feedback control method, guaranteeing PFC operation, is presented. The analytical equations for calculating the power semiconductors stresses with dependency on the input current amplitude and the voltage transfer ratio of the converter are given

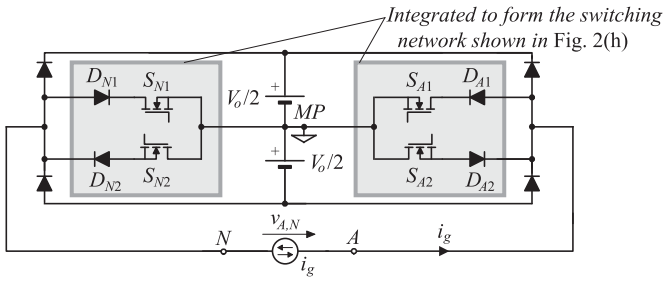


Fig. 3. Single-phase three-level rectifier.

in Section III. Finally, in Section IV, a 3-kW hardware prototype is designed to attest the feasibility of the presented converter. Experimental results with such prototype are presented including measured efficiency levels.

## II. Single-Phase Three-Level Boost-Type PFC Rectifiers

Known single-phase three-level[1] boost-type rectifiers [19], [20], [32]–[45] are shown in Fig. 2(a)–(c). Six new rectifier circuits are proposed in Fig. 2(d)–(i), where the dc-load plus the dc-link capacitors are replaced by two dc voltages ($V_o/2$) and the single-phase power grid plus filters and ac-side boost inductor are replaced by bidirectional current sources $i_g$. These rectifier concepts are suitable solutions for increasing the efficiency of wide input voltage range single-phase high switching frequency PFC rectifiers because of the inherent voltage doubling capability that is achieved through a proper modulation pattern.

The derivation of the topology shown in Fig. 2(d)–(i) can be understood considering the single-phase three-level rectifier topology depicted in Fig. 3. This can be seen as a variation of the circuit shown in Fig. 2(a) [19] or single-phase version of a Vienna-type rectifier [46]. Redrawing this and integrating the switching network composed of $D_{1,N}$, $D_{2,N}$, $D_{1,A}$, $D_{2,A}$, $S_{1,N}$, $S_{2,N}$, $S_{1,A}$, and $S_{2,A}$ leads to the topology shown in Fig. 2(h), which has half the number of turn-off switches. The other topologies are generated by replacing discrete diodes by MOSFETs in Fig. 2(h) or by changing or incorporating the bidirectional four quadrant switch across the terminal $A$ and $N$.

As seen in the comparison characteristics compiled in Table I the new topologies present a lower number of semiconductors in the current paths when compared with the conventional three-level circuits, i.e., the rectifiers in Fig. 2(a)–(c). Additionally, the proposed rectifiers avoid the use of selective switches and allow low conduction losses for wide operation range. Furthermore, even though some of the semiconductors are to be rated to withstand the full dc-link voltage, all commutations occur under half of the dc-link voltage. This leads to reduced switching losses when compared to the converters in Fig. 1.

A relative cost analysis for the considered three-level rectifier is presented in the last row of Table I. This considers only power semiconductor devices, boost inductor, and dc capacitors. The values were obtained from Digi-Key Corporation online in February 2014 considering the price for 1000 pieces of each device according to the example given in Table IV and normalized to the cost of the topology in Fig. 2(b). Even though the number of semiconductors is substantially increased for the proposed ac–dc converters when compared to two-level solutions (see Fig. 1), these topologies are indicated where very high efficiency and/or switching frequencies are required. As the circuits are symmetric and present reduced voltage steps, the generated CM voltages are reduced. The CM voltage steps are one quarter of the full dc-link voltage in contrast to one half of the full dc-link voltage in typical two-level bridgeless rectifiers. The passive components losses are typically dominated by the boost inductor. With the three-level topologies, these losses are typically much lower since the voltage steps over the boost inductor are only one half of the dc-link voltage. Thus, the inductance and the size of the boost inductor are reduced. The circuits in Fig. 2(d)–(i) present redundant switching states for levels 0, $\pm V_o/2$ that allows the distribution of losses among the turn-off devices. Lower conduction losses can be achieved with the topologies in Fig. 2(d), (f), (g), and (i), where only two semiconductors are in the current path while imposing the 0 level. From Table I, it can be observed that the topology depicted in Fig. 2(g) is a very promising PFC solution due to lower conduction losses, and the lower number of diodes and gate driver potentials. This circuit, which is redrawn in Fig. 4 to include the main passive components, is explained and analyzed in the following sections. Finally, the topology in Fig. 2(h) reduces the number of turn-off devices to only two at the expense of higher conduction losses during the level 0. This can be a much lower cost circuit since switches $S_{\mathrm{MP},1}$ and $S_{\mathrm{MP},2}$ are rated for only half of the dc-link voltage. The rectifier in Fig. 2(i) is a hybrid option that incorporates the proposed topology and a conventional two-level bridgeless converter. It can be assembled with $D_{1,A}$ and $S_N$ being exchanged by the gray devices. The disadvantages of the proposed topologies in comparison to two-levels bridgeless ones are: the increased number of power semiconductors, the higher number of isolated gate driver potentials, the increased modulation complexity due to the larger number of possible switching states, and the necessity of splitting the dc-link capacitance into two capacitors.

Comparing the rectifiers in Fig. 2(a)–(c) exemplarily with the one proposed in Fig. 2(g) leads to the following conclusions. The boost inductor ripple for a given switching frequency is also the same since the topologies in Fig. 2(a)–(c) and (g) can be modulated in a similar way and, thus, ideally apply a five-level voltage at the ac-side terminals. The same is valid for the dc-link capacitors current, i.e., the dc-side terminals currents are generated in the same way. In summary, the external characteristics of these topologies are equivalent. However, the efficiency of the proposed topology tends to be higher since conduction losses will be lower. This reduction in conduction losses occurs because the proposed topology presents less power semiconductors in the current path, except in the $\pm V_o$ states with the topology in Fig. 2(a), which is the same as the proposed PFC circuits. Switching losses are approximately unchanged if

[1]This paper considers the synthesizable number of voltage levels per converter leg as the defining factor to define the number of levels of a static converter.

TABLE I
COMPARISON OF SINGLE-PHASE THREE-LEVEL PFC CONCEPTS

| Parameter | Topology | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Fig. 2 | (a) | (b) | (c) | (d) | (e) | (f) | (g) | (h) | (i) |
| Semiconductors in the current path to generate voltage level $V_o = 0$ | 4 | 4 | 4 | 2 | 3 | 2 | 2 | 4 | 2 |
| Semiconductors in the current path to generate voltage level $\pm V_0/2$ | 3 | 4 | 4 | 3 | 3 | 3 | 3 | 3 | 3 |
| Semiconductors in the current path to generate voltage level $\pm V_0$ | 2 | 4 | 4 | 2 | 2 | 2 | 2 | 2 | 2 |
| Total number of MOSFETs | 4 | 2 | 4 | 4 | 3 | 4 | 4 | 2 | 4 |
| MOSFETs rated to $V_o$ | 0 | 0 | 0 | 2 | 1 | 2 | 2 | 0 | 2 |
| MOSFETs rated to $V_o/2$ | 4 | 2 | 4 | 2 | 2 | 2 | 2 | 2 | 2 |
| Total number of diodes | 4 | 6 | 8 | 6 | 8 | 8 | 6 | 8 | 6 |
| Diodes rated to $V_o$ | 4 | 4 | 0 | 6 | 8 | 8 | 6 | 8 | 6 |
| Diodes rated to $V_o/2$ | 0 | 2 | 8 | 0 | 0 | 0 | 0 | 0 | 0 |
| Slow diodes | 0 | 4 | 4 | 0 | 0 | 0 | 0 | 0 | 0 |
| Fast diodes | 4 | 2 | 4 | 6 | 8 | 8 | 6 | 8 | 6 |
| Diodes with reduced reverse recovery | 4 | 2 | 4 | 4 | 4 | 4 | 4 | 4 | 2 |
| Gate drivers insulated potentials | 2 | 2 | 3 | 3 | 2 | 3 | 2 | 2 | 3/4 |
| Power components relative cost | 1.23 | 1.00 | 1.09 | 1.33 | 1.29 | 1.37 | 1.33 | 1.22 | 1.19 |

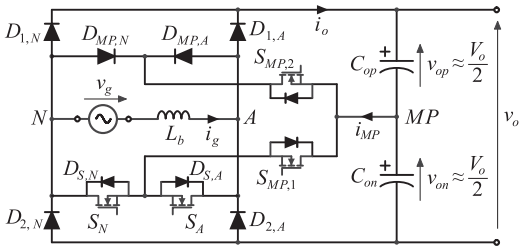


Fig. 4. New unidirectional high-efficiency multilevel single-phase bridgeless rectifier.

similar semiconductors are employed. This is because all switching transitions in the proposed converter occur with just one half of the dc-link voltage.

### A. Current Conduction States

The single-phase boost-type PFC rectifier depicted in Fig. 4 utilizes four active switches ($S_A$, $S_N$, $S_{\mathrm{MP},1}$ and $S_{\mathrm{MP},2}$), and six discrete diodes ($D_{\mathrm{MP},N}$, $D_{\mathrm{MP},A}$, $D_{1,N}$, $D_{1,A}$, $D_{2,N}$, and $D_{2,A}$). Diodes $D_{1,N}$, $D_{1,A}$, $D_{2,N}$, and $D_{2,A}$ are fast-switched devices, i.e., will be required to commutate under current, while the diodes $D_{\mathrm{MP},N}$ and $D_{\mathrm{MP},A}$ and the body diodes of $S_N$ and $S_A$ are switched OFF by $S_{\mathrm{MP},1}$ and $S_{\mathrm{MP},2}$. Therefore, $D_{\mathrm{MP},N}$ and $D_{\mathrm{MP},A}$ can be implemented with standard fast or ultrafast silicon diodes with relatively low forward voltage drop, while the four bridge diodes would benefit from SiC or GaN semiconductor technology. The intrinsic diodes of the MOSFETs $S_A$ and $S_N$ ($D_{S,A}$ and $D_{S,N}$) are used in the circuit operation and can profit from the low forward voltage drop body diode characteristics of superjunction MOSFETs. Interestingly, the switches $S_A$, $S_N$, and $S_{\mathrm{MP},1}$ have the same reference for their gate command, which simplifies and reduces the cost of isolated gate drive circuits. As illustrated in Fig. 4, the dc-link is constructed with two series connected capacitors that allow the formation of five voltage levels across the terminals $A$ and $N$ ($v_{A,N} = 0, \pm V_o/2$, or $\pm V_o$). Figs. 5 and 6 show the rectifier current conduction states for positive and negative input currents $i_{Lb}$, respectively. There are two redundant switching states for the formation of $v_{AN} = \pm V_o/2$ (states 2 and 3), which results in different current $i_{\mathrm{MP}}$ direction across the midpoint MP of the output capacitors $C_{op}$ and $C_{\mathrm{on}}$. Hence, this feature can be used for balancing the voltages across the dc-link capacitors. Enabling $S_{\mathrm{MP},1}$ [see Fig. 5(b)] charges $C_{op}$ and discharges $C_{\mathrm{on}}$, while the opposite occurs if $S_{\mathrm{MP},2}$ conducts. For improved conduction losses while implementing the state $v_{A,N} = 0$ [see Figs. 5(a) and 6(a)], the switches $S_{\mathrm{MP},1}$ and $S_{\mathrm{MP2}}$ could also be turned ON together with $S_A$ and $S_N$. In this case, two parallel paths across the semiconductors are created for the impressed current. Alternatively, the state $v_{A,N} = 0$ could also be implemented by solely turning on $S_{\mathrm{MP},1}$ and $S_{\mathrm{MP},2}$, while all the remaining active devices are switched OFF.

### B. PWM Modulation Strategy and Feedback Control Scheme

A suitable feedback control scheme able to regulate the output voltage of the proposed converter $v_o$ and shape the ac-side current $i_{Lb}$ is presented in Fig. 7. Therein, a slow outer control loop is used to regulate the output voltage $v_o$ to a constant reference voltage $v_o$* and to generate a reference signal $i_{Lb}$* for the fast inner current control loop with similar waveform shape of the rectified input voltage $v_g$. Additionally, a logic signal $S_{\mathrm{MP,sel}}$ is used to guide the selection of the redundant current conduction state (states 2 and 3) in order to balance the partial dc-link voltages $v_{op}$ and $v_{\mathrm{on}}$. The gate commands for $S_A$, $S_N$, $S_{\mathrm{MP},1}$, and $S_{\mathrm{MP},2}$ are guided by the logic signals $s_{\mathrm{AN}}$ and $s_{\mathrm{MP}}$ which are generated by comparing the feedback control signal $m$ with the two interleaved triangular carriers $c_{\mathrm{AN}}$ and $c_{\mathrm{MP}}$. Carriers $c_{\mathrm{AN}}$ and $c_{\mathrm{MP}}$ are particularly arranged as shown in Fig. 8.

In the proposed PWM modulator, the transition of the signal $s_{\mathrm{MP,sel}}$ is synchronized with the peak of $c_{\mathrm{AN}}$ in order to reduce the switching losses across $S_{\mathrm{MP},1}$ and $S_{\mathrm{MP},2}$ for $m < 1/2$. In this case, due to the $180^\circ$ phase-shift between $c_{\mathrm{AN}}$ and $c_{\mathrm{MP}}$ the transition between states 2 and 3 occurs after passing through an intermediate state (see state 1), ensuring the commutation of $S_{\mathrm{MP},1}$ and $S_{\mathrm{MP},2}$ under zero current. Although it is possible to set the converter operation $v_{A,N} = 0$ by solely switching $S_A$ when $i_{Lb}$ is positive or by only gating $S_N$ for negative

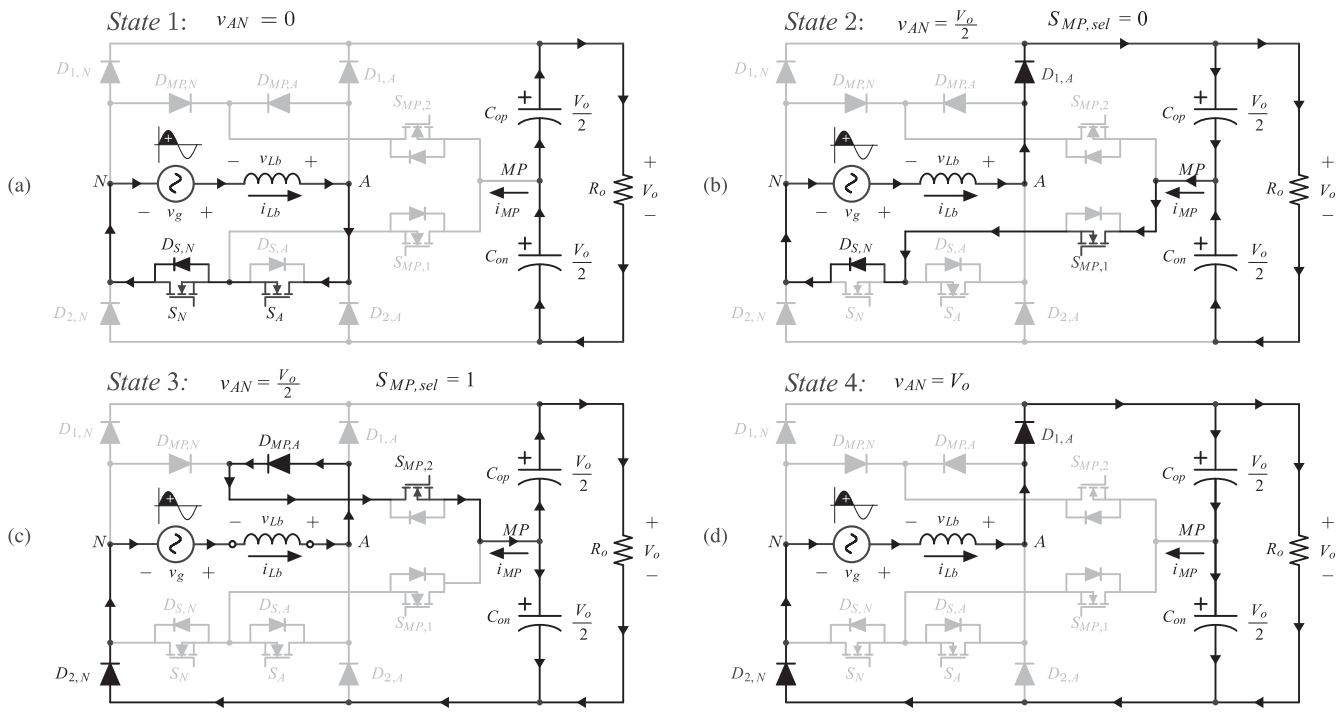


Fig. 5. Rectifier current conduction states for $i_{Lb} > 0$: (a) $v_{A,N} = 0$; (b) and (c) $v_{A,N} = V_o/2$; or (d) $v_{A,N} = V_o$. Note that the state $v_{A,N} = 0$ could also be implemented by solely turning on $S_{\mathrm{MP},1}$ and $S_{\mathrm{MP},2}$, while all the remaining active devices are switched OFF.

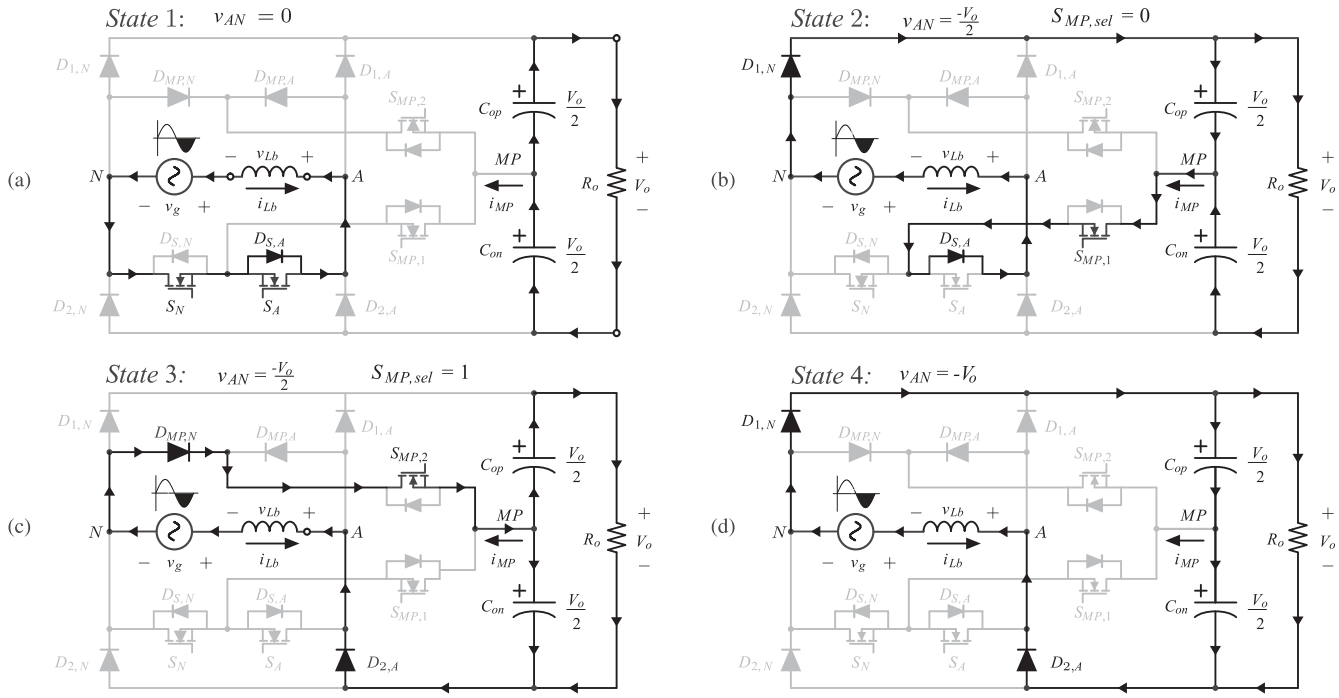


Fig. 6. Rectifier current conduction states for $i_{Lb} < 0$: (a) $v_{A,N} = 0$; (b) and (c) $v_{A,N} = -V_o/2$; or (d) $v_{A,N} = -V_o$. Note that the state $v_{A,N} = 0$ could also be implemented by solely turning on $S_{\mathrm{MP},1}$ and $S_{\mathrm{MP},2}$, while all the remaining active devices are switched OFF.

$i_{Lb}$, these switches are always simultaneously commanded in the suggested scheme, following the comparison between $m$ and $c_{\mathrm{AN}}$. This logic reduces the conduction losses across the MOSFETs $S_A$ and $S_N$ [see Figs. 5(a) and 6(a)] and also simplifies their command circuits. As a result of the suggested PWM modulator, the duty cycle of $S_{\mathrm{AN}}$ and $S_{\mathrm{MP}}$ will be given by

$$d_{\mathrm{AN}} = \begin{cases} 1 - 2m & \text{if } m \leq 1/2 \\ 0 & \text{if } m > 1/2 \end{cases} \tag{1}$$

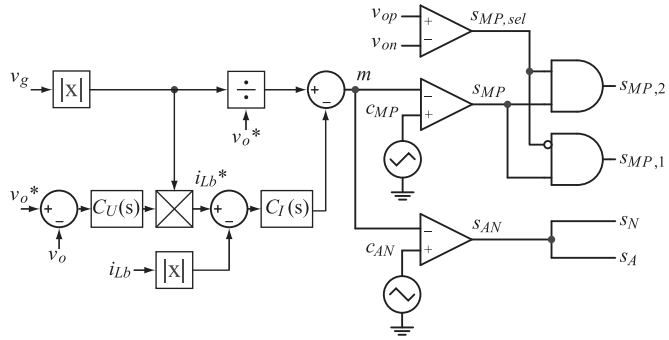


Fig. 7. Appropriate feedback control scheme and PWM modulator circuit.

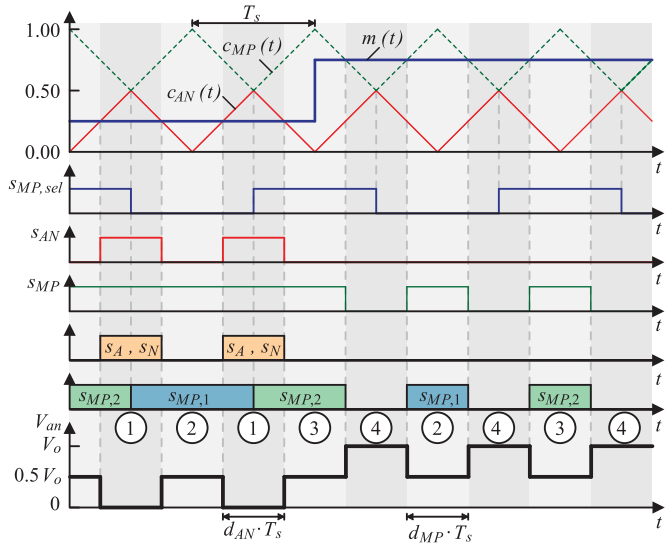


Fig. 8. Suggested PWM modulation scheme. Note that for each switching transition the respective active conduction state is shown.

which leads to a modulated ac terminal voltage $v_{A,N}$ with a time averaged value within a switching period $T_s$ equals

$$\langle v_{A,N}\rangle_{T_s} \approx m \cdot \langle v_o\rangle_{T_s} = m \cdot V_o. \tag{2}$$

Considering that the system is fed by a sinusoidal input voltage $v_g$ with an amplitude value of $V_{gp}$

$$v_g = V_{gp} \cdot \sin(\omega_g t) \tag{3}$$

high power factor operation, where $i_{Lb}$ has sinusoidal shape in-phase with $v_g$

$$i_{Lb} = I_{gp} \cdot \sin(\omega_g t) \tag{4}$$

and also a negligible voltage drop across $L_b$ at the grid frequency, the instantaneous terminal voltage value can be approximated by

$$v_{A,N} = v_g - v_{Lb} = v_g - L_b \cdot \frac{d}{dt} i_{Lb} \tag{5}$$

$$v_{A,N} = V_{gp} \cdot \sin(\omega_g t) - \underbrace{\omega_g \cdot L_b \cdot V_{gp} \cdot \cos(\omega_g t)}_{\approx 0} \tag{6}$$

$$v_{A,N} \approx v_g = V_{gp} \cdot \sin(\omega_g t) = m \cdot V_o. \tag{7}$$

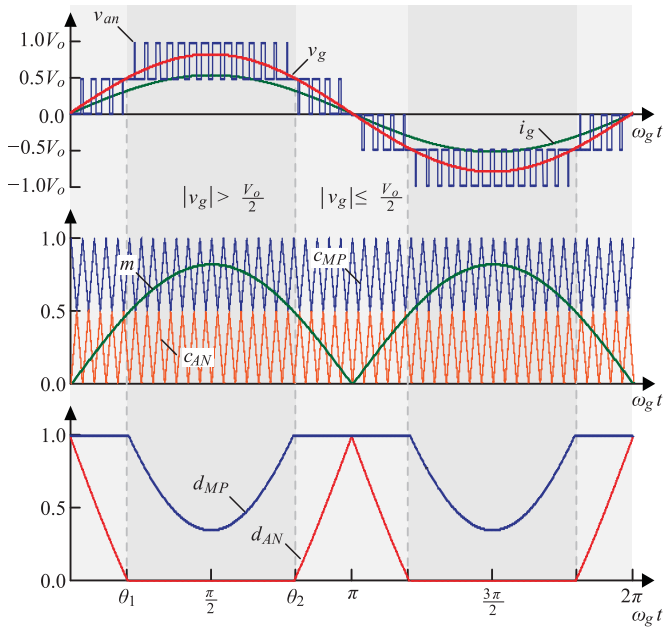


Fig. 9. Idealized main rectifier waveforms for high power factor operation.

Hence, assuming steady-state conditions, high power factor operation and low voltage drop at the mains frequency over the boost inductor the PWM modulation signal $m$ will be given by

$$m = \frac{V_{gp}}{V_o} \cdot \sin(\omega_g t) \tag{8}$$

which, combined with (1) and (2), leads to the duty cycle functions for $S_{\mathrm{AN}}$ and $S_{\mathrm{MP}}$ as follows:

$$d_{\mathrm{AN}} = \begin{cases} 1 - \dfrac{2V_{gp}}{V_o} \cdot \sin(\omega_g t) & \text{if } |v_g| \leq \dfrac{V_o}{2} \\ 0 & \text{if } |v_g| > \dfrac{V_o}{2} \end{cases} \tag{9}$$

$$d_{\mathrm{MP}} = \begin{cases} 1 & \text{if } |v_g| \leq \dfrac{V_o}{2} \\ 2 - \dfrac{2V_{gp}}{V_o} \cdot \sin(\omega_g t) & \text{if } |v_g| > \dfrac{V_o}{2}. \end{cases} \tag{10}$$

Fig. 9 illustrates the main waveforms for rectifier operation during one grid period. Therein, two distinctive converter operating regions can be observed:

1) $|v_g| \leq V_o/2$: the system will alternate between the voltage levels $|v_{A,N}| = 0$ and $|v_{A,N}| = V_o/2$ (switching states 1, 2, and 3);
2) $|v_g| > V_o/2$: the system will operate with the voltage levels $|v_{A,N}| = V_o/2$ and $|v_{A,N}| = V_o$ (states 2, 3, and 4).

Note that the angles $\theta_1$ and $\theta_2$, given in (12), delimit the boundary between these two operating regions

$$\theta_1 = \arcsin\left(\frac{V_0}{2V_{gp}}\right) \tag{11}$$

$$\theta_2 = \pi - \arcsin\left(\frac{V_0}{2V_{gp}}\right). \tag{12}$$

## III. PFC Rectifier Design Guidelines

In this section, means for determining the current and voltage stresses of the active and passive components of the proposed single-phase PFC rectifier depicted in Fig. 2(g) are given. In order to allow estimation of the converter on-state losses, the current rms and average values have to be calculated. Therefore, simple analytical approximations with dependence on the system operating parameters are derived. For the following calculations, it is assumed that the rectifier presents: sinusoidal ac-side current, ohmic fundamental grid behavior, a constant dc voltage $V_o$, no low-frequency voltage drop across the inductor $L_b$, and a switching frequency $f_s$ which is much higher than the grid frequency $f_g$ ($f_s \gg f_g$).

### A. Semiconductor Voltage and Current Stresses

The voltage stress on the switches $S_{\mathrm{MP},1}$ and $S_{\mathrm{MP},2}$ is defined by the partial dc-link voltages, which ideally is $V_o/2$. All the remaining semiconductors ($D_{1,N}$, $D_{1,A}$, $D_{2,N}$, $D_{2,A}$, $D_{\mathrm{MP},N}$, $D_{\mathrm{MP},A}$, $S_A/D_{S,A}$, and $S_N/D_{S,N}$ ) have to block the full output voltage $V_o$. The average and rms current values for the transistors and diodes can be determined as given in (8)–(24). Therein, the analytical calculations for $S_A/D_{S,A}$ and $S_N/D_{S,N}$ consider that during $v_{A,N}=0$ the current $i_{Lb}$ is not shared between these devices, as it would be for MOSFETs (see Figs. 5 and 6)

$$M = \frac{V_{gp}}{V_o} \tag{13}$$

$$\beta = \sqrt{4 - \frac{1}{M^2}} \tag{14}$$

$$I_{D1/2\mathrm{AN,avg}} = \frac{I_{gp} M}{4} \tag{15}$$

$$I_{D_{1/2\mathrm{AN}},\mathrm{rms}} = I_{gp}\sqrt{\frac{2M}{3\pi}} \tag{16}$$

$$I_{D_{\mathrm{SAN}},\mathrm{avg}} = I_{gp}\left[\frac{1}{\pi} - \frac{M}{4}\right] \tag{17}$$

$$I_{D_{\mathrm{SAN}},\mathrm{rms}} = I_{gp}\sqrt{\frac{1}{4} - \frac{2M}{3\pi}} \tag{18}$$

$$I_{S_{\mathrm{AN}},\mathrm{avg}} = \begin{cases} I_{gp}\left[\dfrac{1}{\pi} - \dfrac{M}{2}\right] & \text{if } M \le \dfrac{1}{2} \\ \dfrac{I_{gp}}{\pi}\left[1 - \dfrac{\beta}{4} - M\theta_1\right] & \text{if } M > \dfrac{1}{2} \end{cases} \tag{19}$$

$$I_{S_{\mathrm{AN}},\mathrm{rms}} = \begin{cases} I_{gp}\sqrt{\dfrac{1}{4} - \dfrac{4M}{3\pi}} & \text{if } M \le \dfrac{1}{2} \\ I_{gp}\sqrt{\dfrac{1}{\pi}\left[\beta\left(\dfrac{2M}{3} - \dfrac{1}{24M}\right) - \dfrac{4M}{3} + \dfrac{\theta_1}{2}\right]} & \text{if } M > \dfrac{1}{2} \end{cases} \tag{20}$$

$$I_{S_{\mathrm{MP}},\mathrm{avg}} = \begin{cases} \dfrac{I_{gp} M}{2} & \text{if } M \le \frac{1}{2} \\ I_{gp}\left[\dfrac{\beta}{2\pi} + \dfrac{2M\theta_1}{\pi} - \dfrac{M}{2}\right] & \text{if } M > \dfrac{1}{2} \end{cases} \tag{21}$$

$$I_{S_{\mathrm{MP}},\mathrm{rms}} = \begin{cases} I_{gp}\sqrt{\dfrac{4M}{3\pi}} & \text{if } M \le \dfrac{1}{2} \\ I_{gp}\sqrt{\dfrac{1}{\pi}\left[\beta\left(\dfrac{1}{12M} - \dfrac{4M}{3}\right) + \dfrac{4M}{3} - \theta_1\right] + \dfrac{1}{2}} & \text{if } M > \dfrac{1}{2} \end{cases} \tag{22}$$

$$I_{D_{\mathrm{MP}},\mathrm{avg}} = \begin{cases} \dfrac{I_{gp} M}{4} & \text{if } M \le \dfrac{1}{2} \\ I_{gp}\left[\dfrac{\beta}{4\pi} + \dfrac{M\theta_1}{\pi} - \dfrac{M}{4}\right] & \text{if } M > \dfrac{1}{2} \end{cases} \tag{23}$$

$$I_{D_{\mathrm{MP}},\mathrm{rms}} = \begin{cases} I_{gp}\sqrt{\dfrac{2M}{3\pi}} & \text{if } M \le \dfrac{1}{2} \\ I_{gp}\sqrt{\dfrac{1}{\pi}\left[\beta\left(\dfrac{1}{24M} - \dfrac{2M}{3}\right) + \dfrac{2M}{3} - \dfrac{\theta_1}{2}\right] + \dfrac{1}{4}} & \text{if } M > \dfrac{1}{2}. \end{cases} \tag{24}$$

The current efforts obtained with (8)–(24) are shown graphically in Fig. 10, as a function of the modulation index $M$ and normalized according to the input current peak and the output current. This second normalization procedure shows how the current efforts vary for fixed output voltage and power. This happens with the variation of the ac voltage in a given power level and is very meaningful for the operation of PFC rectifiers.

### B. Frequency Spectra

The five-level ac-side voltage $v_{\mathrm{AN}}$, also known as the rectifier differential mode voltage (DM), for the proposed modulation strategy is defined by

$$v_{\mathrm{AN}} = V_o M\cos(\theta_g) + \frac{2V_o}{\pi}\sum_{m=1}^{\infty}\left[\frac{1}{2m}\sum_{n=-\infty}^{\infty}\mathrm{J}_{2n+1}(2m\pi M) \cdot\cos(n\pi)\cos\left[m\theta_c + (2n+1)\theta_g\right]\right] \tag{25}$$

from where the amplitudes of the frequency harmonics can be found.

The CM voltage of the proposed rectifier is given by

$$v_{\mathrm{CM}} = \frac{v_{A,\mathrm{MP}} + v_{N,\mathrm{MP}}}{2} \tag{26}$$

which finally results in

$$v_{\mathrm{CM}} = \frac{4V_o}{\pi^2}\sum_{m=1}^{\infty}\left\{\frac{1}{2m-1}\sum_{k=1}^{\infty}\left[\frac{\mathrm{J}_{2k-1}(2m-1)\pi m}{(2k-1)}\right] \times\cos\left[\left(\frac{2m-1}{2}\right)\theta_c\right]\right\} + \frac{4V_o}{\pi^2}\left\{\sum_{m=1}^{\infty}\frac{1}{2m-1}\right.$$

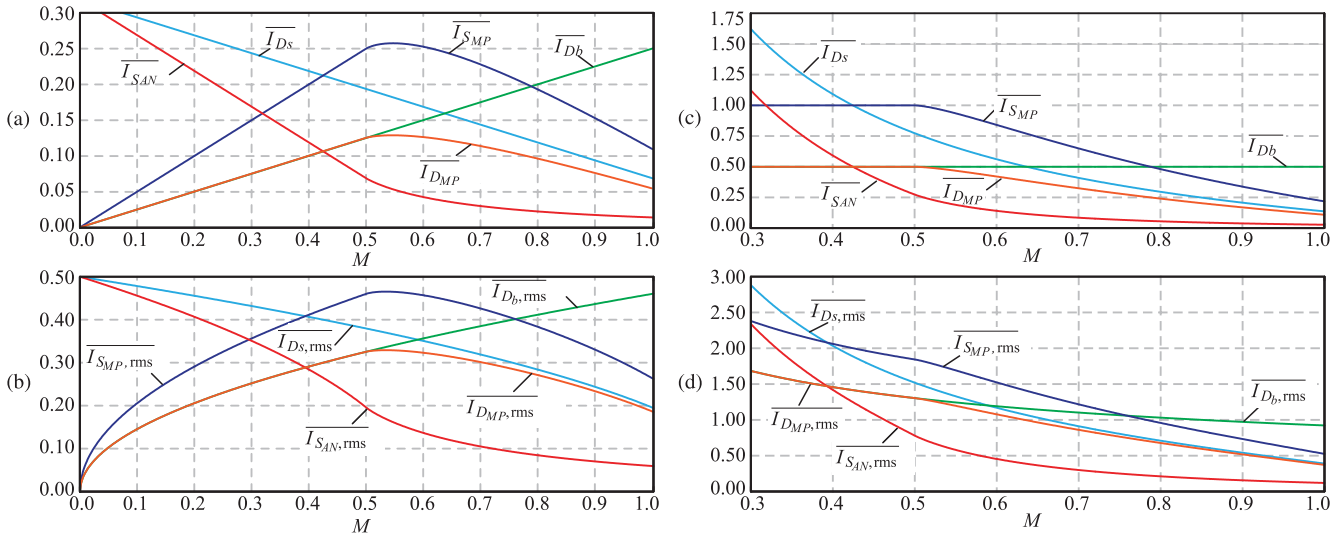


Fig. 10. Semiconductor current efforts as functions of the modulation index $M$ and normalized: (a)–(b) with respect to the input current peak $I_{gp}$; and, (c)–(d) with respect to the output current, given by $P_o/V_o$.

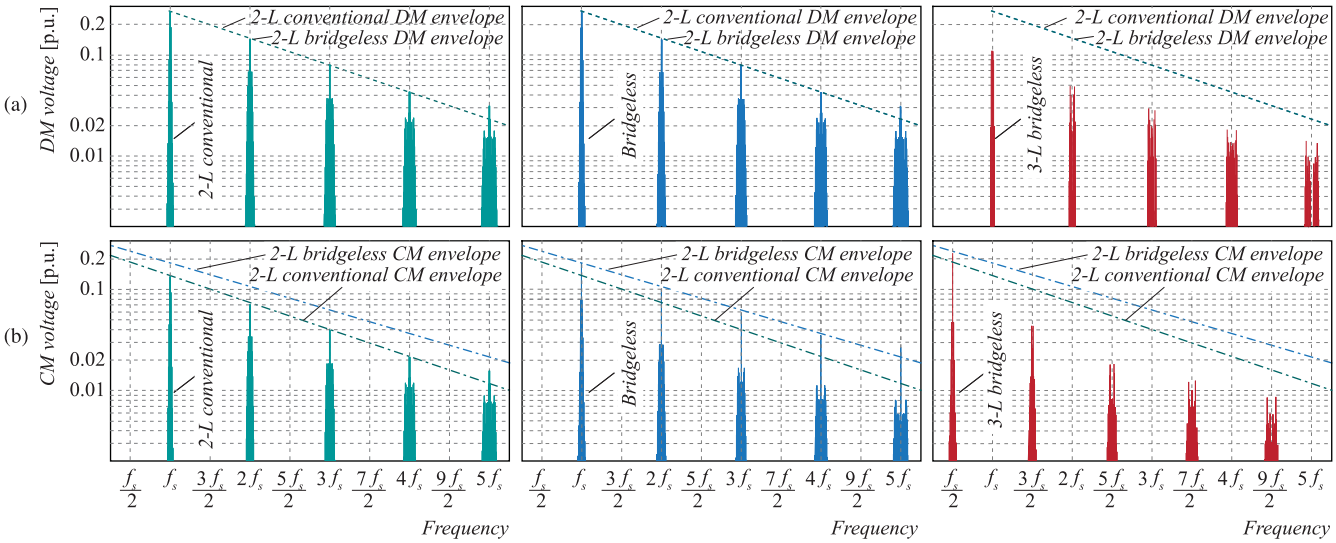


Fig. 11. Voltage spectra for two- and three-level bridgeless PFC rectifiers: (a) differential mode voltage spectrum; and, (b) common mode voltage spectrum, i.e., the spectrum of $v_{\mathrm{CM}} = (v_{A,\mathrm{MP}} + v_{N,\mathrm{MP}})/2$, spectrum. All results are normalized based on the output voltage $V_o$.

$$\times \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \sum_{k=1}^{\infty} \left[ \frac{\mathrm{J}_{2k-1}\left[(2m-1)\,\pi m\right](2k-1)\cos(n\pi)}{(2k-1+2n)(2k-1-2n)} \right.$$

$$\left. \cdot \cos\left[ \left( \frac{2m-1}{2} \right) \theta_c + 2n\theta_g \right] \right\} \tag{27}$$

where $\theta_c = 2\pi f_s t$ and $\theta_g = 2\pi f_g t$ are the instantaneous phase angles of the modulation carrier and the grid voltage, respectively.

Fig. 11 shows the DM and CM voltages comparison of the proposed rectifier with the conventional two-level boost PFC rectifier [see Fig. 1(a)] and the bridgeless rectifier depicted in Fig. 1(b). As shown in Fig. 11(b) and (27) the first harmonic group of the CM voltage appears at $f_s/2$. The proposed three-level PFC rectifier presents reduced spectra amplitudes and, thus, leads to smaller EMC filter components for, both, CM and DM when compared to the bridgeless rectifier. Its conducted emissions generation performance in this regard is comparable to that of an interleaved bridgeless PFC converter with the advantage of using a single inductor. On the other hand, the proposed topology might present higher CM voltage than the conventional boost rectifier [see Fig. 1(a)] since it, as in the case of the bridgeless, does not feature the negative point of the line being always connected to the negative dc bus through some rectification diode. The final CM noise paths will strongly depend on the parasitic elements of the circuit and the analysis of CM spectra presents only part of the required analysis. The proposed topology will typically present a larger CM filter and a smaller DM filter than the conventional PFC rectifier shown in Fig. 1(a).

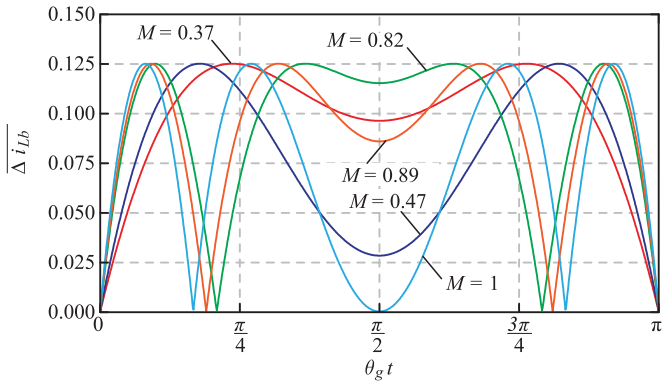


Fig. 12. Boost inductor current ripple as a function of the ac voltage phase angle for different modulation indexes.

### C. Boost Inductor Current Ripple

The normalized boost inductor current ripple is defined by

$$\overline{\Delta i_{Lb}} = \begin{cases} M\sin(\theta_g) - 2M^2\sin^2(\theta_g) & \text{if } \sin(\theta_g) \le \dfrac{1}{2M} \\ 3M\sin(\theta_g) - 2M^2\sin^2(\theta_g) - 1 & \text{if } \sin(\theta_g) > \dfrac{1}{2M} \end{cases} \quad (28)$$

and is graphically shown in Fig. 12 for different modulation indexes $M$ and as a function of the phase angle $\theta_g$, where

$$\overline{\Delta i_{Lb}} = \frac{\Delta i_{Lb}\, L_b\, f_s}{V_o}. \quad (29)$$

Therefore, the boost inductance can be defined as

$$L_b \ge \frac{V_o\, \overline{\Delta i_{Lb}}}{L_b\, f_s}. \quad (30)$$

### D. Passive Components: Current Stresses

The maximum current ripple value of the inductor $L_b$, $\Delta i_{Lb,\max}$, can be found with the maxima in (28). It is determined by

$$\Delta i_{Lb,\max} = \begin{cases} \dfrac{1}{8}\cdot\dfrac{V_o}{L_b\cdot f_s} & \text{if } M \ge \dfrac{1}{4} \\ \dfrac{M\cdot(V_o - 2V_{gp})}{L_b\cdot f_s} & \text{if } M < \dfrac{1}{4}. \end{cases} \quad (31)$$

The rms value of the output capacitor current $I_{Co,\mathrm{rms}}$ is given by

$$I_{Co,\mathrm{rms}} = I_{gp}\cdot\sqrt{\frac{4M}{3\pi} - \frac{M^2}{4}}. \quad (32)$$

In steady-state conditions, the output capacitor current is composed of low and high-frequency components. These current components are given by

$$I_{Co,lf} = \frac{1}{\sqrt{2}}\frac{V_{gp} I_{gp}}{2V_o} \quad (33)$$

$$I_{Co,hf} = \sqrt{{I_{Co,rms}}^2 - {I_{Co,lf}}^2} \quad (34)$$

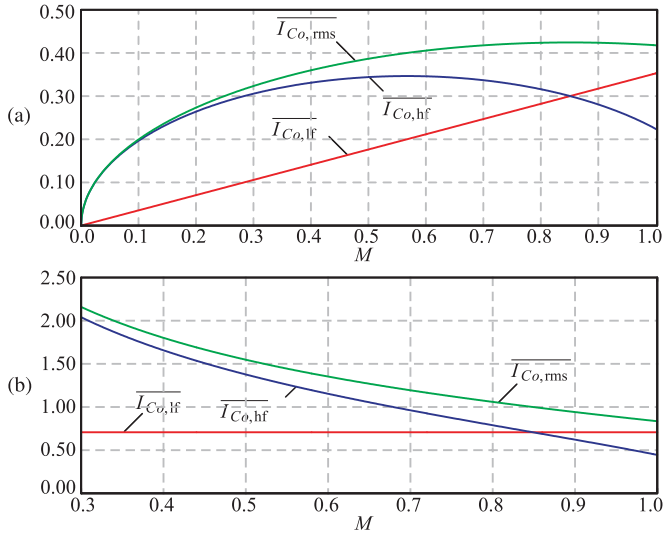


Fig. 13. Normalized output capacitor current components as a function of the modulation index $M$: (a) normalization according to the input current peak and; (b) from the output current given by $P_o/V_o$.

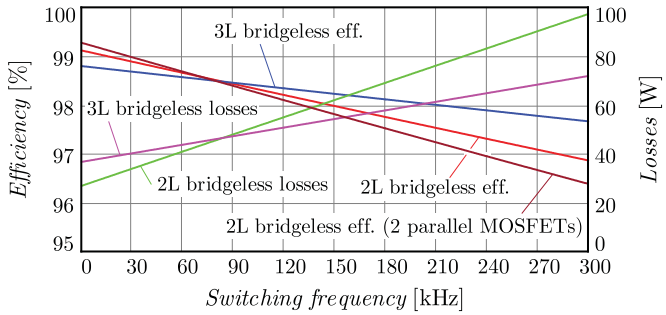


Fig. 14. Efficiency and power semiconductor losses comparison between the proposed topology (3L bridgeless) and a two-level bridgeless (2L bridgeless) according to Fig. 1(b). A second efficiency curve for the 2L bridgeless is shown considering that two 600-V CoolMOS devices are used in parallel in each turn-off device and, thus, the total silicon area becomes more similar. The MOSFET parameters in this case are adjusted to half the resistance values and double the capacitance values. All curves do not consider passive components losses and signal electronics consumption.

and are shown in Fig. 13 as a function of the modulation index $M$.

### E. DC-Link Voltage Ripple

The peak-to-peak value of the output voltage ripple $\Delta v_{co,\max}$ is

$$\Delta v_{Co,\max} = \frac{P_o\,(C_{op} + C_{\mathrm{on}})}{2\pi\cdot f_g\cdot V_o\cdot C_{op}\cdot C_{\mathrm{on}}} \quad (35)$$

while each half of the dc-link presents one half of this value, i.e.,

$$\Delta v_{op,\max} = \Delta v_{\mathrm{on},\max} = \frac{\Delta v_{Co,\max}}{2}. \quad (36)$$

Thus, the dc-link capacitance values can be chosen according to

$$C_{op} = C_{\mathrm{on}} \ge \frac{P_o}{\pi\, f_g\, V_o\, \Delta v_{Co,\max}}. \quad (37)$$

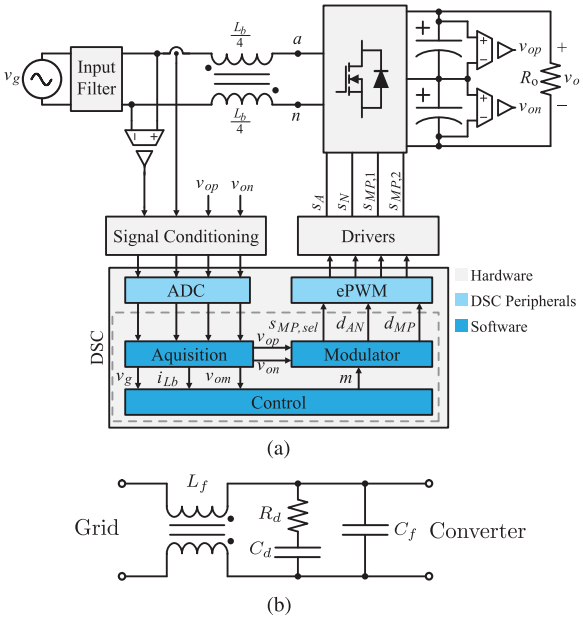


Fig. 15. (a) Circuit diagram of the multilevel unidirectional single-phase PFC rectifier prototype; and (b) input filter.

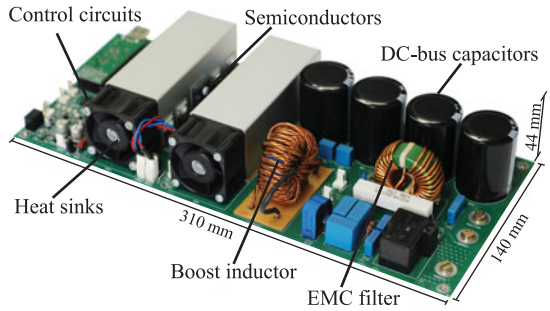


Fig. 16. Implemented 3-kW multilevel unidirectional single-phase PFC rectifier prototype.

TABLE II
UNIDIRECTIONAL SINGLE-PHASE PFC RECTIFIER PROTOTYPE SPECIFICATION

| Specification | Value |
|---|---|
| Input phase rms voltage $V_g$ | 220 V $\pm 15\%$ |
| Output voltage $V_o$ | 380 V |
| Grid $f_g$ and switching frequency $f_s$ | 60 Hz / 140 kHz |
| Rated output power $P_o$ | 3 kW |
| Max. output voltage ripple $\Delta v_{Co,\max}$ | 5 |
| Max. inductor current ripple $\Delta i_{Lb,\max}$ | 20 |

## F. Rectifier Current Stresses Model Accuracy

In order to verify the accuracy of the derived equations modeling the stresses of the studied rectifier devices, an appropriate switching frequency and suitable components for the project specification given in Table II have been selected. A switching frequency of $f_s = 140$ kHz is designated as it constitutes a good compromise between high efficiency, high power density, and high control bandwidth. Advantageously, the switching frequency is found near, but still below the beginning of the considered EMC conducted emissions measurement range starting at 150 kHz. With $f_s = 140$ kHz, the values for the input inductor of $L_b = 96.5\ \mu$H ($\Delta i_{Lb,\max} \approx 18.3\% \cdot I_{gp}$) and $C_{op} = C_{\rm on} = 3000\ \mu$F ($\Delta v_{Co,pp} \approx 3.7\% \cdot V_o$) are selected for the verification of the derived models. In Table III, the values of the average and rms component stresses calculated with the respective expressions are compared to the results obtained with a circuit simulator and show very good agreement.

TABLE III
COMPARISON OF ACTIVE AND PASSIVE COMPONENT STRESSES DETERMINED BY ANALYTICAL CALCULATIONS AND SIMULATIONS

| | Analytical calc. | Simulation results | Deviation [%] |
|---|---|---|---|
| $I_{\rm SAN,avg}$ | 0.41 | 0.41 | 0.0 |
| $I_{\rm SAN,rms}$ | 1.57 | 1.60 | +1.9 |
| $I_{\rm SMP,avg}$ | 3.57 | 3.60 | +0.84 |
| $I_{\rm SMP,rms}$ | 7.20 | 7.22 | +0.27 |
| $I_{\rm DMP,avg}$ | 1.79 | 1.80 | +0.56 |
| $I_{\rm DMP,rms}$ | 5.09 | 5.10 | +0.19 |
| $I_{\rm DSAN,avg}$ | 2.19 | 2.24 | +2.28 |
| $I_{\rm DSAN,rms}$ | 5.325 | 5.37 | +0.75 |
| $I_{D1/2AN,avg}$ | 3.95 | 3.89 | −1.52 |
| $I_{D1/2AN,rms}$ | 8.04 | 7.94 | −1.24 |
| $I_{Co,rms}$ | 8.18 | 8.10 | −0.98 |
| $\Delta i_{Lb,\max}$ | 3.52 | 3.42 | −2.84 |
| $\Delta v_{Co,\max}$ | 13.96 | 13.62 | −2.43 |

## G. Efficiency Comparison

An efficiency comparison involving the topologies shown in Fig. 2(g) (a three-level bridgeless) and Fig. 1(b) (a two-level bridgeless) is presented here, while considering the following devices:

1) *Fast switching diodes ($D_{1,N/A}$, $D_{2,N/A}$):* SiC diodes SCS112AG, Rohm.
2) *600-V MOSFETs ($S_A$, $S_N$, $S_{2,A}$, $S_{2,N}$):* Si CoolMOS IPP60R099CP, Infineon.
3) *300-V MOSFETs ($S_{\rm MP,1}$, $S_{\rm MP,2}$):* Si Mosfet STW75NF30, ST.
4) *Diodes in series with MOSFETs ($D_{\rm MP,A}$, $D_{\rm MP,N}$):* Si diodes RURP3060, Fairchild.

The comparison does not include the passive components losses and it is assumed that no reverse recovery occurs. The rms value of the input voltage is 220 V, frequency is 60 Hz, output voltage is 380 V, and the output power is 3 kW. The switching losses are computed based on the switching times calculations with the method presented in [47]. The conduction losses assume that the diodes can be represented with a constant forward voltage drop $V_{\rm TO}$ in series with a resistance $r_T$, while the MOSFETs are modeled with a constant resistance $R_c$. The following devices parameters are adopted:

1) *Fast switching diodes ($D_{1,N/A}$, $D_{2,N/A}$):* $V_{\rm TO} = 1.0$ V; $r_T = 43$ m$\Omega$.
2) *600-V MOSFETs ($S_A$, $S_N$, $S_{2,A}$, $S_{2,N}$):* $R_c = 175$ m$\Omega$; antiparallel diode $V_{\rm TO} = 0.75$ V and $r_T = 30$ m$\Omega$; total gate resistance $R_g = (8.2 + 1.3)\ \Omega$; gate-to-source capacitance $C_{gs} = 2.74$ nF; gate-to-drain capacitance

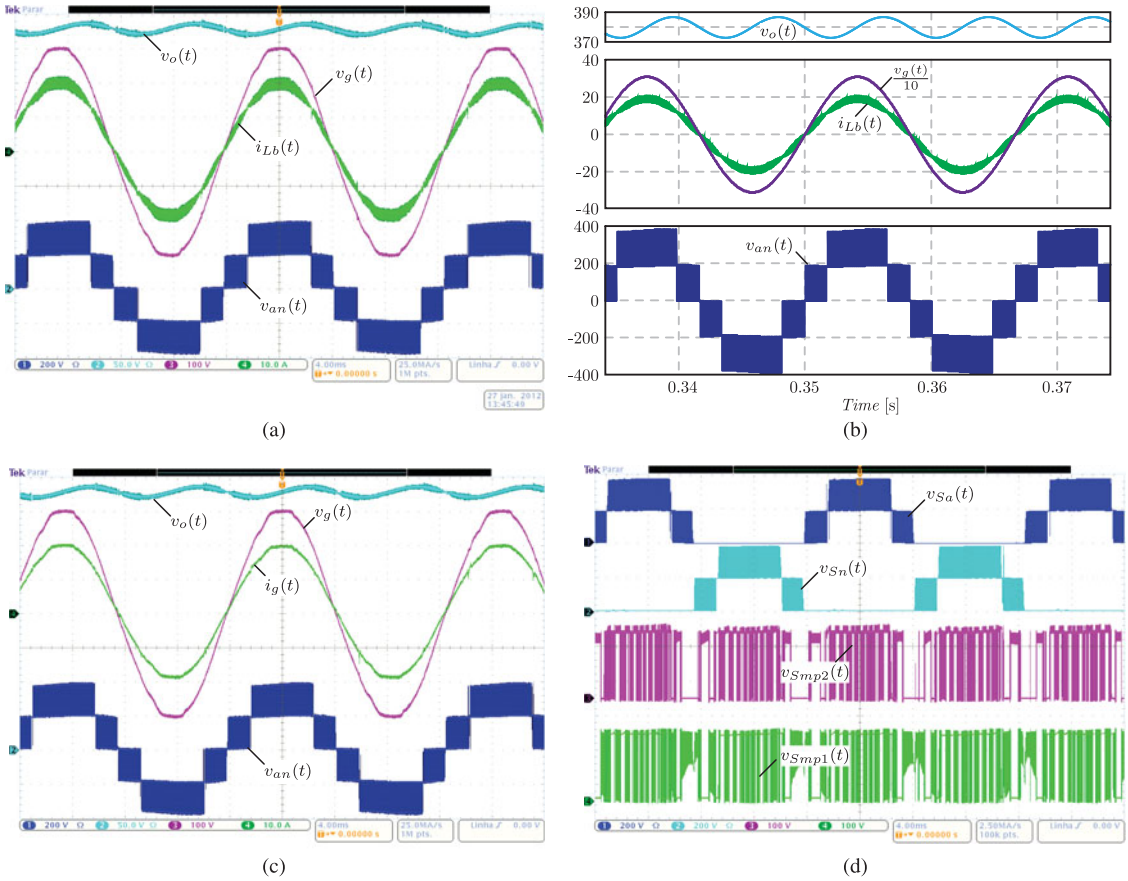


Fig. 17. Main waveforms: (a) measured output voltage $v_o$ (50 V/div), rectifier input current $i_{Lb}$ (10 A/div), grid voltage $v_g$ (100 V/div), and multilevel voltage $v_{A,N}$ at the converter input terminals (200 V/div); (b) main waveforms obtained with a circuit simulator; (c) measured output voltage $v_o$ (50 V/div), grid current $i_g$ (10 A/div), grid voltage $v_g$ (100 V/div), and multilevel voltage $v_{A,N}$ at the converter input terminals (200 V/div); and, (d) measured voltages across $S_A$ $v_{Sa}$ (200 V/div), $S_N$ $v_{Sn}$ (200 V/div), $S_{\mathrm{MP},2}$ $v_{\mathrm{Smp2}}$ (100 V/div) and $S_{\mathrm{MP},1}$ $v_{\mathrm{Smp1}}$ (100 V/div).

$C_{gd} = 60$ pF; drain-to-source capacitance $C_{ds} = 280$ pF; threshold voltage $V_{\mathrm{GS(th)}} = 3$ V; pinch-off voltage $V_p = 5$ V; gate driver voltage $V_G = 15$ V.

3) *300-V MOSFETs ($S_{\mathrm{MP},1}$, $S_{\mathrm{MP},2}$):* $R_c = 64.8$ mΩ; $R_g = (8.2 + 1.55)$ Ω; $C_{gs} = 5.82$ nF; $C_{gd} = 110$ pF; $C_{ds} = 352$ pF; $V_{\mathrm{GS(th)}} = 3$ V; $V_p = 5$ V; $V_G = 15$ V.
4) *Diodes in series with MOSFETs ($D_{\mathrm{MP},A}$, $D_{\mathrm{MP},N}$):* $V_{\mathrm{TO}} = 0.6$ V and $r_T = 23$ mΩ.

Fig. 14 shows the computed power semiconductor losses. The two-level bridgeless presents lower losses at low switching frequencies. This can be further improved with the use of two parallel MOSFETs per turnoff device to achieve efficiency levels close to 99%. This figure is not achievable with the proposed topology. In summary, the two-level bridgeless presents lower conduction losses. However, as the switching frequency rises, the efficiency of the three-level bridgeless is not as affected and from approximately 80 kHz on the proposed topology produces lower total losses. This would be more pronounced if the boost inductor and EMC filter elements were considered.

## IV. Experimental Evaluation

A 3-kW hardware prototype of the proposed unidirectional single-phase PFC rectifier according to the specifications given in Table II and feedback control scheme depicted in Fig. 7 has been built. The circuit diagram and the implemented prototype are shown in Figs. 15 and 16, respectively. A list of the employed semiconductor devices and passive components is given in Table IV.

TABLE IV
Main Components of the 3-kW Three-Level Unidirectional Single-Phase PFC Rectifier Prototype (see Figs. 15 and 16)

| Component | Device Description |
|---|---|
| DSP | Texas Instruments TMS320F28027 |
| $D_{1,N/A}$, $D_{2,N/A}$ | SiC Schottky diodes SCS112AG, Rohm |
| $D_{\mathrm{MP},N}$, $D_{\mathrm{MP},A}$, | Si diodes RURP3060, Fairchild |
| $S_A/D_{S,A}$, $S_N/D_{S,N}$ | CoolMOS IPP60R099CP, Infineon |
| $S_{\mathrm{MP},1}$, $S_{\mathrm{MP},2}$ | STripFET Power Mosfet STW75NF30, ST |
| $L_b$ | 96.5 $\mu$H at 140 kHz, APH40P60 core, 44 turns, 4 × AWG18 Cu wire |
| $L_f$ | 2.4 mH JW Miller 8120-RC |
| $C_{op}$, $C_{\mathrm{on}}$ | 2 × 1.5 mF / 250 V, Panasonic EET-HC2E152EA |
| $C_f$ | 2 × 470 nF |
| $C_d$ | 470 nF |
| $R_d$ | Damping resistor of 56 |
| Gate Driver | FOD 3180 |

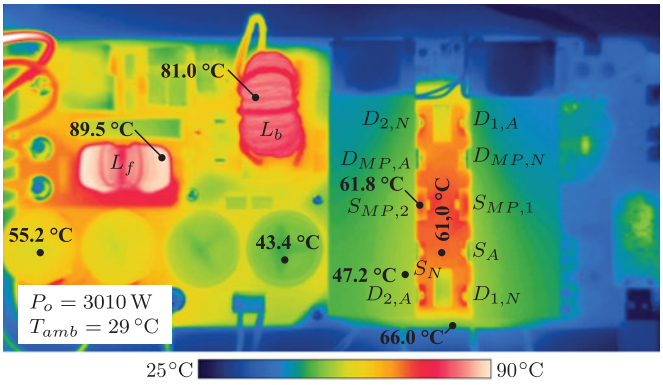


Fig. 18. Prototype measured temperatures while operating at rated power and input voltage $V_g = 187$ V.

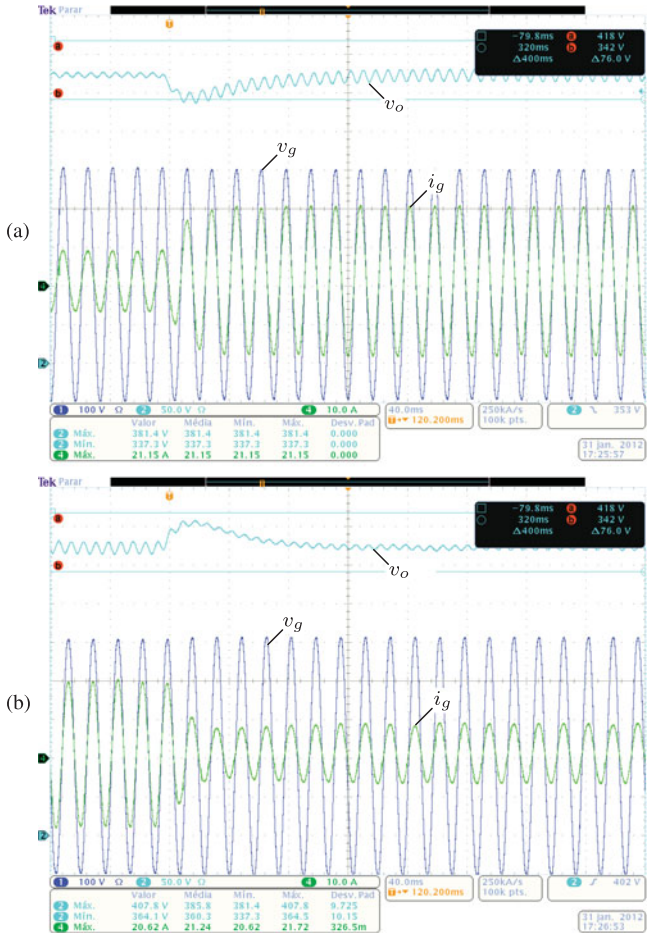


Fig. 19. Load step: (a) from 40% to 100% $P_o$ and (b) from 100% to 40% $P_o$.

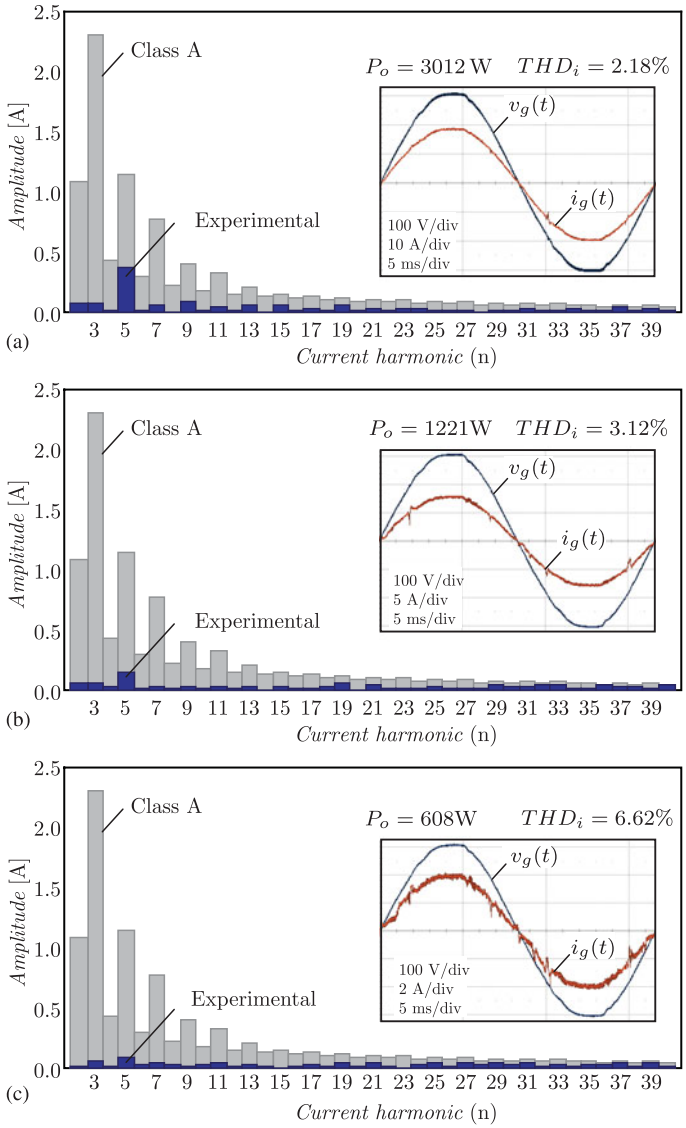


Fig. 20. Input current harmonic analysis for: (a) rated power output power $P_o$; (b) 40% $P_o$; and (c) 20% $P_o$. Measurement conditions with a grid voltage THD of approximately 1.9%.

The main waveforms obtained with the designed prototype operating at rated power ($P_o \approx 3$ kW) are presented in Fig. 17. For comparison purposes, the results presented in Fig. 17(a) are shown with the waveforms obtained in a circuit simulator [see Fig. 17(b)], and show very good correspondence. The observed dc-link voltage ripple is below 4% closely matching the theoretical findings. The boost inductor maximum current ripple also agrees with the derived design expressions, where the maximum measured ripple is approximately 3.6 A. The formation of five voltage levels in $v_{A,N}$ is observed. The filtered input current drained from the grid $i_g$ is shown in Fig. 17(c). Therein, it can be observed that the input voltage distortion near the peak of the $v_g$ waveform appears as well as in the input current $i_g$. This is due to the resistive behavior emulated by the designed converter. The voltages across the MOSFETs are presented in Fig. 17(d), where it is noted that all commutations occur with a voltage level equivalent to half the output voltage, even at the switches that need to block the full dc-link voltage. This produces low switching losses.

Fig. 18 shows the prototype temperature distribution measured with thermal camera FLIR SC655 at an ambient temperature ($T_{\text{amb}}$) of 29 °C. The measurements are taken for the prototype operating at nominal power ($P_o \approx 3$ kW) and minimal input voltage rms value ($V_g = 187$ V) as it constitutes the most critical scenario regarding the converter power losses and,

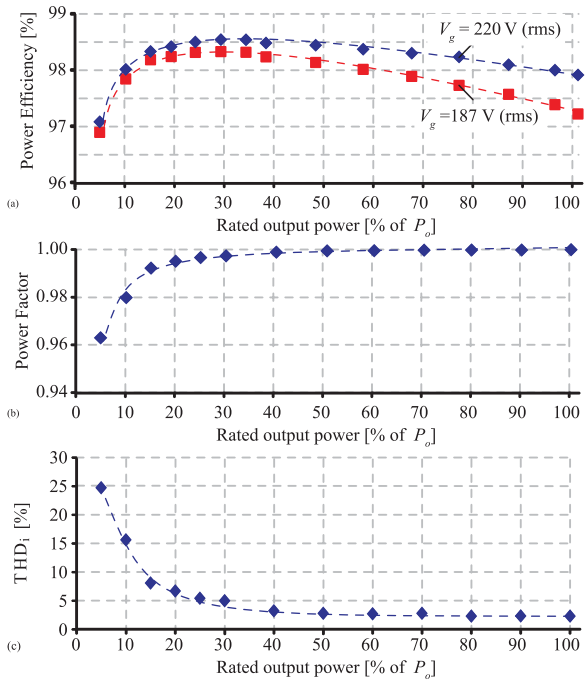


Fig. 21. Prototype measured: (a) power efficiency for different input voltages ($V_g$ = 220 V and 187 V rms); (b) power factor for $V_g$ = 220 V rms; and (c) input current THDi for $V_g$ = 220 V rms as functions of the rated output power.

consequently it is the case where the highest thermal stress across the power elements are generated.

Fig. 19 presents the dynamic performance of the proposed feedback control tested with the converter operating at $V_g = 220$ V (rms) for two resistive load steps: from 40% to 100% $P_o$ [see Fig. 19(a)] and from 100% to 40% $P_o$ [see Fig. 19(b)]. The output voltage could be efficiently regulated in both tests. Fig. 20 shows the harmonic analysis of the converter input current $i_g$ in comparison with the limits of the IEC 61000-3-2 standard for class A equipment. The standard limits have been met for the measured load conditions. The hardware power efficiency ($\eta$), input current THD, and power factor ($\lambda$) as functions of the output power have been measured with a Yokogawa WT3000 power analyzer and the results are shown in Fig. 21. Considering the relatively high switching frequency of $f_s = 140$ kHz for a 3-kW rectifier, a remarkable maximum efficiency of 98.6% at partial load ($\approx$35% $P_o$) and, advantageously, a relatively flat efficiency curve are obtained. From 10% to 100% of $P_o$, the measured efficiency is found between the range of 98.0% and 98.6%. Additionally, the results show a high power quality of the input current, i.e., at full power a high power factor ($\lambda \approx 0.99$) and a low input current THD ($\mathrm{THD_i} \approx 2.18\%$) have been measured. Finally, the experimental results attest that the proposed multilevel PFC rectifier is a very attractive solution for applications in single-phase power supplies targeting for high efficiency, high line power quality, and high power density.

## V. Conclusion

Multilevel high efficiency unidirectional single-phase three-level PFC rectifier topologies well suited for applications aiming for high efficiency and/or high power density have been proposed in this paper. Even though most power semiconductors block the full dc-link voltage, all switching transitions occur with only half of the dc-link voltage. Thus, the proposed concepts present low switching losses when compared to conventional two-level bridgeless rectifiers. In addition, simple to manufacture and small volume are characteristics of the required boost inductor. This leads to manufacturing cost advantages when comparing the proposed systems to interleaved converters. More importantly, the new converters feature similar switching loss performance, but lower conduction losses when compared to state-of-the-art three-level rectifier topologies. In fact, as for the conventional three-level PFCs, the main disadvantages related to two-level topologies are the increased number of semiconductors, isolated gate drivers, and the inherit higher control complexity.

For a selected rectifier, the principle of operation, the main design expressions, suitable modulation scheme, and PWM control have been described. It has been shown that this converter has reduced EMC filter requirements when compared to a conventional bridgeless topology. Additionally, the DM filter requirement is also reduced when compared to a conventional boost PFC rectifier, but the need of a larger CM filter is likely. Finally, in order to verify some advantages of the exemplary PFC circuit, the system has been designed and a 3-kW hardware prototype has been constructed and tested. At a switching frequency of 140 kHz, rated power and nominal input voltage a power efficiency of 98% and an input current THD of 2.18% have been measured, attesting the advantages of the proposed rectifier concept.

## References

[1] D. M. Michell, "AC–DC converter having an improved power factor," U.S. Patent 4 412 277, 1983.

[2] A. de Souza and I. Barbi, "High power factor rectifier with reduced conduction and commutation losses," presented at the 21st Int. Telecommun. Energy Conf., Copenhagen, Denmark, 1999, p. 5.

[3] M. Heldwein, M. Ortmann, and S. Mussa, "Single-phase PWM boost-type unidirectional rectifier doubling the switching frequency," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, 2009, pp. 1–10.

[4] F. Musavi, W. Eberle, and W. Dunford, "A high-performance single-phase bridgeless interleaved PFC converter for plug-in hybrid electric vehicle battery chargers," *IEEE Trans. Ind. Appl.*, vol. 47, no. 4, pp. 1833–1843, Jul./Aug., 2011.

[5] Y. Jang and M. Jovanovic, "A bridgeless PFC boost rectifier with optimized magnetic utilization," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 85–93, Jan. 2009.

[6] M. Kabir, A. Abedin, D. Rahman, R. Mustafiz, and M. A. Choudhury, "Boost and buck topology based single phase AC–DC converters with low THD and high power factor," in *Proc. IEEE 33rd Int. Telecommun. Energy Conf.*, 2011, pp. 1–7.

[7] B. Su and Z. Lu, "An interleaved totem-pole boost bridgeless rectifier with reduced reverse-recovery problems for power factor correction," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1406–1415, Jun. 2010.

[8] B. Su, J. Zhang, and Z. Lu, "Totem-pole boost bridgeless PFC rectifier with simple zero-current detection and full-range ZVS operating at the boundary of DCM/CCM," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 427–435, Feb. 2011.

[9] P. Kong, S. Wang, and F. Lee, "Common mode EMI noise suppression in bridgeless boost PFC converter," in *Proc. IEEE Annu. Appl. Power Electron. Conf.*, 2007, pp. 929–935.

[10] Y. Jang, M. Jovanovic, and D. Dillman, "Bridgeless PFC boost rectifier with optimized magnetic utilization," in *Proc. IEEE 23rd Appl. Power Electron. Conf. Expo.*, 2008, pp. 1017–1021.

[11] J.-W. Shin, J. bok Baek, and B.-H. Cho, "Bridgeless isolated PFC rectifier using bidirectional switch and dual output windings," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 2879–2884.
[12] W.-Y. Choi, J.-M. Kwon, L. Jong-Jae, H.-Y. Jang, and B.-H. Kwon, "Single-stage soft-switching converter with boost type of active clamp for wide input voltage ranges," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 730–741, Mar. 2009.
[13] P. Das, M. Pahlevaninezhad, and G. Moschopoulos, "Analysis and design of a new AC–DC single-stage full-bridge PWM converter with two controllers," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4930–4946, Nov. 2013.
[14] J.-W. Shin, H. Shin, G.-S. Seo, J.-I. Ha, and B.-H. Cho, "Low-common mode voltage h-bridge converter with additional switch legs," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1773–1782, Apr. 2013.
[15] T. Nussbaumer, K. Raggl, and J. Kolar, "Design guidelines for interleaved single-phase boost PFC circuits," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2559–2573, Jul. 2009.
[16] C. Marxgut, F. Krismer, D. Bortis, and J. Kolar, "Ultraflat interleaved triangular current mode (TCM) single-phase PFC rectifier," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 873–882, Feb. 2014.
[17] Y.-S. Kim, B.-K. Lee, and J. Lee, "Topology characteristics analysis and performance comparison for optimal design of high efficiency PFC circuit for telecom," in *Proc. IEEE 33rd Int. Telecommun. Energy Conf.*, 2011, pp. 1–7.
[18] M. Silveira Ortmann, T. B. Soeiro, and M. Lobo Heldwein, "High switches utilization single-phase PWM boost-type PFC rectifier topologies multiplying the switching frequency," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5749–5760, Nov. 2014.
[19] D. Tollik and A. Pietkiewicz, "Comparative analysis of 1-phase active power factor correction topologies," in *Proc. 14th Int. Telecommun. Energy Conf.*, 1992, pp. 517–523.
[20] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC–DC converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.
[21] L. Huber, J. Yungtaek, and M. M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifier," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May 2008.
[22] F. Musavi, M. Edington, W. Eberle, and W. Dunford, "Evaluation and efficiency comparison of front end ac-dc plug-in hybrid charger topologies," *IEEE Trans. Smart Grid*, vol. 3, no. 1, pp. 413–421, Mar. 2012.
[23] Z. Lai, K. Smedley, and Y. Ma, "Time quantity one-cycle control for power-factor correctors," *IEEE Trans. Power Electron.*, vol. 12, no. 2, pp. 369–375, Mar. 1997.
[24] T. Ohnishi and M. Hojo, "DC voltage sensorless single-phase PFC converter," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 404–410, Mar. 2004.
[25] Q. Tao, X. Lei, and S. Jian, "Dual-boost single-phase PFC input current control based on output current sensing," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2523–2530, Nov. 2009.
[26] A. De Bastiani Lange and M. Heldwein, "Light load stability improvement for single-phase boost PFC rectifier using input current self-control technique," in *Proc. Power Electron. Conf.*, 2011, pp. 61–67.
[27] Y. Cho and J.-S. Lai, "Digital plug-in repetitive controller for single-phase bridgeless PFC converters," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 165–175, Jan. 2013.
[28] M. Soldano and V. Lu B., "EMI noise reduction circuit and method for bridgeless PFC circuit," U.S. Patent 7 215 560, 2006.
[29] P. Kong, S. Wang, and F. Lee, "Common mode EMI noise suppression for bridgeless PFC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 291–297, Jan. 2008.
[30] P. Kong, S. Wang, F. Lee, and Z. Wang, "Reducing common-mode noise in two-switch forward converter," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1522–1533, May 2011.
[31] Z. Wang, S. Wang, P. Kong, and F. Lee, "DM EMI noise prediction for constant on-time, critical mode power factor correction converters," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3150–3157, Jul. 2012.
[32] M. Zhang, Y. Jiang, F. Lee, and M. Jovanovic, "Single-phase three-level boost power factor correction converter," in *Proc. 10th Annu. Appl. Power Electron. Conf. Expo.*, 1995, vol. 1, pp. 434–439.
[33] D. Maksimovic and R. Erickson, "Universal-input, high-power-factor, boost doubler rectifiers," in *Proc. 10th Annu. Appl. Power Electron. Conf. Expo.*, 1995, vol. 1, pp. 459–465.
[34] J. Salmon, "Circuit topologies for PWM boost rectifiers operated from 1-phase and 3-phase AC supplies and using either single or split DC rail voltage outputs," in *Proc. Appl. Power Electron. Conf. Expo.*, 1995, pp. 473–479, vol. 1.
[35] P. Bartholomeus, and P. L. Moigne, "A 3 kw unit-power-factor multilevel rectifier based on a double boost converter," in *Proc. Eur. Conf. Power Electron. Appl.*, 1997, pp. 4.204–4.209.
[36] Y. Jiang, "High efficiency boost converters for wide range single-phase AC input power factor correction," in *Proc. 20th Int. Telecommun. Energy Conf.*, 1998, pp. 603–606.
[37] B.-R. Lin, and H.-H. Lu, "Multilevel PWM for single-phase power factor pre-regulator," in *Proc. IEEE Int. Symp. Circuits Syst.*, 1999, vol. 6, pp. 57–60.
[38] B.-R. Lin, and H.-H. Lu, "Single-phase three-level PWM rectifier," in *Proc. IEEE Power Electron. Drive Syst. Conf.*, 1999, pp. 63–68, vol. 1.
[39] B.-R. Lin, C.-N. Wang, and H.-H. Lu, "Multilevel AC/DC/AC converter by using three-level boost rectifier and five-level diode clamped inverter," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst.*, 1999, vol. 1, pp. 444–449.
[40] B.-R. Lin and H.-H. Lu, "Multilevel AC/DC/AC converter for AC drives," *IEE Proc.—Electric Power Appl.*, vol. 146, no. 4, pp. 397–406, 1999.
[41] J. S. C. Krismadinata, and N. A. Rahim, "A novel topology and PWM single-phase three-level rectifier," in *Proc. Int. Conf. Tech. Postgraduate*, 2009, pp. 1–6.
[42] M. Heldwein, S. Mussa, and I. Barbi, "Three-phase multilevel PWM rectifiers based on conventional bidirectional converters," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 545–549, Mar. 2010.
[43] M. Ortmann, S. Mussa, and M. Heldwein, "Generalized analysis of a multistate switching cells-based single-phase multilevel PFC rectifier," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 46–56, Jan. 2012.
[44] J. Zhang, B. Su, and Z. Lu, "Single inductor three-level bridgeless boost power factor correction rectifier with nature voltage clamp," *IET Power Electron.*, vol. 5, no. 3, pp. 358–365, Mar. 2012.
[45] B. Su, J. Zhang, H. Wen, and Z. Lu, "Low conduction loss and low device stress three-level power factor correction rectifier," *IET Power Electron.*, vol. 6, no. 3, pp. 478–487, Mar. 2013.
[46] J. Kolar and F. C. Zach, "A novel three-phase utility interface minimizing line current harmonics of high-power telecommunications rectifier modules," *IEEE Trans. Ind. Electron.*, vol. 44, no. 4, pp. 456–467, Aug. 1997.
[47] L. Balogh, "Design and application guide for high speed MOSFET gate drive circuits," in *Power Supply Design Seminar*, Dallas, TX, USA, Texas Instruments/Unitrode Corporation, 2001.

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