Improving the Scavenged Power of Nonlinear Piezoelectric Energy Harvesting Interface at Off-Resonance by Introducing Switching Delay

Ping-Hsuan Hsieh, *Member, IEEE*, Chi-Huan Chen, and Hung-Chen Chen

***Abstract*—This paper presents two interface circuit designs that improve the piezoelectric energy harvesting performance at off-resonance. Complex impedance matching at different frequencies is achieved by introducing delay into the conventional switching methods. The proposed techniques can also be used in other applications, such as electromagnetic energy harvesting. The system is analyzed using equivalent impedance at fundamental of operating frequency. Design considerations such as two possible modes of operation, sensitivity to voltage and timing errors, loss due to nonlinear operations, and conduction loss of switches are detailed. As compared with the conventional methods, analytical results show that, with the electromechanical coupling coefficient k_e^2 of 0.076 and the mechanical damping ratio ζ_m of 0.02, the proposed techniques can improve the 3-dB bandwidth by 76% with a flipping quality factor of 10. Experimental results with a commercially available piezoelectric device show a 23% improvement in 3-dB bandwidth and a 66% improvement in extracted power with 5% of frequency mismatch.**

***Index Terms*—Complex impedance matching, maximum power transfer, off-resonance, piezoelectric energy harvesting, switching delay, synchronized switching harvesting on an inductor.**

I. Introduction

WIRELESS sensor networks (WSNs) have been used in industrial and consumer applications extensively, including industrial process monitoring and control, health and lifestyle improvement [1], [2]. Typically, these systems are composed of large numbers of small, low-cost sensor nodes working in collaboration to collect and transmit data through wireless networks. In these systems, most of the devices rely on batteries for power source. This limits the lifetime of the device and furthermore increases the cost for maintenance. Energy harvesting, therefore, provides a feasible alternative for potentially battery-free self-sustainable sensor nodes [3]–[19].

Energy harvesting is a process to capture and store energy from an ambient environment. It can convert many possible energy sources into useful electricity. Piezoelectric vibration-to-electricity conversion has received much attention recently [9]–[22] due to the large output power and the compatibility with integrated-circuit (IC) technology. However, the ambient power is by nature time-varying and is often insufficient to supply the system continuously. A power processing circuit is therefore needed along with an energy storage to generate a stable dc output supply, as shown in Fig. 1. Several previous studies have shown that the architecture of interface circuit can impact the extracted power significantly. Nonlinear techniques such as synchronized-switching-harvesting-on-an-inductor (SSHI) and synchronized-switching-and-discharging-to-a-storage-capacitor-through-an-inductor (SSDCI) interfaces [9], [12]–[14], [17], [20], [23]–[26] successfully boost the extracted power by introducing synchronous switching operations when the displacement reaches its peak. However, the extracted power drops dramatically as the operating frequency deviates from the resonant frequency due to the high quality factor of the mechanical structure [12], [14].

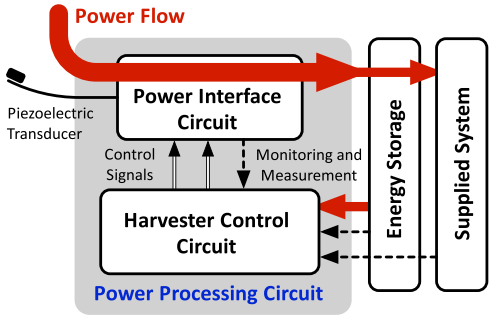

Fig. 1. General block diagram for piezoelectric energy harvesting.

This study presents two techniques that extend the operating frequency range by introducing a phase delay ϕ into the timing of the conventional switching methods. As opposed to the inevitable delay that is due to the limitations of real implementations [26], the delay is introduced *intentionally* in this study. From mechanical point of view, the delay in switching results in a piezoelectric voltage component that is in phase with the displacement and therefore induces a stiffening effect, shifting the resonant frequencies [26], [27]. The damping effect and therefore the converted energy are also changed [26]. From an electrical point of view, this achieves complex impedance matching at different frequencies. As a result, the proposed techniques improve the extracted power from the transducer when operating at off-resonance. The required load impedance can be obtained by adjusting the transducer's output voltage and the switching timing properly.

In fact, the proposed techniques for complex impedance matching is general and therefore, can also be used in other applications, such as electromagnetic energy harvesting in which

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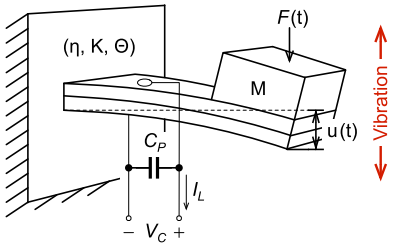

Fig. 2. Piezoelectric energy harvester.

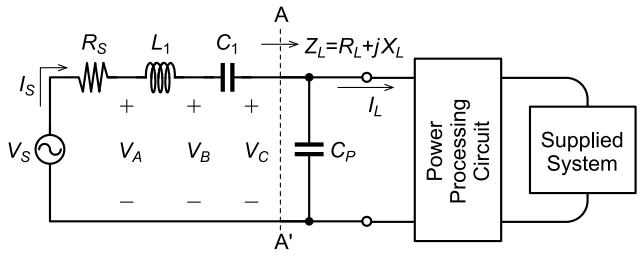

Fig. 3. Equivalent circuit model for a piezoelectric energy harvesting system.

the source impedance is highly inductive. Furthermore, the proposed techniques can be used in conjunction with the conventional passive impedance matching to provide adaptability in cases of parameter variations. The applicability of the proposed methods is limited by 1) the validity of the electrical model when frequency deviation is large, 2) the nonlinear behavior of transducer when output power is large, and 3) the voltage tolerance of the electronic devices used. Analytical results show that, with the electromechanical coupling coefficient k_e^2 of 0.076 and the mechanical damping ratio ζ_m of 0.02, the proposed techniques can improve the 3-dB bandwidth of the conventional methods by 76% with a flipping quality factor of 10.

This paper is organized as follows. Section II-A provides a framework of the proposed techniques by first introducing the equivalent electrical model of a piezoelectric energy harvesting system. Maximum power transfer (MPT) theorem is linked to this model and different interface architectures can therefore be assessed from the perspective of equivalent load impedance at fundamental of operating frequency. After briefly introducing the conventional techniques in Sections II-B–II-D, Section II-E describes the challenges of these conventional techniques and therefore leads to Section III that presents the proposed techniques. Design considerations such as two possible modes of operation, sensitivity to voltage and timing errors, loss due to nonlinear operations that cause high-order harmonics, as well as conduction loss of switches are discussed in Section IV. Section V shows the experimental results and Section VI summarizes the study.

II. Energy Harvesting Basics

A. Modeling and MPT Theorem

Consider a piezoelectric vibrating structure, such as that in Fig. 2, whose modal density is assumed to be widely separated. Suppose that it is vibrating at around its resonant frequency. In this case, the vibrating piezoelectric transducer can be modeled as a mass + spring + damper + piezo structure [14]. The equations governing the model can be described as

$$M\ddot{u}(t) + \eta\dot{u}(t) + Ku(t) + \Theta V_C(t) = F(t) \text{ and} \quad (1)$$

$$-\Theta\dot{u}(t) + C_P\dot{V}_C(t) = -I_L(t) \quad (2)$$

where M, η, K, Θ, and C_P are the mass, the mechanical damping coefficient, the effective stiffness, the piezoelectric coefficient, and the clamped intrinsic capacitance, respectively. In addition, $F(t)$ is the forcing function applied to the system which is assumed to be a single-tone sinusoid, $u(t)$ is the displacement of the mass, $V_C(t)$ is the voltage across the piezoelectric element, and $I_L(t)$ is the current flowing into the following electrical system.

With (1) and (2), the transducer can be further transformed into an equivalent circuit model shown in Fig. 3, with $R_S = \eta/\Theta^2$, $L_1 = M/\Theta^2$, $C_1 = \Theta^2/K$, and $V_S = F_0/\Theta$. Fig. 3 also shows the electromechanical interface as the line A–A′. The transducer structure exhibits two resonant frequencies, namely, the short-circuit resonant frequency $\omega_{\rm SC}$ and the open-circuit resonant frequency $\omega_{\rm OC}$

$$\omega_{\rm SC} = \frac{1}{\sqrt{L_1C_1}} \text{ and } \omega_{\rm OC} = \frac{1}{\sqrt{L_1C_1C_P/(C_1+C_P)}}.$$

As shown in Fig. 3, a power processing circuit transfers the extracted power to the supplied system after proper conditioning, including ac–dc conversion and voltage regulation. In addition, the power processing circuit also sets the loading seen by the transducer [10], [21], [22]. In fact, if the loading and its parallel combination with C_P can be modeled as a linear impedance $Z_L = R_L + jX_L$ as shown in Fig. 3, according to the MPT Theorem, the power that flows into the electrical domain reaches the maximum when the impedances at two sides of the electromechanical interface (A–A′) are complex conjugate to each other. In other words, MPT can be achieved with

$$Z_L = (R_L + jX_L) = Z_S^* = (R_S + jX_S)^* \quad (3)$$

where $X_S = \omega L_1 - 1/(\omega C_1)$ from Fig. 3. In this case, the voltage source V_S sees a loading that is purely resistive with zero reactance and is composed of two resistors, R_S and R_L, with equal resistance. Furthermore, the source current I_S is in phase with the voltage source V_S. At MPT, the extracted power equals the theoretical available power $P_{\rm AVL}$ of $V_S^2/(8R_S) = F_0^2/(8\eta)$, which is determined only by the applying force and the mechanical damping coefficient, but not the piezoelectric coefficient.

In practice, the electrical behavior and the actual extracted power depend significantly on the loading condition and therefore the interface circuit design.

B. Standard Interface

A standard interface [13], [14] is composed of a rectifier followed by a filtering capacitor, as shown in Fig. 4 with the supplied system represented with an equivalent load resistor R_{out}. With a large filtering capacitor C_{out} holding the dc output voltage, the rectifier operation is nonlinear even using ideal diodes

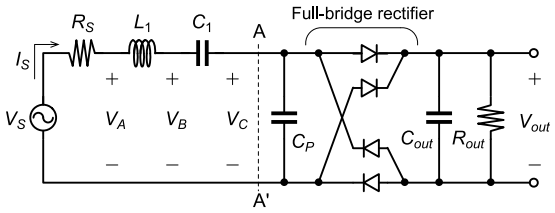

Fig. 4. Block diagram of a standard interface circuit.

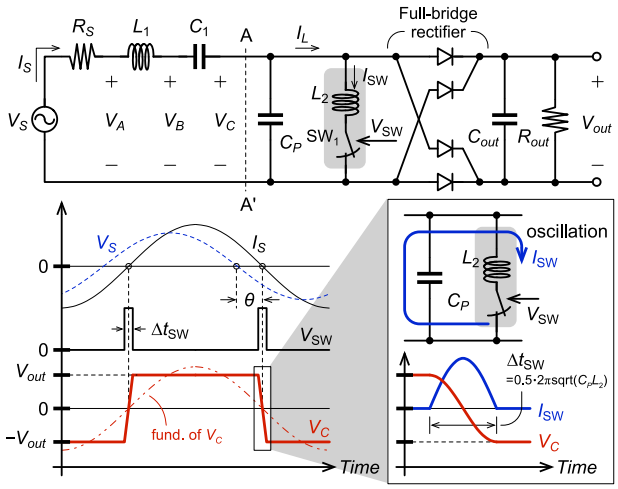

Fig. 5. Block and timing diagrams of conventional parallel-SSHI interface circuit.

with zero turn-on voltage. C_P needs to be charged/discharged for part of the period each time when the source current changes polarity before the rectifier can be turned on [9], [14], [17]. This degrades the amount of energy flowing to output, and the extracted power can be as low as 20% of the available power in case with a large C_P that results in a low electromechanical coupling coefficient ($k_e^2 = C_1/C_P$) [14].

C. Parallel-SSHI Interface

Fig. 5 shows the conceptual block and timing diagrams of parallel-SSHI interface [13], [14]. In parallel-SSHI interface, a switched inductor (L_2+SW$_1$) is added to the standard interface. As the displacement reaches its peak, or equivalently at zero crossing of the source current, the switch SW$_1$ turns ON for a short period of time, $\Delta t_{\rm SW}$, connecting a small inductor L_2 ($L_2 \ll L_1$) in parallel with C_P. With small L_2, the current flowing through L_2 increases rapidly. On the other hand, a large L_1 that corresponds to a large mass M results in small acceleration and therefore prevents the increase of piezoelectric current ($I_S = \Theta\dot{u}$). As a result, L_2 draws current from C_P, causing rapid change of the piezoelectric voltage V_C. Furthermore, $\Delta t_{\rm SW}$ is set so that the oscillation between C_P and L_2 lasts for only half a period, flipping the voltage across C_P, as shown in Fig. 5. Typically, $\Delta t_{\rm SW}$ is much smaller than the operating period. If the switching is ideal and incurs no loss, the capacitor voltage $|V_C|$ before and after the switching stays the same. In between the voltage flipping events, the rectifier is ON in either positive

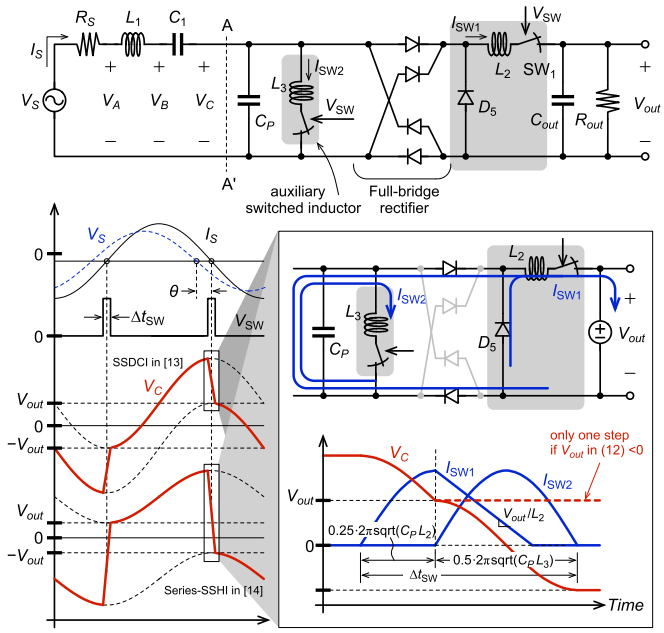

Fig. 6. Block and timing diagrams of conventional series-SSHI interface circuit.

or negative configuration. With ideal zero voltage drop across the rectifier, this effectively shorts the transducer and establishes a constant capacitor voltage $|V_C|$ of V_{out}. The resulting V_C can be considered as a square wave.

The *short-circuit* architecture as well as the switching operation eliminates the need to charge and discharge C_P by the source as needed in the standard interface. Furthermore, by switching at zero crossing of the source current, the voltage and current at A–A′ interface are in phase. If we only consider the fundamental of operating frequency, the transducer sees an equivalent loading that is purely resistive $Z_{L,\rm eq} = R_{L,\rm eq}$.

D. Series-SSHI Interface

On the other hand, in series-SSHI operation as shown in Fig. 6, the transducer is disconnected by turning OFF the switch SW$_1$ and sees an *open-circuit* load for most part of the operation. Therefore, the source current charges and discharges C_P, establishing a capacitor voltage that has 90° phase lag with respect to the source current. In series-SSHI operation, switching events also happen at zero crossings of the source current. However, the switched inductor L_2 is connected in series with the transducer. It is during the switching events when the harvested energy gets transferred to the supplied system.

There have been a few variants of the open-circuit-typed switching operation. For example, series-SSHI in [14], [25] flips the capacitor voltage with respect to the rectified voltage V_{out}. Depending on the values of initial V_C (which is denoted as $V_{\rm M}$) and V_{out}, the resulting end voltage ($-V_{\rm m}$) after flipping can be either positive or negative. SSDCI in [13] discharges C_P either completely or to some positive voltage without flipping it. Synchronous electric charge extraction in [24], synchronous charge extraction in [25], and pulsed synchronous charge extraction in

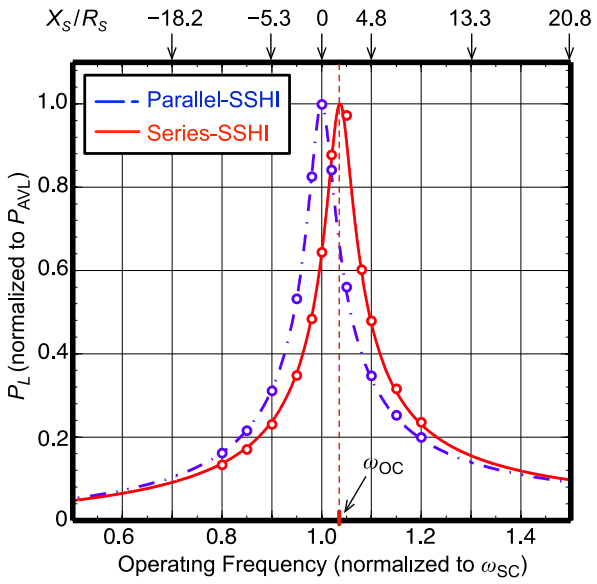

Fig. 7. Extracted power versus operating frequency with conventional parallel- and series-SSHI interfaces. ($R_S = 66.87$ kΩ, $L_1 = 2051$ H, $C_1 = 0.7338$ nF, and $C_P = 9.718$ nF. This gives system parameters of $k_e^2 = \Theta^2/(KC_P) = 0.076$ and $\zeta_m = \eta_m/(2\sqrt{KM}) = 0.02$ [14].) The curves show analytical predictions by loading the transducer with the equivalent load impedance. The data points show the circuit simulation results using ideal *RLC*, diode, and switch components. $L_2 = 10$ mH is used in the simulations. This figure also shows the quality factor of the source impedance X_S/R_S at different frequencies.

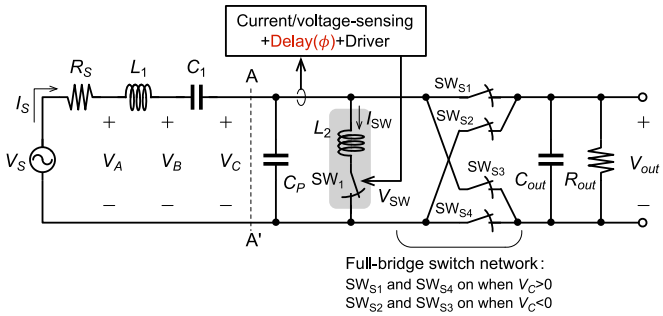

Fig. 8. Block diagram of the proposed P-SSHI-ϕ interface circuit.

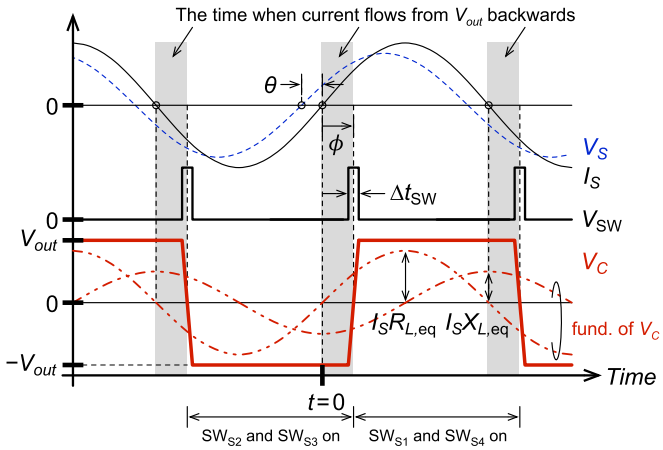

Fig. 9. Conceptual timing diagram of the proposed P-SSHI-ϕ interface circuit. Notice that the fundamental of V_C can be decomposed into two terms, with one in phase with I_S and the other in quadrature phase with I_S. This results in an equivalent complex load impedance.

[19] discharge the C_P completely, and, depending on the values of V_C and V_{out}, two different discharging paths are proposed in [19]. The switching in [18] involves several switching steps that span across a few cycles, and the capacitor C_P is discharged completely at last.

In this study, we propose a general architecture that can cover the single-cycle operations [13], [14], [19], [24], [25] by optionally involving a second step. As shown in Fig. 6, in the first step of the two-step switching operation, the series switch turns ON for a short period of time, connecting the transducer to the rest of the circuit. Therefore, C_P resonates with L_2 in series with $C_{out}//R_{out}$ that can be seen as a voltage source V_{out} during quasi-steady state. The switch SW_1 only turns ON for a quarter of the oscillation period, discharging C_P until the capacitor voltage equals V_{out}. Following this, a second set of auxiliary switch and inductor L_3 turns ON to flip the capacitor voltage. The diode D_5 is to transfer the residual energy in L_2 to the supplied system completely [13].

From the timing diagram in Fig. 6, the voltage V_C can be decomposed into two components, one sinusoidal due to I_S charging C_P from the open-circuit operation, and the other square wave that is in phase with the source current due to switching. In other words, if we only consider the fundamental of operating frequency, by incorporating C_P into the operation and by switching at zero crossing of the source current, series-SSHI presents an equivalent loading at A–A′ interface of a series combination of C_P and an equivalent load resistor $Z_{L,\mathrm{eq}} = 1/(j\omega C_P) + R_{L,\mathrm{eq}}$.

E. Challenge in Frequency Alignment

In order to achieve an MPT so as to extract the maximum power available from the transducer, these synchronous-switching techniques rely on operating at resonant frequencies. Parallel-SSHI interface preferably operates at the *short-circuit resonant frequency* where L_1 and C_1 form a short, while series-SSHI interface preferably operates at the *open-circuit resonant frequency* where the series combination of L_1, C_1, and C_P exhibits zero reactance. Frequency mismatch results in residual reactance seen by the source V_S and a phase shift θ between V_S and I_S as shown in Figs. 5 and 6. Take the parameters in [14] as an example and set $R_S = 66.87$ kΩ, $L_1 = 2051$ H, $C_1 = 0.7338$ nF, and $C_P = 9.718$ nF. The electromechanical coupling coefficient, $k_e^2 = \Theta^2/(KC_P)$, is 0.0755, and the mechanical damping ratio, $\zeta_m = \eta_m/(2\sqrt{KM})$, is 0.02 in this case. Fig. 7 shows the extracted power P_L normalized to P_{AVL} versus the operating frequency with parallel- and series-SSHI interfaces, both from analytical predictions and from Spice circuit simulations. With the residual reactance $X_{\mathrm{res}} = X_S = \omega L_1 - 1/\omega C_1$ for parallel-SSHI and $X_{\mathrm{res}} = X_S - 1/\omega C_P = \omega L_1 - 1/\omega C_1 - 1/\omega C_P$ for series-SSHI, $R_{L,\mathrm{eq}}$ is set to $\sqrt{R_S^2 + X_{\mathrm{res}}^2}$ to maximize the output power. Therefore, the results in Fig. 7 are slightly higher than those in [14] as $R_{L,\mathrm{eq}}$ is adjusted according to the

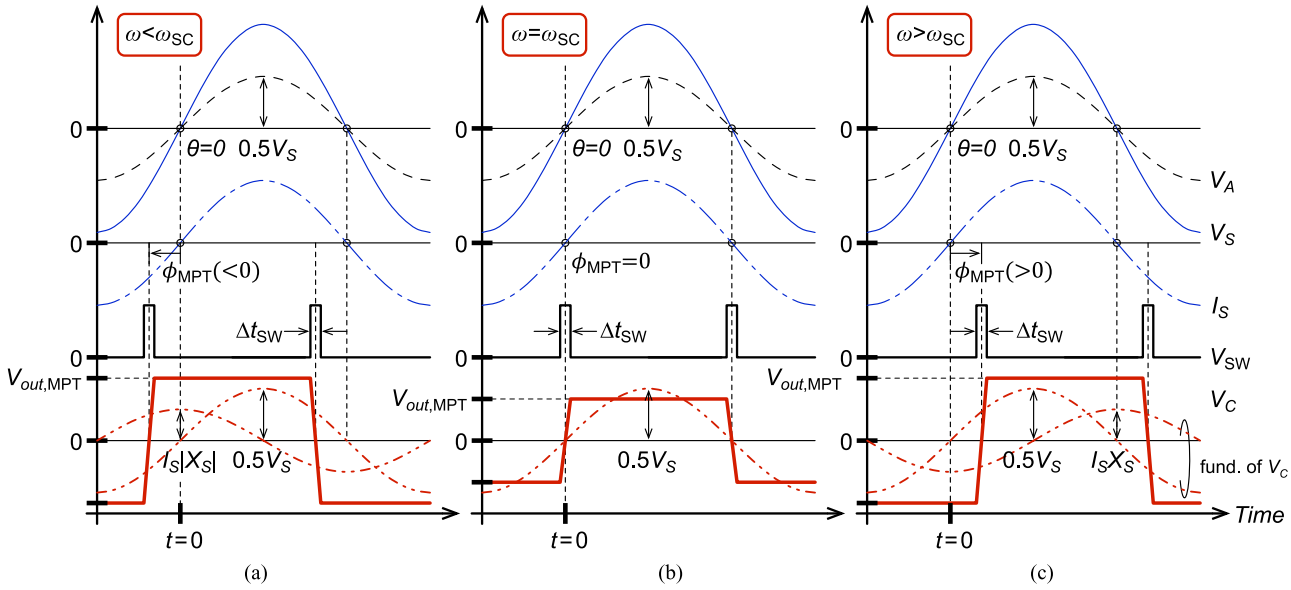

Fig. 10. Conceptual timing diagrams at MPT of the proposed P-SSHI-ϕ interface circuit with $\omega < \omega_{\rm SC}$, $\omega = \omega_{\rm SC}$, and $\omega > \omega_{\rm SC}$. V_{out} and ϕ are adjusted so that $Z^{\rm P}_{L,\rm eq} = Z^*_S$. Therefore, V_S and V_A are in phase with I_S, and the voltage across R_S is half of V_S.

operating frequency instead of a fixed value. However, the extracted power still degrades rapidly as the frequency deviation increases.

Frequency alignment has been a tough challenge in practice. From (1) and (2), the resonant frequencies of the transducer are determined by the mechanical characteristics of the structure, and would not necessarily be the same as the frequency of the external forcing function [22], [28]. In some applications, like the tire pressure sensing system, the applying frequency is even changing with time.

III. Proposed Interface Circuits

From the discussion in Section II-A, when operating at frequencies away from resonant frequencies, loading composed of both resistive and reactive parts is required, in which, the resistive part extracts power from the source while the reactive part cancels the residual reactance of the source impedance. This can be achieved by introducing a delay, either positive or negative, into the switching timing. The technique can be applied to both short-circuit and open-circuit architectures. In other words, the conventional parallel- and series-SSHI interfaces can be viewed as special cases of the proposed methods by setting the delay to zero.

A. Short-Circuit Method (P-SSHI-ϕ)

Figs. 8 and 9 show the conceptual block and timing diagrams for the proposed P-SSHI-ϕ interface circuit with a short-circuit configuration. It is similar to the conventional parallel-SSHI interface that adds a switched inductor ($L_2 + {\rm SW}_1$) to the standard interface, except for an additional delay stage in the control circuit. As the switching takes place at a phase delay ϕ with respect to the zero crossing of source current, and if we only consider the fundamental of operating frequency, the resulting V_C can be written as

$$V^{\rm P}_C(t) = \frac{4}{\pi} V_{out} \sin(\omega t - \phi) \tag{4}$$

where the superscript P stands for P-SSHI-ϕ interface. This is to delay the switching timing by $\Delta t = \phi/\omega$.

Notice that, in our analysis, the phase of each signal is considered with respect to the source current. Therefore, according to Fig. 9, with $I_S(t) = I_S \sin \omega t$ at the fundamental of operating frequency, $V_S(t) = V_S \sin(\omega t + \theta)$ where θ is not necessarily zero depending on the loading condition. Also notice that with $\phi \neq 0$, the voltage (V_C) and current (I_S) at A–A′ interface do not always have the same polarity. For part of the period, the current flows from V_{out} backwards. Therefore, a rectifier composed of diodes cannot be used here. What we need is a full-bridge switch network that allows negative current, such as that in [29], which changes configuration according to its instant input voltage. As shown in Figs. 8 and 9, ${\rm SW}_{\rm S1}$ and ${\rm SW}_{\rm S4}$ are ON when $V_C > 0$. During this time, the current flowing through the switches can be either positive or negative. By the same token, ${\rm SW}_{\rm S2}$ and ${\rm SW}_{\rm S3}$ are ON when $V_C < 0$[1].

From (4), a quadrature term appears by introducing ϕ into the operation. In other words, the fundamental of V_C can be decomposed into two terms, with one in phase with I_S and the other in quadrature phase with I_S. The equivalent load impedance seen at A–A′ interface therefore becomes complex and can be written as $Z^{\rm P}_{L,\rm eq} = R^{\rm P}_{L,\rm eq} + jX^{\rm P}_{L,\rm eq}$ with

$$R^{\rm P}_{L,\rm eq} = \frac{4}{\pi}\frac{V_{out}}{I_S}\cos\phi \ \text{ and} \tag{5}$$

$$X^{\rm P}_{L,\rm eq} = -\frac{4}{\pi}\frac{V_{out}}{I_S}\sin\phi = -R^{\rm P}_{L,\rm eq}\tan\phi \ \text{ where} \tag{6}$$

[1]With a rectifier composed of diodes, the negative current discharges C_P during the time interval of ϕ. This changes the resulting waveform of V_C and can degrade the desired impedance matching characteristics.

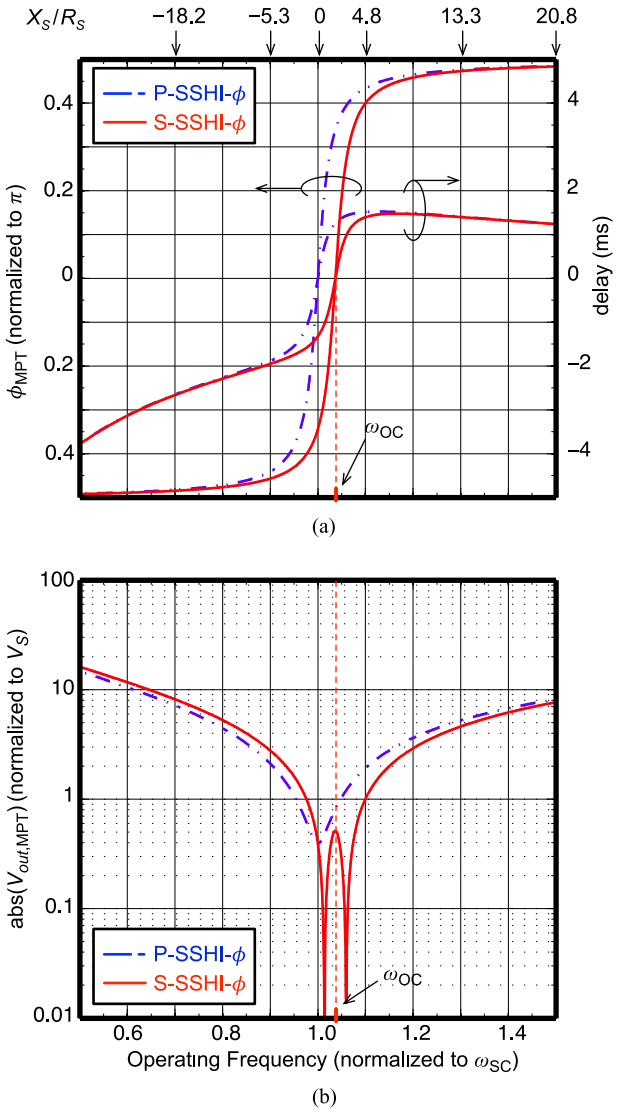

Fig. 11. (a) ϕ_{MPT} and the corresponding delay. (b) $V_{out,\mathrm{MPT}}$ versus operating frequency with the proposed P-SSHI-ϕ and S-SSHI-ϕ interfaces. ($R_S = 66.87$ kΩ, $L_1 = 2051$ H, $C_1 = 0.7338$ nF, and $C_P = 9.718$ nF. This gives $k_e^2 = 0.076$, $\zeta_m = 0.02$, $\omega_{\mathrm{SC}} = 2\pi 130$ rad/s, and $\omega_{\mathrm{OC}} = 2\pi 134.5$ rad/s.)

$$I_S = \frac{V_S}{\sqrt{(R_S + R^{\mathrm{P}}_{L,\mathrm{eq}})^2 + (X_S + X^{\mathrm{P}}_{L,\mathrm{eq}})^2}}. \tag{7}$$

It is clear that $Z^{\mathrm{P}}_{L,\mathrm{eq}}$ and therefore I_S can be varied by adjusting V_{out} and ϕ. Depending on the polarity of ϕ, the additional reactance can be either capacitive or inductive. Delaying the switching timing ($\phi > 0$) results in capacitive load, while advancing it ($\phi < 0$) gives inductive load. MPT can be achieved when $Z^{\mathrm{P}}_{L,\mathrm{eq}} = Z^*_S$. This gives

$$\phi^{\mathrm{P}}_{\mathrm{MPT}} = \arctan\frac{X_S}{R_S}. \tag{8}$$

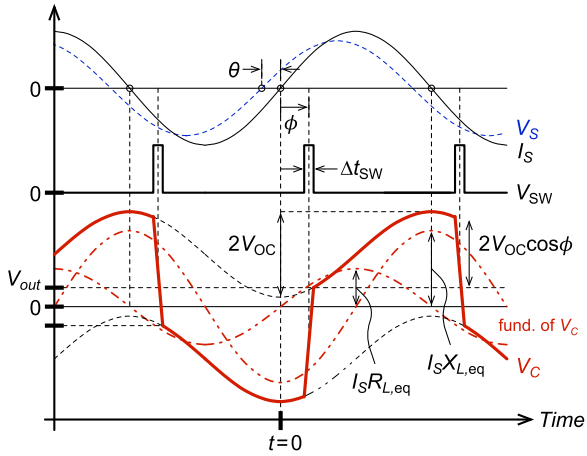

Fig. 12. Conceptual timing diagram of the proposed S-SSHI-ϕ interface circuit. Notice that how the quadrature-phase component of V_C is modified from V_{OC} by introducing the phase delay ϕ.

V_{out} can be further determined by knowing that $I_S = V_S/2R_S$ at MPT,[2] and therefore

$$\frac{V^{\mathrm{P}}_{out,\mathrm{MPT}}}{V_S} = \frac{\pi}{8}\frac{1}{\cos(\phi^{\mathrm{P}}_{\mathrm{MPT}})}. \tag{9}$$

In this case, V_C can be written as

$$\begin{aligned} V^{\mathrm{P}}_{C,\mathrm{MPT}}(t) &= \frac{V_S}{2}\sin\omega t - \frac{V_S}{2}\tan(\phi^{\mathrm{P}}_{\mathrm{MPT}})\cos\omega t \\ &= \frac{V_S}{2}\frac{1}{\cos(\phi^{\mathrm{P}}_{\mathrm{MPT}})}\sin(\omega t - \phi^{\mathrm{P}}_{\mathrm{MPT}}). \end{aligned} \tag{10}$$

With the same design parameters as those in previous section, Fig. 11(a) shows $\phi^{\mathrm{P}}_{\mathrm{MPT}}$ and the corresponding delay in time versus the operating frequency with the proposed P-SSHI-ϕ interface. The sharp slope close to ω_{SC} is from the high quality factor of the piezoelectric transducer. Fig. 11(b) then shows $V^{\mathrm{P}}_{out,\mathrm{MPT}}/V_S$ versus the operating frequency. Equations (8) and (9) also show that $\phi^{\mathrm{P}}_{\mathrm{MPT}} = 0$ and $V^{\mathrm{P}}_{out,\mathrm{MPT}}/V_S = \pi/8$ at ω_{SC}, and the operation is the same as the conventional parallel-SSHI. The increase in V_{out} as the operating frequency deviates from the resonant frequency can be seen as a result of the source current I_S flowing into a complex load. The high voltage could limit the applicability of the proposed method by increasing the leakage current and potentially damaging the electronic devices.

Fig. 10 shows the conceptual timing diagrams at MPT for three different frequencies. It can clearly be seen how the in-phase and quadrature-phase components of the loading can be set to match the source impedance by varying V_{out} and ϕ.

B. Open-Circuit Method (S-SSHI-ϕ)

Fig. 12 shows the conceptual timing diagram for the proposed S-SSHI-ϕ interface circuit with an open-circuit configuration. It is similar to the conventional series-SSHI interface except for

[2]With detailed calculations in Section II-A, it can be shown that, for each set of (V_{out}, ϕ), there can be two sets of possible solutions of ($Z^{\mathrm{P}}_{L,\mathrm{eq}}$, I_S).

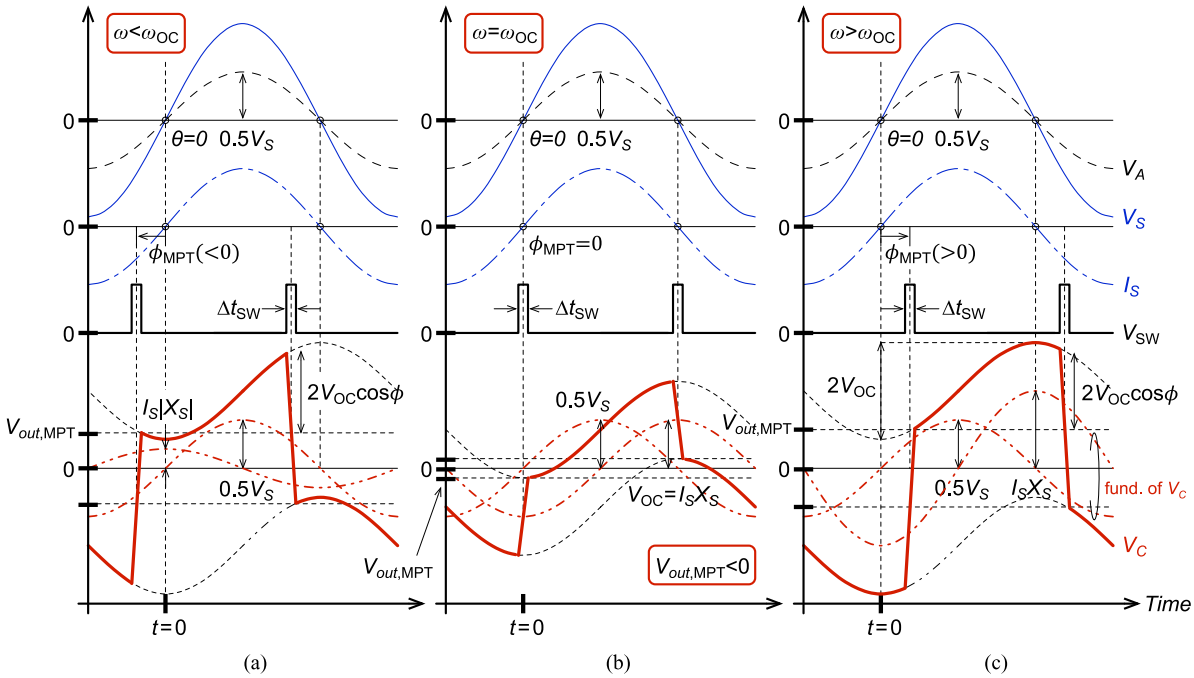

Fig. 13. Conceptual timing diagrams at MPT of the proposed S-SSHI-ϕ interface circuit with $\omega < \omega_{\rm OC}$, $\omega = \omega_{\rm OC}$, and $\omega > \omega_{\rm OC}$. V_{out} and ϕ are adjusted so that $Z^{\rm S}_{L,\rm eq} = Z^*_S$. Therefore, V_S and V_A are in phase with I_S, and the voltage across R_S is half of V_S.

a phase delay ϕ in the switching timing. Due to the fact that the harvested energy is transferred to the supplied system only during the switching event, the current flowing into V_{out} is never negative. In this case, either diodes or switches can be used for ac–dc conversion.

From Fig. 12, the square-wave component of V_C is shifted due to the phase delay ϕ. If we only consider the fundamental of operating frequency, the resulting V_C can be written as

$$V^{\rm S}_C(t) = \frac{4}{\pi}(V_{out} + V_{\rm OC}\cos\phi)\sin(\omega t - \phi) - V_{\rm OC}\cos\omega t \qquad (11)$$

where $V_{\rm OC} = I_S/\omega C_P$ is the amplitude of the open-circuit sinusoid.

With $\phi \neq 0$, an *additional* quadrature term appears by introducing ϕ into the operation. The equivalent load impedance can therefore be written as $Z^{\rm S}_{L,\rm eq} = R^{\rm S}_{L,\rm eq} + jX^{\rm S}_{L,\rm eq}$ with

$$\begin{aligned} R^{\rm S}_{L,\rm eq} &= \frac{4}{\pi}\left(\frac{V_{out}}{I_S} + \frac{\cos\phi}{\omega C_P}\right)\cos\phi \text{ and} \\ X^{\rm S}_{L,\rm eq} &= -\frac{1}{\omega C_P} - \frac{4}{\pi}\left(\frac{V_{out}}{I_S} + \frac{\cos\phi}{\omega C_P}\right)\sin\phi \\ &= -\frac{1}{\omega C_P} - R^{\rm S}_{L,\rm eq}\tan\phi. \end{aligned}$$

Similar to P-SSHI-ϕ, $Z^{\rm S}_{L,\rm eq}$ and therefore I_S can be varied by adjusting V_{out} and ϕ. Furthermore, the additional reactance can be increased or decreased by adjusting ϕ. Therefore, with frequency deviation, MPT can still be achieved by setting $Z^{\rm S}_{L,\rm eq} = Z^*_S$. This gives

$$\phi^{\rm S}_{\rm MPT} = \arctan\frac{X_S - 1/\omega C_P}{R_S}.$$

V_{out} can be further determined by knowing that $I_S = V_S/2R_S$ at MPT, and therefore

$$\frac{V^{\rm S}_{out,\rm MPT}}{V_S} = \frac{\pi}{8}\frac{1}{\cos(\phi^{\rm S}_{\rm MPT})} - \frac{\cos(\phi^{\rm S}_{\rm MPT})}{2\omega R_S C_P}. \qquad (12)$$

In this case, V_C can be written as

$$\begin{aligned} &V^{\rm S}_{C,\rm MPT}(t) \\ &= \frac{V_S}{2}\sin\omega t - \frac{V_S}{2}\tan(\phi^{\rm S}_{\rm MPT})\cos\omega t - V_{\rm OC,MPT}\cos\omega t \\ &= \frac{V_S}{2}\frac{1}{\cos(\phi^{\rm S}_{\rm MPT})}\sin(\omega t - \phi^{\rm S}_{\rm MPT}) - V_{\rm OC,MPT}\cos\omega t \qquad (13) \end{aligned}$$

where $V_{\rm OC,MPT} = V_S/(2\omega R_S C_P)$ is the amplitude of the open-circuit sinusoid when MPT is achieved.

Fig. 11 also shows the results with S-SSHI-ϕ interface in red curves. Notice that $\phi^{\rm S}_{\rm MPT} = 0$ and $V^{\rm S}_{out,\rm MPT}/V_S = (\pi/8 - 1/2\omega_{\rm OC}R_S C_P)$ at $\omega_{\rm OC}$, and the operation is the same as conventional series-SSHI interface. Furthermore, $V^{\rm S}_{out,\rm MPT} = 0$ at $\omega_{\rm OC}$ when $\pi/4 = 1/\omega_{\rm OC}R_S C_P$, which matches (25) in [25]. Also notice that, depending on the values of R_S and C_P, $V^{\rm S}_{out,\rm MPT}$ can be negative when close to $\omega_{\rm OC}$. To avoid redundancy and to minimize loss, as shown in Fig. 6, the switching can be reduced to only one step. Fig. 13 shows the conceptual timing diagrams at MPT for three different frequencies for S-SSHI-ϕ interface.

Furthermore, as the operation transfers energy to the supplied load twice in a period, the average extracted power can be written as

$$P^{\rm S}_L = 2\left(\frac{1}{2}C_P(V_{out} + V_{\rm OC})^2 - \frac{1}{2}C_P V^2_{out}\right)\frac{\omega}{2\pi}.$$

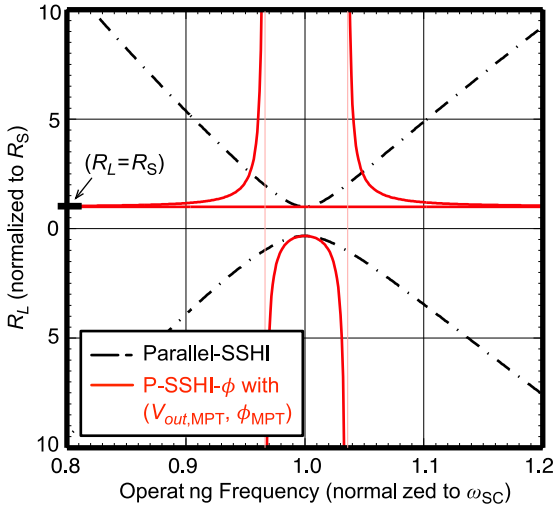

Fig. 14. Resulting $R^{\mathrm{P}}_{L,\mathrm{eq}}$ with the proposed P-SSHI-ϕ and the conventional parallel-SSHI interfaces.

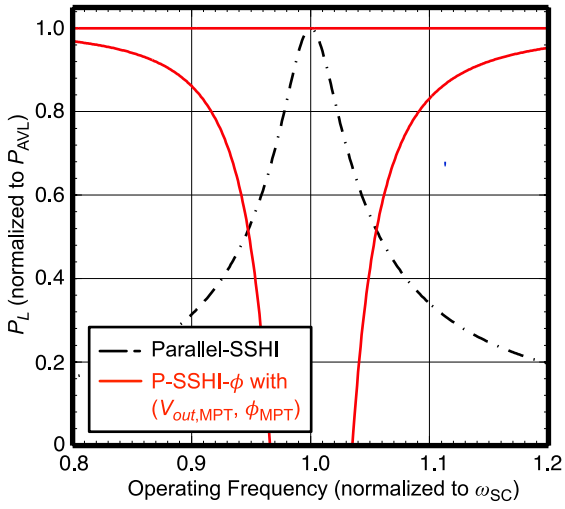

Fig. 15. Extracted power versus operating frequency with the proposed P-SSHI-ϕ and the conventional parallel-SSHI interfaces.

It can be shown that, with $V_{out} = V^{\mathrm{S}}_{out,\mathrm{MPT}}$ and $V_{\mathrm{OC}} = V_{\mathrm{OC,MPT}}$, the system delivers a power that equals P_{AVL} to the load.

IV. Design Considerations

From Section III, the proposed methods achieve MPT by adjusting the load impedance so that it matches the source impedance. This greatly boosts the extracted power and therefore extends the operating frequency range. To give more insight into the switching operation, in this section, we discuss a few design considerations that can offset the performance improvement from the proposed techniques.

A. Two Possible Modes

Considering the proposed P-SSHI-ϕ interface, for a given set of V_{out} and ϕ, the equivalent load impedance and the resulting source current can be calculated from (5), (6), and (7), which are repeated here again for clarity

$$R^{\mathrm{P}}_{L,\mathrm{eq}} = \frac{4}{\pi}\frac{V_{out}}{I_S}\cos\phi \text{ and}$$

$$X^{\mathrm{P}}_{L,\mathrm{eq}} = -\frac{4}{\pi}\frac{V_{out}}{I_S}\sin\phi = -R^{\mathrm{P}}_{L,\mathrm{eq}}\tan\phi \text{ where}$$

$$I_S = \frac{V_S}{\sqrt{(R_S + R^{\mathrm{P}}_{L,\mathrm{eq}})^2 + (X_S + X^{\mathrm{P}}_{L,\mathrm{eq}})^2}}.$$

By manipulating the three equations, we have the following:

$$\left(\frac{1}{V_S^2} - \frac{\pi^2}{16V_{out}^2}\right)\frac{\left(R^{\mathrm{P}}_{L,\mathrm{eq}}\right)^2}{\cos^2\phi} + (2R_S - 2X_S\tan\phi)\frac{R^{\mathrm{P}}_{L,\mathrm{eq}}}{V_S^2} + \frac{(R_S)^2 + (X_S)^2}{V_S^2} = 0 \quad (14)$$

and there are two possible solutions for $R^{\mathrm{P}}_{L,\mathrm{eq}}$. Fig. 14 shows the resulting $R^{\mathrm{P}}_{L,\mathrm{eq}}$ if (V_{out}, ϕ) are set to $(V^{\mathrm{P}}_{out,\mathrm{MPT}}, \phi^{\mathrm{P}}_{\mathrm{MPT}})$. As shown in Fig. 14, one of the two solutions always equals R_S that achieves MPT as expected. The second solution is negative when the operating frequency is close to ω_{SC}. As a result, instead of extracting power from the transducer, the load system behaves like a source, providing power back to the transducer. This is due to the use of a switch network that allows negative current to flow from V_{out} backwards. This can drain the stored energy, resulting in system failure. A possible solution would be to incorporate a power meter, such as the one in [30], into the system and restart the power extraction process once a power leakage instead of power extraction is detected. One thing to notice is that, for S-SSHI-ϕ interface, the analysis would seem exactly the same. However, the use of diodes instead of switches for ac–dc conversion prevents negative current that flows from V_{out} backwards. As a result, there exists only one positive solution for the load resistance $R^{\mathrm{S}}_{L,\mathrm{eq}}$ in S-SSHI-ϕ interface.

From (14), the two solutions become both positive when $V^{\mathrm{P}}_{out,\mathrm{MPT}}/V_S > \pi/4$. From (8) and (9), this happens when the frequency deviation is large enough so that $|X_S| > \sqrt{3}R_S$, as can be seen from Fig. 14. Fig. 15 shows the resulting extracted power with the two solutions. For large frequency deviation when two positive solutions are possible, the proposed method could settle to the inferior solution, and the extracted power degrades.

By the same token, the conventional parallel-/series-SSHI interfaces can exhibit two modes of operation as well, if a full-bridge switch network [5], [29] is used to improve the ac–dc conversion efficiency. Given $\phi = 0$ and V_{out} that maximizes the extracted power, Fig. 14 also shows the resulting $R_{L,\mathrm{eq}}$ for conventional parallel-SSHI interface. The second solution is always negative across the operating frequency range.

One thing to notice is that the two solutions exhibit the same V_{out} and ϕ, which is the phase relationship between the switching timing and zero crossing of source current. However, because the total impedances seen by the voltage source are different, the two solutions exhibit different phase relationship

between the switching timing and zero crossing of the voltage source. In a piezoelectric energy harvesting system, a low-power accelerometer [31], [32] can be used to provide information about the phase of voltage source. The switching timing can be adjusted accordingly to guarantee the optimal solution.

B. Impact of Errors in V_{out} and ϕ

From the previous section, it is clear that the equivalent loading and therefore extracted power can be adjusted by varying the output voltage V_{out} and the delay in switching timing ϕ. This, therefore, raises the issue of sensitivity of the extracted power on V_{out} and ϕ errors.

From (14) and using the same design parameters as in previous sections, Fig. 16(a) shows how the extracted power is degraded when ϕ is fixed at $\phi^{\rm P}_{\rm MPT}$ while V_{out} is set to $V^{\rm P}_{out,\rm MPT}$ with errors of -10% to -50%. Furthermore, Fig. 16(b) shows the case with *positive* errors in switching timing from $+0.1$ to $+1\%$ of the oscillation period with step of $+0.1\%$ ($\sim$10 μs in this case). With positive errors, the switching timing is delayed or advanced even more. Apparently, voltage and timing errors degrade the extracted power, and the extracted power is much more sensitive to timing than to voltage error. Furthermore, the impact becomes more severe as the operating frequency deviates from resonant frequencies.

Notice that from Fig. 14, as the frequency deviation becomes large, the two solutions for $R^{\rm P}_{L,\rm eq}$ become close. Errors in V_{out} or ϕ can potentially lead to nonreal solutions. This is what happens when V_{out} is increased or when negative error is introduced into the switching timing at ($V^{\rm P}_{out,\rm MPT}$, $\phi^{\rm P}_{\rm MPT}$).

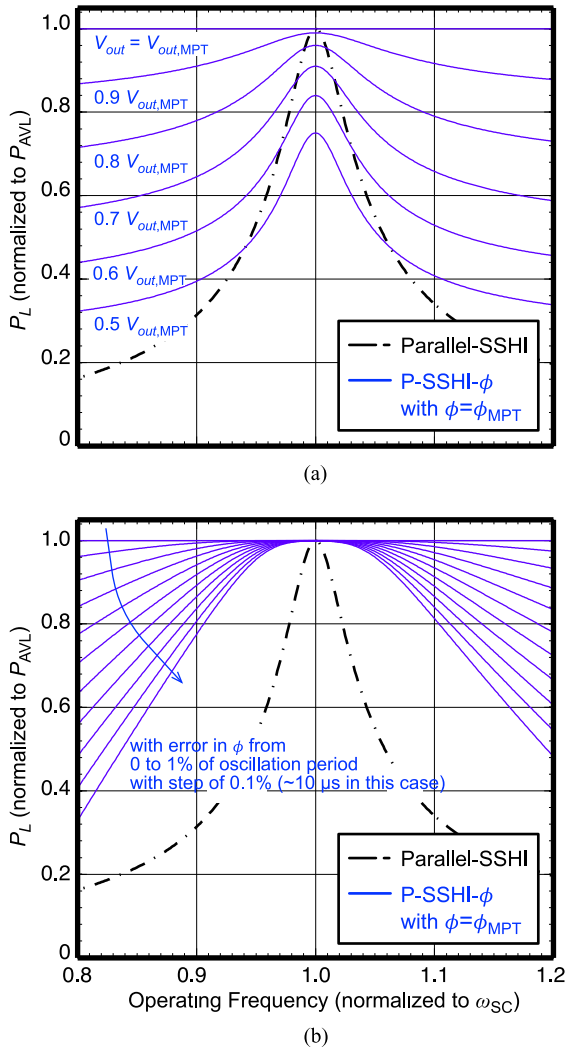

Fig. 16. Extracted power with the proposed P-SSHI-ϕ interface versus operating frequency with errors in (a) V_{out} and (b) switching timing. ($R_S = 66.87$ kΩ, $L_1 = 2051$ H, $C_1 = 0.7338$ nF, and $C_P = 9.718$ nF. This gives $k_e^2 = 0.076$ and $\zeta_m = 0.02$.)

C. Impact of High-Order Harmonics

Due to the switching operations, the system is highly nonlinear in nature and we have to consider the existence of high-order harmonics in the system. Equations (10) and (13) can be modified into (15) and (16), shown at the bottom of the page.

At high-order frequencies, the voltage source V_S is a short. High-order voltage components at V_C result in high-order currents flowing back to the source. Considering the third-order harmonic 3ω, the current magnitude depends on the source impedance of R_S, L_1, and C_1 in series at 3ω. For both interfaces, the source current can therefore be written as (17), shown at the bottom of the page, where $Q(3\omega)$ is the quality factor of the source impedance Z_S at 3ω

$$Q(3\omega) = \frac{3\omega L_1 - 1/3\omega C_1}{R_S}.$$

$$V^{\rm P}_{C,\rm MPT}(t) = \frac{V_S}{2}\frac{1}{\cos(\phi^{\rm P}_{\rm MPT})}(\sin(\omega t - \phi^{\rm P}_{\rm MPT}) + \frac{1}{3}\sin(3\omega t - 3\phi^{\rm P}_{\rm MPT}) + \cdots) \tag{15}$$

$$V^{\rm S}_{C,\rm MPT}(t) = \frac{V_S}{2}\frac{1}{\cos(\phi^{\rm S}_{\rm MPT})}(\sin(\omega t - \phi^{\rm S}_{\rm MPT}) + \frac{1}{3}\sin(3\omega t - 3\phi^{\rm S}_{\rm MPT}) + \cdots) - V_{\rm OC,MPT}\cos\omega t \tag{16}$$

$$I_S(t) = \frac{V_S}{2R_S}\sin\omega t - \frac{V_S}{6}\frac{1}{\cos(\phi_{\rm MPT})}\frac{1}{R_S\sqrt{1+Q^2(3\omega)}}\sin(3\omega t - 3\phi_{\rm MPT} - \arctan(Q(3\omega))) + \cdots \tag{17}$$

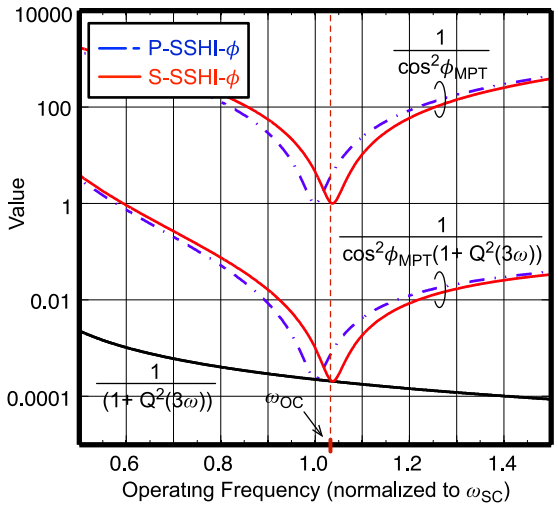

Fig. 17. Impact of high-order harmonics from switching events on extracted power.

The current component at 3ω incurs power loss through heat dissipation in R_S, and this power loss (at 3ω) can be written as

$$P_{\text{loss},3} = \frac{1}{9}\frac{P_{\text{AVL}}}{\cos^2\phi_{\text{MPT}}\,(1+Q^2(3\omega))}. \tag{18}$$

In (18), both terms $\cos\phi_{\text{MPT}}$ and $Q(3\omega)$ vary with the operating frequency. Using the same design parameters as in previous sections, Fig. 17 shows $1/\cos^2\phi_{\text{MPT}}$ and $1/(1+Q^2(3\omega))$ versus the operating frequency. As the operating frequency deviates from resonant frequencies, the term $1/\cos^2\phi_{\text{MPT}}$ increases rapidly. However, the effect is suppressed at high frequencies due to better quality factor of Z_S. Fig. 18 then shows the resulting extracted power by taking $P_{\text{loss},3}$ into consideration for both interfaces. The loss is not significant ($< 0.1P_{\text{AVL}}$) unless the operating frequency is way off-resonance ($\omega < 0.6\omega_{\text{SC}}$).[3] Fig. 18 also shows the simulated extracted power using Spice simulations with ideal *RLC*, diode, and switch components. From the simulation results, considering only the third-order harmonic gives decent accuracy.

In P-SSHI-ϕ, the lost energy comes from the supplied system as the charges on C_P stay constant and only change plates during switching. In S-SSHI-ϕ, the third-order current and the associated power come from C_P. Part of the charges, instead of flowing to the supplied system, flow back to the source. In fact, MPT is achieved at fundamental frequency in these switching systems. However, part of the extracted power gets translated to high-order harmonics and gets dissipated by flowing back through the source resistance R_S.

D. Switching Loss

The analysis in previous sections has assumed that the switching is ideal. In other words, no energy is lost during the switching. However, parasitic resistance in the current loop consumes power. Considering P-SSHI-ϕ interface, with the switch on-resistance R_{SW}, the capacitor voltage $|V_C|$ drops by $\exp(-0.5\pi R_{\text{SW}}\sqrt{C_P/L_2})$ during each switching event. The associated power loss can be written as

$$P_{\text{loss,SW}} = C_P V_{out}^2\left(1-\exp\left(-\pi R_{\text{SW}}\sqrt{\frac{C_P}{L_2}}\right)\right)\frac{\omega}{2\pi}. \tag{19}$$

Setting (V_{out}, ϕ) to ($V_{out,\text{MPT}}$, ϕ_{MPT}) and considering the switching loss, Fig. 18 shows the resulting extracted power for P-SSHI-ϕ and S-SSHI-ϕ interfaces with the switch resistance that corresponds to a flipping quality factor $Q_F = \sqrt{L_2/C_P}/R_{\text{SW}}$ of 100 and 10. The impact increases as the operating frequency deviates from the resonant frequencies. This is due to the increase in $V_{out,\text{MPT}}$ as can be seen from Fig. 11(b). The amount of energy stored on C_P also increases. Therefore, the same percentage of energy loss during each switching event corresponds to a more energy loss while P_{AVL} does not change. The resulting P_L can even be worse than that of the conventional parallel- and series-SSHI interfaces when the frequency deviation is large.

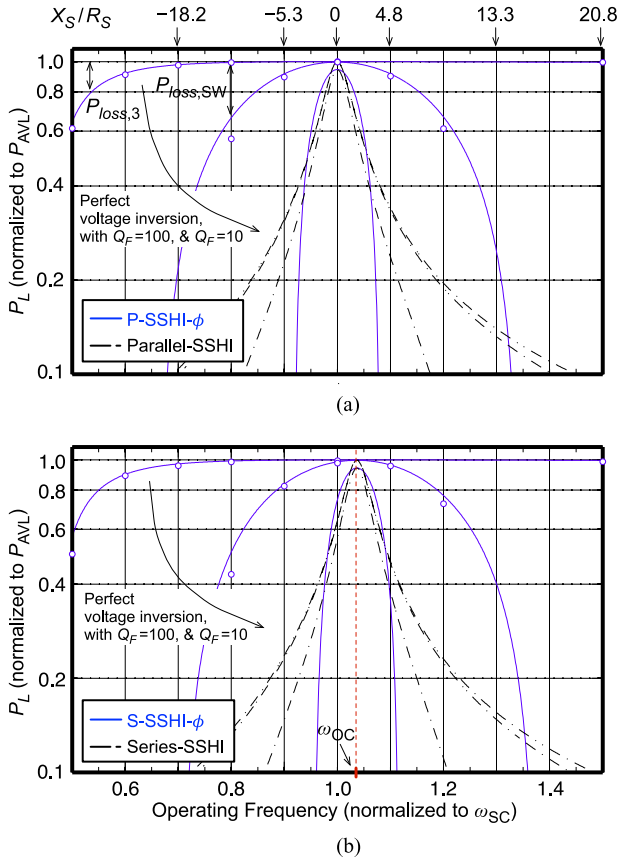

Fig. 18. Extracted power versus operating frequency with the proposed (a) P-SSHI-ϕ and (b) S-SSHI-ϕ interfaces with $V_{out,\text{MPT}}$ and ϕ_{MPT}. (R_S = 66.87 kΩ, L_1 = 2051 H, C_1 = 0.7338 nF, and C_P = 9.718 nF. This gives $k_e^2 = 0.076$ and $\zeta_m = 0.02$.) The curves show theoretical results by considering $P_{\text{loss},3}$ from (18) and $P_{\text{loss,SW}}$ from (19) with Q_F of 10 and 100. The data points show the circuit simulation results using ideal *RLC*, diode, and switch components. L_2 = 10 mH is used in the simulations. This figure also shows the quality factor of the source impedance X_S/R_S at different frequencies.

[3] If there is another vibration mode at the vicinity of odd multiples of operating frequency (such as $3 \times 0.6\omega_{\text{SC}}$) and the quality factor is high, the switching activities can indeed very likely excite this vibration mode, changing the overall system dynamics.

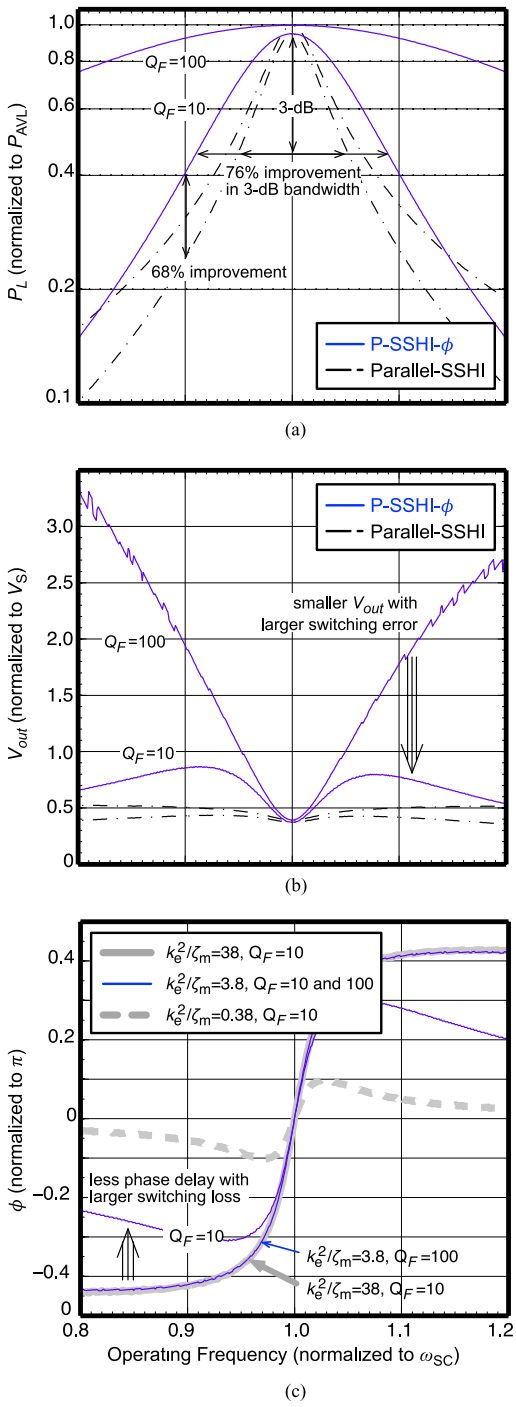

Fig. 19. (a) The maximum extracted power and the corresponding (b) V_{out} and (c) ϕ with $Q_F = 10$ and 100 for the proposed P-SSHI-ϕ interface. $R_S = 66.87$ kΩ, $L_1 = 2051$ H, $C_1 = 0.7338$ nF, and $C_P = 9.718$ nF. This gives $k_e^2 = 0.076$, $\zeta_m = 0.02$, and resulting k_e^2/ζ_m of 3.8. In (c), two additional cases with C_P of 0.9718 and 97.18 nF that result in k_e^2/ζ_m of 38 and 0.38 are also shown with $Q_F = 10$.

In fact, a lower V_{out} can be chosen in order to reduce the impact from imperfect voltage inversion. While a $V_{out} \neq V_{out,\mathrm{MPT}}$ results in imperfect impedance matching, a net improvement over the conventional parallel- and series-SSHI interfaces can still be obtained. Fig. 19 shows the results with $Q_F = 100$ and 10 by setting (V_{out}, ϕ) to values that maximize

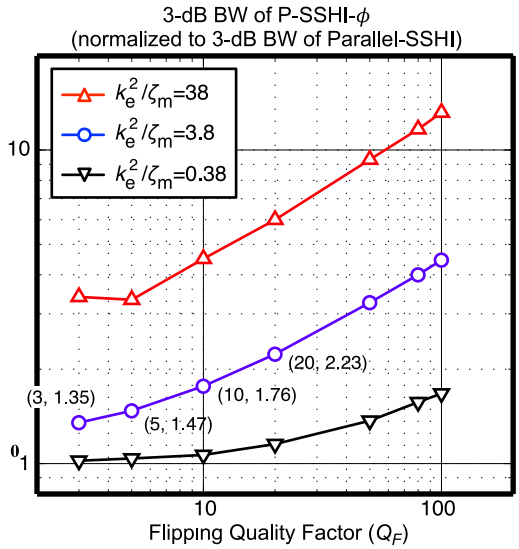

Fig. 20. Improvement in 3-dB bandwidth of the proposed P-SSHI-ϕ interface over the conventional parallel-SSHI interface versus the flipping quality factor. $R_S = 66.87$ kΩ, $L_1 = 2051$ H, and $C_1 = 0.7338$ nF, resulting in $\zeta_m = 0.02$. C_P is set to 0.9718, 9.718, and 97.18 nF that correspond to k_e^2/ζ_m of 38, 3.8, and 0.38, respectively.

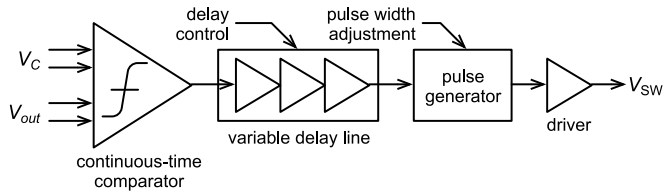

Fig. 21. Possible implementation of the control circuit in Fig. 8.

the extracted power for P-SSHI-ϕ interface. From Fig. 19(b) and (c), as $V_{out} < V_{out,\mathrm{MPT}}$ is used to suppress the loss from switching, a smaller phase delay is also preferred to properly balance the load resistance and reactance. In Fig. 19(c), two additional cases with different C_P values are also shown in gray curves with $Q_F = 10$. Smaller C_P value corresponds to a higher electromechanical coupling coefficient and reduces switching loss [from (19)]. This alleviates the need for lowering V_{out} and ϕ to compensate the switching loss even with Q_F of 10.

From Fig. 19(a), the proposed technique always outperforms the conventional method. For a flipping quality factor Q_F of 10, the extracted power of the conventional parallel-SSHI interface can be improved up to $\sim 68\%$ and the 3-dB bandwidth is extended by 76%. Fig. 20 further shows how the improvement in 3-dB bandwidth increases with the flipping quality factor for three cases with k_e^2/ζ_m of 38, 3.8, and 0.38, respectively.

E. Control Circuit Implementation

A possible implementation of the control circuit for the proposed P-SSHI-ϕ and S-SSHI-ϕ interfaces is shown in Fig. 21. The proposed techniques require an additional delay element in the control circuit as compared to the conventional interface. As shown in Figs. 11(a) and 16, the delay needs to be tuned with microsecond accuracy over a millisecond range, depending on the

operating frequency. Such a timing control can be obtained using a variable current sourcing and sinking a capacitor followed by a voltage detector, which is the basic operation principle of relaxation oscillators [33]. Prior designs with nanosecond of tuning accuracy [17] and millisecond of tuning range [33]–[36] have been reported with submicrowatt of power consumption using state-of-the-art IC technology.

Similar to the conventional parallel- and series-SSHI interfaces that need to optimize the load resistance to extract the maximum power, a complete system for the proposed techniques requires an algorithm that performs the searching for optimal (V_{out}, ϕ) settings. A start-up calibration can be performed in cases with a fixed operating frequency. In applications where the applying frequency is changing with time, like a tire pressure sensing system, V_{out} and ϕ need to be tuned dynamically according to the instantaneous input frequency, which requires an additional control circuit and results in additional power consumption. A system-level optimization is needed when incorporating such adaptive adjustments into the operation to ensure a net improvement in harvested power. A compromised method would be to set a fixed delay that corresponds to the average input frequency.

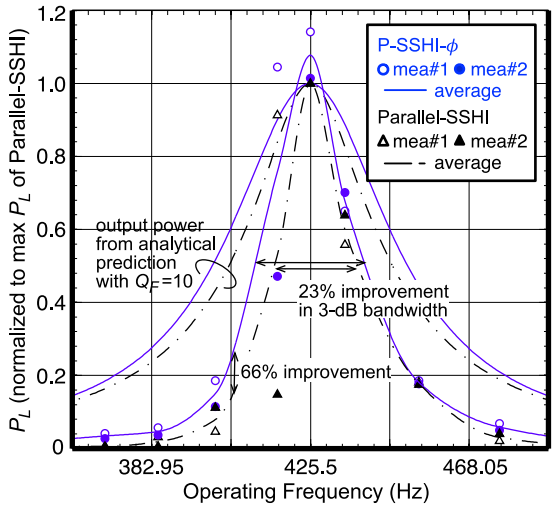

Fig. 22. Measured output power versus the operating frequency. The curves show the scaled version of theoretical predictions with system parameters of $R_S = 37.2$ kΩ, $L_1 = 260.0$ H, $C_1 = 0.551$ nF, and $C_P = 15.5$ nF. This gives $k_e^2 = 0.036$ and $\zeta_m = 0.027$.

V. Experimental Validation

In order to validate the proposed techniques and the theoretical analysis presented in previous sections, an experiment was set up using a commercially available piezoelectric device (model V22B) from Midé. The piezoelectric device was mounted on a shaker (LDS V406) which was excited using a sinusoidal wave from a signal generator amplified through a power amplifier (LDS PA 100E). The acceleration is set to 2.5 g for the measurement.

The measured open-circuit resonant frequency is at ~ 425 Hz. With the parameters given by the manufacturer ($\Theta = 1.07 \times 10^{-3}$, $\eta = 0.0426$, and $K = 2076.5$), the system parameters are estimated to be $R_S = 37.2$ kΩ, $L_1 = 260.0$ H, and $C_1 = 0.551$ nF. The mechanical damping ratio ζ_m is 0.027 in this case. In the experiment, a switching inductor L_2 of 880 μH is used. $\Delta t_{\rm SW}$ is adjusted to 11.6 μs for best voltage inversion results. We can therefore estimate C_P to be 15.5 nF, and the resulting electromechanical coupling coefficient k_e^2 is 0.036.

N-Channel MOSFETs (VN0606L) and P-Channel MOSFETs (VP030) are used for the electronic interface similar to that in [17]. As mentioned in Section III-A, a full-bridge switch network [29] that allows negative current is used for voltage rectification. With short-circuit operations (parallel-SSHI and P-SSHI-ϕ), the resulting flipping quality factor Q_F is roughly 7. A pulse generator that has the timing synchronized with the vibrational signal generator is used to control the switch $\rm SW_1$. The pulse width, the relative phase delay, and the output loading R_{out} are adjusted manually to maximize the extracted power. Results with conventional parallel-SSHI interface are obtained by making sure that the voltage drop across the rectifier is zero, which indicates $I_S = 0$, right before the switching takes place [17].

Fig. 22 shows the measured results along with the theoretical predictions. The experiment is performed twice, and the measured output power is averaged after being normalized to the maximum power for the conventional parallel-SSHI case. For the two sets of measurement, introducing delay into the switching timing always improves the output power. Curve-fitting using the built-in function "pchip" in Matlab shows a 23% improvement in 3-dB bandwidth and a 66% improvement in extracted power with 5% of frequency mismatch over the conventional parallel-SSHI interface. One of the factors that causes discrepancy between experimental results and analytical predictions is that the output power is measured after the rectifier whose efficiency varies with V_{out}, while in the analysis, it is the input power (at A–A′ interface) to the rectifier. Other possible factors include the nonlinear characteristics as well as the other vibration modes of the transducer that are not captured by the model in Fig. 3.

VI. Discussion and Conclusion

This paper presents two interface circuit designs for piezoelectric energy harvesting system. The proposed architectures involve nonlinear switching activities and improve the extracted power when the system is operating at off-resonance. MPT is achieved with complex impedance matching by presenting adequate loading to the front-end transducer. The equivalent loading can be adjusted by varying the transducer's output voltage and switching timing.

Detailed analysis is provided to estimate the performance with practical considerations, such as V_{out} and ϕ errors as well as parasitic loss due to high-frequency components and series resistance in switches. A complete system requires an algorithm that performs the searching for optimal (V_{out}, ϕ) settings either upon start-up or dynamically under different operating conditions. Proper monitoring signals that indicate the extracted power and the external applying force will also be needed. Furthermore, the building blocks need to consume low power

because they are, in most cases, also supplied by the harvested power.

Considering only the power interface, analytical results show that, with the electromechanical coupling coefficient k_e^2 of 0.076 and the mechanical damping ratio ζ_m of 0.02, the proposed techniques can improve the 3-dB bandwidth of the conventional methods by 76% with a flipping quality factor of 10. Furthermore, experimental results with a commercially available piezoelectric device (model V22B) from Midé show that the 3-dB bandwidth is improved by 23% and the extracted power with 5% of frequency mismatch is improved by 66% as compared with the conventional method with zero switching delay.

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REFERENCES

[1] J. A. Paradiso and T. Starner, "Energy scavenging for mobile and wireless electronics," *IEEE Pervasive Comput.*, vol. 4, no. 1, pp. 18–27, Jan. Mar.2005.

[2] R. J. Vullers, R. V. Schaijk, H. J. Visser, J. Penders, and C. V. Hoof, "Energy harvesting for autonomous wireless sensor networks," *IEEE Solid-State Circuits Mag.*, vol. 2, no. 2, pp. 29–38, Jun. 2010.

[3] J. A. Hagerty, F. B. Helmbrecht, W. H. McCalpin, R. Zane, and Z. B. Popovic, "Recycling ambient microwave energy with broad-band rectenna arrays," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 3, pp. 1014–1024, Mar. 2004.

[4] T. Paing, J. Shin, R. Zane, and Z. Popovic, "Resistor emulation approach to low-power RF energy harvesting," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1494–1501, May2008.

[5] P. Hsieh and T. Chiang, "An RF energy harvester with 35.7% PCE at PIN of -15 dBm," in *Proc. Symp. VLSI Circuits Dig. Tech. Papers*, 2013, pp. C224–C225.

[6] E. J. Carlson, K. Strunz, and B. P. Otis, "A 20 mv input boost converter with efficient digital control for thermoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 741–750, Apr. 2010.

[7] Y. K. Ramadass and A. P. Chandrakasan, "A battery-less thermoelectric energy harvesting interface circuit with 35 mv startup voltage," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 333–341, Jan. 2011.

[8] K. Kadirvel, Y. Ramadass, U. Lyles, J. Carpenter, V. Ivanov, V. McNeil, A. Chandrakasan, and B. Lum-Shue-Chan, "A 330na energy-harvesting charger with battery management for solar and thermoelectric energy harvesting," in *Proc. IEEE ISSCC Dig. Tech. Papers*, 2012, pp. 106–108.

[9] D. Guyomar, A. Badel, E. Lefeuvre, and C. Richard, "Toward energy harvesting using active materials and conversion improvement by nonlinear processing," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 52, no. 4, pp. 584–595, Apr. 2005.

[10] J. Liang and W. H. Liao, "Impedance modeling and analysis for piezoelectric energy harvesting systems," *IEEE/ASME Trans. Mechatronics*, vol. 17, no. 6, pp. 1145–1157, Dec. 2012.

[11] Y. C. Shu and I. C. Lien, "Analysis of power output for piezoelectric energy harvesting systems," *Smart Mater. Struct.*, vol. 15, no. 6, pp. 1499–1512, 2006.

[12] Y. C. Shu, I. C. Lien, and W. J. Wu, "An improved analysis of the SSHI interface in piezoelectric energy harvesting," *Smart Mater. Struct.*, vol. 16, no. 6, pp. 2253–2264, 2007.

[13] W. J. Wu, A. M. Wickenheiser, T. Reissman, and E. Garcia, "Modeling and experimental verification of synchronized discharging techniques for boosting power harvesting from piezoelectric transducers," *Smart Mater. Struct.*, vol. 18, no. 5, pp. 055012-1–055012-14, 2009.

[14] I. C. Lien, Y. C. Shu, W. J. Wu, S. M. Shiu, and H. C. Lin, "Revisit of series-SSHI with comparisons to other interfacing circuits in piezoelectric energy harvesting," *Smart Mater. Struct.*, vol. 19, no. 12, pp. 125009-1–125009-12, 2010.

[15] D. Kwon and G. A. Rincon-Mora, "A single-inductor ac-dc piezoelectric energy-harvester/battery-charger ic converting $\pm$(0.35 to 1.2 v) to (2.7 to 4.5 v)," in *Proc. IEEE ISSCC Dig. Tech. Papers*, 2010, pp. 494–495.

[16] E. O. Torres and G. A. Rincon-Mora, "A 0.7-μm BiCMOS electrostatic energy-harvesting system IC," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 483–496, Feb. 2010.

[17] Y. K. Ramadass and A. P. Chandrakasan, "An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 189–204, Jan. 2010.

[18] R. D. Prabha, D. Kwon, O. Lazaro, K. D. Peterson, and G. A. Rincon-Mora, "Increasing electrical damping in energy-harnessing transducers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 12, pp. 787–791, Dec. 2011.

[19] T. Hehn, F. Hagedorn, D. Maurath, D. Marinkovic, I. Kuehne, A. Frey, and Y. Manoli, "A fully autonomous integrated interface circuit for piezoelectric harvesters," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2185–2198, Sep. 2012.

[20] M. Dini, M. Filippi, M. Tartagni, and A. Romani, "A nano-power power management ic for piezoelectric energy harvesting applications," in *Proc. 9th Conf. Ph.D. Res. Microelectron. Electron.*, 2013, pp. 269–272.

[21] E. Lefeuvre, D. Audigier, C. Richard, and D. Guyomar, "Buck-boost converter for sensorless power optimization of piezoelectric energy harvester," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 2018–2025, Sep. 2007.

[22] I. C. Lien and Y. C. Shu, "Array of piezoelectric energy harvesting by the equivalent impedance approach," *Smart Mater. Struct.*, vol. 21, no. 8, pp. 082001-1–082001-8, 2012.

[23] G. W. Taylor, J. R. Burns, S. A. Kammann, W. B. Powers, and T. R. Welsh, "The energy harvesting eel: A small subsurface ocean/river power generator," *IEEE J. Ocean. Eng.*, vol. 26, no. 4, pp. 539–547, Oct. 2001.

[24] E. Lefeuvre, A. Badel, C. Richard, and D. Guyomar, "Piezoelectric energy harvesting device optimization by synchronous electric charge extraction," *J. Intell. Mater. Syst. Struct.*, vol. 16, no. 10, pp. 865–876, 2005.

[25] E. Lefeuvre, A. Badel, C. Richard, L. Petit, and D. Guyomar, "A comparison between several vibration-powered piezoelectric generators for standalone systems," *Sens. Actuators A: Phys.*, vol. 126, no. 2, pp. 405–416, 2006.

[26] M. Lallart, Y.-C. Wu, and D. Guyomar, "Switching delay effects on nonlinear piezoelectric energy harvesting techniques," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 464–472, Jan. 2012.

[27] D. Guyomar, M. Lallart, and T. Monnier, "Stiffness tuning using a low-cost semiactive nonlinear technique," *IEEE/ASME Trans. Mechatronics*, vol. 13, no. 5, pp. 604–607, Oct. 2008.

[28] S. Shelton, A. Guedes, R. Przybyla, R. Krigel, D. Horsley, and B. Boser, "Aluminum nitride piezoelectric micromachined ultrasound transducer arrays," in *Proc. Hilton Head Solid-State Sens., Actuators Microsyst. Workshop*, 2012, pp. 291–294.

[29] K. Kotani, A. Sasaki, and T. Ito, "High-efficiency differential-drive CMOS rectifier for UHF RFIDs," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3011–3018, Nov. 2009.

[30] S. Uprety and H. Lee, "A 43 v 400 mw-to-21 w global-search-based photovoltaic energy harvester with 350 transient time, 99.9% mppt efficiency, and 94% power efficiency," in *Proc. IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 404–405.

[31] H. Sun, D. Fang, K. Jia, F. Maarouf, H. Qu, and H. Xie, "A low-power low-noise dual-chopper amplifier for capacitive CMOS-MEMS accelerometers," *IEEE Sens. J.*, vol. 11, no. 4, pp. 925–933, Apr. 2011.

[32] S. S. Tan, C. Y. Liu, L. K. Yeh, Y. H. Chiu, M. S.-C. Lu, and K. Y.-J. Hsu, "An integrated low-noise sensing circuit with efficient bias stabilization for CMOS MEMS capacitive accelerometers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 11, pp. 2661–2672, Nov. 2011.

[33] U. Denier, "Analysis and design of an ultralow-power CMOS relaxation oscillator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1973–1982, Aug. 2010.

[34] C. Hwang, S. Bibyk, M. Ismail, and B. Lohiser, "A very low frequency, micropower, low voltage CMOS oscillator for noncardiac pacemakers," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 42, no. 11, pp. 962–966, Nov. 1995.

[35] J. Lim, K. Lee, and K. Cho, "Ultra low power RC oscillator for system wake-up using highly precise auto-calibration technique," in *Proc. ESSCIRC*, Sep. 2010, pp. 274–277.

[36] Y.-C. Shih, T. Shen, and B. P. Otis, "A 2.3 μw wireless intraocular pressure/temperature monitor," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2592–2601, Nov. 2011.

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