Hybrid Phase-Shift-Controlled Three-Level and *LLC* DC–DC Converter With Active Connection at the Secondary Side

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***Abstract*—This paper proposes a hybrid phase-shift-controlled three-level (TL) and *LLC* dc–dc converter. The TL dc–dc converter and *LLC* dc–dc converter have their own transformers. Compared with conventional half-bridge TL dc–dc converters, the proposed one has no additional switch at the primary side of the transformer, where the TL converter shares the lagging switches with the *LLC* converter. At the secondary side of the transformers, the TL and *LLC* converters are connected by an active switch. With the aid of the *LLC* converter, the zero voltage switching (ZVS) of the lagging switches can be achieved easily even under light load conditions. Wide ZVS range for all the switches can be ensured. Both the circulating current at the primary side and the output filter inductance are reduced. Furthermore, the efficiency of the converter is improved dramatically. The features of the proposed converter are analyzed, and the design guidelines are given in the paper. Finally, the performance of the converter is verified by a 1-kW experimental prototype.**

***Index Terms*—*LLC*, phase shift, three-level (TL), zero voltage switching (ZVS).**

I. Introduction

A THREE-LEVEL (TL) dc–dc converter with voltage stress of the switches reduced to half of the input voltage is widely used in industry applications. A family of the TL dc–dc converter has been investigated, and the essential relationships among them have been revealed [1]. The TL dc–dc converter is first proposed in [2]. The main feature of the converter is that the ZVS is achieved for all the switches. However, it is difficult for conventional TL dc–dc converters to achieve the ZVS for lagging switches especially at light loads. The switching noise and electromagnetic interference caused by hard switching degrade the performance of the converter. Moreover, the circulating current reduces the efficiency as the input voltage increases.

A series of practicable TL ZVS dc–dc converters has been introduced in [3]. The simplest implementation for achieving the ZVS of lagging switches is to add an external inductor at the primary side of the transformer [3]. However, the inductor leads to a large duty cycle loss and a large ringing of the secondary rectifiers. An inductor combined with two capacitors is used to achieve wide ZVS [4]. However, the additional inductor causes large circulating currents. An additional inductor with two clamping diodes can be used to achieve ZVS for lagging switches, and overshoot for secondary rectifiers can be suppressed [5]. Nevertheless, it still results in the increase of duty cycle loss. Another approach for achieving ZVS for the lagging switches is to enhance the magnetizing current to charge and discharge the junction capacitors by using two coupling inductors integrated in one core [6]. Besides, a TL converter achieving the ZVS for all switches is proposed in [7] by using two series-connected transformers. For the sake of extending the ZVS range for lagging switches, a TL dc–dc converter with an auxiliary coupling inductor at the primary side is introduced [8]. The energy stored in the auxiliary circuit is minimal at full loads and gradually increases as the load current decreases. However, large circulating currents still exist at the primary side. For ZVZCS TL dc–dc converters, MOSFETs are used for leading switches to achieve ZVS, and insulated-gate bipolar transistors (IGBTs) are used for lagging switches to achieve zero current switching (ZCS) [9], [10]. Moreover, the primary side circulating current is reduced. A new concept of dc–dc conversion with asymmetric pair of switches achieves hybrid ZVS–ZCS scheme is presented in [11], which can be regarded as a TL-derived dc–dc converter. In addition, multiphase TL dc–dc converter extending the duty cycle range for high power application is another solution for ZVZCS [12]. However, using IGBTs limits the switching frequency, which is not suitable for high frequency dc–dc conversion. Most of the researches aforementioned are based on half-bridge (HB) TL dc–dc converters. Full-bridge (FB) TL dc–dc converter is an alternative scheme for high voltage applications [13]–[15], but there are still some challenges for the FB TL dc–dc converters to achieve high efficiency and soft switching.

Resonant TL dc–dc converter with ZVS feature is investigated in [16]–[19]. Due to the elimination of output filter inductor, the voltage stress of the secondary diodes can be reduced. An *LLC* TL dc–dc converter with double resonant tanks by modulating the switching frequency is proposed in [18]. However, the variable switching frequency makes the electromagnetic compatibility design difficult. Resonant TL dc–dc converters with a constant switching frequency are provided in [17] and [19]. The main advantage is that the output voltage is regulated by using simple phase-shift or pulse width modulation (PWM) schemes.

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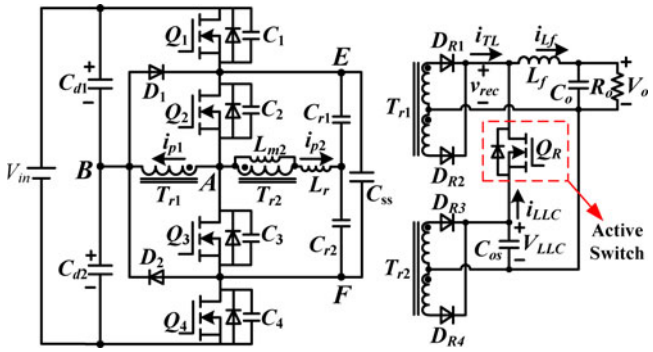

Fig. 1. Proposed hybrid TL and *LLC* converter.

A TL dc–dc converter combined with an FB converter is used to reduce the output filter inductance [20], [21]. However, more additional switches have to be used. Besides, a TL converter using two transformers without additional switches also can reduce the output filter size [22]. Recently, hybrid converters are attractive due to their outstanding performance. The hybrid converters integrate two or more converters into a new one, such as hybrid boost TL dc–dc converter [23], hybrid dual FB dc–dc converter [24], hybrid resonant and PWM converter [25], [26], three-phase TL dc/dc converter [27], and so on.

In this paper, a hybrid TL and *LLC* dc–dc converter is proposed with simple phase-shift control. The TL converter and *LLC* converter have their individual transformers. At the primary side of the transformers, the TL converter shares the lagging switches with the *LLC* converter. At the secondary side, the TL and *LLC* converters are connected by an active switch to minimize the conduction loss. The ZVS of the leading switches is similar to conventional HB TL dc–dc converters, while the ZVS of the lagging switches is determined by the *LLC* converter. Therefore, wide ZVS range can be achieved. Furthermore, the primary-side circulating current can be reduced, so the conversion efficiency can be improved.

This paper is organized as follows. The circuit and mode operation of the proposed converter is described in Section II. In Section III, the main features of the proposed converter are analyzed. The design guidelines of the converter are presented in Section IV. The experimental prototype with 550–600 V input voltage and 50 V/20 A output is built to verify the performance of the proposed converter in Section V. Finally, the conclusions are given in Section VI.

II. Proposed Hybrid TL and *LLC* DC–DC Converter

Fig. 1 shows the circuit configuration for the proposed converter, which is composed of an HB TL dc–dc converter and an HB *LLC* dc–dc converter. The divided capacitors C_{d1}, C_{d2}, and the flying capacitor C_{ss} are large enough to be treated as voltage sources of $V_{\rm in}/2$. Q_1 and Q_4 are leading switches; Q_2 and Q_3 are lagging switches. The TL converter shares the lagging switches Q_2 and Q_3 with the *LLC* converter. $C_1 - C_4$ are junction capacitors of the switches, and $C_1 = C_2 = C_3 = C_4 = C$. T_{r1} is the transformer of the TL converter, and T_{r2} is the transformer

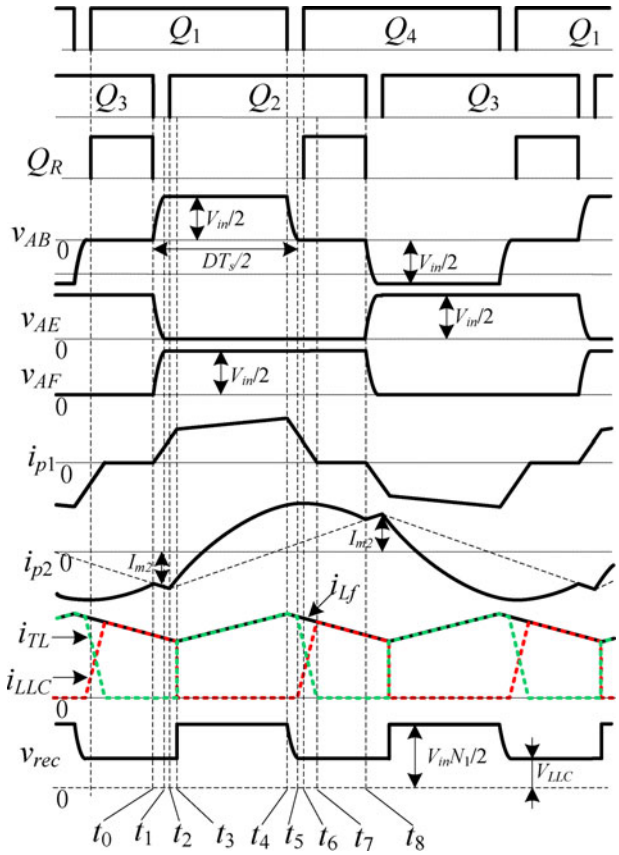

Fig. 2. Key waveforms of the proposed converter.

of the *LLC* converter. The turns ratio of the two transformers T_{r1} and T_{r2} is n_1:1:1 and n_2:1:1, respectively. L_{k1} is the leakage inductor of T_{r1}. The magnetizing inductor of T_{r1} is large enough to ignore the magnetizing current during the switching period. L_r is the resonant inductor of the *LLC* converter, and L_{m2} is the magnetizing inductor of T_{r2}. C_{r1} and C_{r2} are resonant capacitors, and $C_{r1} = C_{r2} = C_r$. Q_R, named as an active switch, works as a controlled rectifier to reduce the conduction loss.

Fig. 2 shows the key waveforms of the proposed converter. The proposed hybrid converter works with a constant switching frequency. The output voltage of the converter is controlled by the phase-shift manner. Gate signal of Q_R is expressed as $Q_R = Q_1 \cdot Q_3 + Q_2 \cdot Q_4$.

The *LLC* converter works in open-loop control. The resonant frequency is expressed as $f_r = 1/\left(2\pi\sqrt{2C_r L_r}\right)$. The *LLC* resonant frequency is chosen to be the switching frequency, so the voltage gain of the *LLC* converter is independent of the load and equal to 1 [28]. Therefore, the output voltage of the *LLC* converter is expressed as

$$V_{LLC} = \frac{V_{\rm in}}{4n_2}. \tag{1}$$

Moreover, the rectifiers D_{R3} and D_{R4} work in ZCS, so the reverse recovery is avoided. In view of the output voltage control, V_{LLC} should be less than the output voltage V_o. There are

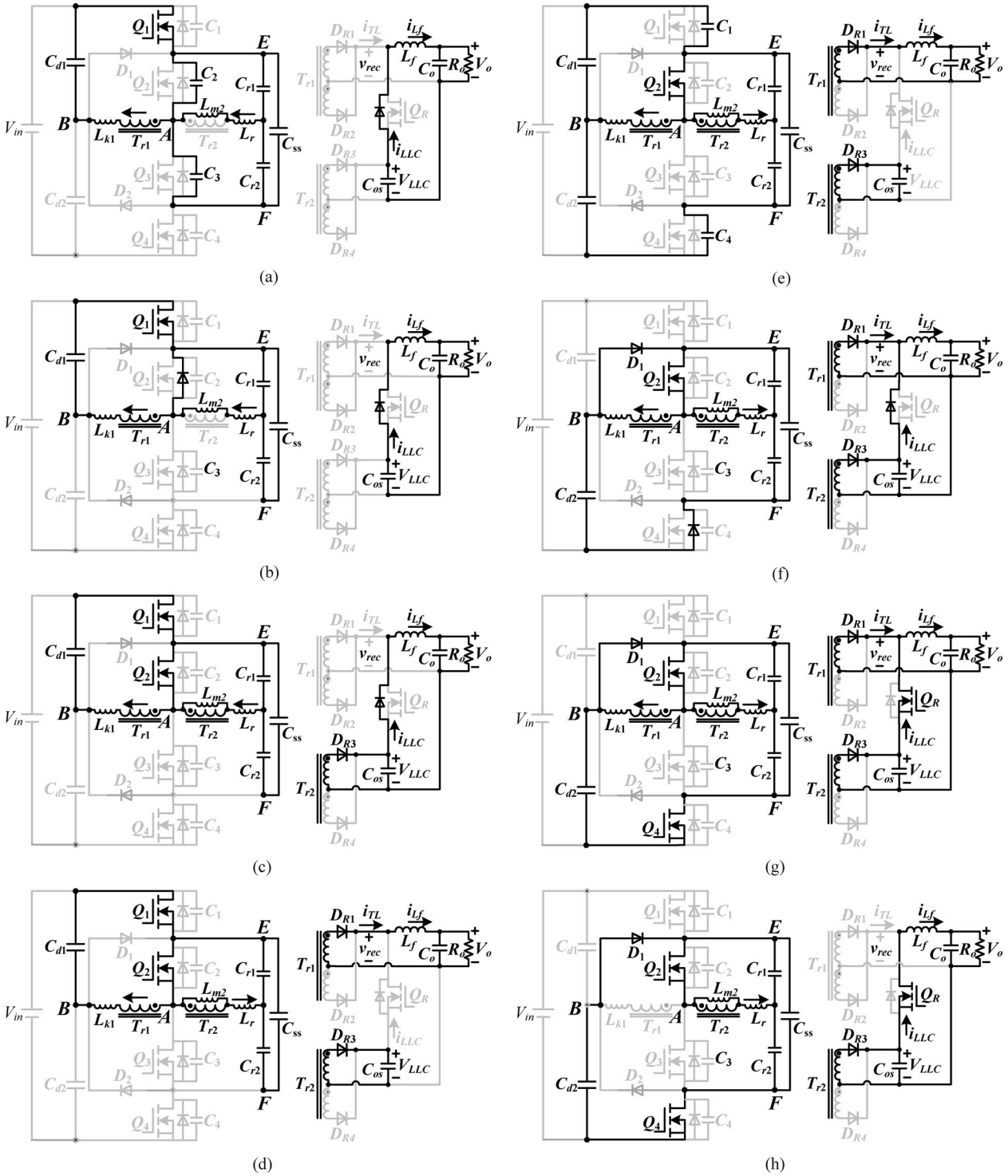

Fig. 3. Topological stages with half-switching cycle: (a) $[t_0, t_1]$, (b) $[t_1, t_2]$, (c) $[t_2, t_3]$, (d) $[t_3, t_4]$, (e) $[t_4, t_5]$, (f) $[t_5, t_6]$, (g) $[t_6, t_7]$, and (h) $[t_7, t_8]$.

seven working stages in each half-switching period, as shown in Fig. 2.

Stage 1 [t_0, t_1] [see Fig. 3(a)]: Prior to t_0, Q_1 and Q_3 are ON, and Q_2 and Q_4 are OFF. At time t_0, Q_3 is turned OFF. The primary winding current of transformer T_{r2} starts to charge and discharge the junction capacitors of Q_3 and Q_2, respectively. The primary winding current of T_{r1} starts to increase. Since $D_{R1} - D_{R4}$ are reverse biased, T_{r1} and T_{r2} do not transfer energy from the primary side to the secondary side, and i_{pr2} is equal to the magnetizing current of T_{r2}. The amplitude of the magnetizing current I_{m2} is expressed as

$$I_{m2} = \frac{V_{\text{in}} T_s}{16 L_{m2}} \tag{2}$$

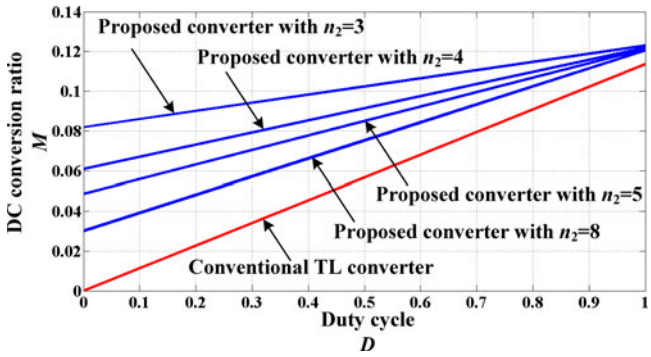

Fig. 4. DC conversion ratio versus duty cycle.

where T_s is the switching period. The output filter inductor current i_{Lf} freewheels through $C_{\rm os}$ and the body diode of Q_R. The primary winding current and voltages of the junction capacitors C_2 and C_3 are expressed as

$$\begin{aligned} i_{pr1} &= I_{m2} - I_{m2}\cos\left[\omega_m(t-t_0)\right] \\ v_{C2}(t) &= \frac{V_{\rm in}}{2} - \frac{I_{m2}}{2C\omega_m}\cdot\sin\left[\omega_m(t-t_0)\right] \\ v_{C2}(t) &= \frac{I_{m2}}{2C\omega_m}\cdot\sin\left[\omega_m(t-t_0)\right] \end{aligned} \tag{3}$$

where $\omega_m = \frac{1}{\sqrt{2CL_{k1}}}$.

Stage 2 [t_1, t_2] [see Fig. 3(b)]: At time t_1, the drain–source voltage of Q_2 reaches zero, and i_{pr2} flows through the body diode of Q_2. i_{pr2} is equal to I_{m2}. i_{pr1} increases linearly. The output filter inductor current i_{Lf} freewheels through $C_{\rm os}$ and the body diode of Q_R. i_{pr1} in this stage is expressed as

$$i_{pr1}(t) = i_{pr1}(t_1) + \frac{V_{\rm in}}{2L_{k1}}(t-t_1). \tag{4}$$

Stage 3 [t_2, t_3] [see Fig. 3(c)]: At time t_2, Q_2 is switched ON with ZVS. The inductor L_r starts to resonate with C_{r1} and C_{r2}. D_{R3} is forward biased. The *LLC* circuit starts to transfer power to the output. i_{Lf} still freewheels through $C_{\rm os}$ and the body diode of Q_R. i_{pr1} still increases linearly as expressed in (4).

Stage 4 [t_3, t_4] [see Fig. 3(d)]: At time t_3, D_{R1} is forward biased. The TL circuit transfers energy through T_{r1} to the output. At this time, the voltage of $v_{\rm rec}$ is larger than V_{LLC}, so the body diode of Q_R is reverse biased. The *LLC* circuit still charges the capacitor $C_{\rm os}$. i_{pr1} in this stage is expressed as

$$i_{pr1}(t) = i_{pr1}(t_3) + \frac{V_{\rm in}/2 - n_1 V_o}{L_{k1} + n_1^2 L_f}(t-t_3). \tag{5}$$

Stage 5 [t_4, t_5] [see Fig. 3(e)]: When Q_1 is turned OFF at t_4, the voltages across the junction capacitors C_1 and C_4 are charged and discharged linearly by the energy stored in the output filter inductor L_f. Since $v_{\rm rec}$ is larger than V_{LLC}, the body diode of Q_R is still reverse biased.

Stage 6 [t_5, t_6] [see Fig. 3(f)]: When C_1 reaches $V_{\rm in}/2$ and C_4 reaches zero, the body diode of Q_4 is forward biased. Simultaneously, when the voltage $v_{\rm rec}$ is less than V_{LLC}, the body diode of Q_R is forward biased. i_{LLC} starts to increase and flows through the body diode of Q_R, while $i_{\rm TL}$ decreases. The *LLC* circuit starts to transfer energy to the output.

Stage 7 [t_6, t_7] [see Fig. 3(g)]: At time t_6, Q_4 and Q_R are turned ON with ZVS. The primary winding current of T_{r1} decreases and freewheels through D_1 and Q_2. $i_{\rm TL}$ decreases, while i_{LLC} increases and flows through Q_R.

Stage 8 [t_7, t_8] [see Fig. 3(h)]: Stage 8 starts when i_{pri1} and $i_{\rm TL}$ reach zero. Then, D_{R1} and D_{R2} are both OFF, and $v_{\rm rec}$ is equal to V_{LLC}. The filter inductor current i_{Lf} is equal to i_{LLC}. i_{Lf} freewheels through Q_R and $C_{\rm os}$.

III. Analysis of the Converter

A. DC Conversion Ratio

The dc conversion ratio of the converter in continuous conduction mode can be derived from the volt–second balance for the output filter. It yields

$$\left(\frac{V_{\rm in}}{2n_1} - V_o\right)D_{\rm eff} + (V_{LLC} - V_o)(1 - D_{\rm eff}) = 0 \tag{6}$$

where $D_{\rm eff}$ is the effective duty cycle. Substituting (1) into (6), the dc conversion ratio of the converter is expressed as

$$M = \frac{V_o}{V_{\rm in}} = \frac{D_{\rm eff}}{2n_1} + \frac{1 - D_{\rm eff}}{4n_2}. \tag{7}$$

The effective duty cycle is expressed as

$$D_{\rm eff} = D - D_{\rm loss} = D - \frac{4V_o L_{k1}}{V_{\rm in} R_o n_1 T_s} = D - M\frac{4L_{k1}}{R_o n_1 T_s} \tag{8}$$

where R_o is the load resistance, T_s is the switching period, and L_{k1} is the leakage inductance of T_{r1}. Substituting (8) into (7), the dc conversion ratio in view of duty cycle loss is written by

$$M = \frac{V_o}{V_{\rm in}} = \frac{\frac{D}{2n_1} + \frac{1-D}{4n_2}}{1 + \left(\frac{2}{n_1} - \frac{1}{n_2}\right)\frac{L_{k1}}{R_o n_1 T_s}}. \tag{9}$$

For conventional TL converters analyzed in the same manner, the dc conversion ratio is expressed as

$$M = \frac{V_o}{V_{\rm in}} = \frac{\frac{D}{2n_1}}{1 + \frac{4L_{k1}}{R_o n_1^2 T_s}}. \tag{10}$$

Fig. 4 shows dc conversion ratio versus duty cycle for specifications $n_1 = 4$, $L_{k1} = 10\ \mu$H, $T_s = 10\ \mu$s, $R_o = 2.5\ \Omega$, and different n_2. The figure illustrates that the dc conversion ratio of the proposed converter is larger than the conventional TL converter.

The power distribution ratio of the two transformers is expressed as

$$\eta = \frac{P_{T_{r1}}}{P_{T_{r2}}} = \frac{(V_{\rm in}/2n_1)D_{\rm eff} I_{Lf}}{(V_{\rm in}/4n_2)(1 - D_{\rm eff})I_{Lf}} = \frac{2n_2 D_{\rm eff}}{n_1(1 - D_{\rm eff})}. \tag{11}$$

According to (7) and (11), the power distribution ratio is rewritten as

$$\eta = \frac{4n_2 M - 1}{1 - 2n_1 M}. \tag{12}$$

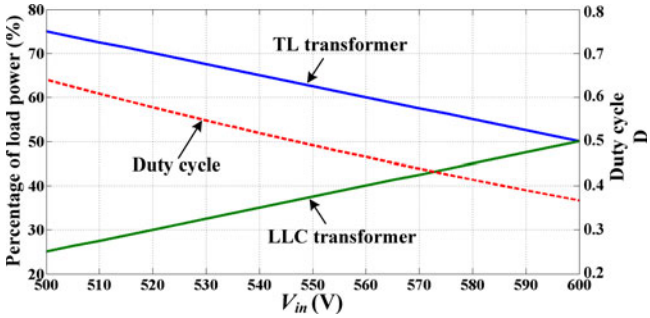

Fig. 5. Load distribution between the two transformers and the duty cycle with different input voltages.

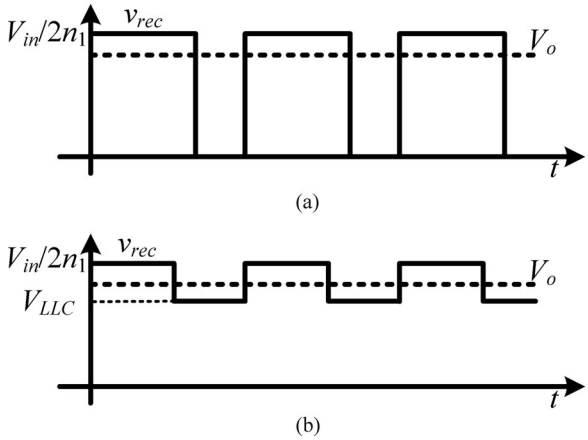

Fig. 6. Idealized rectifier voltage $v_{\rm rec}$: (a) conventional TL converter, and (b) proposed converter.

Fig. 5 shows the load power percentage of the two transformers and the duty cycle versus input voltage with specifications $V_{\rm in} = 500 - 600$ V, $V_o = 50$ V, $n_1 = 4$, $n_2 = 4$, $L_k = 10\ \mu$H, and $R_o = 2.5\ \Omega$. The two solid lines are the load power percentage of the two transformers, and the dashed line is the duty cycle of the converter. For constant output voltage, the duty cycle decreases with the increase of the input voltage. Meanwhile, the *LLC* transformer undergoes more load power and the TL transformer undergoes less power, as the duty cycle decreases.

B. Power Losses of the Active Switch

The active switch Q_R works as a controlled rectifier. If the active switch Q_R is replaced by a diode, the key waveforms of the converter are the same as that shown in Fig. 2. However, the voltage drop across the diode causes larger conduction loss especially in low output voltage and high output current conditions.

After the output current flows through the body diode of Q_R, Q_R is turned ON with ZVS. Due to the ZVS of Q_R, the switching loss is negligible. By using low voltage MOSFETs, the voltage drop is much lower than the diode. Therefore, the conduction loss is dramatically reduced.

C. ZVS Condition of Switches

In order to achieve ZVS for leading switches, the primary winding currents of the transformer should make their junction capacitor voltage to reach zero before the switch is turned ON. In this working stage, the primary current is reflected from the energy stored in the output filter inductor, which is similar to the conventional HB TL converter. Conventionally, the output filter is large enough to achieve ZVS even at light loads.

For the conventional HB TL dc–dc converter, the ZVS of lagging switches is achieved by the energy stored in the leakage inductor. For the proposed converter, the ZVS of lagging switches is achieved by the energy stored in the magnetizing inductor of T_{r2}. Taking Stage 1, for example, in order to achieve ZVS for lagging switches, v_{C2} should reach zero within the dead time, so the ZVS condition derived form (3) can be expressed as follows:

$$\begin{aligned} v_{C2} &= \frac{V_{\rm in}}{2} - \frac{I_{m2}}{2C\omega_m}\sin\omega_m t_{\rm dead} \\ &= \frac{V_{\rm in}}{2} - \frac{V_{\rm in}T_s}{32L_{m2}C\omega_m}\sin\omega_m t_{\rm dead} \le 0. \end{aligned} \tag{13}$$

Therefore, the magnetizing inductor L_{m2} for the ZVS condition should be selected as follows:

$$L_{m2} \le \frac{T_s}{16C\omega_m}\sin\omega_m t_{\rm dead} \tag{14}$$

where $t_{\rm dead}$ is the dead time between Q_2 and Q_3. The ZVS condition of the lagging switches is independent of the load. With the aid of the magnetizing inductor of the *LLC* transformer, the ZVS of lagging switches can be achieved within a wide load range.

D. Filter Inductor and Current Ripple

For conventional HB TL dc–dc converter, the rectifier voltage $v_{\rm rec}$ is zero during the freewheeling period, so the voltage across the filter inductor is $-V_o$. Therefore, the current ripple of the filter inductor Δi_{Lf_c} is expressed as

$$\Delta i_{Lf\_c} = \frac{V_{\rm in}(1-D)DT_s}{4n_1L_f}. \tag{15}$$

As seen in Fig. 6, for the proposed converter, $v_{\rm rec}$ is equal to V_{LLC} during the freewheeling period, so the voltage across the filter inductor is $V_{LLC} - V_o$. The current ripple of the filter inductor for the proposed converter is expressed as

$$\Delta i_{Lf} = \frac{V_{\rm in}\left[1 - D - \frac{(1-D)n_1}{2n_2}\right]DT_s}{4n_1L_f}. \tag{16}$$

As seen in both (15) and (16), with the same duty cycle, the current ripple of the proposed converter is less than the conventional TL converter. For the desired output current ripple $\Delta I_{Lf} = 0.5$ A and specifications $n_1 = 4$, $n_2 = 4.5$, $T_s = 10\ \mu$s, $R_o = 2.5\ \Omega$, and $V_o = 50$ V, the output filter inductance as the function of input voltages is shown in Fig. 7. As seen in Fig. 7, compared with the conventional TL converter, the filter

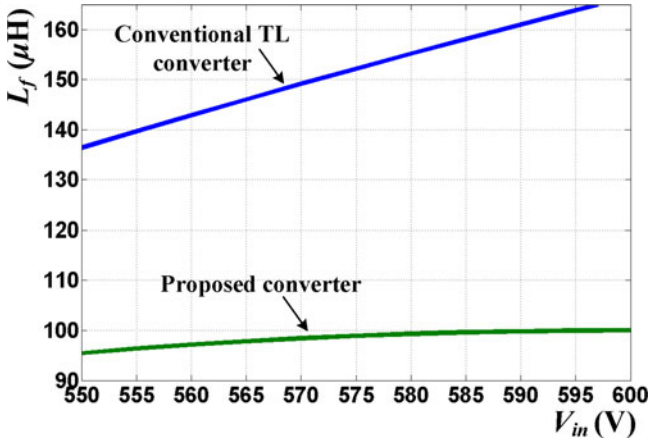

Fig. 7. Filter inductance as the function of input voltage for the desired current ripple.

inductance of the proposed converter is dramatically reduced. Furthermore, the filter size and copper loss of the inductor can be reduced.

E. Current Stress of the Primary Semiconductors

The primary currents of the transformers for the conventional TL converter and proposed converter are shown in Fig. 8(a) and (b). Fig. 8(c) shows the currents of the primary semiconductors. As seen in Fig. 8(a), ignoring the duty cycle loss and output current ripple, the primary winding rms current of the conventional HB TL dc–dc converter $I_{pr1\_c}^{\rm rms}$ can be expressed as

$$I_{pr1\_c}^{\rm rms} \approx \frac{V_o}{n_1 R_o}. \tag{17}$$

Therefore, the rms current of the leading switches Q_1 and Q_4 is approximately evaluated as $I_{pr1\_c}^{\rm rms}\sqrt{\frac{D}{2}} \approx \frac{V_o}{n_1 R_o}\sqrt{n_1 M}$. Furthermore, the rms current of the lagging switches Q_2 and Q_3 is expressed as $I_{pr1\_c}^{\rm rms}/\sqrt{2}$. The current freewheels through the clamping diode and lagging switch during the freewheeling interval. Ignoring the output current ripple and duty cycle loss, the rms current of the primary clamping diodes for conventional TL converter is expressed as

$$i_{D1,D2\_\rm conv}^{\rm rms} = \sqrt{\frac{1}{T_s}\int_{D\frac{T_s}{2}}^{\frac{T_s}{2}} \left(\frac{V_o}{n_1 R_o}\right)^2 dt} = \frac{V_o}{n_1 R_o}\sqrt{\frac{1-D}{2}}$$
$$\approx \frac{V_o}{n_1 R_o}\sqrt{\frac{1}{2} - n_1 M}. \tag{18}$$

As seen in Fig. 8(b) and (c), when the TL transformer transfers power to the output, the current flowing through the leading switch is approximately equal to $\frac{V_o}{n_1 R_o}$. During Stages 5–8, the current flows through the leading switch and clamping diode to charge the capacitor C_{ss}, and the current is approximately equal to $\left(\frac{V_o}{R_o} V_{LLC}\right) \Big/ \frac{V_{\rm in}}{2} = \frac{V_o}{2n_2 R_o}$. Therefore, ignoring the output current ripple and duty cycle loss, the rms current of the leading switches for the proposed converter is approximately evaluated as

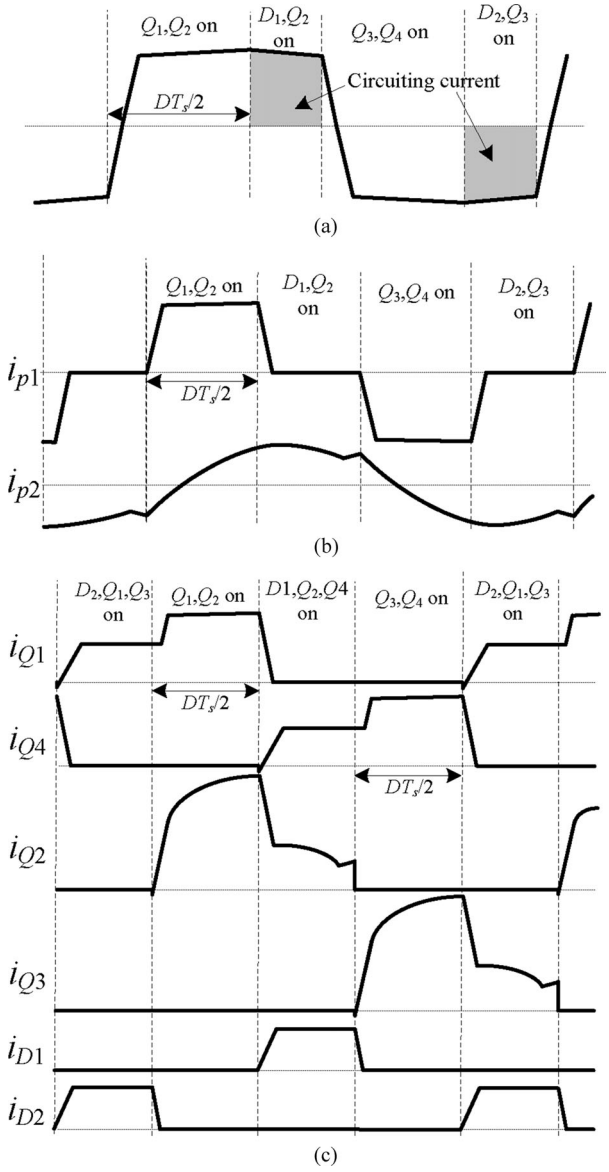

Fig. 8. Primary winding current of the transformers and the currents of the primary semiconductors. (a) Conventional TL converter. (b) Proposed converter. (c) Currents of the primary semiconductors.

$$i_{Q1,Q4}^{\rm rms} = \sqrt{\frac{1}{T_s}\left(\int_0^{D\frac{T_s}{2}} \left(\frac{V_o}{n_1 R_o}\right)^2 dt + \int_{D\frac{T_s}{2}}^{\frac{T_s}{2}} \left(\frac{V_o}{2n_2 R_o}\right)^2 dt\right)}$$
$$= \frac{V_o}{R_o}\sqrt{\frac{1}{8n_2^2} + \left(\frac{1}{2n_1^2} - \frac{1}{8n_2^2}\right) D}$$
$$\approx \frac{V_o}{R_o}\sqrt{\frac{1}{8n_2^2} + \left(\frac{1}{2n_1^2} - \frac{1}{8n_2^2}\right)\frac{4n_1 n_2 M - n_1}{2n_2 - n_1}}. \tag{19}$$

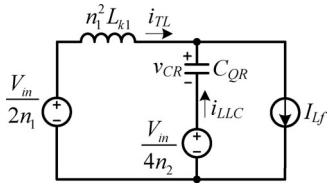

Fig. 9. Equivalent circuit of the secondary side in Stage 4.

The rms current of the clamping diodes is equal to

$$i_{D1,D2}^{\mathrm{rms}} = \sqrt{\frac{1}{T_s}\int_{D\frac{T_s}{2}}^{\frac{T_s}{2}} \left(\frac{V_o}{2n_2R_o}\right)^2 dt} = \frac{V_o}{2n_2R_o}\sqrt{\frac{1-D}{2}}$$
$$\approx \frac{V_o}{2n_2R_o}\sqrt{\frac{1}{2} - \frac{4n_1n_2M - n_1}{2(2n_2 - n_1)}}. \tag{20}$$

In terms of [29], the primary rms current of T_{r2} is expressed as

$$I_{pr2}^{\mathrm{rms}} = \frac{V_{\mathrm{in}}}{32n_2^2R_e}\sqrt{\frac{2n_2^4T_s^2R_e^2}{L_{m2}^2} + 8\pi^2} \tag{21}$$

where $R_e = R_o/(1-D)$. During Stages 3–8, the primary winding current of T_{r2} is expressed as

$$i_{pr2}(t) = \sqrt{2}I_{pr2}^{\mathrm{rms}}\sin\left[2\pi f_r(t-t_2) + \phi\right] \tag{22}$$

where $\phi = -\arcsin\left(\frac{V_{\mathrm{in}}T_s}{16\sqrt{2}L_{m2}I_{pr2}^{\mathrm{rms}}}\right)$. Therefore, the rms current of the lagging switches for the proposed converter is evaluated as

$$i_{Q2,Q3}^{\mathrm{rms}} = \sqrt{\frac{1}{T_s}\left[\int_0^{D\frac{T_s}{2}}\left(\frac{V_o}{n_1R_o} + i_{pr2}(t)\right)^2 dt + \int_{D\frac{T_s}{2}}^{\frac{T_s}{2}}(i_{pr2}(t))^2 dt\right]}$$
$$= \sqrt{\frac{V_o^2D}{2n_1^2R_o^2} - \frac{\sqrt{2}V_oI_{pr2}^{\mathrm{rms}}\left[\cos(\pi D+\phi) - \cos(\phi)\right]}{\pi n_1R_o} + \frac{\left(I_{pr2}^{\mathrm{rms}}\right)^2}{2}}$$
$$\approx \sqrt{\frac{V_o^2(4n_1n_2M - n_1)}{2n_1^2R_o^2(2n_2 - n_1)} - \frac{\sqrt{2}V_oI_{pr2}^{\mathrm{rms}}\left[\cos(\pi D+\phi) - \cos(\phi)\right]}{\pi n_1R_o} + \frac{\left(I_{pr2}^{\mathrm{rms}}\right)^2}{2}}. \tag{23}$$

The rms current of the primary semiconductors is associated with the turns ratio of the transformers. In order to minimize the conduction loss, the turns ratio of the transformer should be optimum designed. The detailed turns ratio design and conduction loss is analyzed in Section IV.

F. Voltage Stress of the Secondary Diodes and Switch

The equivalent circuit of the secondary side in Stage 4 is shown in Fig. 9, where C_R is the junction capacitance of the active switch. Output filter inductor is large enough, so the output filter inductor current is regarded as a current source. The initial state in this stage is $v_{CR}(0) = 0$, $i_{\mathrm{TL}}(0) = I_{Lf}$, and $i_{LLC}(0) = 0$.

$v_{CR}(t)$, $i_{\mathrm{TL}}(t)$, and $i_{LLC}(t)$ are expressed as

$$i_{\mathrm{TL}}(t) = \left(\frac{V_{\mathrm{in}}}{2n_1} - \frac{V_{\mathrm{in}}}{4n_2}\right)\frac{1}{n_1^2L_{k1}\omega_n}\sin(\omega_n(t-t_3)) + I_{Lf}$$
$$i_{LLC}(t) = -\left(\frac{V_{\mathrm{in}}}{2n_1} - \frac{V_{\mathrm{in}}}{4n_2}\right)\frac{1}{n_1^2L_{k1}\omega_n}\sin(\omega_n(t-t_3))$$
$$v_{CR}(t) = \left(\frac{V_{\mathrm{in}}}{2n_1} - \frac{V_{\mathrm{in}}}{4n_2}\right)\left[1 - \cos(\omega_n(t-t_3))\right] \tag{24}$$

where $\omega_n = \frac{1}{\sqrt{n_1^2L_{k1}C_{QR}}}$. Therefore, ignoring the reverse recovery of the body diode, the maximum voltage of the active switch Q_R is equal to $\left(\frac{V_{\mathrm{in}}}{n_1} - \frac{V_{\mathrm{in}}}{2n_2}\right)$. The maximum voltage over the diodes D_{R1} and D_{R2} is expressed as

$$v_{DR1,DR2\_\max} = 2\left(v_{CR\_\max} + V_{LLC}\right) = \frac{2V_{\mathrm{in}}}{n_1} - \frac{V_{\mathrm{in}}}{2n_2}. \tag{25}$$

Moreover, the maximum voltage of the diodes D_{R3} and D_{R4} is equal to $2V_{LLC} = \frac{V_{\mathrm{in}}}{2n_2}$. In terms of (24), in order to reduce the ringing of the output diode, the junction capacitance of the active switch Q_R should be small enough.

For conventional TL dc–dc converter analyzed in the same manner, the maximum voltage at the rectifier output is expressed as $v_{\mathrm{rec\_max}} = \frac{V_{\mathrm{in}}}{n_1}$. Therefore, the maximum voltage of the diodes D_{R1} and D_{R2} for conventional TL converter is equal to $2v_{\mathrm{rec\_max}} = \frac{2V_{\mathrm{in}}}{n_1}$, which is larger than that of the proposed converter.

IV. Design Considerations

This section introduces a design example of the proposed converter with 550–600 V input voltage and 50 V/20 A output. Therefore, the rated load resistance is 2.5 Ω. A switching frequency of 100 kHz is adopted.

A. Turns Ratio of the Two Transformers

In order to design the two transformers, the power ratio of the two transformers should be chosen to the desired value. The power ratio can be designed within a range of $[\eta_{\min}, \eta_{\max}]$. As seen from (12), with the increase of the dc conversion ratio *M*, the power ratio η increases. Therefore, $\eta_{\min}$ is related with the minimum dc conversion ratio $M_{\min}$, and $\eta_{\max}$ is related with the maximum dc conversion ratio $M_{\max}$. They are given as follows:

$$\begin{cases} \eta_{\min} = \dfrac{4n_2M_{\min} - 1}{1 - 2n_1M_{\min}} \\ \eta_{\max} = \dfrac{4n_2M_{\max} - 1}{1 - 2n_1M_{\max}}. \end{cases} \tag{26}$$

Rearranging (26), the turns ratio of the two transformers are written by

$$\begin{cases} n_1 = \dfrac{M_{\min}\eta_{\max} - M_{\max}\eta_{\min} + M_{\min} - M_{\max}}{2M_{\max}M_{\min}\left(\eta_{\max} - \eta_{\min}\right)} \\ n_2 = \dfrac{\left(M_{\max} - M_{\min}\right)\eta_{\max}\eta_{\min} + M_{\max}\eta_{\max} - M_{\min}\eta_{\min}}{4M_{\max}M_{\min}\left(\eta_{\max} - \eta_{\min}\right)}. \end{cases} \tag{27}$$

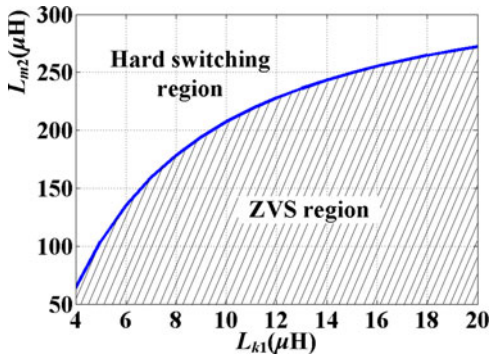

Fig. 10. Magnetizing inductance of T_{r2} versus the leakage inductance of T_{r1}.

According to the specifications shown in this section, the maximum dc conversion ratio is $M_{\max} = \frac{V_o}{V_{\text{in\_min}}} = \frac{50}{550} = 0.0909$, and the minimum dc conversion ratio is $M_{\min} = \frac{V_o}{V_{\text{in\_max}}} = \frac{50}{600} = 0.0833$.

In this paper, the power ratio distribution of the two transformers is desired to be approximately 2. Therefore, the maximum power ratio of the two transformers $\eta_{\max}$ is designed to be 2.33, when the TL transformer supplies 70% load power and the *LLC* transformer supplies 30% load power. The minimum power ratio of the two transformers $\eta_{\min}$ is designed to be 1.5, when the TL transformer supplies 60% load power and the *LLC* transformer supplies 40% load power. Then, the turns ratio of the two transformer obtained from (27) is expressed as (28) shown at the bottom of the page.

Consequently, the turns ratio of the two transformers are chosen as $n_1 = 4$ and $n_2 = 4.5$. At minimum input voltage, the effective duty cycle in light of (7) is 0.51. At the maximum input voltage, the effective duty cycle is 0.4.

B. Magnetizing Inductance of the LLC Transformer

With the specification of $C = 180$ pF, $T_s = 10\,\mu$s and $t_{\text{dead}} = 100$ ns, the magnetizing inductance of T_{r2} versus the leakage inductance L_{k1} in terms of (14) is shown in Fig. 10. As seen, with the increase of L_{k1}, the magnetizing inductance L_{m2} increases. In this case, the magnetizing current of T_{r2} can be reduced, and the circulating current can be reduced. However, larger L_{k1} causes larger duty cycle loss. Therefore, there is a tradeoff between the duty cycle loss and circulating current for the ZVS of the lagging switches.

In this paper, the leakage inductance L_{k1} is chosen as 10 μH. Therefore, the ZVS condition of lagging switches is $L_{m2} \leq 207\ \mu$H. Eventually, the magnetizing inductor L_{m2} is designed as 200 μH in this paper.

C. Current Stress Comparison of the Primary Semiconductors

According to the turns ratio of the transformers and magnetizing inductance of T_{r2} in this section, the rms currents of the switches in per unit as the function of the input voltage in terms of (19) and (23) are shown in Fig. 11. As seen in Fig. 11, the current stress of the proposed converter is much lower than the conventional TL converter. Equation (19) indicates that the rms current of the leading switches is associated with the duty cycle. Fig. 4 shows that the duty cycle of the proposed converter is much lower than that of the conventional TL converter for the same dc conversion ratio. Therefore, the rms current of the leading switches can be reduced dramatically. Fig. 8(a) illustrates the circulating current of the conventional TL converter. During the freewheeling period, the lagging switches have to handle large circulating currents, which causes large conduction loss. Fig. 8(b) illustrates that i_{pr1} is reset to zero when the output inductor works in the freewheeling period, leading to the reduction of the rms current for lagging switches. Moreover, during the freewheeling period, the *LLC* circuit still transfers energy to the output. Only the magnetizing inductor current of T_{r2} freewheels at the primary side. Therefore, the proposed converter works in low conduction loss, achieving high efficiency.

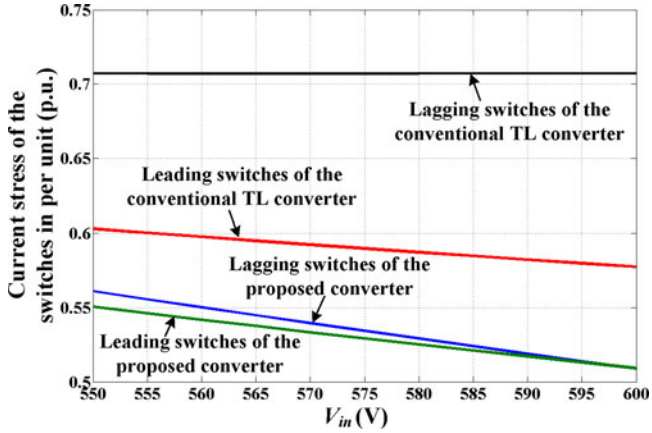

Fig. 11. Rms current of the switches in per unit as the function of the input voltage.

Fig. 12 shows the rms current of the primary clamping diodes in per unit as the function of the input voltage. For the turns ratio of the transformers and the magnetizing inductance of T_{r2} designed in this section, the conduction loss of the clamping diodes is less than the conventional TL converter.

D. Resonant Capacitance C_{r}

The voltage across the resonant capacitor is expressed as

$$v_{Cr1} = \frac{V_{\text{in}}}{4} + \frac{1}{2C_r}\int i_{pr2}(t)dt$$
$$= \frac{V_{\text{in}}}{4} - \frac{\sqrt{2}I_{pr2}^{\text{rms}}}{4\pi f_r C_r}\cos\left[2\pi f_r(t-t_2)+\phi\right]$$

$$\begin{cases} n_1 = \dfrac{0.0833\times 2.33 - 0.0909\times 1.5 + 0.0833 - 0.0909}{2\times 0.0833\times 0.0909\times(2.33-1.5)} = 3.99 \\ n_2 = \dfrac{(0.0909-0.0833)\times 1.5\times 2.33 + 0.0909\times 2.33 - 0.0833\times 1.5}{4\times 0.0833\times 0.0909\times(2.33-1.5)} = 4.51 \end{cases} \tag{28}$$

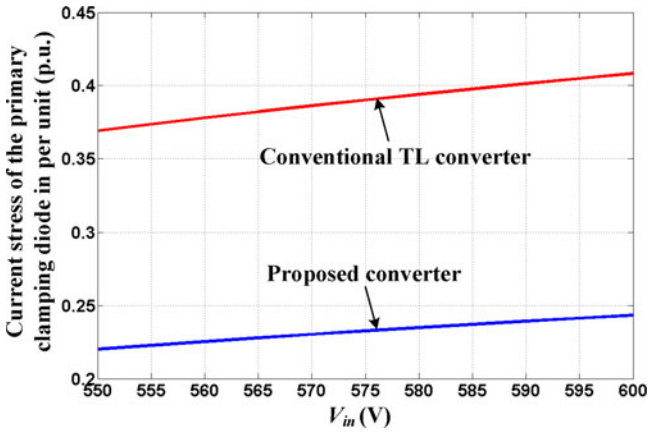

Fig. 12. Rms current of the primary clamping diodes in per unit as the function of the input voltage.

$$v_{Cr2} = \frac{V_{\rm in}}{4} - \frac{1}{2C_r}\int i_{pr2}(t)dt$$
$$= \frac{V_{\rm in}}{4} + \frac{\sqrt{2}I_{pr2}^{\rm rms}}{4\pi f_r C_r}\cos\left[2\pi f_r(t-t_2)+\phi\right]. \quad (29)$$

Therefore, the maximum voltage of the resonant capacitor is expressed as

$$V_{Cr\_\max} = \frac{V_{\rm in}}{4} + \frac{\sqrt{2}I_{pr2}^{\rm rms}}{4\pi f_r C_r}. \quad (30)$$

With the increase of the resonant capacitor, the maximum voltage of the capacitor can be reduced. When $V_{Cr\_\max}$ is desired to be less than 250 V, C_r should be larger than 21 nF. Then, the resonant capacitance C_r is chosen as 30 nF in this paper.

E. Resonant Inductance L_r

The resonant frequency is equal to the switching frequency. Therefore, the resonant inductance L_r is expressed as

$$L_r = \frac{1}{8\pi^2 f_r^2 C_r} = 42.26(\mu\text{H}). \quad (31)$$

Then, L_r is chosen as 43 μH.

F. Selection of the Secondary Semiconductors

According to the analyses in Section III-F, the voltage stress of the D_{R1} and D_{R2} is equal to $\frac{2V_{\rm in\_max}}{n_1} - \frac{V_{\rm in\_max}}{2n_2} = \frac{2\times600}{4} - \frac{600}{2\times4.5} = 233$ (V). The voltage stress of Q_R is equal to $\frac{V_{\rm in\_max}}{n_1} - \frac{V_{\rm in\_max}}{2n_2} = \frac{600}{4} - \frac{600}{2\times4.5} = 83$ (V). The voltage stress of D_{R3} and D_{R4} is equal to $\frac{V_{\rm in\_max}}{4n_2} = \frac{600}{4\times4.5} = 33.5$ (V). The current stress of all the secondary semiconductors can be designed no less than 20 A. In terms of the voltage stress and current stress, the secondary semiconductors can be determined.

V. Experimental Verifications

In order to verify the performance of the proposed converter, a 1-kW prototype is built. The specifications of the prototype are given as follows: $V_{\rm in} = 550 \sim 600$ V, $V_o = 50$ V, $n_1 = 4$, $n_2 = 4.5$, $C_{d1} = C_{d2} = C_{ss} = 20$ μF, $C = 180$ pF, $L_r = 43$ μH, $C_r = 30$ nF, $L_{m2} = 200$ μH, $L_f = 110$ μH, $C_o = 200$ μF, and $C_{os} = 30$ μF. Therefore, the resonant frequency of the *LLC* circuit is 99.1 kHz. The switching frequency is 100 kHz. Two pieces of FQP8N60C in parallel are selected as each primary switch. The primary clamping diode is DSEP12-12A. The active switch is FDP150N10. The rectifiers D_{R1} and D_{R2} are two pieces of MBR20200CT. Two *RC* snubber circuits are parallel connected with D_{R1} and D_{R2}. The snubber circuit is composed of a 400 Ω resistor in series with a 1 nF capacitor. The rectifiers D_{R3} and D_{R4} are DSSK20-015A. The experimental results are shown in Figs. 13–16.

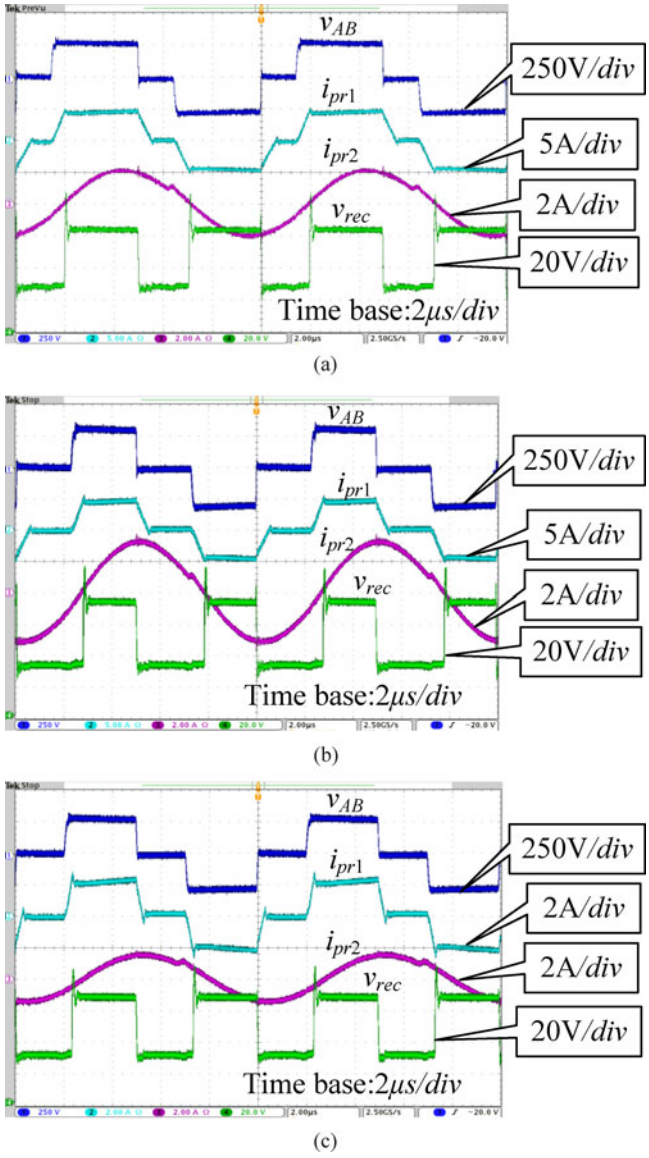

Fig. 13. Measured key waveform of the proposed converter (a) at $V_{\rm in} = 550$ V and $P = 1000$ W, (b) at $V_{\rm in} = 600$ V and $P = 1000$ W, and (c) at $V_{\rm in} = 550$ V and $P = 200$ W.

Fig. 13 shows the key waveforms at different input voltages and output power, where *P* is the output power. Fig. 13(a) shows the experimental waveforms when $V_{\rm in} = 550$ V and

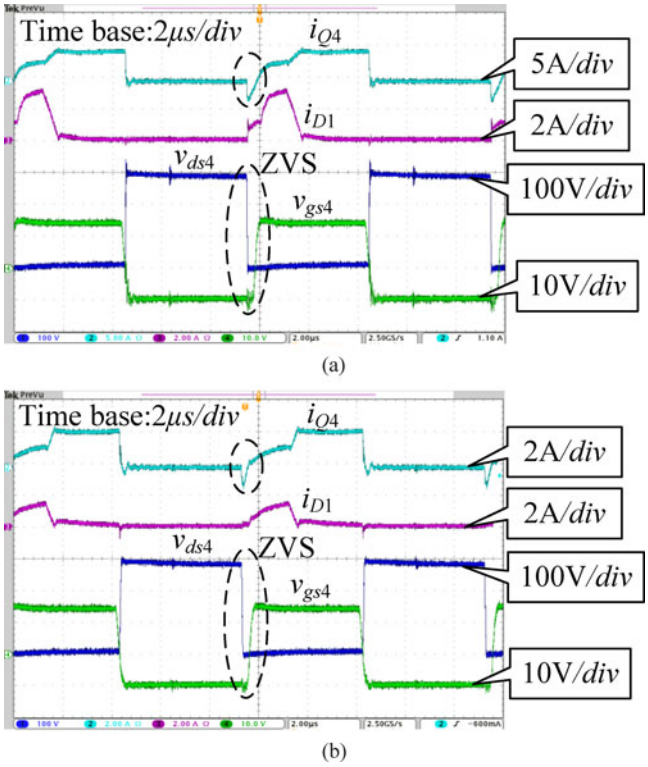

Fig. 14. Current of Q_4, primary current of the clamping diode D_1, and gate signal and drain–source voltage of switch Q_4, (a) at $V_{\rm in} = 550$ V and $P = 1000$ W and (b) at $V_{\rm in} = 550$ V and $P = 200$ W.

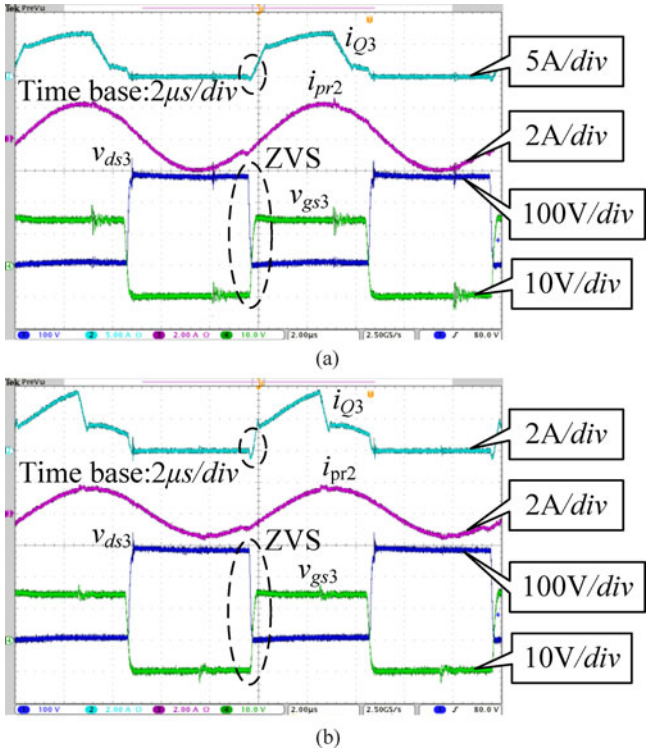

Fig. 15. Current of Q_4, current of T_{r2}, and gate signal and drain–source voltage of switch Q_3 (a) at $V_{\rm in} = 550$ V and $P = 1000$ W and (b) at $V_{\rm in} = 550$ V and $P = 200$ W.

$P = 1000$ W. Fig. 13(b) shows the experimental waveforms when $V_{\rm in} = 600$ V and $P = 1000$ W. With the increase of the input voltage, the duty cycle of the proposed converter decreases, while the amplitude of i_{pr2} increases. It demonstrates that the *LLC* circuit transfers more power to the load as the input voltage increases. Fig. 13(c) shows the experimental waveforms when $V_{in} = 550$ V and $P = 200$ W. The current amplitudes of i_{pr1} and i_{pr2} are both reduced as the output power decreases. As expected, the currents i_{pr1} for the three cases mentioned previously are all reset to zero during the freewheeling period, which minimizes the conduction loss of the primary circuit.

Fig. 14 shows current of Q_4, current of the clamping diode D_1, and gate signal and drain–source voltage of switch Q_4. Fig. 14(a) shows the ZVS operation of the leading switches at heavy loads. Fig. 14(b) shows the ZVS operation of the leading switches at light loads. Before Q_4 is turned ON, the current of Q_4 is negative and the current flows through its body diode. Fig. 15 shows current of Q_3, primary current of T_{r2}, and gate signal and drain–source voltage of switch Q_3. Fig. 15(a) shows the ZVS operation of the lagging switches at the heavy load. Fig. 15(b) highlights the ZVS operation of the lagging switches at the light load. As seen in the experimental results, before Q_3 is turned ON, the current of Q_3 is negative and the current flows through its body diode. Therefore, ZVS for all the switches is achieved over the wide load range. Fig. 16 highlights the ZVS operation of active switch Q_R.

The measured efficiency curves for the proposed converter, the conventional TL converter, and the proposed converter replacing the active switch to a diode are shown in Fig. 17.

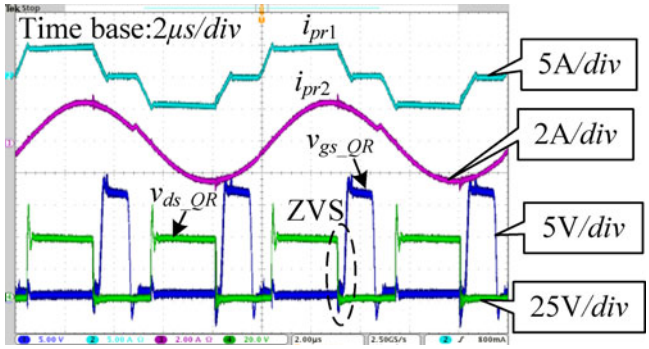

Fig. 16. Gate signal and drain–source voltage of Q_R at $V_{\rm in} = 550$ V and $P = 1000$ W.

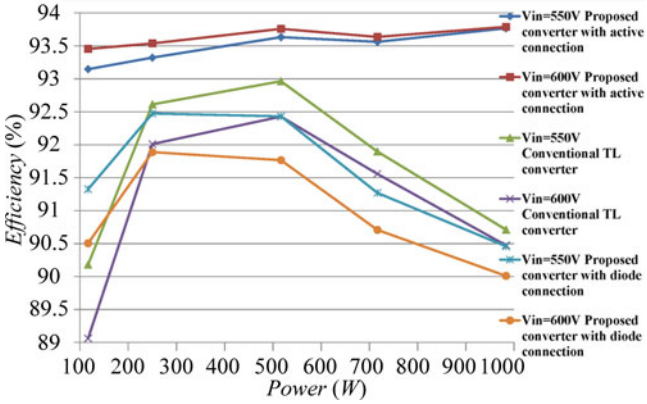

Fig. 17. Efficiency for the proposed converter, the conventional TL converter, and the proposed converter replacing the active switch to a diode.

Compared with the conventional TL converter, the efficiency of the proposed converter is greatly improved. At $V_{\rm in} = 600\ V$, the maximum improvement at light loads is more than 3.5%, and the improvement at heavy loads is more than 3%. For the proposed converter replacing the active switch to a diode, the efficiency is not effectively improved. Although the ZVS of the switches is achieved and circulating current is reduced at the primary side, the replaced diode causes large conduction loss especially at heavy loads. As the input voltage increases, more power is transferred to the load from the *LLC* circuit. More conduction loss is generated by using the replaced diode. Therefore, when the input voltage increases, the efficiency of the proposed converter with the replaced diode decreases.

VI. Conclusion

In this paper, a hybrid TL and *LLC* converter by sharing the lagging switches is proposed for higher efficiency. Since the switches only withstand half of the input voltage, the proposed converter is suitable for high input voltage applications. The *LLC* circuit can extend the ZVS range of the lagging switches. The output current ripple and circulating current of the primary side are reduced. Connecting the hybrid TL output and *LLC* by the proposed active switch based on the proposed switching sequence can significantly increase the conversion efficiency further during the wide load range. The good performance of the proposed converter and design method has been verified by a 1-kW experimental prototype.

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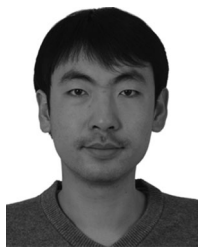

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