Letters

High-Mobility Stable 1200-V, 150-A 4H-SiC DMOSFET Long-Term Reliability Analysis Under High Current Density Transient Conditions

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***Abstract*—For SiC DMOSFETs to obtain widespread usage in power electronics their long-term operational ability to handle the stressful transient current and high temperatures common in power electronics needs to be further verified. To determine the long-term reliability of a single 4H-SiC DMOSFET, the effects of extreme high current density were evaluated. The 4H-SiC DMOSFET has an active conducting area of 40 mm^2, and is rated for 1200 V and 150 A. The device was electrically stressed by hard-switching transient currents in excess of four times the given rating (>600 A) corresponding to a current density of 1500 A/cm^2. Periodically throughout testing, several device characteristics including $R_{DS(on)}$ and $V_{GS(th)}$ were measured. After 500 000 switching cycles, the device showed a 6.77% decrease in $R_{DS(on)}$, and only a 132-mV decreased in $V_{GS(th)}$. Additionally, the dc characteristics of the device were analyzed from 25 to 150 °C and revealed a 200-mV increase in on-state voltage drop at 20 A and a 2-V reduction in $V_{GS(th)}$ at 150 °C. These results show this SiC DMOSFET has robust long-term reliability in high-power applications that are susceptible to pulse over currents, such as pulsed power modulators and hard-switched power electronics.**

***Index Terms*—DMOSFET, high current density, reliability testing, 4H-SiC.**

I. Introduction

4H-SiC DMOSFETs are a leading option for specialized high energy density power electronics because of 4H-SiC's characteristic wide bandgap, superior thermal conductivity, high critical electric field yielding low specific-on resistance, and high saturation electron drift velocity [1]–[7]. SiC DMOSFETs rated for 1200-V and 33-A continuous are commercially available [8] and research grade SiC DMOSFETs have been fabricated that are capable of 180-A continuous at 1200 V [9]. Additionally, high voltage variants have been fabricated that are capable of switching 10 kV with an $R_{DS(on)}$ of 123 mΩ [10]. However, for SiC DMOSFETs to expand out of specialized systems and obtain widespread usage in power electronics, their long-term reliability under high-stress transient currents and high temperatures that are common in many power electronic applications needs to be further verified through testing and modeling [3], [9], [11]–[18].

In this letter, the effects of the extreme high current density on the long-term operational reliability of a single research grade 4H-SiC DMOSFET made by Cree, Inc., are reported. The 4H-SiC DMOSFET has an active conducting area of 40 mm^2, and is rated for a blocking voltage of 1200 V and a continuous forward current of 150 A. The DMOSFET was hard switched 500 000 times in a *RLC* ring-down test bed at current densities in excess of 1500 A/cm^2 at peak currents in excess of 600 A. The first 16 000 switching events were used to characterize the performance of the device across temperature; with 1000 switching cycles performed at 1, 2, 5, and 10 Hz at each temperature of 25, 50, 100, and 150 °C. The remaining 484 000 switching cycles were performed at 2 Hz and 25 °C. After the 500 000 shots were completed, the device's $R_{DS(on)}$ had burned in to 6.77% below the initial level, the $V_{GS(th)}$ had decreased by only 132 mV below the initial level of 4.825 V, and the B_{VDSS} remained unchanged. Furthermore, the device's electrical characteristics were measured at 25, 50, 100, and 150 °C and were found to be within acceptable limits that would not significantly alter the performance of the device or require compensation in the gate drive circuit. These results show that this SiC DMOSFET will have robust long-term reliability in common power electronic applications susceptible to dc bus shoot through, or specialized applications that require repetitive exposure to the high short-circuit current such as capacitor chargers, spark gap triggers, and plasma igniters.

II. Device Structure and Fabrication

The Cree 4H-SiC DMOSFET has a chip size of 56 mm^2 and an active conducting area of 40 mm^2 [19]. Specific information about the device's fabrication can be found elsewhere [19], [20]. The device is packaged in a high-power three-terminal package that includes a Kelvin measurement pin. Fig. 1 shows a simplified cross-sectional diagram of a unit cell of the DMOSFET structure [19].

III. Test Setup and Procedure

To generate the 1500-A/cm^2 current pulse, an *RLC* pulse-ring-down test bed was utilized [9], [17]. The RLC pulse-ring-down

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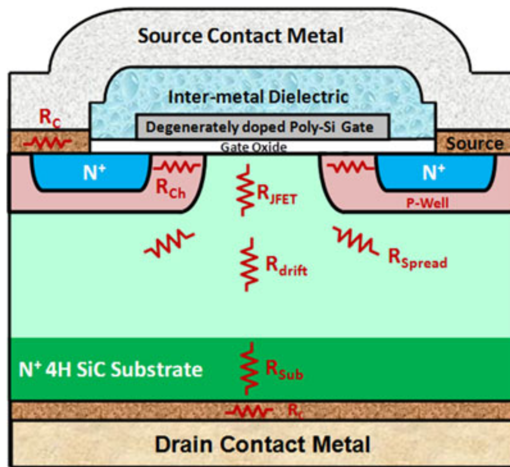

Fig. 1. Cross-sectional diagram of a unit cell of the 4H-SiC DMOSFET [19].

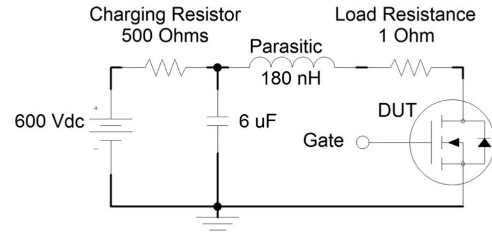

Fig. 2. Schematic of RLC pulse-ring-down test bed used to provide transient switching conditions for the DUT.

test bed was designed to generate transient current waveforms common in power electronic systems such as dc bus shoot-through, capacitive loads, and short-circuit conditions. The charging resistor and load resistance were chosen to meet the pulse repetition rate and peak current of 10 Hz and 600 A. In the RLC circuit, the capacitors are charged to the desired switching voltage by an external high-voltage power supply. The initial energy stored in the capacitors was discharged through the load resistance and DMOSFET under test to the ground, when the DMOSFET under test was switched ON. A peak *di*/*dt* of 618 A/μs was achieved by minimizing the parasitic inductance of the test bed to 180 nH using a radially symmetric physical layout where multiple capacitors are set in parallel along an outer ring, with multiple load resistors in parallel connecting the outer ring to the device under test. This configuration minimized inductance by overlapping opposing current-carrying paths within the test bed [21]. An equivalent resistance of 1 Ω was used for the load to limit the peak current through the DMOSFET under test to the desired value of 600 A. Specifically, this resulting amplitude and shape of the current can occur during shoot-through of a half bridge if there is a gate driver malfunction or a high drain–source *dV*/*dt* transient. In the shoot-through scenarios, both devices would have low $R_{\mathrm{DS(on)}}$, and an equivalent resistance of 1 Ω could exist between the dc bus and ground. In all of the scenarios modeled by the *RLC* pulse-ring-down test bed previously stated, there is a fast *L*/*R* rise in the current followed by an RC_{Bus} decay; where the current rise time and peak current are limited by the parasitic inductance and resistance of the system's path to ground. To enable switching of the DMOSFET at elevated temperatures, a heating element consisting of two power resistors was bolted directly to the DMOSFET's package. A high current power supply was then utilized to heat the resistors, and the temperature of the DMOSFET was measured with a thermocouple bolted to the device's package. A schematic of the test bed is shown in Fig. 2.

The Cree power 4H-SiC DMOSFET's long-term ability to handle stressful high current density transients was evaluated through a process of measuring the device's electrical characteristics, subjecting the device to hard-switching current pulses, and then, remeasuring the device's electrical characteristics. The device's electrical characteristics were determined by measurement with an Agilent B1505A high-power device analyzer. The voltage and current transient switching waveforms were captured using a Tektronix MSO4054 oscilloscope. The drain–source voltage and gate–source voltage were measured using Tektronix P5200 differential voltage probes. The drain–source current was measured with a Power Electronic Measurements CWT 6B ultramini Rogowski current transducer. The gate–source current was measured via the voltage drop across a current sense resistor with a Tektronix P5200 differential voltage. From these waveforms, the peak power, energy dissipated during each switching cycle, and the energy required to charge the gate were calculated in Origin 8. The interval between testing with the device analyzer was increased semilogarithmically with the number of switching cycles performed. To clearly capture initial degradation and provide useful thermal performance data, the device was characterized every 500 switching cycles for the first 16 000. This provided clear resolution of the initial changes in device characteristics that occurred over the first 16 000 switching cycles. After the initial burn in, the device was characterized every 5000 cycles until a total of 60 000 cycles were completed. The device was then characterized every 10 000 pulses performed at 2 Hz and 25 °C until the total number of pulses had reach 500 000. Table I summarizes the tests performed. Characterization of the device every 5000 cycles allowed for the gradual changes post initial burn in to be captured. Finally, a characterization interval of 10 000 was chosen to capture long-term changes in the device's performance and characteristic warning signs of the potential stress-induced device failure. The frequencies and temperatures utilized simulated intermittent short circuits over a temperature range of four discrete points commonly encountered in pulsed power and power electronic systems. The DMOSFET's electrical characteristics were also measured on the high-power device analyzer after cycle 16 000, at 25, 50, 100, and 150 °C. Output characteristics, drain–source breakdown voltage, and transconductance were measured between each pulse current switching set, and at each of the temperatures previously stated. The threshold voltage was taken from the transconductance plot.

The gate of the DUT was driven with a function generator through a Fairchild FOD3182 optocoupler isolated push–pull high speed MOSFET gate driver to provide protection for the function generator in the event of gate oxide failure in the DUT.

TABLE I
OVERVIEW OF TESTS PERFORMED

Hard Switches	Characterization Interval	Frequency (Hz)	Temp. (°C)	Voltage (V)	Approx. Peak Current (A)
16 000	500	1, 2, 5, 10	25, 50, 100, 150	600	600
44 000	5 000	2	25	600	600
440 000	10 000	2	25	600	600
Total: 500 000					

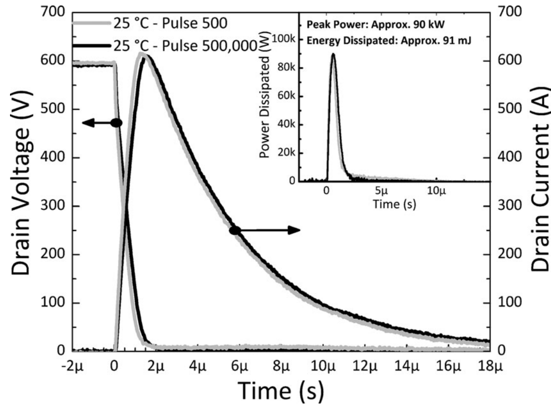

Fig. 3. Two drain–source transient current switching waveforms of the DMOSFET in the pulse-ring-down test bed. The subplot displays the power dissipated during both switching cycles.

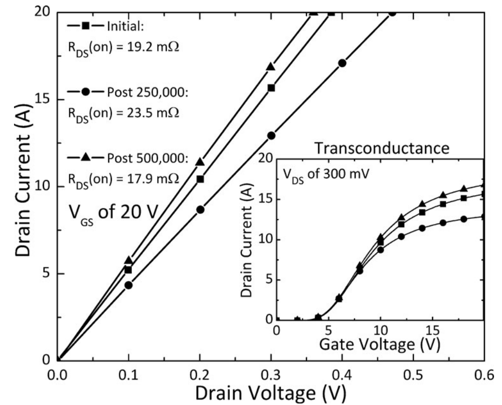

Fig. 4. Comparison of the device's output characteristics and transconductance as a function of pulse number.

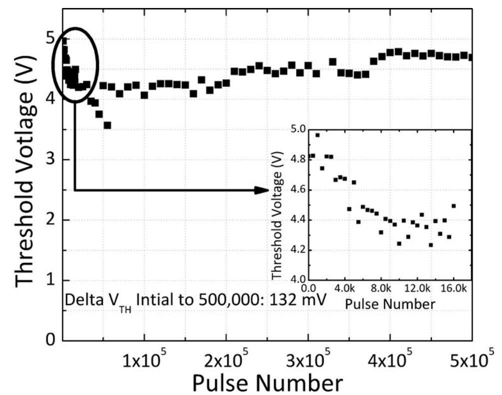

Fig. 5. Threshold voltage measured throughout the testing period. The lack of significant degradation demonstrates long-term stability.

The gate was driven from −5 to + 25 V to minimize on-state losses and minimize the leakage current during the "OFF" interval. Integration of the gate current waveform revealed that a total gate charge of 695 nC was required to charge the gate from -5 to $+ 25\ V_{\mathrm{GS}}$.

IV. RESULTS AND DISCUSSION

Using the previously described test setup and procedure, the DMOSFET's transient current switching waveforms were captured and plotted. Fig. 3 shows the 500th switching waveform performed at 1 Hz and 25 °C (gray curve), plotted with the 500 000th switching waveform performed at 2 Hz and 25 °C (black curve). The peak power and energy dissipated during switching cycle 500 was 88.83 kW and 91 mJ. The peak power and energy dissipated for switching cycle 500 000 was 90.12 kW and 91.2 mJ. Comparison of the switching waveforms' shape, peak power, and energy dissipation reveals that the SiC DMOSFET's switching characteristics did not significantly change. The lack of significant degradation over the course of 500 000 high current density pulses demonstrates that the device would be ideal for rugged applications, where intermittent heavy loads or faults exist. Examples include systems with transient short-circuit conditions such as high-power half bridges, dc–dc converters, or pulsed power applications. This result verifies that the device would robustly handle daily intermittent short circuits for years without needing to be removed from the field.

The device's output characteristics and transconductance measured initially, post 250 000 switching cycles, and post 500 000 switching cycles are plotted in Fig. 4. Fig. 5 shows the threshold voltage measured over the entire testing period. The changes to the device's characteristics measured between switching cycles were permanent. The device's characteristics were stable at the measured values over extended periods of time, revealing that the changes were not due to movement of short-term mobile charges at the gate oxide. The device's $R_{\mathrm{DS(on)}}$ started at 19.2 mΩ, increased to 23.5 mΩ over 250 000 switching cycles, and then, decreased to 17.9 mΩ. The threshold voltage displayed minimal instability, with an overall decrease of only 132 mV after 500 000 switching cycles. A comparison of the plots of $V_{\mathrm{GS(th)}}$ and $R_{\mathrm{DS(on)}}$ shows that the changing $V_{\mathrm{GS(th)}}$, due to changes in the 4H-SiC/SiO_2 interface trap density [22], did not alter the $R_{\mathrm{DS(on)}}$ as significantly as changes

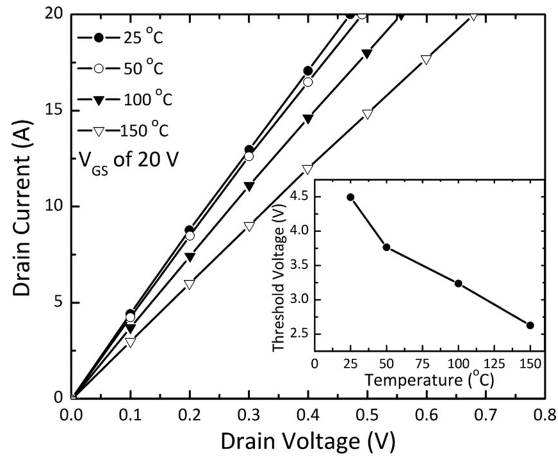

Fig. 6. Output characteristics and threshold voltage plotted as a function of temperature.

in inversion layer carrier mobility. After cycle number 250 000, the $V_{\mathrm{GS(th)}}$ had decreased, but the $R_{\mathrm{DS(on)}}$ had increased. This result reveals that the dominate factor causing slight changes in $R_{\mathrm{DS(on)}}$ of this device in high current density transient conditions is electron mobility in the inversion layer. However, these results show that this SiC DMOSFET maintained acceptably stable forward characteristics with no overall degradation to $R_{\mathrm{DS(on)}}$ over the testing period. These measurements demonstrate that the device's electrical characteristics maintained long-term operational reliability during high current density transient conditions.

The temperature dependence on the 4H-SiC device's output characteristics and threshold voltage is shown in Fig. 6. These measurements were taken after the initial 16 000 switching cycles. The temperature results verify previous simulation and experimental work investigating the temperature dependence of threshold voltage and channel mobility in 4H-SiC [23], and further demonstrate the electrical characteristic stability of this 150-A device. The reduction in threshold voltage occurs at elevated temperature due to the reduction in the number of filled traps at the SiO_2/4H-SiC interface [23]. Although the threshold voltage of this device decreased by approximately 50%, the threshold voltage remained high enough at 150 °C to maintain adequate noise immunity in applications with common push–pull gate drive circuits. These results show that the implementation of this device in high-temperature applications would not require significant customization of the gate drive circuit.

V. Conclusion

A Cree 4H-SiC DMOSFET rated for a blocking voltage of 1200 V and a forward current of 150 A was stress tested to determine its operational long-term reliability. The device was hard-switched 500 000 times with high density transient currents in excess of four times the device's rating. The first 16 000 switching cycles were performed in a temperature range of 25–150 °C and used to characterize the device performance over temperature. The device showed no overall increase in $R_{\mathrm{DS(on)}}$, minimal changes to threshold voltage, and no degradation to breakdown voltage as a result of repetitive pulsed over currents. The switching results and high-temperature characteristics gathered demonstrated the DMOSFET's long-term robust ability to handle the transient over currents and high temperatures that are commonly experienced in power electronic applications. In addition, the results gathered show that the gate drive circuit does not require temperature compensation when operated at up to 150 °C. Future work to be performed on additional Cree 4H-SiC DMOSFETs will include characterization on an in-house built 500-A high current curve tracer, failure mode analysis, and implementation in pulsed power, half bridge, and dc–dc converters for high-temperature applications.

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