Design of a 300-W Isolated Power Supply for Ultrafast Tracking Converters

Khiem Nguyen-Duy, *Student Member, IEEE*, Ziwei Ouyang, *Member, IEEE*, Lars Press Petersen, *Member, IEEE*, Arnold Knott, *Member, IEEE*, Ole C. Thomsen, *Member, IEEE*, and Michael A. E. Andersen, *Member, IEEE*

***Abstract*—This paper presents the design of a medium-power-rating isolated power supply for ultrafast tracking converters and MOS-gate driver circuits in medium- and high-voltage applications. The key feature of the design is its very low circuit input-to-output parasitic capacitance, which maximizes its immunity from noise due to fast changes in voltage. The converter is a voltage-controlled current source, utilizing a transformer with extremely low interwinding parasitic capacitance, which is achieved by separating the windings by a significant distance. Experimental measurements show that an overall circuit input-to-output parasitic capacitance of 10 pF in a 300-W prototype can be achieved. The circuit input-to-output capacitance per watt is therefore 30 times lower than that of existing approaches. A mathematical model of the interwinding capacitance of the proposed transformer, circuit analysis, and experimental results are provided to prove the feasibility of the converter.**

***Index Terms*—Current transformers, dc–dc power converters, parasitic capacitance, stacking, switching converters.**

I. Introduction

COMMON mode (CM) noise is a typical problem in most switching power electronics converters and is well known to cause various adverse effects. Among them are electromagnetic interference, false measurements, and unexpected triggering of sensitive control electronics. In particular, the problem becomes more severe where modular stacking of converters is used to increase the total power rating, as the total CM noise may add up, change the output impedance, or resonate in different coupling paths [1], [2]. As a result, many studies have been dedicated to mitigate CM noise generated by power electronics converters [1]–[5].

CM noise occurs due to different sources and coupling through different paths. Among them, CM noise current exists when there are switching nodes with stiff changes of voltage over time (high *dv/dt*), and when there are capacitive coupling paths. Unfortunately, high *dv/dt* switching nodes are inherent in most switching converters and are unavoidable. Due to the use of more advanced power switches capable of switching at higher frequency for a higher efficiency, CM noise has become more notable. As a result, one of the common approaches to reduce effects of CM noise current is to improve the capacitive coupling paths.

In [4] and [5], a method called current balancing technique is proposed to cancel the CM noise for several nonisolated converters. For example, in [4], analysis is performed on the boost converter, where different equivalent circuits for CM sources are drawn, and the major main noise source is identified. After that, circuit modification, mainly with the insertion of an extra capacitor and splitting of the main inductor are suggested, so that the resulting generated CM currents cancel out the original CM current on the line impedance stabilization network [6].

In most galvanic isolated converter topologies that utilize a transformer, the CM noise couples through the interwinding parasitic capacitance of the transformer. Their coupling paths may also include the parasitic capacitances from the converter chassis to ground, or from the drain of the converter switches to heat sink and from heat sink to ground. If a proper design is achieved to minimize most of these parasitic capacitances due to circuit structure, the element that predominantly contributes to the circuit total input-to-output parasitic capacitance is the transformer [1]–[5]. Therefore, many studies have focused on mitigating CM noise by minimizing the interwinding capacitance of the transformer [1], [2], [7]–[9], compensating the noise generated by the converters [8], [10], or inserting line filters [11]. The existing transformers in medium-power converters (up to 1.2 kW) have their interwinding capacitance in the range of several tens of picofarads for low-output power converters to hundreds of nanofarads for higher power ratings. For example, the existing transformer in a 1.2-kW converter is reported to have 1.5-nF interwinding capacitance [12]. An E-core transformer used in a flyback converter with a power rating of 30 W is reported to have 34 pF of interwinding capacitance [13]. The interwinding capacitance per unit output power is approximately 1 pF/W. The question, however, is how to further minimize the interwinding capacitance of the transformer in order to reduce the effect of the CM noise.

In [1], a novel converter topology supplying energy to MOS-gate driver circuits [e.g., MOSFETs, insulated-gate bipolar transistor (IGBT)s or MOS-controlled thyristor (MCT)s] is proposed that possesses a very low circuit input-to-output parasitic capacitance. The topology is redrawn in Fig. 1. In that topology, a unique structured ring core current transformer is used, where the primary winding is placed in the center of the ring,

Manuscript received February 17, 2014; revised May 26, 2014; accepted June 26, 2014. Date of publication July 11, 2014; date of current version January 16, 2015. Recommended for publication by Associate Editor G. Moschopoulos.

K. Nguyen-Duy, Z. Ouyang, L. P. Petersen, A. Knott, and M. A. E. Andersen are with the Department of Electrical Engineering, Technical University of Denmark, 2800 Kgs. Lyngby, Denmark (e-mail: knduy@elektro.dtu.dk; zo@elektro.dtu.dk; lpet@elektro.dtu.dk; akn@elektro.dtu.dk; ma@elektro.dtu.dk).

O. C. Thomsen, retired, was with the Department of Electrical Engineering, Technical University of Denmark, 2800 Kgs. Lyngby, Denmark (e-mail: oct@elektro.dtu.dk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2014.2338834

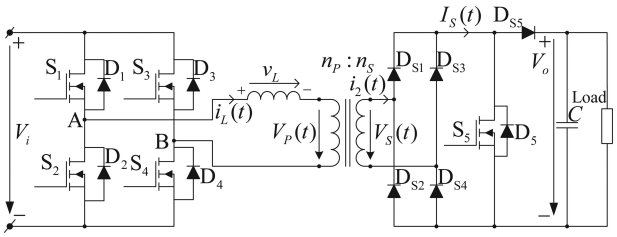

Fig. 1. Topology of the proposed converter.

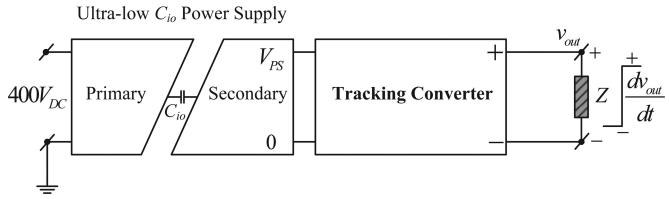

Fig. 2. Example of the proposed ultralow circuit input-to-output capacitance power supply connected with an ultrafast tracking converter.

TABLE I
DESIGN SPECIFICATION

Input voltage	400 V
Output voltage	60 V
Output current	5 A
Maximum output power	300 W
Circuit input-to-output capacitance	10 pF

displacing with the secondary winding a distance equal to the radius of the core. With this special structure, the distance between windings is maximized; therefore, the parasitic capacitance between them is minimized. An R25/10 toroid ferrite core with one primary winding and a 30-turn secondary winding was claimed to achieve as low as 1 pF of parasitic capacitance. The application is primarily to supply energy to MOS-gate driver circuits. Particularly, the purpose is to drive 15 gate driver circuits, with a full output voltage of 36 V and a current supply per channel of 0.2 A. Following this proposal, similar ideas of using the ring core transformer with that unique winding structure have been reported [3], [14]. In [3], the ring core transformer is used as a current loop to provide isolation and energy to supply gate drivers of power switches in medium-voltage applications of up to 16 kV dc. Specifically, 12 channels are stacked in parallel to provide output voltage adaptation for the IGBT driver boards. The power rating is 75 W per channel.

Despite being very promising, works in [1], [3], and [14] lack supporting experimental results from the ideas proposed. As a result, further work should be carried out to verify the ideas and improve the work. First, a detailed analysis and calculation on the transformer design are greatly desired, of which the results should indicate how to further improve the transformer in terms of minimizing the interwinding capacitance. Second, the power rating of the converter, which was 36 V and 0.2 A per channel as in [1], can be increased if applications require. Third, the work can be improved with elaborate circuit operation analysis and control together with presentation of supporting experimental data. Finally, it would be much appreciated if proper assessments of advantages as well as disadvantages of the converter were made.

This paper seeks to further investigate and validate the merit of the converter shown in Fig. 1. A higher output power rating is desired (300 W per module). The prototype is designed in a way that minimizes the circuit input-to-output parasitic capacitance, making it less susceptible to high *dv/dt* noise and therefore suitable for modular stacking. The paper is divided into the following sections. The first section is the introduction. Section II provides information on the system specification. Following that, Section III presents the targeted applications and selection of a suitable topology. Next, the CM noise current paths are briefly discussed in Section IV. Afterward, Section V discusses the design and specification of the proposed toroidal transformer. Mathematical expressions of the transformer interwinding capacitance are derived based on the method of stored energy balancing. The results indicate how to further improve the design in terms of minimizing the interwinding capacitance. Following that, Section VI discusses the circuit operation and control approach in detail. Section VII presents and examines the experimental results. Section VIII is dedicated to an overall discussion, where the advantages as well as disadvantages of the proposed converter are assessed. Finally, Section IX summarizes the contributions. The experimental results show that an overall circuit input-to-output parasitic capacitance of 10 pF is achieved. To the authors' best knowledge, this is the lowest circuit input-to-output parasitic capacitance achieved among similar devices with similar power ratings. It is also experimentally verified that the main contributor to the overall circuit input-to-output parasitic capacitance is the interwinding capacitance of the transformer.

II. SYSTEM DESCRIPTION

Referring to the converter in Fig. 1, the input dc supply voltage of the converter is usually the output of a power factor correction converter which converts a single phase 220-V ac voltage into 400-V dc voltage. Therefore, a dc input of 400 V is chosen in the design. The output voltage is chosen to be 60 V dc, since it allows a variety of power switch selections which have a breakdown voltage of 100 V. If, for example, higher output voltage is desired, then either design specification can be changed or multiple converter modules can be stacked in series. The output current is designed to be 5 A average value at its maximum. This specification implies that the maximum output power that is available in the output terminals is 300 W. Furthermore, an extremely low total circuit input-to-output parasitic capacitance of 10 pF is sought. All of these specifications are stated in Table I.

III. TARGETED APPLICATIONS AND SELECTION OF TOPOLOGIES

A. Targeted Applications

One of the primary applications of this study is supplying energy for ultrafast tracking converters. Fig. 2 shows a configuration in which a module of the proposed power supply provides

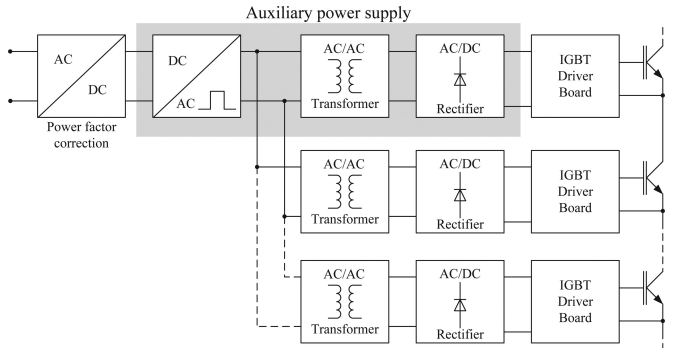

Fig. 3. Auxiliary power supply for MOS-gate driver circuits in medium- and high-voltage application [15].

energy to a module of an ultrafast tracking converter. An ultrafast tracking converter is typical of radio frequency power amplifiers used in communication system based stations [16]–[18]. The output voltage of such an ultrafast tracking converter can be required to have a step response settled within 10 μs. Due to the high *dv/dt* at the output of the tracking converters, there will be a large amount of conductive CM current drawn from their output. This current is linearly proportional to the input–output capacitance of the power supply

$$i_{\rm com} = C_{io}\frac{dv_{\rm out}}{dt}. \tag{1}$$

However, the ripple voltage requirement of the output of the tracking converter is usually in the range of tens of millivolts peak to peak; for example, 10 mV as in [16] and [17]. The performance of the tracking converter can be degraded if a reasonable amount of conductive current is drawn from the output through the circuit input-to-output capacitance. The adverse effects become worse if there are more than one converter stacked together to increase the power rating. Therefore, in order to have high immunity to the fast voltage step response, the circuit input-to-output parasitic capacitance must be minimized, especially in the modular stacking applications.

Another important application of this study is to power the gate-drive circuits of medium- and high-voltage applications. Existing approaches can be found in [3], [15], and [19]. The medium- and high-voltage applications are defined as applications with operating voltage in the range of tens of kilovolts. For example, a high-speed IGBT switch which acts as a circuit breaker for the operating voltage of 16 kV dc and a permanent load current of 10 A dc is demonstrated [15]. This is performed by connecting in series a total of 18 IGBTs, each with a reverse voltage of 2500 V. Each IGBT has its own attached gate drive circuit, all of which were driven by a single auxiliary power supply unit. The block diagram of this system is redrawn and shown in Fig. 3. According to [15], the following features of the auxiliary power supply unit that generates the control power required to activate the high-power IGBT switches are required:

1) Insulation between individual stages and with respect to earth potential.
2) A small coupling capacitance in order to achieve a high level of noise immunity between the individual stages.

In [3], [15], and [19], it is shown that the auxiliary power supply should be implemented in the form of a current loop shared by all switch stages. The current loop provides power to a gate drive circuit by using a ring core transformer. This results in a solution with low coupling capacitance and compact construction volume [15].

A small coupling capacitance of the power supply circuit can make the converter highly immune to high *dv/dt* and thus increase reliability in such applications. The main focus of this paper is to develop a converter that has minimized circuit input-to-output capacitance for applications that require high immunity to a large change of output voltage over time.

B. Effect of Isolated Feedback to the Circuit Performance

In consideration of feedback control applied to isolated power converters, it is very common to feedback signals from one side of the circuit to the other side across the isolation boundary. The feedback elements must provide electrical isolation to the control feedback paths; at the same time, they must be able to transfer information as quickly and accurately as possible. Examples of such elements are optocouplers and signal-level isolation transformers. However, these components possess several undesirable attributes that need to be taken into account.

For the optocoupler, there are two main disadvantages. First, they have very low bandwidth and limited accuracy that lower the converter's overall bandwidth and might inhibit fault protection of the circuit. This is due to the fact that the optocoupler must have large based region in order to be sensitive to light and have very thick based region in order to minimize the losses in radiant energy transfer, which implies a relatively large Miller capacitance in the range of nanofarads [20]. This large capacitance effectively reduces the bandwidth of the optocoupler. The typical value of the bandwidth of a commercially available optocoupler used in power supplies is less than 5 kHz [20].

Second, the input–output coupling capacitance inherent in an optocoupler will add to the overall circuit input-to-output parasitic capacitance. Therefore, an optocoupler is not a suitable candidate for the targeted applications. Signal-level isolation transformers have better bandwidth than the optocoupler, but they have higher coupling capacitance. The typical coupling capacitance of a signal-level transformer is from 2 pF [21] to 12 pF [22], which will add 20% and 120% to the total circuit input-to-output capacitance, respectively. Hence, the use of an isolation transformer in feedback is not acceptable in such applications.

In summary, the control approach which uses feedback paths across the isolation boundary is not optimal where minimization of circuit input-to-output parasitic capacitance is the primary goal. Next, the selection of a suitable topology will be discussed.

C. Topology Selection

Based on the targeted applications and the awareness of the effect of isolated feedback on the circuit performance, a power supply suitable for these applications must possess the following features:

1) Low circuit input–output capacitance.
2) Reduced number of crossings of the isolation barrier.

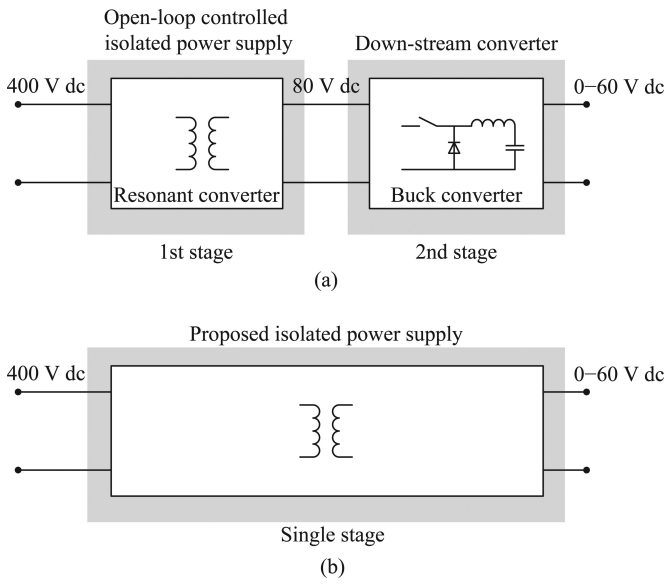

Fig. 4. Minimized circuit input–output capacitance systems: a) Two-stage solution with existing topologies, b) one-stage solution with the proposed topology.

The first requirement implies a loosely coupled transformer to be used. However, one property of the magnetic component to be noted is that the leakage inductance and the interwinding parasitic capacitance are inversely proportional to each other [23]. Taking this into account, it can be concluded that conventional full-bridge converters such as buck- or boost-derived converters are not suitable for these applications. This is because, in those topologies, the transformer requires low leakage inductance and consequently high interwinding capacitance due to the close proximity requirement between windings. This will increase the total circuit input–output capacitance. Furthermore, those topologies usually involve the use of feedback elements crossing the isolation boundary and thus violate the aforementioned second requirement.

The relatively high transformer leakage inductance due to the loose coupling can be useful in resonant topologies [24]–[26] This suggests an approach shown in Fig. 4(a), based on a two-stage converter. The configuration utilizes only standard existing topologies. The system is powered by a power factor correction whose output voltage is assumed to be 400 V dc. The resonant converter operates with open-loop control to eliminate the feedback from output to the input. Its output voltage is used to supply a nonisolated down-stream converter, such as a buck converter, as demonstrated in Fig. 4(a). The closed-loop regulation of the final output voltage is performed by the down-stream converter, while the low circuit input-to-output capacitance is determined by the loose coupling and feedback-free operation of the resonant converter. For example, if the down-stream buck converter has a maximum output voltage level of 60 V, then the resonant converter can be designed for a voltage output of about 80 V. In short, in order to attain the two aforementioned goals, it must be done with a two-stage converter with a separate control loop for each stage. This approach, however, can be costly and require significant effort to develop a separate control loop for each stage.

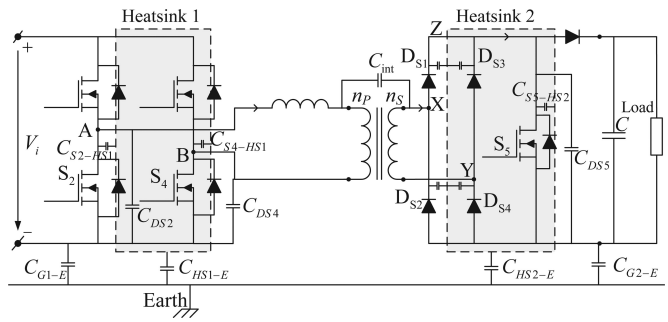

Fig. 5. CM noise paths.

Considering the control performance, a feedback-free resonant converter design is only optimal if the switching frequency is fixed at the load-independent frequency, where the converter gain is independent of variation in the load. However, this creates disadvantages if the open-loop control fails to track the load-independent point due to the tolerances of the control and sensing circuits as well as of the power circuit. The variation of the voltage gain around the vicinity of the load-independent point can cause the voltage to fail. Moreover, the regulation of the down-stream converter speed is limited by the output filter used.

This paper proposes a converter and control that combine two stages into one stage. The concept is shown in Fig. 4(b). The proposed converter and its control is free from feedback across the isolation boundary. However, the output voltage is locally controlled by a closed loop in the secondary side, and thus, it maintains the high performance and robustness against the control circuit tolerance and circuit parameter variation. The transformer structure, modeling, and validation will be presented in Section V. The detailed analysis of the control approach will be presented in Section VI.

IV. CM Noise Current Paths

To better understand the effect of the difference coupling capacitance to the overall circuit input-to-output capacitance, the CM noise current paths are studied in this section.

The CM noise paths are shown in Fig. 5. In this topology, the nodes that have high *dv/dt* are nodes A, B, X, Y, and Z. In nodes A and B, there are changes of voltage from $\pm V_i$ to $\mp V_i$ with respect to the primary-side return. Nodes X, Y, Z see a change of 0 to 60 V with respect to the secondary-side return. These nodes are sources of CM noise currents. In the developed prototype, there are two heat sinks used, one for each side to reduce the capacitive coupling between the two sides. Since the drains of switch S_2 and S_4 are switching nodes and they are both attached to heat sink 1, the coupling paths include capacitances from the drains of S_2 and S_4 to heat sink 1, and capacitance from heat sink 1 to chassis/earth. In implementation, the heat sink can be electrically connected to the return path (not the chassis/earth) to further mitigate the transmission of CM noise current. The coupling paths in the secondary side include capacitances from cathodes of D_{S1}, D_{S2}, D_{S3}, D_{S4}, and the

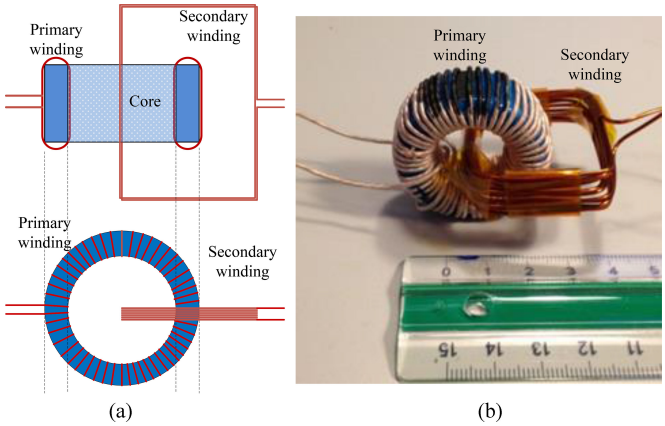

Fig. 6. Transformer structure. (a) Conceptual structure top and side view and (b) the transformer prototype.

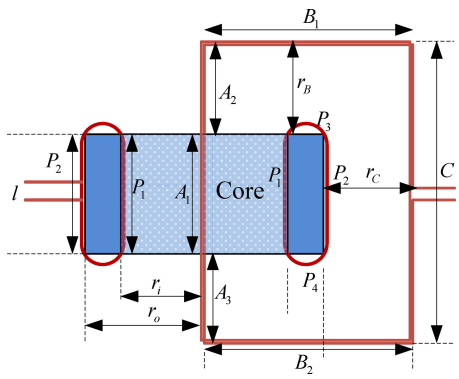

Fig. 7. Proposed transformer structure and geometry.

drain of S_5 to heat sink 2, and capacitance from heat sink 2 to chassis/earth. The coupling path caused by the transformer comes from the interwinding capacitance, $C_{\rm int}$. It can be clearly seen that $C_{\rm int}$ is in series with the other coupling capacitances, forming a loop of CM noise paths. Therefore, the value of $C_{\rm int}$ determines the overall CM noise performance [27]. The typical value of the other coupling capacitance falls into a range from 100 pF to tens of microfarads [2], [12], [13]. If $C_{\rm int}$ can be made much smaller than the other coupling capacitances, the overall circuit input-to-output capacitance will be governed by only $C_{\rm int}$.

V. Transformer Structure, Interwinding Capacitance Modeling, and Validation

In this section, the transformer structure, its specification, and its interwinding capacitance mathematical model will be presented first. After that, key measurement data including the transformer's primary to secondary winding impedance, the interpreted transformer's interwinding capacitance, and the leakage inductance referred to the primary side will be given.

A. Transformer Structure

The general structure of the proposed transformer is illustrated in Fig. 6(a), and the transformer prototype photo is shown in Fig. 6(b). In its winding configuration, the winding with fewer turns will be placed in the geometrical center of the core, forming a rectangular frame. The remaining winding with more turns is tightly wound around the core. This is, respectively, the case of the secondary winding and primary winding in Fig. 6. With this structure, the two windings are separated from each other by a reasonably large distance. Moreover, the dielectric material between them is only the surrounding air that has the second lowest permittivity to vacuum. All of these features result in the transformer's extremely low interwinding parasitic capacitance.

To arrive at a design procedure or guideline of making a transformer that has a specific interwinding parasitic capacitance, depending on how precise it is expected to be, this normally requires mathematical modeling or simulation based on the finite-element method (FEM). Apart from that, the design of the transformer is a compromise of other issues such as the power losses and physical size of the whole circuit. The transformer is often the most bulky part in the prototype of a power electronics converter. As a result, the size of the transformer greatly affects the size of the prototype. It is preferable to select as small a transformer size as possible so that the prototype is smaller; therefore, the parasitic capacitance coupling from the prototype to earth is smaller.

Transformer parasitic capacitance cannot be ignored. The voltage potential between turns, between winding layers, and between windings and the core create this parasitic element. In fact, this parasitic capacitance significantly affects the magnetic component performance, such that the current waveform on the excitation side would be distorted, and the overall efficiency of converters would be decreased. Subjected to high-voltage stresses, the interwinding capacitance causes leakage currents and consequently contributes to the EMI problem [28].

The specifications of the developed transformer are provided in Table II. It also provides dimensional information about the core and winding with respect to the notations in Fig. 7. It is an R36/23/15 toroid core from Epcos with N87 material. The primary winding is made by Litwize with 60 0.2-mm-diameter twisted parallel wires. The secondary winding uses copper wire with a 1-mm diameter. The turns ratio is 55:11.

The interwinding capacitance can be calculated by using the stored electric energy method [28]–[33], in which voltage distribution plays a vital role. The energy stored can be derived by either an FEM simulation model based on commercial software or a mathematical model. However, FEM has a particular disadvantage in deriving the interwinding capacitance of the proposed transformer. A 2-D FEM simulation model based on Ansoft/Maxwell software has been built to observe the energy stored in the transformer. Fig. 8 shows the result of the energy stored created by the segment of the secondary winding that is in the center of the core and the primary winding. Because the displacement distance between the secondary winding and the primary winding is large and the turn to turn distances of each winding are much smaller, the energies stored between turn to turn of the windings dominate the interwinding energies. The simulation result in Fig. 8 shows that the energy is concentrated

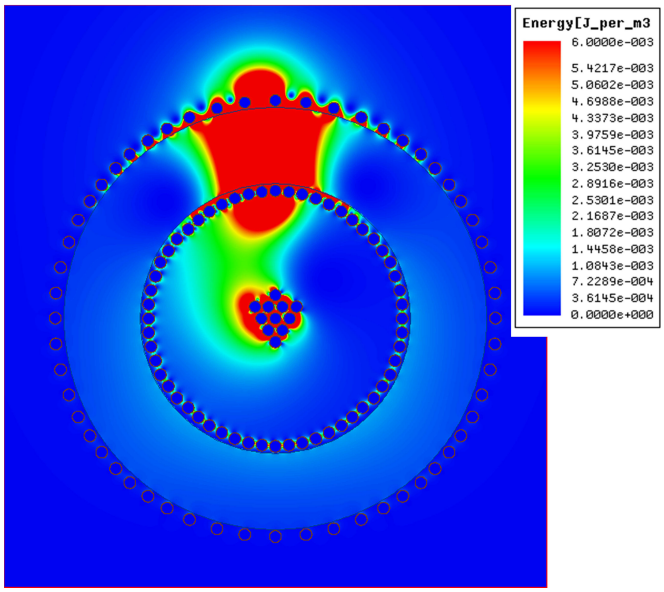

Fig. 8. 2D FEM simulation result of the winding energy distribution.

near the two ends of the primary winding. This is reasonable because in the proximity of the two ends, the voltage differences are maximum and the turn to turn displacements are minimum.

The two kinds of energy, turn-to-turn energy and interwinding energy, cannot be simulated separately with FEM software. This is one of the reasons why a mathematical model is adopted for this paper. The other reason to model the interwinding capacitance with mathematics is that it will allow fast recalculation with minor parameter modifications if a transformer with the same structure is used but possesses different geometry, turns ratio, and winding parameters. It, therefore, allows performance of an optimization routine of the transformer design.

The calculation based on a mathematical model will be presented next.

B. Mathematical Model of the Interwinding Capacitance

First, the interwinding capacitance caused by the interaction between segment A_1 of the secondary winding through the core center to the parallel segments P_1 and P_2 of the primary winding (see Fig. 7) will be calculated. Segments P_1 and P_2 are the winding segments around the perimeters of the inner ring and outer ring, respectively. The secondary winding has 11 turns stranded together, so each turn is located in the approximate center of the magnetic core, as shown in Fig. 6. The static capacitance between the inner primary turns and the secondary turns can be expressed as [28], [30]

$$C_i = \frac{\epsilon_0 S}{r_i} = \frac{\epsilon_0 d\pi l}{2r_i}, \tag{2}$$

where ϵ_0 is the permittivity of free air space, d is the diameter of each turn (the same size of wire is selected for both primary and secondary turns), and l and r_i are the overlapped length and the distance between the inner primary turns and the secondary turns, respectively.

With respect to the outer ring of the primary winding, the static capacitance can be expressed with a different distance r_o

$$C_o = \frac{\epsilon_0 S}{r_o} = \frac{\epsilon_0 d\pi l}{2r_o}. \tag{3}$$

Assuming that the voltage potential distribution along the primary winding varies linearly

$$V_P[i] = \frac{i}{n_p - 1} V_P \quad (i = 0, 1, 2, 3, \ldots, n_p - 1). \tag{4}$$

Then, the total stored electric energy between all secondary turns lying in segment A_1 and the inner ring of primary winding P_1 is

$$E_i = \frac{1}{2} C_i \sum_{j=0}^{n_s-1} \sum_{i=0}^{n_p-1} \left(\frac{V_P i}{n_p - 1} - \frac{V_S j}{n_s - 1} \right)^2. \tag{5}$$

With the same analytical approach, the total stored electric energy between all secondary turns and the outer ring of the primary winding P_2 can be expressed as

$$E_o = \frac{1}{2} C_o \sum_{j=0}^{n_s-1} \sum_{i=0}^{n_p-1} \left(\frac{V_P i}{n_p - 1} - \frac{V_S j}{n_s - 1} \right)^2. \tag{6}$$

The contribution of segment *B* of the secondary winding to the total energy is computed as follows. The capacitance caused by the side segments B_1 , B_2 to the primary winding is

$$C_B = \frac{\epsilon_0 d\pi l_B}{2r_B}. \tag{7}$$

Segments B_1 and B_2 face the middle parts of the primary winding. It is appropriate to assume that there are five turns from the primary winding that lie in segment P_3 or P_4 of Fig. 7 facing segment B_1 and B_2, respectively. They are turn number $(n_p - 1)/2 - 2$ to $(n_p - 1)/2 + 2$. In a specific design with 55 primary turns, these will correspond to turn number 25 to 29. Then, the stored electric energy caused by B_1 and B_2 is

$$E_B = 2 \left(\frac{1}{2} C_B \sum_{j=0}^{n_s-1} \sum_{i=(n_p-1)/2-2}^{(n_p-1)/2+2} \left(\frac{V_P i}{n_p - 1} - \frac{V_S j}{n_s - 1} \right)^2 \right). \tag{8}$$

Next, the contribution of segment *C* of the secondary winding to the outer ring of the primary winding is computed. Referring to Fig. 9(c), it is helpful to mathematically express the distance from segment *C* to the turns lying in the outer ring of the primary. In triangle CDB, distance $\overline{\mathrm{CB}}$ is related to other sides of the triangle by

$$\begin{aligned} \overline{\mathrm{CB}}^2 &= \overline{\mathrm{CD}}^2 + \overline{\mathrm{BD}}^2 - 2\overline{\mathrm{CD}}\overline{\mathrm{BD}}\cos(\Phi) \\ &= (r_i + r_o)^2 + r_o^2 - 2(r_i + r_o) r_o \cos(\pi - 2\pi/n_p). \end{aligned} \tag{9}$$

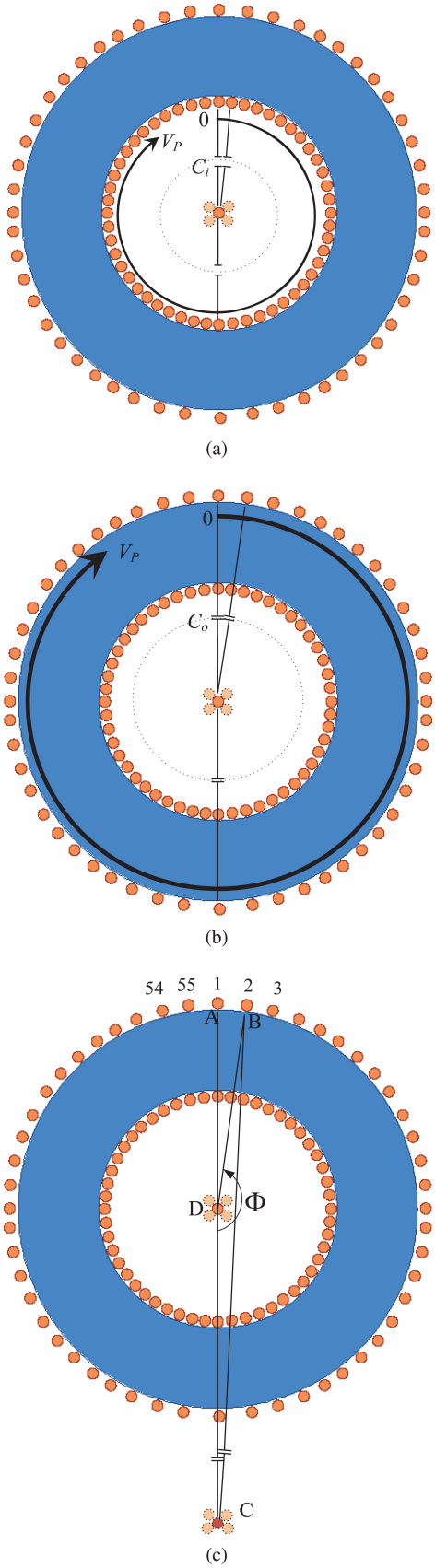

Fig. 9. Effect of parasitic capacitance from the secondary winding of (a) segment A to the inner ring of the primary winding, (b) segment A to the outer ring of the primary winding, and (c) segment C to the outer ring of the primary winding.

Therefore, the distances from C to the ith turn of the outer-primary winding are

$$r_{C\text{out},i} = \sqrt{(r_i + r_o)^2 + r_o^2 - 2(r_i + r_o)r_o \cos\left(\pi - \frac{i2\pi}{n_p}\right)} \quad (i = 1, 2, 3, ..., n_p - 1). \tag{10}$$

The capacitance from segment C of the secondary winding to turn number ith of the outer primary winding is

$$C_{C\text{out},i} = \frac{\epsilon_0 d\pi l_C}{2\sqrt{(r_i + r_o)^2 + r_o^2 - 2(r_i + r_o)r_o \cos\left(\pi - \frac{i2\pi}{n_p}\right)}} \quad (i = 1, 2, 3, ..., n_p - 1) \tag{11}$$

The total stored energy caused by segment C of secondary winding to the outer ring of primary winding is then

$$E_{C\text{out}} = \frac{1}{2}\sum_{j=0}^{n_s-1}\sum_{i=0}^{n_p-1} C_{C\text{out},i}\left(\frac{V_P i}{n_p - 1} - \frac{V_S j}{n_s - 1}\right)^2. \tag{12}$$

Similarly, the stored energy caused by segment C of secondary winding to the inner ring of primary winding is

$$E_{C\text{in}} = \frac{1}{2}\sum_{j=0}^{n_s-1}\sum_{i=0}^{n_p-1} C_{C\text{in},i}\left(\frac{V_P i}{n_p - 1} - \frac{V_S j}{n_s - 1}\right)^2, \tag{13}$$

where

$$C_{C\text{in},i} = \frac{\epsilon_0 d\pi l_C}{2\sqrt{(r_i + r_o)^2 + r_i^2 - 2(r_i + r_o)r_i \cos(\pi - \frac{i2\pi}{n_p})}} \quad (i = 1, 2, 3, ..., n_p - 1). \tag{14}$$

The total stored electric energy is then

$$\begin{aligned} E_{\text{total}} &= E_i + E_o + E_B + E_{C\text{in}} + E_{C\text{out}} \\ &= \frac{1}{2}C_{\text{int}}(V_P - V_S)^2. \end{aligned} \tag{15}$$

The calculated interwinding capacitance, C_{int}, based on the parameters in Table II is 10 pF. Table III shows the calculated energy and capacitance. It is observed that segment A_1 dominates the stored energy, and the contributions of segments B_1 and B_2 are negligible. The design guideline is that increasing the core geometry and increasing distance from segment C to the core will effectively reduce the interwinding capacitance.

C. Measurement Results

Fig. 10 shows the experimental data of the interwinding impedance magnitude and phase of the transformer. It is done with both terminals of each winding shorted. As can be seen, the impedance magnitude has a constant slope with -20 dB/dec roll off, and the phase is around $-90°$. Therefore, the interwinding impedance is capacitive, and it is appropriate to model the interwinding impedance as a lump-element circuit with an interwinding capacitor. The measured data are in the form of digital values of impedance magnitude and phase at a sweep of different frequencies. They are imported into MATLAB and

TABLE II
PARAMETERS OF MAGNETIC CORE AND WINDING GEOMETRIES OF THE TRANSFORMER

Core material	N87
Core dimension	36 mm × 23 mm × 15 mm
Turns ratio	55:11
Primary winding	Litz-wire 60 × 0.2 mm
Secondary winding	copper 1.0 mm
ϵ_0	$8.85.10^{-12}$ F/m
d	1 mm
l	16 mm
r_i	11.5 mm
r_o	18 mm
n_p	55
n_s	11
V_P	300 V
V_S	60 V
r_B	12 mm
l_B	6.5 mm
l_C	16 mm

TABLE III
CALCULATED ENERGY AND CAPACITANCE

Parameter	E_i (J)	E_o (J)	E_B (J)	$E_{C\,\mathrm{in}}$ (J)	$E_{C\,\mathrm{out}}$ (J)	E_{total} (J)	C_{int} (F)
Value	1.3 e-7	8.4 e-8	1.1 e-9	3.8 e-8	3.2 e-8	2.9 e-7	9.97 e-12

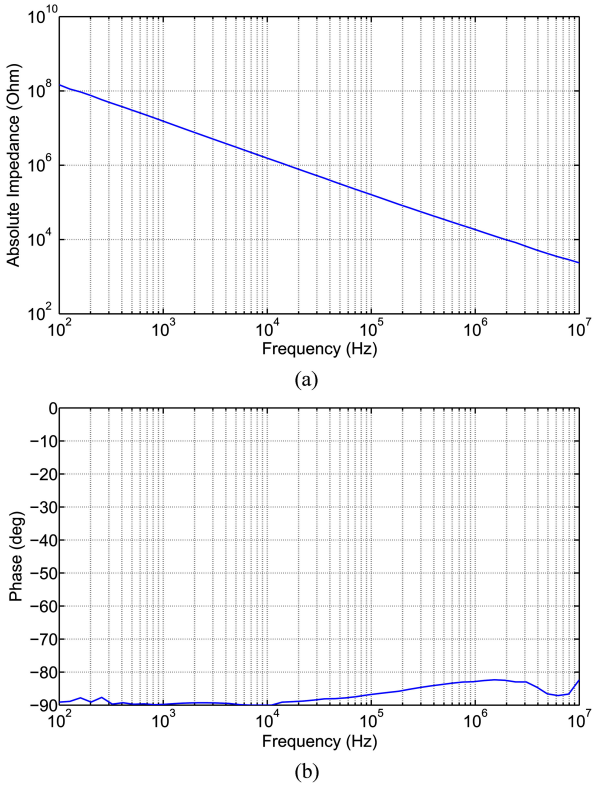

Fig. 10. Interwinding impedance measurement: (a) magnitude and (b) phase.

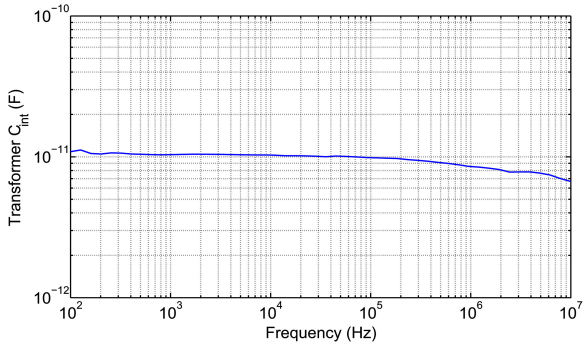

Fig. 11. Measured interwinding parasitic capacitance.

processed by proper scripts to yield the interpreted coupling capacitance, whose values are shown in Fig. 11. It can be seen that the capacitance value is around 10 pF in the wide range of frequency from dc to 10 MHz. It is validated that with the proposed configuration of the transformer, an extremely low interwinding parasitic capacitance can be achieved.

The process is repeated for the measurement of the impedance between two terminals of the primary side while the two terminals of the secondary side shorted. This impedance can be modeled as a leakage inductor. The impedance magnitude and phase are shown in Fig. 12(a) and (b). The impedance behaves like a resistor at frequencies up to 1 kHz due to winding ohmic resistance, like a leakage inductor from 2 kHz to 1.5 MHz due to leakage flux, and like a capacitor from above 1.5 MHz due to the self-capacitance of the leakage inductor. The interpreted magnitude of the leakage inductor is shown in Fig. 12(c). The leakage inductance value is 170 μH in the range of 100–300 kHz. The consequential relatively high leakage inductance may be explained by the large geometrical separation of the two windings that produces relatively large leakage flux outside the core. Hence, the proposed topology as well as its associated control approach must be designed to utilize the leakage inductor. The control approach will be presented in the next section.

VI. PROPOSED CONTROL APPROACH

A. Proposed Control Approach

In this paper, the control approach without isolated feedback is adopted in order to achieve minimum circuit input-to-output parasitic capacitance for the requirements of the targeted applications. The proposed converter physical configuration is shown in Fig. 13. There are two control loops where one resides in the primary and the other one resides in the secondary. The secondary-side controller regulates the output voltage to be constant at 60 V. The primary-side controller controls the primary-side inductor current; thus, it indirectly regulates the nominal output current. The secondary-side circuit can be seen as a current source supplying the output capacitor in parallel with the load.

On the secondary side, the output voltage is sensed by a voltage divider and compared to a hysteresis reference to switch the shunt switch S_5 ON and OFF. When S_5 is switched OFF, the converter operates in its *power mode* [see Fig. 14(a)] and the output

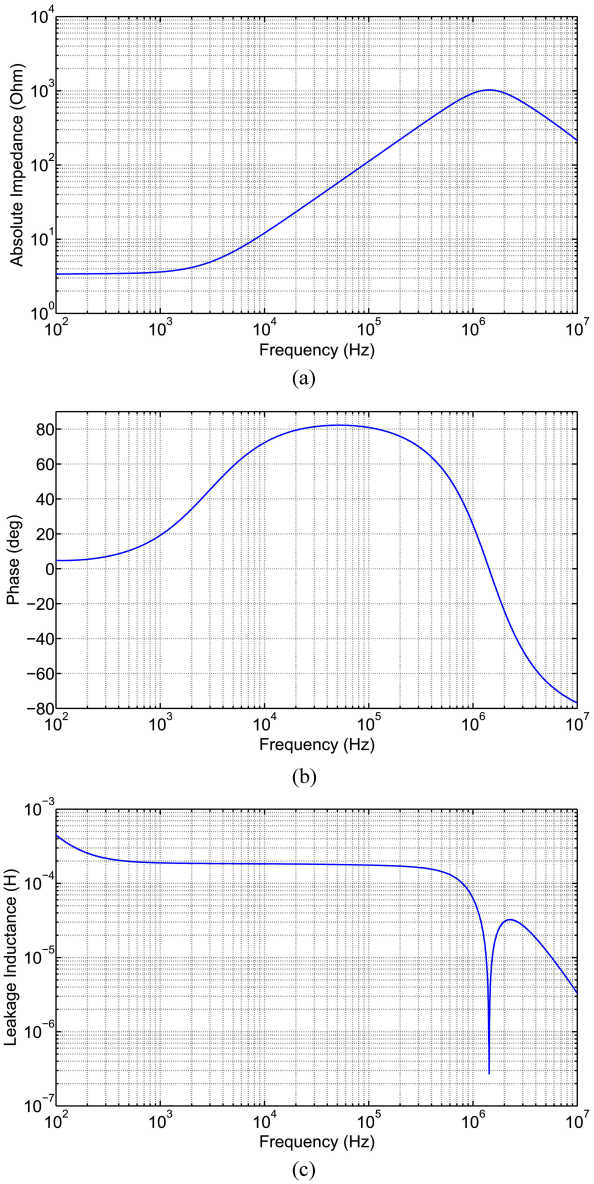

Fig. 12. Primary leakage impedance measurement. (a) Magnitude, (b) phase, and (c) leakage inductance.

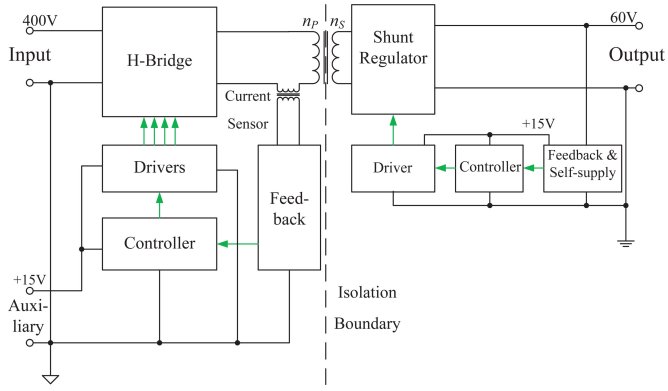

Fig. 13. Block diagram of the circuit layout.

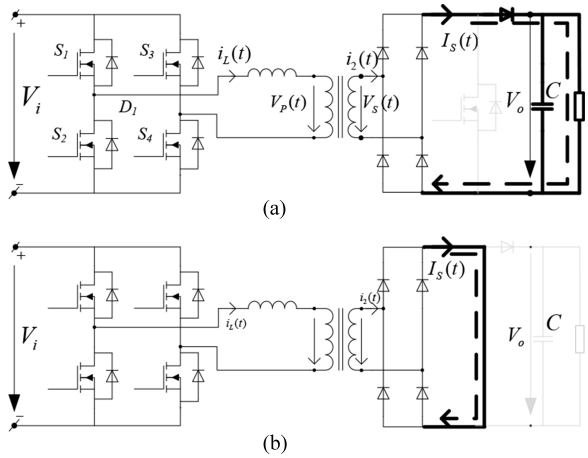

Fig. 14. Operation mode: (a) Power mode and (b) shunt mode.

voltage increases. On the other hand, when S_5 is ON, shunting the secondary side, the converter operates in its *shunt mode*, which is shown in Fig. 14(b); the output voltage decreases. This control approach is different from the control method of the conventional full-bridge topology or single active bridge topology in that the output voltage regulation is independent from the regulation of the active switches of the primary side. Normally, the former topologies involve a feedback of the output voltage across the isolation boundary, and utilization of a compensator to adjust the switching fashion of the active bridge in order to control the output voltage. However, as mentioned in Section III, those topologies and their control approach are not optimal for the targeted applications.

On the primary side, because the leakage inductance is relatively high, at 170 μH, it is utilized as the main inductor in the circuit, and there is no external inductor added. In this way, the leakage inductor, although being relatively high Henry value compared to a traditional converter, has become an integral part of the converter. The primary-side inductor current can be controlled by adjusting one variable among the three variables of the primary switches: frequency, phase shift, and duty cycle. In this paper, the frequency modulation is chosen. The duty cycle of the switches is fixed at 50%, and the phase-shift is therefore at 0°. The primary-side current i_L is first sensed and rectified. It is then low-pass filtered to produce a rectified-dc value. This value is then compared to a rectified-dc reference and processed by an analogue proportional-integral (PI) compensator. The output of the PI compensator is fed to a voltage-controlled oscillator (VCO) that automatically adjusts the switching frequency to keep the rectified primary dc current to be a constant 1 A dc. With a turns ratio of 5:1, the rectified dc current at the secondary side is controlled at 5 A dc. The analytical waveforms of the converter in the two operation modes are shown in Fig. 15, whereas the block diagrams of the two control loops are shown in Fig. 16.

B. Power Mode Operation

The power mode is the operation mode where the shunt MOSFET S_5 is open, allowing the output current to supply the output

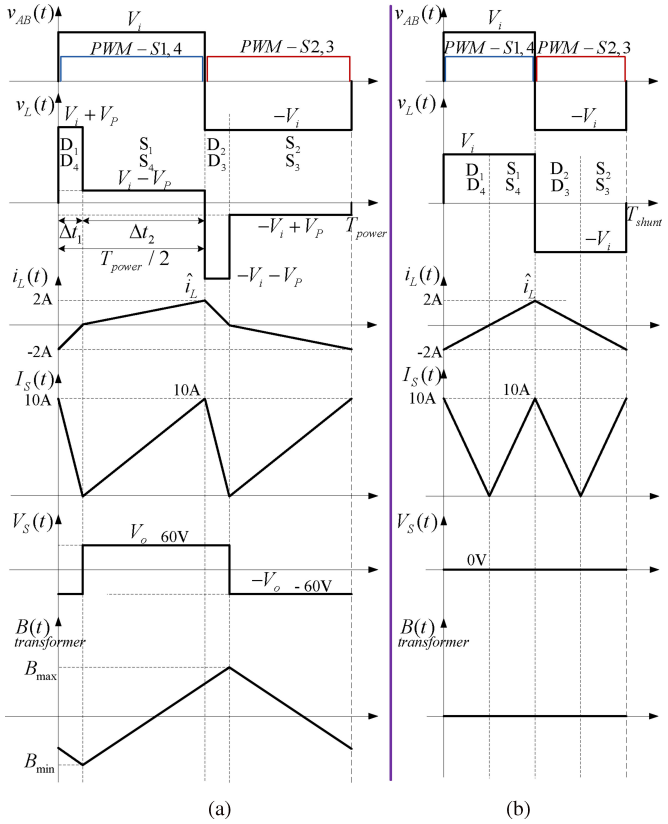

Fig. 15. Analytical waveforms when the converter operates in: (a) Power mode and (b) shunt mode.

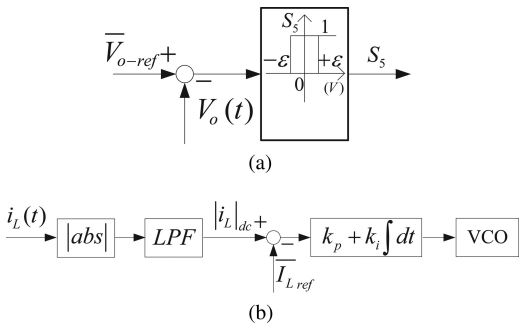

Fig. 16. Control block diagram. (a) Hysteresis control in the secondary side and (b) average current mode control in the primary side.

load as in Fig. 14(a). The analytical waveforms of the converter operating in power mode are shown in Fig. 15(a). As mentioned earlier, the pulse width modulation (PWM) signal for each pair of switches (S_1, S_4) and (S_2, S_3) is a pulse with 50% duty cycle. A complete period consists of 50% of the time where (S_1, S_4) are commanded to turn ON, and 50% of the time where (S_2, S_3) are commanded to turn ON. There is no phase shift between the PWM signals except for a small amount of dead time.

When the PWM signal sent to (S_1, S_4) is ON and the PWM signal sent to (S_2, S_3) is OFF, the inductor current $i_L(t)$ will increase from the most negative value $-\widehat{i}_L$ to the most positive value $\widehat{i}_L$. During the duration where $i_L(t)$ is increasing from $-\widehat{i}_L$ to zero, the body diodes (D_1, D_4) of the two switches conduct the current [see Figs. 1 and 15(a)]. Because $i_L(t)$ is negative during this duration, the secondary-side current $i_2(t)$ is negative; it conducts through diodes (D_{S2}, D_{S3}). The voltage across the secondary winding is $V_S(t) = -V_o$, which is a negative value. This voltage is reflected to the primary side by the turns ratio: $V_P(t) = (n_P/n_S)V_S(t) = -(n_P/n_S)V_o = -V_P$, where $V_P(t) = V_P \text{sgn}(i_L(t))$ and the operator sgn denotes the sign of the operand.

As a result, the voltage across the leakage inductor during the time when the inductor current is negative is $v_L(t) = V_{\text{AB}}(t) - V_P(t) = V_i + V_P$. The current increases linearly with time with a slope of $(V_i + V_P)/L$.

After the inductor current reaches zero, diodes (D_1, D_4) stop conducting and the current flows through the channels of (S_1, S_4) instead. This results in a zero voltage, zero current switching at turn-on of switch (S_1, S_4). This means there is no switching loss in turning ON switches (S_1, S_4), and it is one of the advantages of this control approach. The inductor current changes direction to positive, as does the secondary-side current $i_2(t)$. Current $i_2(t)$ flows through diodes (D_{S1}, D_{S4}), making the voltage across the secondary-side transformer positive, $V_S(t) = V_o$. Hence, the voltage across the primary side of the transformer becomes positive.

The voltage across the leakage inductor during the time when the inductor current is positive is $v_L(t) = V_{\text{AB}}(t) - V_P(t) = V_i - V_P$. The slope of the current during this duration is $(V_i - V_P)/L$ [see Fig. 15(a)].

During the next half-period, the PWM signal of switches (S_1, S_4) is OFF and the PWM signal of switches (S_2, S_3) is ON. At the transition of these PWM signals, (S_1, S_4) is turned OFF and, because the current is positive, it is transferred from the channels of (S_1, S_4) to the body diodes (D_2, D_3) of switches (S_2, S_3). The voltage difference between two nodes A and B changes polarity. The voltage across the inductor is $v_L(t) = V_{\text{AB}}(t) - V_P(t) = -V_i - V_P$ as long as the inductor current is positive. When the inductor current decreases and reaches zero, the body diodes (D_2, D_3) stop conducting and the current is transferred to the channels of switches (S_2, S_3). Again, the turn-on transient of switches (S_2, S_3) occurs with the zero voltage, zero current feature, resulting in no switching loss. Similarly, when the inductor current is negative and (S_2, S_3) are ON, the voltage across the inductor is $-V_i + V_P$.

Based on the above analysis, the inductor current has the resulting form which is shown in Fig. 15(a). It is a nonsymmetrical triangular ac signal with zero dc bias. Due to the presence of the diode bridge in the secondary side, the output current $I_S(t)$ is the result of the rectified inductor current multiplying with the inversion of the turns ratio

$$I_S(t) = |i_2(t)| = \frac{n_p}{n_s}|i_L(t)|. \tag{16}$$

Diode D_{S5} in the power mode is forward-biased. The output current $I_S(t)$ is a positive triangular signal with twice the frequency of the leakage inductor current. Its peak value is $(n_P/n_S)\widehat{i}_L$ or 10 A in this design. The dc value of this signal is therefore half its peak value: $0.5(n_P/n_S)\widehat{i}_L$ or 5 A.

The switching frequency that ensures the primary side is regulated at the peak value of $\widehat{i}_L$ can be derived by equating the product of voltage across the inductor and time when the current is negative to that when the current is positive. The peak value when the inductor current is negative is equal to that when the current is positive (see Fig. 15)

$$\widehat{i}_L = \frac{V_i + V_P}{L}\Delta t_1 = \frac{V_i - V_P}{L}\Delta t_2, \tag{17}$$

where

$$\Delta t_1 + \Delta t_2 = \frac{T}{2} = \frac{1}{2f}. \tag{18}$$

From (17) and (18), it can be proved that

$$f = \frac{V_i}{4\widehat{i}_L L}\left(1 - \left(\frac{V_P}{V_i}\right)^2\right). \tag{19}$$

As a result, the switching frequency in power mode is

$$f_{\text{power}} = \frac{V_i}{4\widehat{i}_L L}\left(1 - \left(\frac{n_p V_o}{n_s V_i}\right)^2\right). \tag{20}$$

Given the input and output voltage value from Table I, leakage inductor $L = 170$ μH, peak value of the inductor current $\widehat{i}_L = 2$ A, we can derive the expected switching frequency in power mode: $f_{\text{power}} = 128$ kHz.

C. Shunt Mode Operation

The shunt mode is the operation mode where the shunt MOSFET S_5 is shorted, which is illustrated in Fig. 14(b). The voltage of the anode of diode D_{S5} with respect to the secondary-side return path is approximately zero if the voltage across the on-resistance of S_5 is neglected. Because the output voltage is regulated at V_o and there is an output capacitor C that prevents output voltage from being changed drastically, the voltage at cathode of D_{S5} is V_o. Hence, D_{S5} is reverse-biased.

In a similar way, the analytical waveforms of the converter operating in shunt mode are shown in Fig. 15(b). Because now the shunt switch is shorted, the output current $I_S(t)$ will circulate through either (D_{S1}, S_5, D_{S4}) or (D_{S2}, S_5, D_{S3}) when the secondary-side current $i_2(t)$ is positive or negative, respectively. The voltage across the secondary-side transformer, $V_S(t)$, becomes zero, which is demonstrated in the bottom of Fig. 15(b). Thus, $V_P(t)$ also becomes zero.

As a result, the voltage across the leakage inductor when the PWM signal for (S_1, S_4) is ON is V_i regardless of the sign of the current. Likewise, the voltage across the leakage inductor when the PWM signal for (S_2, S_3) is ON is $-V_i$. This results in a symmetrical leakage inductor current as shown in Fig. 15(b). The output current $I_S(t)$ is a symmetrical positive signal.

From (19), given $V_P = 0$, the expected switching frequency in shunt mode is

$$f_{\text{shunt}} = \frac{V_i}{4\widehat{i}_L L}. \tag{21}$$

The calculated expected switching frequency in shunt mode is, therefore, $f_{\text{shunt}} = 294$ kHz.

D. Comparison With Existing Control Approaches

A very loosely coupled transformer, as is the case here, has a significant high leakage inductance. This is, in this paper, used as the inductance of the circuit (see Fig. 1). Many resonant converters utilize similar concept [24]–[26]. The practice of using the high leakage inductance as the main inductor is also adopted in dual active bridge converters [34]–[36]. In this paper, the control circuit, to some extent, can be regarded as nonconventional. The primary side uses a combination of average current mode (peak current mode could also be used) and variable frequency control to keep the inductor current at a constant level. However, average and peak current mode controls are conventional control methods [37]–[40]. Variable frequency control is widely used by many resonant converters [24]–[26], [41]. In this paper, those two methods are combined on the primary side. On the secondary side, the output voltage hysteresis control of the shunt switch is used. This practice, to some extent, can be regarded as nonconventional, but relatively straight forward to implement.

Using the combination of the previously mentioned primary- and secondary-side controls enables a complete elimination of the feedback loop crossing the isolation boundary, which would, in almost all implementations, imply additional parasitic capacitance added (such as the input–output capacitance of an optocoupler or of a high-frequency feedback transformer) between primary and secondary sides.

VII. Experimental Results

The specifications of the converter were described in Section II, and they will be summarized briefly here. The input voltage to the converter is 400 V dc, which represents the output of a typical power factor correction circuit. The inductor current is to be controlled at 2 A peak. This results in a rectified current of 10 A peak in the output because the turns ratio of 5:1 is used. The dc offset value of the secondary-side rectified current $I_S(t)$ is therefore 5 A. The output voltage is controlled at 60 V. This allows the converter to output 300-W nominal power. The expected switching frequency of the active bridge in steady state in shunt and power modes is 294 and 128 kHz, respectively. Most importantly, an overall circuit input-to-output capacitance of no more than 10 pF is desired.

The experimental studies have examined circuit input-to-output parasitic capacitance, converter transient response, and converter power efficiency. A photo of the prototype can be found in Fig. 17. As can be seen from the photo, the proposed transformer is the only element that links between the primary side and secondary side. There is no feedback element added across the isolation boundary.

A. Circuit Input-to-Output Parasitic Capacitance

The circuit input-to-output capacitance is measured by the Agilent 4294A precision impedance analyzer. The accuracy claimed by the manufacturer is $\pm 3\%$ in the measured range. The two input terminals are shorted and so are the two output terminals. After that, the ground planes of the primary side and secondary side are measured with the instrument. Fig. 18 shows

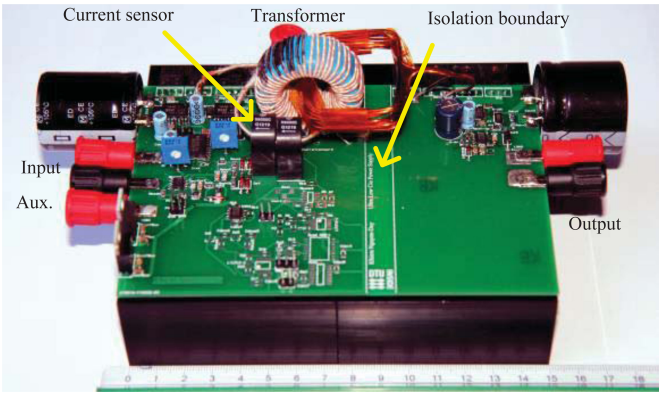

Fig. 17. Photo of the prototype.

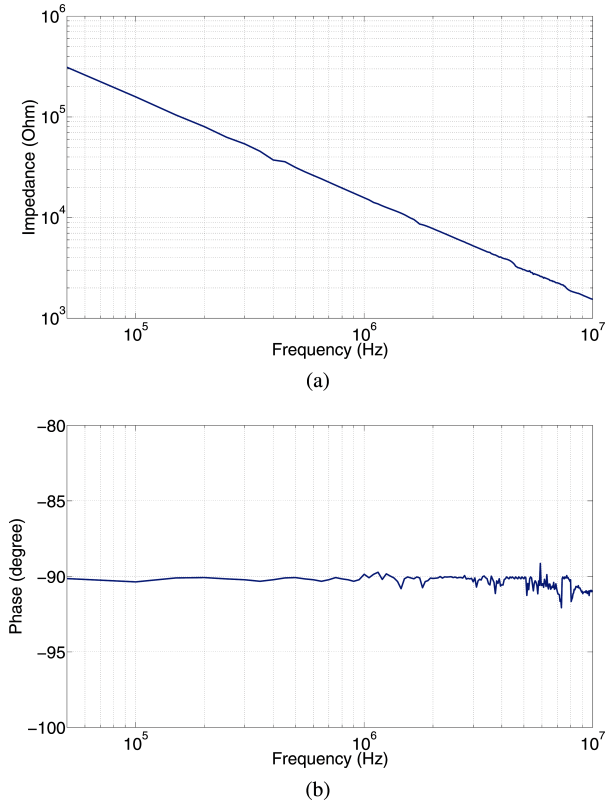

Fig. 18. Circuit input-to-output impedance measurement: (a) magnitude and (b) phase.

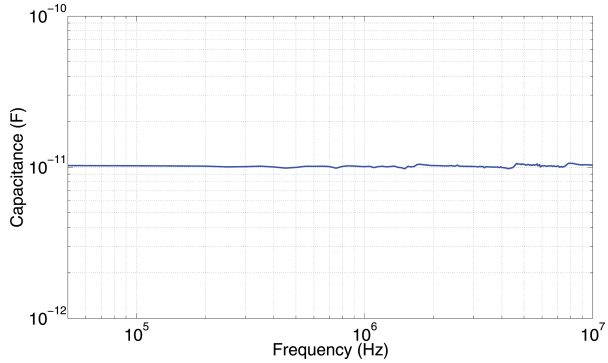

Fig. 19. Circuit input-to-output parasitic capacitance.

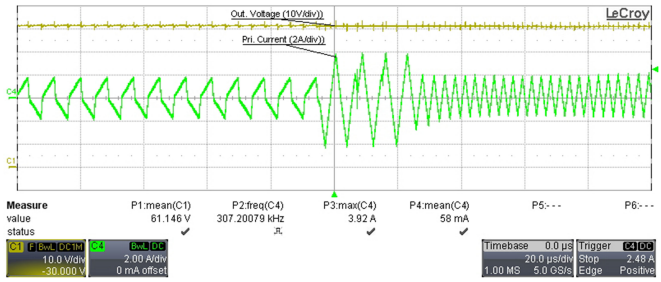

Fig. 20. Transient response from power mode to shunt mode. Top: output voltage $V_o(t)$ (10 V/div); bottom: inductor current $i_L(t)$ (2 A/div); time scale: 20 μs/div.

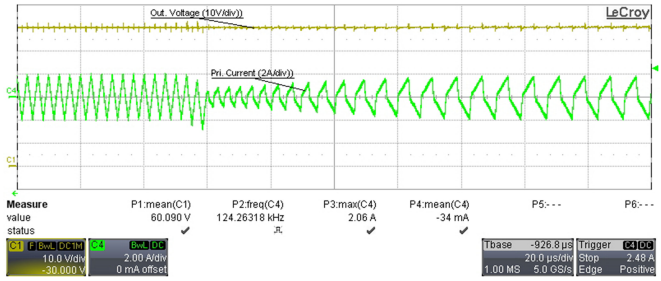

Fig. 21. Transient response from shunt mode to power mode. Top: output voltage $V_o(t)$ (10 V/div); bottom: inductor current $i_L(t)$ (2 A/div); time scale: 20 μs/div.

the circuit input-to-output impedance magnitude and phase measurement. Its magnitude slope of -20 dB/dec and phase around -90° makes it appropriate to model as a capacitor. The measured value of the capacitance is around 10 pF, which is shown in Fig. 19. In short, an extremely low value of circuit input-to-output capacitance has been achieved, and it has been proven to be dominated by the interwinding parasitic capacitance.

B. Converter Transient Response

In this section, two key measurement waveforms are presented and discussed. They are the inductor current on the primary side and the output voltage on the secondary side. The measurement of the inductor current is performed by the LeCroy AP015 current probe, which has a claimed accuracy of $\pm 1\%$. In addition, the measurement of the output voltage is done with the SI-9000 differential probe with an accuracy of $\pm 2\%$ as claimed by the manufacturer.

Fig. 20 shows the transient response from power mode to shunt mode. In a similar way, the transient from shunt mode to power mode is shown in Fig. 21. The value of the output voltage threshold, ε, is set to 0.5 V. It can be observed that, both the inductor current and the output voltage are well regulated at their desired steady-state values, which are 2 A peak and 60 V dc, respectively. The transient of the current from power mode to shunt mode and vice versa finishes within about 30 and 40 μs, respectively. The time needed for the inductor current

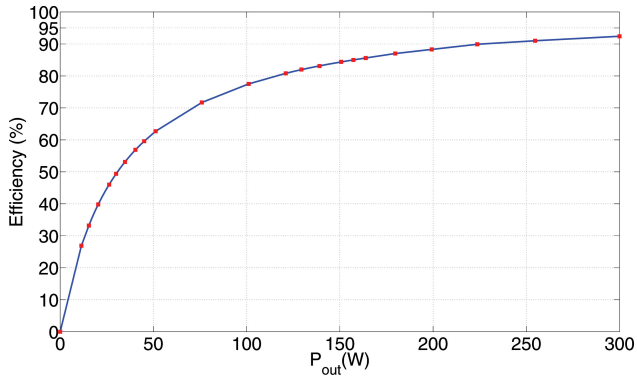

Fig. 22. Converter's power efficiency.

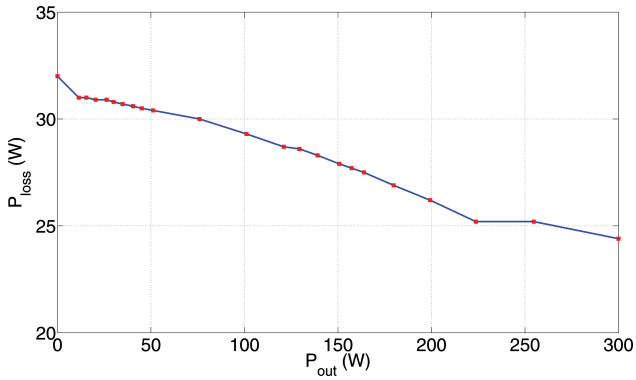

Fig. 23. Converter's power loss.

to settle is mainly determined by the dynamic of the average current control scheme described in Fig. 16. The experimental switching frequencies of the primary-side switches in power mode and shunt mode are 124 and 307 kHz, respectively. They are respectively 3% and 4% different from the expected values derived in Section VI. This is simply due to the tolerance of the components used in the analogue control circuitry and sensing, and the ignorance of the small forward voltage drop in the diodes on the secondary side. Nevertheless, the transient and steady state are both stable and satisfactory. The behavior of the circuit matches accurately with the aforementioned circuit analysis.

C. Converter Power Efficiency

The power measurement is done with the PPA5530 precision power analyzer. The accuracy claimed by the manufacturer is $\pm 0.4\%$ in the operation condition under test. The measured efficiencies at different output powers are shown in Fig. 22. At the nominal output of 300 W, the converter operates entirely in its power mode. The switching frequency on the primary side is then the smaller one, f_{power}. Therefore, the primary switching loss and both conduction loss and switching loss of shunt MOSFET S_5 are reduced. That is the reason why the peak efficiency is attained at the nominal output power. This value is 92.4%. As output power reduces, the duration in which the converter operates in shunt mode increases linearly; the loss increases slightly as shown in Fig. 23. As a result, the efficiency drops. Zero efficiency is attained at zero output power when the converter fully operates in its shunt mode. In general, the overall efficiency of the converter is satisfactory particularly ranging from 1/3 nominal power to full nominal power. Its efficiency in this range is from 77.5% to 92.4%.

VIII. Discussion

This study has been primarily concerned with minimizing converter input-to-output parasitic capacitance in order to achieve maximum noise immunity to high *dv/dt* from the loads. This goal has been approached by fulfilling two objectives. First, a novel topology with minimized interwinding capacitance transformer has been introduced. Second, a new control strategy has been proposed that both eliminates the feedback path across the isolation boundary and maintains the desired output voltage.

If a conventional full-bridge converter is used, taking the isolated boost converter as an example, the transformer should then be required to have a very low leakage inductance. Such a transformer will require very close proximity between the windings. Because the interwinding capacitance is inversely proportional to the relative distance between the windings, this configuration therefore increases the transformer parasitic capacitance. Additional EMI filtering, if added to the full-bridge converter, would not correct the high input-to-output capacitance. While the added secondary switch increases size and cost, the major goal is high *dv/dt* immunity between the primary and secondary, which provides good CM immunity.

Several advantages of the developed converter's prototype and its control strategy are as follows. First, the topology and its control allow zero current, zero voltage switching at the turn-on transitions of the switches (refer to Fig. 15 and the discussion in Section VI-B), resulting in lower switching loss at turn-on transients.

Second, this topology has higher power (60 V/300 W) per channel than 36 V/5 W designs of prior art [1] with a similar topology. This allows the converter to supply a wider range of load, from 0 to 60 V and up to 300 W.

Third, the proposed control strategy improves the reliability of the control electronics because there are no feedback elements across the isolation boundary. Specifically, it provides a more reliable fault protection if necessary because input and output voltage or current levels can be monitored and fault protection can be triggered with minimum delay.

Fourth, the regulation of the output power is very fast. Whenever the output current is not consumed by the load, it is circulated through the shunt-switch and the secondary-side diode bridge. As soon as S_5 is turned OFF, there will be 300 W of power immediately available to supply the output. Furthermore, the elimination of feedback prevents saturation of the control circuitry during transients. All of these proposed topology and control features make the converter react very quickly to changes in power demand compared to existing topologies and controls.

Finally, an extremely low circuit input-to-output capacitance is achieved: 10 pF in a 300-W prototype. Its parasitic

capacitance per watt is 0.033 pf/W, which is approximately 30 times lower than that of existing converters reported in the literature [12], [13].

It must be acknowledged, however, that the proposed approach contains several disadvantages. First, the MOSFETs on the primary side turn off at their peak currents, resulting in higher turn-off loss. Second, the slightly increased loss at lighter load makes the converter's efficiency relatively low at low output power. This issue may be considered in a separate study.

IX. Conclusion

In this paper, the authors have presented the design of a 300-W isolated power supply with very high *dv/dt* immunity. The main advantage of the power supply is the extremely low interwinding capacitance in the transformer, which makes the circuit input-to-output capacitance ultralow, considering the output power. The converter is specially designed for applications with very large changes of voltage over short durations of time. Circuit operation and control have been presented, and experimental data have also been provided that prove to match well with expectations. Furthermore, the advantages and disadvantages of the converter have been discussed. In summary, the converter is suitable for a wide range of applications, especially where fast output power response and minimization of the circuit input-to-output capacitance are vital.

Acknowledgment

The authors would like to thank the reviewers for their constructive suggestions, which greatly improved the revised manuscript. A particular thanks is also extended to A. Brissette, Graduate Research Assistant at University of Colorado Boulder, CO, USA, for his tremendous help in proofreading the revised manuscript.

References

[1] M. A. E. Andersen, "MOS gate driver circuit with extremely high galvanic isolation," in *Proc. Eur. Conf. Power Eletron. Appl.*, 1995, pp. 747–551.

[2] D. Knurek, "Reducing EMI in switch mode power supplies," in *Proc. 10th Int. Telecommun. Energy Conf.*, 1988, pp. 411–420.

[3] (Mar. 2011). Auxilliary power supplies for medium and high voltage applications. in *Proc. Bodo's Power Syst.* [Online]. Available: http://www.gva-leistungselektronik.de/_gva/gva_downloads/GvA_Auxiliary_Power_Supplies.pdf

[4] S. Wang, P. Kong, and F. Lee, "Common mode noise reduction for boost converters using general balance technique," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1410–1416, Jul. 2007.

[5] M. Shoyama, G. Li, and T. Ninomiya, "Balanced switching converter to reduce common-mode conducted noise," *IEEE Trans. Ind. Electron.*, vol. 50, no. 6, pp. 1095–1099, Dec. 2003.

[6] D. Fu, S. Wang, P. Kong, F. Lee, and D. Huang, "Novel techniques to suppress the common-mode EMI noise caused by transformer parasitic capacitances in dc-dc converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4968–4977, Nov. 2013.

[7] M. Borage, S. Tiwari, and S. Kotaiah, "Common-mode noise source and its passive cancellation in full-bridge resonant converter," in *Proc. 8th Int. Conf. Electromagn. Interference Compat.*, 2003, pp. 9–14.

[8] P. Kong, S. Wang, F. Lee, and Z. Wang, "Reducing common-mode noise in two-switch forward converter," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1522–1533, May 2011.

[9] W. Hong and R. O'Connell, "Effects of parasitic transformer capacitances on switching transients at a HV capacitor bank," in *Proc. 40th North Amer. Power Symp.*, 2008, pp. 1–6.

[10] W. Xin, F. N. K. Poon, C. M. Lee, M. Pong, and Z. Qian, "A study of common mode noise in switching power supply from a current balancing viewpoint," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst.*, 1999, vol. 2, pp. 621–625.

[11] J.-h. Choi, M. Madafshar, and K. Parmenter, "Designing common-mode (CM) EMI noise cancellation without y-capacitor," in *Proc. 22nd Annu. IEEE Appl. Power Electron. Conf.*, 2007, pp. 936–940.

[12] D. Garabandic, W. Dunford, and M. Edmunds, "Zero-voltage-zero-current switching in high-output-voltage full-bridge PWM converters using the interwinding capacitance," *IEEE Trans. Power Electron.*, vol. 14, no. 2, pp. 343–349, Mar.1999.

[13] P. Kong and F. Lee, "Transformer structure and its effects on common mode EMI noise in isolated power converters," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo*, 2010, pp. 1424–1429.

[14] "Interlink coupling high-voltage impact isolation transformer," cN Patent 2318 700, May 12, 1999. [Online]. Available: https://www.google.com/patents/CN2318700Y?cl=en

[15] (Dec. 4, 2012). Medium-voltage high-speed switches with IGBT power semiconductors. *Bodo's Power Syst*. [Online]. Available: http://www.powerguru.org/medium-voltage-high-speed-switches-with-igbt-power-semiconductors

[16] M. Hoyerby and M. A. E. Andersen, "Ultrafast tracking power supply with fourth-order output filter and fixed-frequency hysteretic control," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2387–2398, Sep. 2008.

[17] M. Hoyerby, and M. A. E. Andersen, "Optimized envelope tracking power supply for tetra2 base station RF power amplifier," in *Proc. 23th IEEE Annu. Appl. Power Electron. Conf. Expo.*, Feb. 2008, pp. 777–783.

[18] M. Hoyerby and M. A. E. Andersen, "TEDS base-station power amplifier using low-noise envelope tracking power supply," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 7, pp. 1687–1693, Jul. 2009.

[19] (2013, Feb. 25). Power electronics for medium-voltage applications, *Bodo's Power Syst.* [Online]. Available: http://www.powerguru.org/power-electronics-for-medium-voltage-applications/

[20] "An-1095 design of isolated converters using simple switchers," (2013, Apr.) Appl. Note. [Online]. Available: http://www.ti.com/lit/an/snva005b/snva005b.pdf

[21] (2013, Oct.). Miniature surface mount transformer, Document 606-1. [Online]. Available: http://www.coilcraft.com/mintrans.cfm

[22] (2014). Max250/max251 compatible converter transformers. 78250 Series. [Online]. Available: http://www.murata-ps.com/data/magnetics/kmp_78250.pdf

[23] A. J. Binnie and T. R. Foord, "Leakage inductance and interwinding capacitance in toroidal ratio transformers," *IEEE Trans. Instrum. Meas.*, vol. 16-IM, no. 4, pp. 307–314, Dec.1967.

[24] I.-H. Cho, Y.-D. Kim, and G.-W. Moon, "A half-bridge LLC resonant converter adopting boost PWM control scheme for hold-up state operation," *IEEE Trans. Microw. Theory Techn.*, vol. 29, no. 2, pp. 841–850, Feb. 2014.

[25] W. Feng, F. Lee, and P. Mattavelli, "Optimal trajectory control of LLC resonant converters for led PWM dimming," *IEEE Trans. Microw. Theory Techn.*, vol. 29, no. 2, pp. 979–987, Feb. 2014.

[26] W. Feng and F. Lee, "Optimal trajectory control of LLC resonant converters for soft start-up," *IEEE Trans. Microw. Theory Techn.*, vol. 29, no. 3, pp. 1461–1468, Mar. 2014.

[27] K. Nguyen-Duy, L. Petersen, A. Knott, O. Thomsen, and M. A. E. Andersen, "Design of a 300-Watt isolated power supply with minimized circuit input-to-output parasitic capacitance," in *Proc. 7th IET Int. Conf. Power Electron., Mach. Drive*, Apr. 8–10, 2014, pp. 1–6.

[28] Z. Ouyang, O. Thomsen, and M. A. E. Andersen, "Optimal design and tradeoff analysis of planar transformer in high-power dc-dc converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2800–2810, Jul. 2012.

[29] J. Biela and J. Kolar, "Using transformer parasitics for resonant converter—A review of the calculation of the stray capacitance of transformers," *IEEE Trans. Ind. Appl.*, vol. 44, no. 1, pp. 223–233, Jan./Feb. 2008.

[30] L. Dalessandro, F. da Silveira Cavalcante, and J. Kolar, "Self-capacitance of high-voltage transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 2081–2092, Sep. 2007.

[31] H.-Y. Lu, J. G. Zhu, and S. Hui, "Experimental determination of stray capacitances in high frequency transformers," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 1105–1112, Sep. 2003.

[32] T. Duerbaum and G. Sauerlaender, "Energy based capacitance model for magnetic devices," in *Proc. 16th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2001, vol. 1, pp. 109–115.
[33] K. Nguyen-Duy, Z. Ouyang, A. Knott, and M. A. E. Andersen, "Minimization of the transformer interwinding parasitic capacitance for modular stacking power supply applications," in *Proc. 16th Eur. Conf. Power Electron. Appl.*, 26–28, Aug. 2014.
[34] D. Costinett, D. Maksimovic, and R. Zane, "Design and control for high efficiency in high step-down dual active bridge converters operating at high switching frequency," *IEEE Trans. Microw. Theory Techn.*, vol. 28, no. 8, pp. 3931–3940, Aug. 2013.
[35] H. van Hoek, M. Neubert, and R. De Doncker, "Enhanced modulation strategy for a three-phase dual active bridge–boosting efficiency of an electric vehicle converter," *IEEE Trans. Microw. Theory Techn.*, vol. 28, no. 12, pp. 5499–5507, Dec. 2013.
[36] G. Oggier, M. Ordonez, J. Galvez, and F. Luchino, "Fast transient boundary control and steady-state operation of the dual active bridge converter using the natural switching surface," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 946–957, Feb. 2014.
[37] J.-W. Shin and B.-H. Cho, "Digitally implemented average current-mode control in discontinuous conduction mode PFC rectifier," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3363–3373, Jul. 2012.
[38] Y. Yan, F. Lee, and P. Mattavelli, "Analysis and design of average current mode control using a describing-function-based equivalent circuit model," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4732–4741, Oct. 2013.
[39] J. Wang and J. Xu, "Peak current mode bifrequency control technique for switching dc–dc converters in DCM with fast transient response and low EMI," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1876–1884, Apr. 2012.
[40] M. Hallworth and S. Shirsavar, "Microcontroller-based peak current mode control using digital slope compensation," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3340–3351, Jul. 2012.
[41] Q. Zhang, C. Hu, L. Chen, A. Amirahmadi, N. Kutkut, Z. Shen, and I. Batarseh, "A center point iteration MPPT method with application on the frequency-modulated LLC microinverter," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1262–1274, Mar. 2014.

Khiem Nguyen-Duy (S'09) was born in Hanoi, Vietnam, on June 29, 1986. He received the B.S. degree in electrical engineering from the Hanoi University of Science and Technology, Hanoi, Vietnam, in 2009, the M.Sc. degree in electrical engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 2011. He is currently working toward the Ph.D. degree in power electronics at the Technical University of Denmark, Kongens Lyngby, Denmark.

He has been a Visiting Scholar with the Colorado Power Electronics Center, University of Colorado Boulder, Boulder, CO, USA, since Summer 2014. His research interests include power electronics, motor drives, and the application of advanced control theories to these fields, especially in matrix converters and switch-mode power supplies.

Ziwei Ouyang (S'07– M'11) received the B.S. degree in electrical engineering from the Naval University of Engineering, Wuhan, China, in 2004, the M.S. degree from the Tianjin University of Technology, Tianjin, China, in 2007, and the Ph.D. degree from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2011.

He has been with the Gelsenkirchen University of Applied Science, Technical University of Delft and National University of Ireland, as a Visiting Scholar, in 2006, 2011, and 2013, respectively. He was a Postdoctoral Researcher at the Technical University of Denmark from 2011 to 2013 and is currently an Assistant Professor in the Department of Electrical Engineering, Technical University of Denmark. His current research interests include advanced magnetics design, modeling, and integration in switch-mode power supplies, dc/dc converters, and digital control in high-power reversible converters. He has more than 30 peer-reviewed journal and conference publications. He holds three US/EP/PCT patents.

Dr. Ouyang received the Chinese Government Award for Outstanding Ph.D. Students Abroad in 2010 and the Best Ph.D. Dissertation of the Year Award 2012 at the Technical University of Denmark. He received the Young Engnieer Award at PCIM Asia 2014 and Best Paper Awards in ECCE-Asia conferences in 2010 and 2012, respectively. He has served as a Session Chair in conferences and a Reviewer for the IEEE TRANSACTIONS ON POWER ELECTRONICS. He is Member of the IEEE Power Electronics Society, the IEEE Industrial Electronics Society, and the IEEE Magnetics Society.

Lars Press Petersen (M'14) received the master's degree in electrical engineering and the Ph.D. degree in power electronics from the Technical University of Denmark, Kongens Lyngby, Denmark, in 1999 and 2003, respectively.

In 2003, he joined Bang&Olufsen working with offline converters for Class D amplifiers. In 2008, he founded Upcon Technology A/S, a start-up company developing high-efficiency ac/dc converters for telecom and server applications. Since 2012, he has been with the Department of Electrical Engineering, Technical University of Denmark, where he is currently a Senior Researcher.

Arnold Knott (M'10) received the Diplom-Ingenieur (FH) degree from the University of Applied Sciences, Deggendorf, Germany, in 2004. In 2010, he received the Ph.D. degree from the Technical University of Denmark, Kongens Lyngby, Denmark, working on a research project under the title "Improvement of Out-of-Band Behaviour in Switch-Mode Amplifiers and Power Supplies by their Modulation Topology."

From 2004 until 2009, he has been working with Harman/Becker Automotive Systems GmbH in Germany and USA, designing switch-mode audio power amplifiers and power supplies for automotive applications. From 2010 to 2013, he was an Assistant Professor and, since 2013, has been an Associate Professor at the Technical University of Denmark. His research interests include switch-mode audio power amplifiers, power supplies, active and passive components, integrated circuit design, acoustics, radio frequency electronics, electromagnetic compatibility, and communication systems.

Ole C. Thomsen (M'06) received the B.S.E.E. degree in electronics from the Engineering Academy of Denmark, Kongens Lyngby, Denmark, in 1970.

He was as an RF R&D Engineer at Skandinavisk Teleindustri A/S from 1970 to 1976. From 1976 to 1980, he was the Power Electronic Project Manager in the Space Department at Christian Rovsing A/S. In 1980, he founded Powerlab A/S, operating within R&D and manufacturing of professional power electronic, and served as General Manager until 2004. From 2005 to 2013, he was with the Technical University of Denmark, Kongens Lyngby, where he was an Associate Professor. He is currently retired. His main research interests include switch-mode power supplies, power factor correction, and electromagnetic compatibility.

Michael A. E. Andersen (M'88) received the M.Sc.E.E. and Ph.D. degrees in power electronics from the Technical University of Denmark, Kongens Lyngby, Denmark, in 1987 and 1990, respectively.

He is currently a Professor of power electronics at the Technical University of Denmark. Since 2009, he has been Deputy Head of Department at the Department of Electrical Engineering. He is the author or coauthor of more than 200 publications. His research interests include switch-mode power supplies, piezoelectric transformers, power factor correction, and switch-mode audio power amplifiers.