Automatic Current Sharing of an Input-Parallel Output-Parallel (IPOP)-Connected DC–DC Converter System With Chain-Connected Rectifiers

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***Abstract*—Input-parallel output-parallel (IPOP)-connected converter systems allow the use of low-power converter modules for high-power applications. An IPOP converter topology with half-wave, daisy chain-connected rectifiers is presented which consists of multiple half-bridge (HB) dc–dc converter modules. By utilizing a common-duty-ratio control scheme, without a dedicated current-sharing controller, automatic sharing of input current and load current in the IPOP converter is achieved even in the presence of differences of more than 10% in various module parameters. The steady-state and dynamic-state current-sharing performance of the proposed IPOP converter is analyzed by using a steady-state dc model and a small-signal model of the system, respectively. It is concluded that steady-state current sharing among modules can be realized by applying a common-duty-ratio control scheme and by reducing the difference in transformer turn ratios, while dynamic-state current sharing is only slightly affected by substantial module parameter mismatches. The stability and current-sharing performance are verified by Saber simulation and an 800-W prototype consisting of two HB modules. The IPOP converter topology under the common-duty-ratio scheme can be extended to any system of three or more converter modules, including full-bridge dc–dc converters.**

***Index Terms*—Automatic sharing of currents, chain-connected rectifier, common-duty-ratio control, half-bridge (HB) dc–dc converters, input-parallel output-parallel (IPOP) connection, mismatches in various converter parameters.**

I. Introduction

CONNECTING modular dc–dc converters in parallel at the input and output terminals can be an efficient and reliable method to increase the power rating of converter, specifically the current rating [1]–[10]. Furthermore, the input-parallel output-parallel (IPOP)-connected converter system offers several advantages, namely [6]–[16]: 1) reduced magnetic component size, specifically transformers and inductors; 2) reduced component current stress by dividing the total power between converters; and 3) higher global efficiency, better thermal distribution, improved system reliability and power density.

The use of an IPOP converter system may be suitable for specific high-power applications, where individual converter modules operate in unison. However, parameter mismatch, such as transformers turn ratio mismatches, will introduce power imbalance problems between modules, which will cause inductor saturation, thermal stress imbalance, performance degradation, and possibly failure of some modules [17]–[21]. Hence, the challenge with an IPOP system is to ensure sharing of input and load current in the presence of quantifiable differences in module parameters.

Current-sharing techniques for IPOP converters have been extensively studied [9], [20]–[30]. The passive droop method and active current-sharing method are the most widely used sharing techniques [26]–[30]. Compared with the droop method, the active current-sharing technique can achieve a near perfect current distribution and better output-voltage regulation [22]. However, active current-sharing schemes are usually implemented with additional load-sharing circuitry based on output current sensing on each converter module. Consequently, the accuracy of these current control methods is affected by the inductor current sensing circuitry and the current sharing bus. Thus, active current-sharing control schemes involve increased controller complexity, leading to decreased overall system reliability.

In order to improve the overall system reliability and simplify the controller, some methods have been proposed for the automatic current sharing [21], [31]–[35]. A common-duty-ratio control scheme was presented for some input-serious output-parallel (ISOP) systems without dedicated control loop for input-voltage and load-current sharing, but still ensure the sharing of input voltage and load current, due to the inherent self-correcting characteristic of the ISOP connection [32]–[34]. However, the IPOP converter systems do not have the same inherent self-correcting characteristic as the ISOP systems. In IPOP systems, some methods must be taken to realize the automatic current sharing. Zhang *et al*. [32] presented a common-duty-ratio control scheme for an IPOP converter, which consists of two forward converters employing a common *LC* output filter. The same duty ratio is applied to all the converter modules. The scheme does not require an additional input or load current sharing controller, but is able to ensure equal sharing of the input and load currents among the modules. Wang *et al*. [35] presented an interleaved flyback-forward boost converter, in which the switching capacitors are used to balance the currents of the interleaved two modules without an additional current-sharing controller. Shi *et al*. [8] presented a common-duty-ratio control scheme for an IPOP connected converter system, which consists of two dual active full-bridge (FB) dc–dc converter modules, and by using a small-signal model and a steady-state dc model of the

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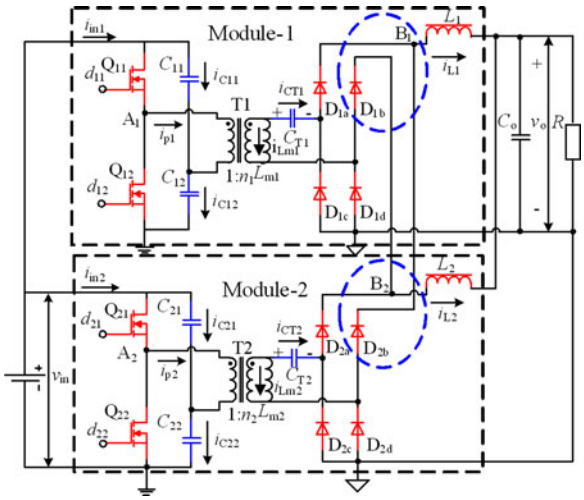

Fig. 1. Topology of IPOP converter system with chain-connected rectifiers, employing HB as basic modules.

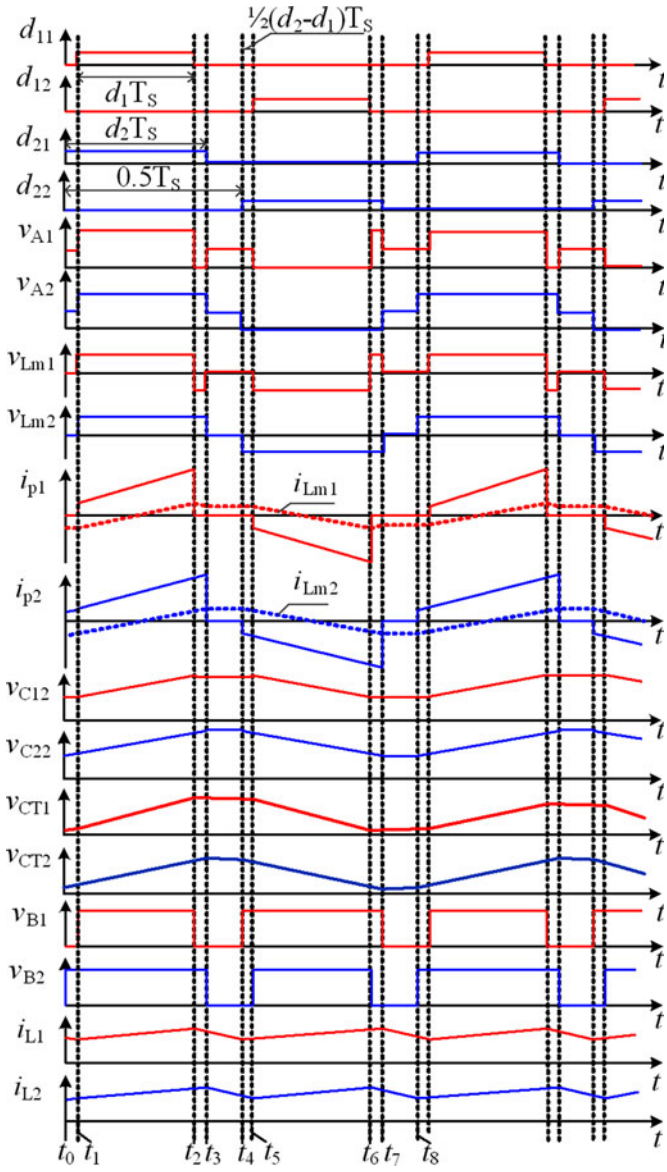

Fig. 2. Switching time sequence and main theoretical waveforms of the IPOP converter system with $d_1 \neq d_2$.

IPOP system, an automatic current-sharing mechanism is realized even in the presence of substantial parameter mismatching.

In this paper, an IPOP connected converter system with chain-connected rectifiers is proposed, which consists of two half-bridge (HB) dc–dc modules and operates in the continuous current model (CCM). By using a common-duty-ratio control scheme, without a dedicated control loop for current sharing, automatic current sharing can be achieved in the presence of substantial differences in various module parameters. The topology of the IPOP converter system and its operation modes are analyzed in Section II. In Section III, the system steady-state dc model is presented, and the steady-state current-sharing performance is analyzed in the presence of module parameter mismatch. In Section IV, the system small-signal model is deduced, and the dynamic-state current-sharing performance is analyzed in the presence of parameter mismatch. The simulation and experimental verification for the IPOP converter system are presented in Section V and Section VI, respectively. Finally, conclusions are presented in Section VII.

Additionally, automatic current sharing can be achieved in any IPOP converter systems with half-wave, daisy chain-connected rectifiers, which consist of multiple (three or more) modules, and said modules include FB dc–dc converters.

II. Analysis for Topology of an IPOP Converter System

As shown in Fig. 1, the proposed IPOP converter system consists of two HB converter modules. The rectifier diodes and the filter inductors in the two modules are chain connected, with the cathode of diode D_{1b} in module-1 connected to the filter inductor L_2 in module-2, while the cathode of the diode D_{2b} in module-2 connected to the filter inductor L_1 in module-1. Additionally, capacitors C_{T1} and C_{T2} are connected in series with the secondary winding of transformers T_1 and T_2, respectively. The capacitors C_{T1} and C_{T2} isolate dc voltages resulting from different direct-current equivalent resistances in the two module rectifiers, and thereby ensure that the average values of the magnetizing currents in two transformers T_1 and T_2 are zero.

For the analysis convenience, the following terms are defined (The reference directions of all the current and voltage variables are shown in Fig. 1):

v_{in}: input voltage of the IPOP converter system;

v_o: output voltage of the IPOP converter system;

C_o: output-filter capacitor;

C_{T1}, C_{T2}: series capacitors of module-1 and module-2, respectively;

$C_{jk}(j=1,2;k=1,2)$: HB capacitors of module-j $(j=1,2)$;

$Q_{jk}(j=1,2;k=1,2)$: power switches of module-j $(j=1,2)$;

$D_{jm}(j=1,2;m=a,b,c,d)$: rectifier diodes of module-j $(j=1,2)$;

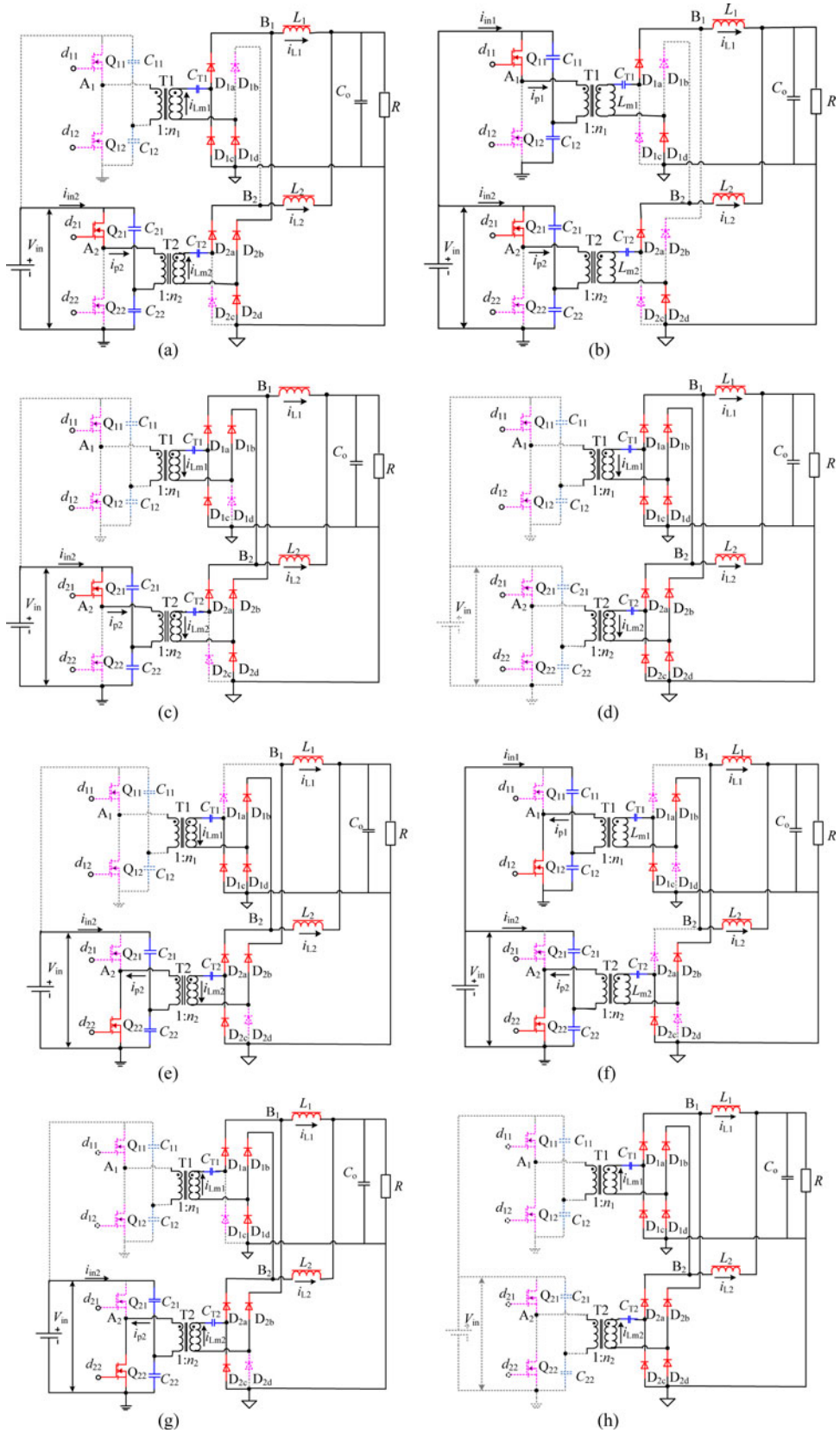

Fig. 3. Converter system CCM operating stages with $d_1 \neq d_2$. (a) Stage 1 $[t_0, t_1]$. (b) Stage 2 $[t_1, t_2]$. (c) Stage 3 $[t_2, t_3]$. (d) Stage 4 $[t_3, t_4]$. (e) Stage 5 $[t_4, t_5]$. (f) Stage 6 $[t_5, t_6]$. (g) Stage 7 $[t_6, t_7]$. (h) Stage 8 $[t_7, t_8]$.

T_1, T_2: transformers of module-1 and module-2, respectively;

L_1, L_2: output-filter inductors of module-1 and module-2, respectively;

L_{m1}, L_{m2}: magnetizing inductors of T_1 and T_2, respectively;

i_{in1}, i_{in2}: input currents of module-1 and module-2, respectively;

i_{p1}, i_{p2}: primary currents of T_1 and T_2, respectively;

$i_{L_{m1}}$, $i_{L_{m2}}$: currents through L_{m1} and L_{m2}, respectively;

$i_{C_{T1}}$, $i_{C_{T2}}$: currents through C_{T1} and C_{T2}, respectively;

i_{L_1}, i_{L_2}: currents through L_1 and L_2, respectively;

$d_{jk}(j = 1, 2; k = 1, 2)$: the high-frequency square-wave signals for driving $Q_{jk}(j = 1, 2; k = 1, 2)$;

d_1, d_2: real duty cycles for the power switches in module-1 and module-2, respectively;

n_1, n_2: turns ratios of T_1 and T_2, respectively.

A common-duty-ratio control scheme is used for the IPOP converter system by applying the same drive signals to Q_{11} and Q_{21} and the same drive signals to Q_{12} and Q_{22}, with the power switches (e.g., Q_{11} and Q_{12}) in each modules operating with the same switch duty ratio *d*, which is less than 0.5 but phase shifted by 180°. However, as a result of the mismatch in characteristics of the gate-drive-circuitry or/and power switches in the various modules, the real duty ratios of the power switches (e.g., Q_{11} and Q_{21}) in individual modules may be slightly different. The IPOP converter system operation for $d_1 \neq d_2$ is different and more complicated than when $d_1 = d_2$. Hence, we analyze the general IPOP converter system operational mode where $d_1 \neq d_2$. So, as shown in Fig. 2, it is assumed that the duty ratios of the power switches in module-2 are larger than those in module-1, namely $d_2 > d_1$. This means that the power switches in module-2 turn on earlier than the corresponding power switches in module-1 for $1/2(d_2 - d_1)T_S$, and that the power switches in module-2 turn off later than the corresponding ones in module-1 for $1/2(d_2 - d_1)T_S$. The switching time sequence and the main theoretical waveforms for the IPOP converter system when $d_1 \neq d_2$ are shown in Fig. 2, where v_{A1} is the voltage between the point A_1 (as marked in Fig. 1) and input ground, and v_{A2} is the voltage between point A_2 (as marked in Fig. 1) and input ground; $v_{L_{m1}}$ and $v_{L_{m2}}$ are the voltages across L_{m1} and L_{m2}, respectively; $v_{C_{12}}$ and $v_{C_{22}}$ are the voltages across C_{12} and C_{22}, respectively; $v_{C_{T1}}$ and $v_{C_{T2}}$ are the voltages across C_{T1} and C_{T2}, respectively; v_{B1} is the voltages between point B_1 (as marked in Fig. 1) and output ground, and v_{B2} is the voltages between the point B_2 (as marked in Fig. 1) and output ground; T_S is the switching period of the converter system. Additionally, the voltage waveforms of C_{T1} and C_{T2} shown in Fig. 2 is one of the cases, since the average values of $v_{C_{T1}}$ and $v_{C_{T2}}$ can be positive or negative. They are determined by the direct-current equivalent resistances in the two module rectifiers.

To simplify the circuit analysis, it is assumed that the IPOP converter operates in a CCM. In practical applications, $C_{11} \approx C_{12}$ and $C_{21} \approx C_{22}$, but it is assumed that $C_{11} = C_{12}$ and $C_{21} = C_{22}$ for analysis convenience.

Based on the aforementioned assumptions, there are eight operating modes to be considered within one switching period under CCM and $d_1 \neq d_2$ operation. Because of CCM operation, the continuous inductor current ensures that release of the magnetizing current energy manifests itself in the secondary circuit, wherein the inductor voltage adjust to realize a lower effective potential than would be seen by the magnetizing energy being released in the primary side. Fig. 2 illustrates the typical waveforms and Fig. 3 shows topological stages of the proposed converter. The operating modes are described as follows.

A. Stage 1 [t_0–t_1]

At $t = t_0$, the power switch Q_{21} turns on, thereby commutating off diodes D_{1b} and D_{2c}. Energy stored in C_{21}, provided by the input dc source, is delivered to L_2 and the load through T_2. Meanwhile, the power switches in module-1 are both OFF, with D_{1a} and D_{1c}, as well as D_{2b} and D_{2d}, freewheeling, releasing the energy stored in L_1. The magnetizing energy stored in L_{m1} is transferred to C_{T1}, L_1 and the load via D_{1a} and D_{1d}. This stage operates until t_1 when Q_{11} is turned on, for $1/2(d_2 - d_1)T_S$. During this stage, the input current of module-1 and the currents through C_{11} and C_{12} are zero; the input current of module-2 and the currents through C_{21} and C_{22} are

$$i_{in2} = -i_{C21} = i_{C22} = \frac{1}{2} n_2 (i_{Lm2} + i_{L2}). \tag{1}$$

B. Stage 2 [t_1–t_2]

At $t = t_1$, Q_{11} turns on, and therefore, D_{1c} and D_{2b} turn off. Meanwhile, through D_{1a} and D_{1d} in module-1, the input dc source provides energy for L_1 and the load; via D_{2a} and D_{2d} in module-2, the input dc source transfers energy to L_2 and the load. The transformers T_1 and T_2 are both positively excited, and $i_{L_{m1}}$ and $i_{L_{m2}}$ flow through the primary side of the respective transformers T_1 and T_2. For $d_1 T_S$, this stage operates until t_2 when Q_{11} turns off. During this stage, the currents through C_{11}, C_{12}, C_{21} and C_{22}, and the input currents of module-1and module-2 are

$$i_{in1} = -i_{C11} = i_{C12} = \frac{1}{2} n_1 (i_{Lm1} + i_{L1}) \tag{2}$$

$$i_{in2} = -i_{C21} = i_{C22} = \frac{1}{2} n_2 (i_{Lm2} + i_{L2}). \tag{3}$$

C. Stage 3 [t_2–t_3]

At $t = t_2$, Q_{11} is switched off, thereby D_{1d} is reversed-biased and turned off; D_{1a} and D_{1c}, as well as D_{2b} and D_{2d}, serve as freewheel diodes for releasing the energy stored in L_1. D_{1b} and D_{1c} provide a path for the magnetizing current $i_{L_{m1}}$. Meanwhile, module-1 stops transferring energy from the input dc source to the load; module-2 continues providing energy from the dc source to L_2 and the load, with diodes D_{2a} and D_{2d} acting as rectifier diodes. For $1/2(d_2 - d_1)T_S$, this stage operates until t_3, when Q_{21} is switched off. During this stage, the currents through C_{11} and C_{12} and the input currents of module-1 are zero. The input currents of module-2 and the currents through C_{21} and C_{22} are given by

$$i_{in2} = -i_{C21} = i_{C22} = \frac{1}{2} n_2 (i_{L2} + i_{Lm2} - i_{Lm1}). \tag{4}$$

D. Stage 4 [t_3–t_4]

At $t = t_3$, all the power switches are switched off, thereby all the rectifier diodes freewheel the magnetizing currents of T_1 and T_2, through L_1 and L_2. Meanwhile, the currents through C_{11}, C_{12}, C_{21}, C_{22} and the input currents of both modules are zero. For $(1/2 - d_2)\mathrm{T}_S$, this stage operates until $t = t_4$, when Q_{22} is turned on.

E. Stage 5 [t_4–t_5]

At $t = t_4$, Q_{22} in module-2 turns on, thereby turning off $D_{1\mathrm{a}}$ and $D_{2\mathrm{d}}$. The energy stored in C_{22} and provided by the input dc source is delivered to L_2 and the load through T_2. Meanwhile, the power switches in module-1 remain off, with $D_{2\mathrm{a}}$ and $D_{2\mathrm{c}}$, as well as $D_{1\mathrm{b}}$ and $D_{1\mathrm{d}}$, serving as freewheel diodes for releasing the energy stored in L_2. The energy stored in $L_{\mathrm{m}1}$ is transferred to $C_{\mathrm{T}1}$, L_2 and load via the diodes $D_{1\mathrm{b}}$ and $D_{1\mathrm{c}}$. This stage continues until t_5 when Q_{12} in module-1 is turned on, for $1/2(d_2 - d_1)\mathrm{T}_S$. During this stage, the currents through C_{11} and C_{12} and the input current of module-1 are zero, while the currents through C_{21} and C_{22} and the input currents of module-2 are

$$i_{\mathrm{in}2} = i_{C21} = -i_{C22} = \frac{1}{2}n_2(i_{L1} - i_{L\mathrm{m}2}). \tag{5}$$

F. Stage 6 [t_5–t_6]

At $t = t_5$, Q_{12} is turned on, and therefore, $D_{1\mathrm{c}}$ and $D_{2\mathrm{a}}$ are turned off. Meanwhile, through $D_{1\mathrm{b}}$ and $D_{1\mathrm{c}}$ in module-1, the input dc source provides energy for L_2 and the load; via $D_{2\mathrm{a}}$ and $D_{2\mathrm{d}}$ in module-2. The input dc source delivers energy to L_1 and the load. T_1 and T_2 are both negatively excited, and $i_{L_{\mathrm{m}1}}$ and $i_{L_{\mathrm{m}2}}$ flow through the primary side of the respective transformers T_1 and T_2. For $d_1\mathrm{T}_S$, this stage operates until t_6 when Q_{12} turns off. During this stage, the currents through C_{11}, C_{12}, C_{21}, and C_{22}, and the input currents of module-1and module-2 are

$$i_{\mathrm{in}1} = \ i_{C11} = -i_{C12} = \frac{1}{2}n_1(i_{L2} - i_{L\mathrm{m}1}) \tag{6}$$

$$i_{\mathrm{in}2} = \ i_{C21} = -i_{C22} = \frac{1}{2}n_2(i_{L1} - i_{L\mathrm{m}2}). \tag{7}$$

G. Stage 7 [t_6–t_7]

At $t = t_6$, Q_{12} is switched off. Thus, $D_{1\mathrm{d}}$ is reversed-biased and turned off; $D_{1\mathrm{b}}$ and $D_{1\mathrm{d}}$, as well as $D_{2\mathrm{a}}$ and $D_{2\mathrm{c}}$, serve as the freewheel diodes for releasing the energy stored in L_2. $D_{1\mathrm{a}}$ and $D_{1\mathrm{d}}$ provide a path for $i_{L_{\mathrm{m}1}}$. Meanwhile, the module-1 stops transferring energy from the input dc source to the load; module-2 continues delivering energy from the dc source to L_1 and the load, with $D_{2\mathrm{b}}$ and $D_{2\mathrm{c}}$ serving as rectifier diodes. For $1/2(d_2 - d_1)\mathrm{T}_S$, this stage operates until t_7, when Q_{22} is switched off. During this stage, the currents through C_{11} and C_{12} and the input current of module-1 are zero, the input currents of module-2 and the currents through C_{21} and C_{22} are

$$i_{\mathrm{in}2} = i_{C21} = -i_{C22} = \frac{1}{2}n_2(i_{L1} + i_{L\mathrm{m}1} - i_{L\mathrm{m}2}). \tag{8}$$

H. Stage 8 [t_7–t_8]

At $t = t_7$, all the power switches are switched off, whereby all the rectifier diodes circulate the magnetizing currents of T_1 and T_2, and the currents in L_1 and L_2. Meanwhile, the currents through C_{11}, C_{12}, C_{21}, and C_{22}, and the input currents of both modules are zero. For $(1/2 - d_2)\mathrm{T}_S$, this stage operates until $t = t_8$, when Q_{21} is turned on in the new switching period.

For $d_1 = d_2$, there will be four operational stages during one switching period, namely stages of second, fourth, sixth, and eighth.

III. Steady-State Current-Sharing Analysis of the IPOP Converter System

The objective for each module in an IPOP converter to transfer power evenly can be realized by ensuring equal sharing of input current and output current. Thus, in steady-state operation of the IPOP converter shown in Fig. 1, the input and output current sharing in the two modules must be ensured even in the presence of substantial mismatch of various module parameters, such as duty ratios, transformer turn ratios, and filter inductances.

From the topology shown in Fig. 1, the chain-connected rectifier breaks traditional rectifier structure, flipping half a rectified current to another HB converter. The output inductor current receives half-cycle current from the module itself and another half-cycle current from the other module. Moreover, load current sharing is realized depending on the charge balance of the blocking capacitors on the secondary side of transformers.

During the time interval of each operating stage in a switching period, the IPOP converter can be represented by a set of linear state-space equations. For the eight operating stages in a switching period, the corresponding eight sets of state-space equations are

$$\begin{cases} \dot{x} = A_i m \ \ (i = 1, \ldots, 8) \\ y = B_i m \ (i = 1, \ldots, 8) \end{cases} \tag{9}$$

where

$$\dot{x} = \begin{bmatrix} (C_{11} + C_{12})\frac{dv_{C12}}{dt} \\ (C_{21} + C_{22})\frac{dv_{C22}}{dt} \\ C_{\mathrm{T}1}\frac{dv_{C\mathrm{T}1}}{dt} \\ C_{\mathrm{T}2}\frac{dv_{C\mathrm{T}2}}{dt} \end{bmatrix}^{\mathrm{T}}$$

$$m = \begin{bmatrix} i_{L\mathrm{m}1} & i_{L\mathrm{m}2} & i_{L1} & i_{L2} \end{bmatrix}^{\mathrm{T}}, \quad y = \begin{bmatrix} i_{\mathrm{in}1} & i_{\mathrm{in}2} \end{bmatrix}^{\mathrm{T}}$$

and A_1–A_8 and B_1–B_8 are the system matrices for each operational stage, as shown, respectively, in Fig. 3, and are expressed as

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & n_2 & 0 & n_2 \\ -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}, \ B_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & \frac{n_2}{2} & 0 & \frac{n_2}{2} \end{bmatrix} \tag{9.1}$$

$$A_2=\begin{bmatrix} n_1 & 0 & n_1 & 0 \\ 0 & n_2 & 0 & n_2 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix},\ B_2=\begin{bmatrix} \frac{n_1}{2} & 0 & \frac{n_1}{2} & 0 \\ 0 & \frac{n_2}{2} & 0 & \frac{n_2}{2} \end{bmatrix} \tag{9.2}$$

$$A_3=\begin{bmatrix} 0 & 0 & 0 & 0 \\ -n_2 & n_2 & 0 & n_2 \\ -1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 1 \end{bmatrix},\ B_3=\begin{bmatrix} 0 & 0 & 0 & 0 \\ -\frac{n_2}{2} & \frac{n_2}{2} & 0 & \frac{n_2}{2} \end{bmatrix} \tag{9.3}$$

$$A_4=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix},\quad B_4=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{9.4}$$

$$A_5=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & n_2 & -n_2 & 0 \\ -1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 \end{bmatrix},\quad B_5=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & -\frac{n_2}{2} & \frac{n_2}{2} & 0 \end{bmatrix} \tag{9.5}$$

$$A_6=\begin{bmatrix} n_1 & 0 & 0 & -n_1 \\ 0 & n_2 & -n_2 & 0 \\ 0 & 0 & 0 & -1 \\ 0 & 0 & -1 & 0 \end{bmatrix}$$
$$B_6=\begin{bmatrix} -\frac{n_1}{2} & 0 & 0 & \frac{n_1}{2} \\ 0 & -\frac{n_2}{2} & \frac{n_2}{2} & 0 \end{bmatrix} \tag{9.6}$$

$$A_7=\begin{bmatrix} 0 & 0 & 0 & 0 \\ -n_2 & n_2 & -n_2 & 0 \\ -1 & 0 & 0 & 0 \\ -1 & 0 & -1 & 0 \end{bmatrix}$$
$$B_7=\begin{bmatrix} 0 & 0 & 0 & 0 \\ \frac{n_2}{2} & -\frac{n_2}{2} & \frac{n_2}{2} & 0 \end{bmatrix} \tag{9.7}$$

$$A_8=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix},\quad B_8=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}. \tag{9.8}$$

The intrinsic concept of the state-space averaging method is the replacement of the above eight sets of state-space equations by a single equivalent set of state-space equation as follows [36]:

$$\begin{cases} \dot{x}=Am \\ y=Bm \end{cases} \tag{10}$$

where the equivalent matrixes are defined as follows:

$$\begin{aligned} A=&\ \frac{1}{2}(d_2-d_1)A_1+d_1A_2+\frac{1}{2}(d_2-d_1)A_3 \\ &+\left(\frac{1}{2}-d_2\right)A_4+\frac{1}{2}(d_2-d_1)A_5+d_1A_6 \\ &+\frac{1}{2}(d_2-d_1)A_7+\left(\frac{1}{2}-d_2\right)A_8 \end{aligned} \tag{10.1}$$

$$\begin{aligned} B=&\ \frac{1}{2}(d_2-d_1)B_1+d_1B_2+\frac{1}{2}(d_2-d_1)B_3 \\ &+\left(\frac{1}{2}-d_2\right)B_4+\frac{1}{2}(d_2-d_1)B_5+d_1B_6 \\ &+\frac{1}{2}(d_2-d_1)B_7+\left(\frac{1}{2}-d_2\right)B_8. \end{aligned} \tag{10.2}$$

Thereby, with ac variables replaced by dc ones through capital letters, the steady-state equations can be obtained by setting $\dot{x}=0$ as follows:

$$\begin{aligned} \dot{x}=&\begin{bmatrix} (C_{11}+C_{12})\frac{dV_{C12}}{dt} \\ (C_{21}+C_{22})\frac{dV_{C12}}{dt} \\ C_{\mathrm{T}1}\frac{dV_{C\mathrm{T}1}}{dt} \\ C_{\mathrm{T}2}\frac{dV_{C\mathrm{T}2}}{dt} \end{bmatrix} \\ =&\begin{bmatrix} 2n_1D_1 & 0 & n_1D_1 & -n_1D_1 \\ n_2(D_1-D_2) & 2n_2D_2 & -n_2D_2 & n_2D_2 \\ 2D_1-1 & 0 & D_1 & -D_1 \\ D_1-D_2 & 2D_2-1 & -D_2 & D_2 \end{bmatrix} \\ &\begin{bmatrix} I_{L\mathrm{m}1} \\ I_{L\mathrm{m}2} \\ I_{L1} \\ I_{L2} \end{bmatrix}=\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \end{aligned} \tag{11}$$

$$\begin{aligned} Y=&\begin{bmatrix} I_{\mathrm{in}1} \\ I_{\mathrm{in}2} \end{bmatrix}=\begin{bmatrix} 0 & 0 & \frac{D_1n_1}{2} & \frac{D_1n_1}{2} \\ 0 & 0 & \frac{D_2n_2}{2} & \frac{D_2n_2}{2} \end{bmatrix}\begin{bmatrix} I_{L\mathrm{m}1} \\ I_{L\mathrm{m}2} \\ I_{L1} \\ I_{L2} \end{bmatrix} \\ =&\begin{bmatrix} \frac{D_1n_1(I_{L1}+I_{L2})}{2} \\ \frac{D_2n_2(I_{L1}+I_{L2})}{2} \end{bmatrix}. \end{aligned} \tag{12}$$

From (11), the steady-state dc operational points for the IPOP converter system can be derived as follows:

$$n_1D_1(I_{L1}-I_{L2}+2I_{\mathrm{Lm}1})=0 \tag{13}$$

$$n_2D_2(I_{L2}-I_{L1}+2I_{\mathrm{Lm}2})-n_2I_{\mathrm{Lm}1}(D_2-D_1)=0 \tag{14}$$

$$D_1(I_{L1}-I_{L2})-I_{\mathrm{Lm}1}(1-2D_1)=0 \tag{15}$$

$$D_2(I_{L2}-I_{L1})-(1-2D_2)I_{\mathrm{Lm}2}-I_{\mathrm{Lm}1}(D_2-D_1)=0. \tag{16}$$

From (13) and (15), the dc currents through the magnetizing inductor L_{m1} can be derived as follows:

$$I_{\mathrm{Lm}1}=0. \tag{17}$$

From (14) and (16), the dc currents through the magnetizing inductor L_{m2} is

$$I_{\mathrm{Lm2}} = 0. \tag{18}$$

From (15) to (18), the dc currents through the filter inductors L_1 and L_2 are as follows:

$$I_{L1} = I_{L2}. \tag{19}$$

From (17) to (19), it can be concluded: 1) the dc currents through the magnetizing inductors L_{m1} and L_{m2} are always zero, which means no magnetic saturation in the transformers T_1 and T_2; 2) the average currents through the filter inductors L_1 and L_2 are always equal, which illustrates that the proposed IPOP converter system can achieve equal sharing of output currents even in the presence of substantial mismatches in various module parameters, such as duty ratios, transformer turns ratios, etc.

The previous analysis is based on the charge balance of the capacitors, and furthermore, the voltage second balances of output inductors are well met too. As shown in Figs. 2 and 3, during a switching period, the inductor current is made up of two different rectified half-cycle currents. Thus, the switching period can be divided into two intervals. In the first interval, inductor current is from the module itself; in the other interval, the inductor current is from another module. Therefore, the voltage second balance of output inductors is met over the whole switching period, although it is not met in one interval.

From (12), the ratio of differences between input currents of two modules to total input currents is defined and derived as follows:

$$\frac{\Delta I_{\mathrm{in}}}{I_{\mathrm{in}}} = \frac{I_{\mathrm{in1}} - I_{\mathrm{in2}}}{I_{\mathrm{in1}} + I_{\mathrm{in2}}} = \frac{D_1 n_1 - D_2 n_2}{D_1 n_1 + D_2 n_2} \tag{20}$$

where I_{in} is the total input current provided by the input dc source.

For the convenience of analysis, defining $\Delta D = D_2 - D_1$ and $\Delta n = n_2 - n_1$, and considering the condition $\Delta D \ll D_1$ and $\Delta n \ll n_1$ is viable in practice, the following equation can be derived from (20):

$$\begin{aligned} \frac{\Delta I_{\mathrm{in}}}{I_{\mathrm{in}}} &= \frac{D_1 n_1 - (D_1 + \Delta D)(n_1 + \Delta n)}{D_1 n_1 + (D_1 + \Delta D)(n_1 + \Delta n)} \\ &\approx -\frac{1}{2}\left(\frac{\Delta D}{D} + \frac{\Delta n}{n}\right). \end{aligned} \tag{21}$$

In (21), for matched duty ratios and turn ratios (namely, $\Delta D = 0$ and $\Delta n = 0$), $I_{\mathrm{in1}} = I_{\mathrm{in2}}$ results, indicating that steady-state sharing of input currents is realized. Furthermore, duty ratio and/or turn ratio mismatch (namely, $\Delta D \neq 0$ and/or $\Delta n \neq 0$) have a little effect on the steady-state sharing of input currents. However, with advanced modern transformer manufacturing techniques, such as planar transformers with printed windings, transformer turn ratio mismatch can be negligible. By using dedicated gate driving circuitry and choosing power switches with similar junction capacitance, duty ratio mismatch can also be made negligible.

From the aforementioned analysis, equal sharing of load current in the proposed IPOP system can be achieved, even with various module parameter mismatches. The equal sharing of input current in the IPOP converter system can be achieved by using a common-duty-ratio control scheme and by reducing mismatch of transformer turn ratios, which is viable in practice.

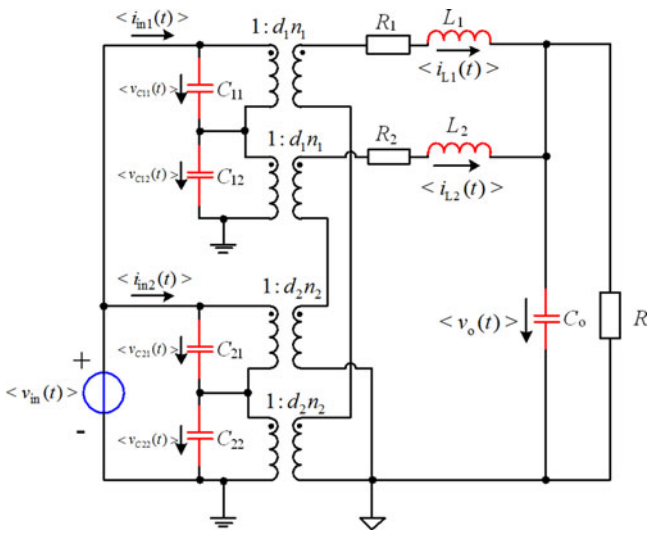

Fig. 4. Large-signal equivalent circuit model of the IPOP converter.

IV. Dynamic Current Sharing Analysis of the IPOP Converter System

During IPOP converter starting or with a step change in input voltage or/and load current occurs, one of the two converter modules may take higher current, which may exceed the current ratings of switching devices leading to damage of the associated module. Hence, it is necessary to analyze the dynamic sharing of currents in the presence of various module parameter mismatches.

A. Proposed IPOP Converter System Model Derivation

In order to study the dynamic current-sharing performance of the IPOP system, its small-signal average model must be considered. As the magnetizing currents $i_{\mathrm{L}_{m1}}$ and $i_{L_{\mathrm{m2}}}$ are relatively small compared to i_{L_1} and i_{L_2}, they can be neglected. Similarly, since the voltages across C_{T1} and C_{T2} are much smaller than $v_{C_{12}}$ and $v_{C_{22}}$, which are the voltages across C_{12} and C_{22}, they are also neglected. Based on the averaged switch modeling, the large signal (average mode) equivalent circuit of the IPOP converter system is derived, as shown in Fig. 4, where the equivalent resistors R_1 and R_2 indicate the dc resistance of inductors L_1 and L_2, respectively. This average model is valid even for large-scale transfers such as step changes in input voltage or load current, and furthermore, the time-domain simulations, to be presented in Section V, are also obtained from the model.

Fig. 5(a) shows the small-signal equivalent circuit for the IPOP converter system, which is derived from the large signal equivalent circuit (shown in Fig. 4) and linearized around a specific operating condition (specifically input voltage V_{in}, output voltage V_{o}, and steady-state duty ratios D_1 and D_2). To simplify analysis, it is assumed that the capacitance of the

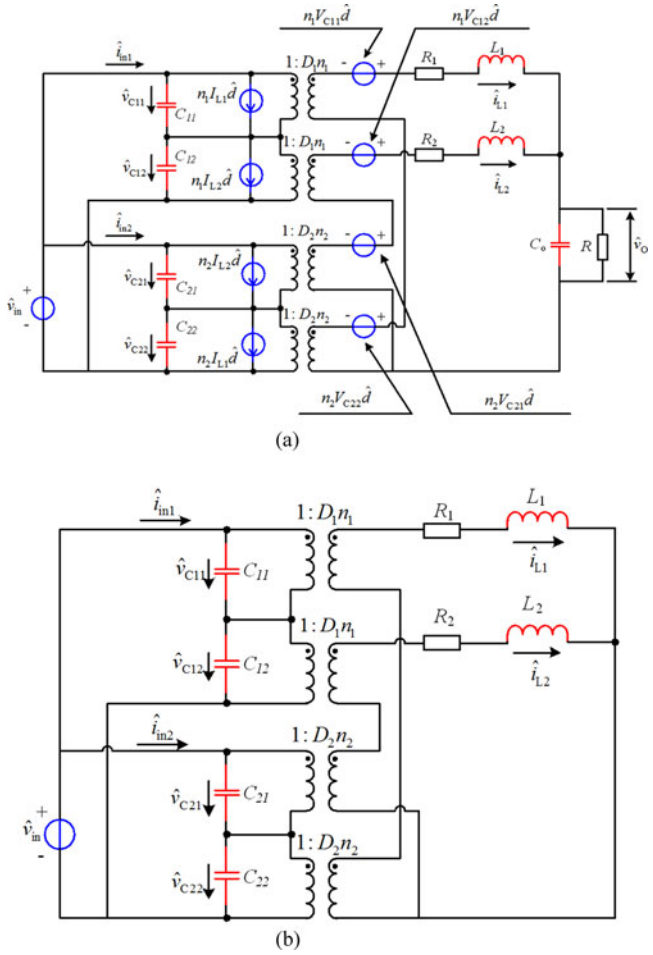

Fig. 5. Models for the IPOP converter. (a) Small-signal equivalent circuit model. (b) Simplified small-signal equivalent circuit model.

output capacitor C_o is large, and an ideal fast output-voltage controller is used. Thus, the perturbations in output voltage $\hat{v}_O$ can be neglected, when analyzing current-sharing under condition of small-signal perturbation in input voltage and load current. Therefore, Fig. 5(b) shows the simplified small-signal equivalent circuit for the IPOP converter system.

B. Analysis of Dynamic Sharing of Output Current With Input-Voltage Disturbance

In practical applications, $C_{11} \approx C_{12}$ and $C_{21} \approx C_{22}$. For the convenience of analysis, it is assumed that $C_{11} = C_{12}$, $C_{21} = C_{22}$, $C_1 = C_{11} + C_{12}$, and $C_2 = C_{21} + C_{22}$.

From the small-signal model in Fig. 5(b), the input voltage to inductor-current transfer function for each module can be derived as shown (22) and (23), at the bottom of the page.

Subtracting (23) from (22), the transfer function for the IPOP system is derived as shown (24), at the bottom of the page.

Equation (24) is equal to zero as the respective parameters in individual modules are the same. Therefore, the two modules share the output currents in the presence of various module parameter matches.

According to the initial-value theorem, the initial value of the step response of $G_1(s)$ is derived from (24), and is

$$\begin{aligned}[\mathrm{i}_{L1}(t) - \mathrm{i}_{L2}(t)]\,|_{t=0+} &= \lim_{\mathrm{s}\to\infty} s \cdot \mathrm{G}_1(\mathrm{s}) \cdot \tfrac{1}{\mathrm{s}} \\ &= \lim_{\mathrm{s}\to\infty} \tfrac{C_1C_2(L_1-L_2)(D_1n_1+D_2n_2)}{2C_1C_2L_1L_2\mathrm{s}} = 0. \end{aligned} \tag{25}$$

Expression (25) shows that, even in the presence of substantial module parameter mismatches, equal sharing of load current is achieved at $t = 0+$ during the step response.

$$\frac{\hat{i}_{L1}}{\hat{v}_{\mathrm{in}}} = \frac{(D_1n_1+D_2n_2)\cdot(C_1C_2L_2s^2+C_1C_2R_2s+2C_2D_1^2n_1^2+2C_1D_2^2n_2^2)}{2C_1C_2L_1L_2s^3+2C_1C_2(L_1R_2+L_2R_1)s^2+[(2C_1D_2^2n_2^2+2C_2D_1^2n_1^2)(L_1+L_2)+2C_1C_2R_1R_2]s+(2C_1D_2^2n_2^2+2C_2D_1^2n_1^2)(R_1+R_2)} \tag{22}$$

$$\frac{\hat{i}_{L2}}{\hat{v}_{\mathrm{in}}} = \frac{(D_1n_1+D_2n_2)\cdot(C_1C_2L_1s^2+C_1C_2R_1s+2C_2D_1^2n_1^2+2C_1D_2^2n_2^2)}{2C_1C_2L_1L_2s^3+2C_1C_2(L_1R_2+L_2R_1)s^2+[(2C_1D_2^2n_2^2+2C_2D_1^2n_1^2)(L_1+L_2)+2C_1C_2R_1R_2]s+(2C_1D_2^2n_2^2+2C_2D_1^2n_1^2)(R_1+R_2)} \tag{23}$$

$$G_1(s) = \frac{\hat{i}_{L1}-\hat{i}_{L2}}{\hat{v}_{\mathrm{in}}} = \frac{C_1C_2(L_1-L_2)(D_1n_1+D_2n_2)s^2+(R_1-R_2)(D_1n_1+D_2n_2)s}{2C_1C_2L_1L_2s^3+2C_1C_2(L_1R_2+L_2R_1)s^2+[(2C_2D_1^2n_1^2+2C_1D_2^2n_2^2)(L_1+L_2)+2C_1C_2R_1R_2]s+(2C_1D_2^2n_2^2+2C_2D_1^2n_1^2)(R_1+R_2)} \tag{24}$$

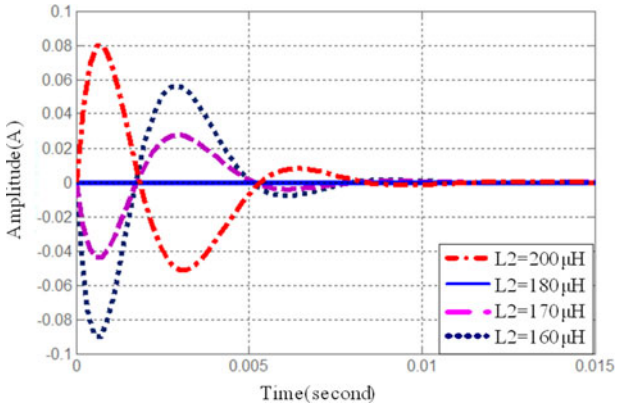

Fig. 6. Step response of $G_1(s)$ with difference in output-filter inductances ($L_1 = 180\ \mu$H).

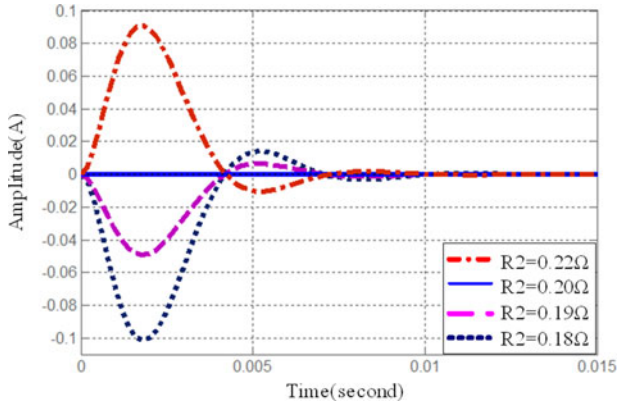

Fig. 7. Step response of $G_1(s)$ with difference in individual module equivalent resistances ($R_1 = 0.2\ \Omega$).

Similarly, the terminal value of the step response of $G_1(s)$ can be derived through the terminal-value theorem and is

$$[i_{L1}(t) - i_{L2}(t)]\,|_{t=\infty} = \lim_{s\to 0} s \cdot G_1(s) \cdot \frac{1}{s}$$
$$= \lim_{s\to 0} \frac{(R_1 - R_2)(D_1 n_1 + D_2 n_2)\cdot s}{(2C_1 D_2^2 n_2^2 + 2C_2 D_1^2 n_1^2)(R_1 + R_2)} = 0. \quad (26)$$

Equation (26) shows that the differences between the currents through the filter inductors L_1 and L_2 converges to zero in time. Therefore, it is concluded that module parameter mismatches do not affect the steady-state sharing of the output current, which is as concluded from (19) in Section III.

However, from (24), the differences between i_{L_1} and i_{L_2} may not be zero when $L_1 \neq L_2$ or/and $R_1 \neq R_2$, which means that the mismatches in other parameters have no effect on output current sharing when $L_1 \neq L_2$ and $R_1 \neq R_2$. Thus, the conditions $L_1 \neq L_2$ or/and $R_1 \neq R_2$ needed further analysis.

A typical IPOP converter is now considered with the following parameters: $V_{\text{in}} = 85$ V, $V_o = 36$ V, $I_o = 13.5$ A, $n_1 = n_2 = 6:9 = 1.5$, $D_1 = D_2 = 0.33$, $L_{m1} = L_{m2} = 1000\ \mu$H, $L_1 = L_2 = 180\ \mu$H, $C_{T1} = C_{T2} = 40\ \mu$F, $C_{11} = C_{12} = C_{21} = C_{22} = 2000\ \mu$F, $R_1 = R_2 = 0.2\ \Omega$, and a 60 kHz switching frequency.

First, only $L_1 \neq L_2$ is considered with other parameters identical. Fig. 6 shows the MATLAB simulated step response of $G_1(s)$, $i_{L1}(t) - i_{L2}(t)$, with filter inductance L_2 of 160, 170, 180, and 200 μH. Fig. 6 indicates that, even with a 10% filter inductance difference (e.g., $L_1 = 180\ \mu$H and $L_2 = 160\ \mu$H), the maximum step response of $G_1(s)$ is less than 0.1 A (1.5% mismatch).

Second, $R_1 \neq R_2$ is considered with other parameters matched. Fig. 7 shows the MATLAB simulated step response of $G_1(s)$, $i_{L1}(t) - i_{L2}(t)$, with effective resistances R_2 of 0.18, 0.19, 0.2, and 0.22 Ω. Fig. 7 indicates that, even with the difference of 10% in effective resistance (e.g., $R_1 = 0.2\ \Omega$ and $R_2 = 0.18\ \Omega$), the maximum step response of $G_1(s)$ is less than 0.1 A (1.5% mismatch).

From the aforementioned analysis, in the presence of various module parameter mismatches and input-voltage disturbance, the load-current sharing performance of the IPOP system achieves the following: 1) filter inductance mismatch slightly affects the dynamic sharing of output currents, but has no effect on the steady-state sharing of the output currents; 2) effective resistance mismatch is similar to filter inductance mismatch, which slightly affects current dynamic sharing, but has no effect on the steady-state current sharing; 3) with filter inductance and effective resistance match, other parameter mismatches do not affect output current dynamic sharing, and also have no effect on the steady-state output current sharing.

C. Analysis of Dynamic Sharing of Output Current With Load Current Step Change

From the small-signal model in Fig. 5(b), the IPOP converter system output transfer functions are derived as follows:

$$\frac{\hat{i}_{L1}}{\hat{i}_o} = \frac{C_1C_2L_2s^2 + C_1C_2R_2s + 2C_2D_1^2n_1^2 + 2C_1D_2^2n_2^2}{C_1C_2(L_1+L_2)s^2 + C_1C_2(R_1+R_2)s + 4C_2D_1^2n_1^2 + 4C_1D_2^2n_2^2} \quad (27)$$

$$\frac{\hat{i}_{L2}}{\hat{i}_o} = \frac{C_1C_2L_1s^2 + C_1C_2R_1s + 2C_2D_1^2n_1^2 + 2C_1D_2^2n_2^2}{C_1C_2(L_1+L_2)s^2 + C_1C_2(R_1+R_2)s + 4C_2D_1^2n_1^2 + 4C_1D_2^2n_2^2}. \quad (28)$$

Subtracting (28) from (27) yields

$$G_2(s) = \frac{\hat{i}_{L1} - \hat{i}_{L2}}{\hat{i}_o} = -\frac{C_1C_2(L_1-L_2)s^2 + C_1C_2(R_1-R_2)s}{C_1C_2(L_1+L_2)s^2 + C_1C_2(R_1+R_2)s + 4C_2D_1^2n_1^2 + 4C_1D_2^2n_2^2}. \quad (29)$$

From (29), the difference between i_{L_1} and i_{L_2} is zero when the respective module parameters are the same; hence, the two modules equally share the output currents with module parameter match.

However, from (29), the difference between i_{L_1} and i_{L_2} may not be zero when $L_1 \neq L_2$ or/and $R_1 \neq R_2$, which means that other parameter mismatches have no effect on load current

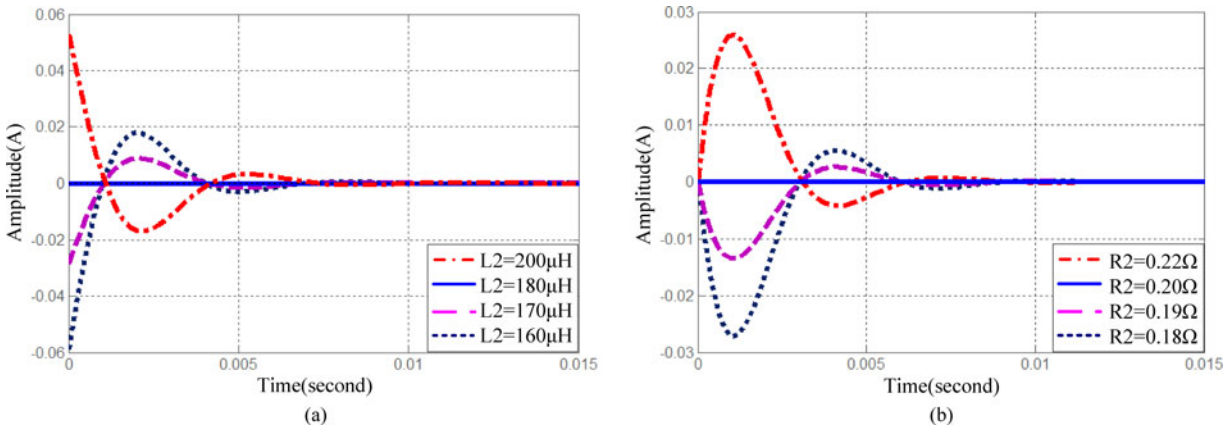

Fig. 8. Step response of $G_2(s)$ with differences in: (a) filter inductance ($L_1 = 180\,\mu$H) and (b) effective resistance ($R_1 = 0.2\,\Omega$).

sharing when $L_1 = L_2$ and $R_1 = R_2$. Hence, $G_2(s)$ needs analysis only for $L_1 \neq L_2$ or/and $R_1 \neq R_2$.

According to the initial-value theorem, the initial step response of $G_2(s)$ with $L_1 \neq L_2$ and/or $R_1 \neq R_2$ is

$$[i_{L1}(t) - i_{L2}(t)]\,|_{t=0+} = \lim_{s\to\infty} s \cdot G_2(s) \cdot \frac{1}{s} = \lim_{s\to\infty} G_2(s) = \frac{L_2 - L_2}{L_2 + L_2}. \tag{30}$$

Equation (30) indicates that output current sharing is only affected by the differences between filter inductances L_1 and L_2 at $t = 0+$ during a step-change in load current.

The final value of the step response of $G_2(s)$ with $L_1 \neq L_2$ or/and $R_1 \neq R_2$ can be derived from the terminal-value theorem and is

$$[i_{L1}(t) - i_{L2}(t)]\,|_{t=\infty} = \lim_{s\to 0} s \cdot G_2(s) \cdot \frac{1}{s} = \lim_{s\to 0} G_2(s) = 0. \tag{31}$$

From (31), it is shown that the differences between the currents through the filter inductors L_1 and L_2 converge to zero, even with various module parameter mismatches. Therefore, the various parameter mismatches do not affect steady-state output current sharing, which is the same as that concluded from (19) in Section III.

Fig. 8 shows the MATLAB simulated step response of $G_2(s)$, $i_{L1}(t) - i_{L2}(t)$, in the presence of filter inductance or effective resistance mismatch. Fig. 8 shows that the dynamic output current sharing is slightly affected by the differences in filter inductances or effective resistances. Near ideal filter inductor current sharing is achieved by minimizing module parameter mismatch, which is practically achievable.

From the aforementioned analysis, in the presence of various module parameter mismatches and load-current disturbance, the load-current sharing performance of the IPOP system is similar to that in Section IV-B.

D. Analysis of Dynamic Sharing of Input Current With Input-Voltage Disturbance

From the small-signal model in Fig. 5(b), the input current of each module is

$$\hat{i}_{\text{in}1} = \frac{1}{2} D_1 n_1 (\hat{i}_{L1} + \hat{i}_{L2}) \tag{32}$$

$$\hat{i}_{\text{in}2} = \frac{1}{2} D_2 n_2 (\hat{i}_{L1} + \hat{i}_{L2}). \tag{33}$$

From (22), (23), (32), and (33), the input voltage to input current transfer functions are

$$G_3(s) = \frac{\hat{i}_{\text{in}1} - \hat{i}_{\text{in}2}}{\hat{v}_{\text{in}}} = \frac{D_1 n_1 - D_2 n_2}{2} \cdot \frac{\hat{i}_{L1} + \hat{i}_{L2}}{\hat{v}_{\text{in}}} \tag{34}$$

$$G_4(s) = \frac{\hat{i}_{\text{in}1} + \hat{i}_{\text{in}2}}{\hat{v}_{\text{in}}} = \frac{D_1 n_1 + D_2 n_2}{2} \cdot \frac{\hat{i}_{L1} + \hat{i}_{L2}}{\hat{v}_{\text{in}}} \tag{35}$$

where (36), shown at the bottom of the page.

From (34) to (36), the initial and terminal values of $G_4(s)$ and $G_5(s)$ are

$$[i_{\text{in}1}(t) - i_{\text{in}2}(t)]|_{t=0+} = \lim_{s\to\infty} s \cdot G_3(s) \cdot \frac{1}{s} = \lim_{s\to\infty} \frac{C_1 C_2 (L_1 + L_2)(D_1 n_1 + D_2 n_2)(D_1 n_1 - D_2 n_2)}{4 C_1 C_2 L_1 L_2 s} = 0 \tag{37}$$

$$[i_{\text{in}1}(t) - i_{\text{in}2}(t)]\,|_{t=\infty}$$

$$\frac{\hat{i}_{L1} + \hat{i}_{L2}}{\hat{v}_{\text{in}}} = \frac{(D_1 n_1 + D_2 n_2) \cdot \left[C_1 C_2 (L_1 + L_2) s^2 + C_1 C_2 (R_1 + R_2) s + 4 C_2 D_1^2 n_1^2 + 4 C_1 D_2^2 n_2^2\right]}{2 C_1 C_2 L_1 L_2 s^3 + 2 C_1 C_2 (L_1 R_2 + L_2 R_1) s^2 + \left[(2 C_1 D_2^2 n_2^2 + 2 C_2 D_1^2 n_1^2)(L_1 + L_2) + 2 C_1 C_2 R_1 R_2\right] s + (2 C_1 D_2^2 n_2^2 + 2 C_2 D_1^2 n_1^2)(R_1 + R_2)} \tag{36}$$

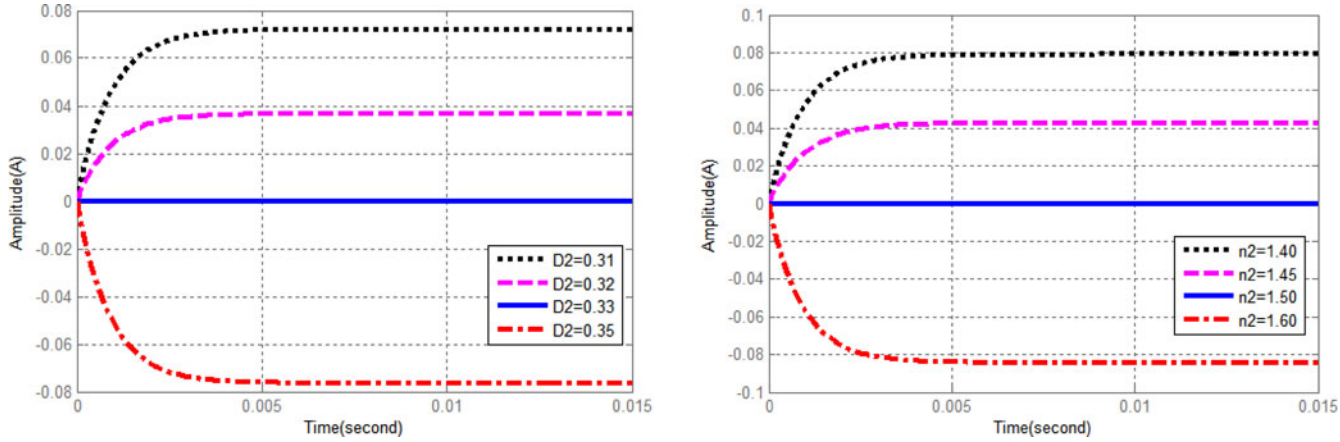

Fig. 9. Step response of $G_3(s)$ with differences in: (a) duty ratios ($D_1 = 0.33$) and (b) transformer turn ratios ($n_1 = 1.5$).

$$= \lim_{s\to 0} s \cdot G_3(s) \cdot \frac{1}{s} = \frac{(D_1 n_1 + D_2 n_2)(D_1 n_1 - D_2 n_2)}{R_1 + R_2} \quad (38)$$

$$\left[\frac{i_{\text{in}1}(t) - i_{\text{in}2}(t)}{i_{\text{in}1}(t) + i_{\text{in}2}(t)}\right] |_{t=\infty} = \frac{D_1 n_1 - D_2 n_2}{D_1 n_1 + D_2 n_2}. \quad (39)$$

Equation (37) shows that, even with substantial parameter mismatches, equal input current sharing is achieved at $t = 0+$ during a step-change in input voltage.

Equation (39) illustrates that the steady-state sharing of input current is affected by duty ratio and transformer turn ratio mismatches, which is as concluded from (20) in Section III. However, the relationship $(D_1 n_1 - D_2 n_2) \ll (D_1 n_1 + D_2 n_2)$ can be practically realized by using dedicated gate driving circuitry and using power switches with similar junction capacitance; hence, the expression $[(i_{\text{in}1} - i_{\text{in}2})/(i_{\text{in}1} + i_{\text{in}2})] |_{t=\infty} \approx 0$ can be achieved practically.

Fig. 9 shows the MATLAB simulated step response of $G_3(s)$, $i_{\text{in}1}(t) - i_{\text{in}2}(t)$, for duty ratio or transformer turn ratio mismatch. In Fig. 9, the simulated results are the same as those for (37) and (38).

E. Analysis of Dynamic Sharing of Input Current With a Load Current Step Change

To analyze the dynamic sharing of input current with a load current step change, the output-current transfer function can be derived from (32) and (33) and is

$$G_5(s) = \frac{\hat{i}_{\text{in}1} - \hat{i}_{\text{in}2}}{\hat{i}_o} = \frac{\hat{i}_{\text{in}1} - \hat{i}_{\text{in}2}}{\hat{i}_{L1} + \hat{i}_{L2}}$$

$$= \frac{1}{2}(D_1 n_1 - D_2 n_2). \quad (40)$$

From (40), the step response of $G_5(s)$ is constant, and is only affected by transformer turn ratio and the duty ratio mismatch. Since the relationship $D_1 n_1 - D_2 n_2 \approx 0$ can be practically realized by modern manufacturing techniques, the condition $i_{\text{in}1}(t) - i_{\text{in}2}(t) \approx 0$ can be achieved in practice.

From the aforementioned analysis of IPOP system current-sharing performances in the presence of various module parameter mismatches, it is concluded: 1) with input-voltage disturbance, the mismatched filter inductances and/or effective resistances slightly affect the dynamic output current sharing but have no effect on steady-state output current sharing; 2) with input-voltage disturbance and matched filter inductances and effective resistances, other parameter mismatches do not affect the dynamic and steady-state output current sharing; 3) with a load current step change, filter inductance and/or effective resistance mismatch slightly affect dynamic output current sharing, but have no effect on steady-state output current sharing; 4) with load current step changes and matched filter inductances and effective resistances, mismatched other parameters do not affect dynamic and steady-state output current sharing; 5) with input-voltage disturbance, steady-state input-current sharing is only affected by the mismatched in duty ratios and transformer turn ratios, but the result $[(i_{\text{in}1} - i_{\text{in}2})/(i_{\text{in}1} + i_{\text{in}2})] |_{t=\infty} \approx 0$ can be practically achieved by using dedicated gate drive circuitry and power switches with similar junction capacitances; 6) with load current disturbance, the differences between input currents $i_{\text{in}1}(t)$ and $i_{\text{in}2}(t)$ are constant, and are only affected by transformer turn ratio and the duty ratio mismatch, while the expression $i_{\text{in}1}(t) - i_{\text{in}2}(t) \approx 0$ can be achieved in practice.

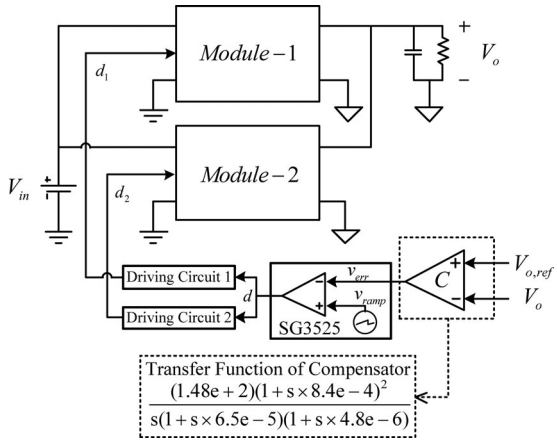

Fig. 10. Closed-loop system of the IPOP converter.

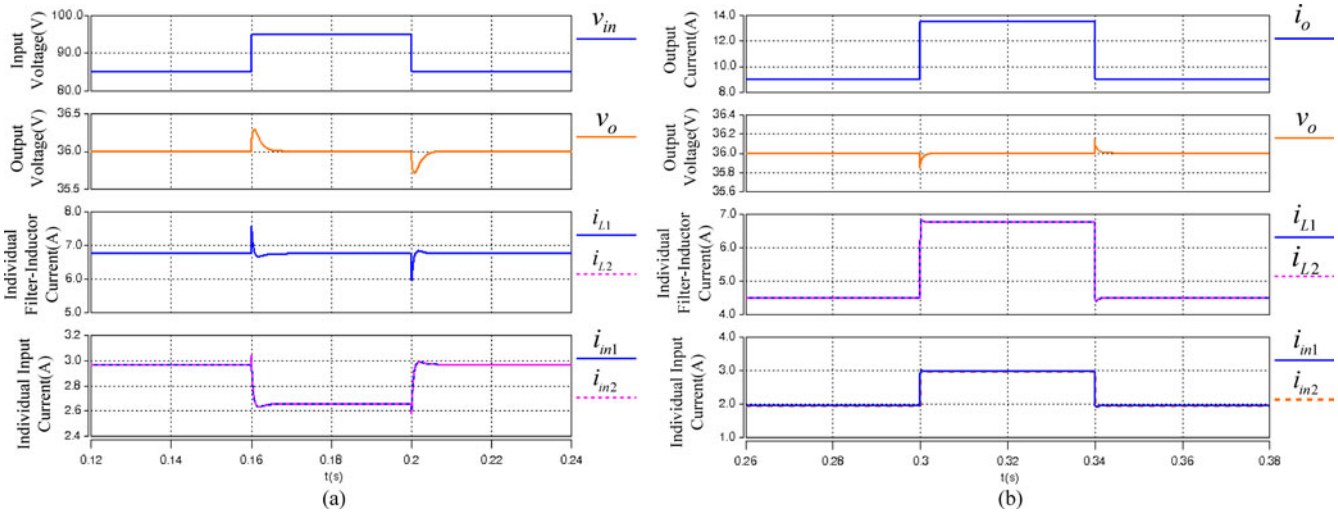

Fig. 11. With matched module parameters, simulation responses of output voltage, filter-inductor currents and input currents, to step change of (a) 10 V in input voltage and (b) 4.5 A in total load current.

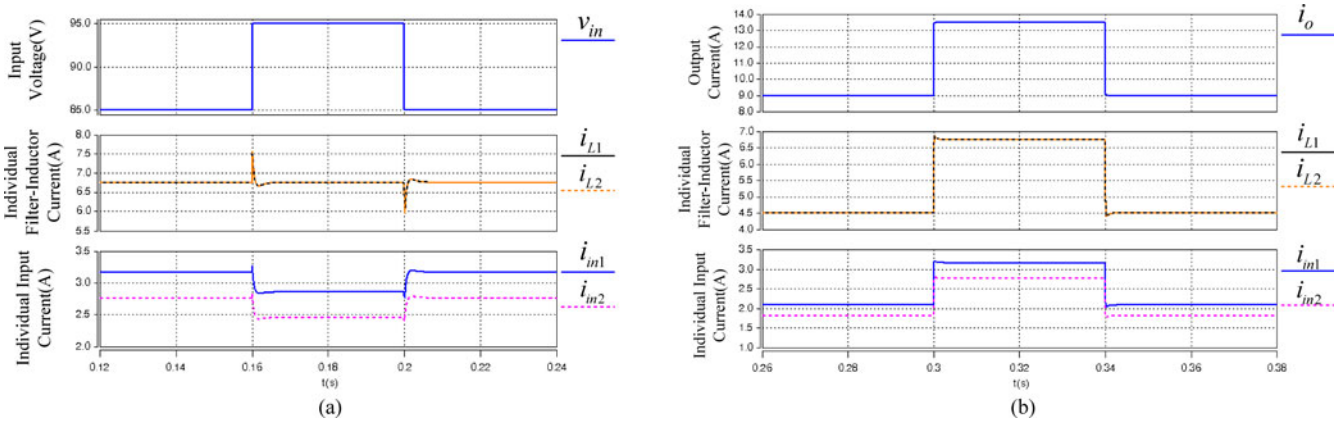

Fig. 12. With $d_1 = 0.31$ and $d_2 = 0.27$, simulation responses of filter-inductor currents and input currents, to step change of (a) 10 V in input voltage and (b) 4.5 A in total load current.

V. Simulation Verification

The closed-loop system of the proposed IPOP converter is shown in Fig. 10. An output voltage controller and a common-duty-ratio control scheme are utilized in the system. However, with parameter mismatches in the drive circuitry and the power switches, the real duty ratios of the two modules are of small difference. In this section, the closed-loop system is simulated in Saber, in which the converter module-1 and module-2 are replaced by the large-signal model shown in Fig. 4. The same parameters as used in Section IV are used here, specifically: $V_{\rm in} = 85\,{\rm V}$, $V_o = 36\,{\rm V}$, $I_o = 13.5\,{\rm A}$, $n_1 = n_2 = 6:9$, $L_1 = L_2 = 180\,\mu{\rm H}$, $C_{T1} = C_{T2} = 40\,\mu{\rm F}$, $C_{11} = C_{12} = C_{21} = C_{22} = 2000\,\mu{\rm F}$, and $R_1 = R_2 = 0.2\,\Omega$, and a switching frequency of 60 kHz. The controller is implemented with a phase lead-phase lag compensator, with the cross-over frequency of the voltage loop being 11 kHz.

Fig. 11 shows the simulation results with matched module parameters. Fig. 11(a) shows the responses of output voltage, filter-inductor currents, and input currents to a step change of 10 V in input voltage, where the input voltage steps from 85 to 95 V and then drops to 85 V, resulting in a 0.3 V output-voltage overshoot within a 2 ms transient process. Fig. 11(b) shows the responses of output voltage, filter-inductor currents, and input currents to a 4.5 A total load-current step change, where the load current step increases from 9 to 13.5 A and then drops to 9 A, resulting in a 0.1 V output-voltage overshoot within a 1 ms transient process. From Fig. 10, the IPOP system has good closed-loop response performance, and the two converter modules equally share the input and load current, with matched parameters.

Fig. 12 shows the simulation results with different duty ratios ($d_1 = 0.31$, $d_2 = 0.27$), which have no effect on inductor current sharing. However, from Fig. 12, mismatched duty ratios slightly affect input-current sharing, with a 0.4 A maximum difference between input currents at the 10 V input-voltage step change and a maximum difference of 0.35 A between input currents at the 4.5 A total load-current step change. Hence, from Fig. 12, general input-current sharing is achieved in steady state

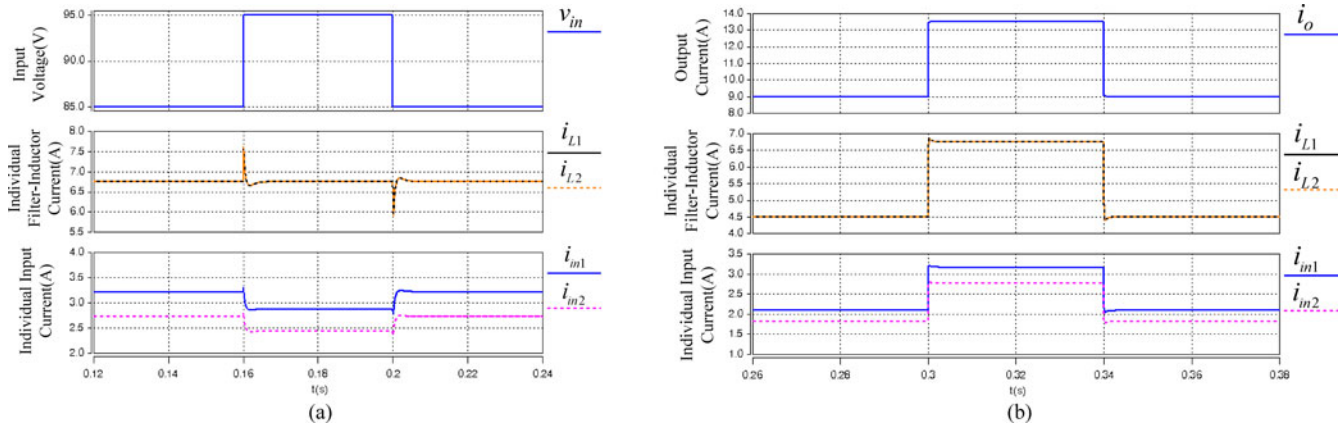

Fig. 13. With $n_1 = 1.50$ and $n_2 = 1.27$, simulation responses of filter-inductor currents and input currents, to step change of (a) 10 V in input voltage and (b) 4.5 A in total load current.

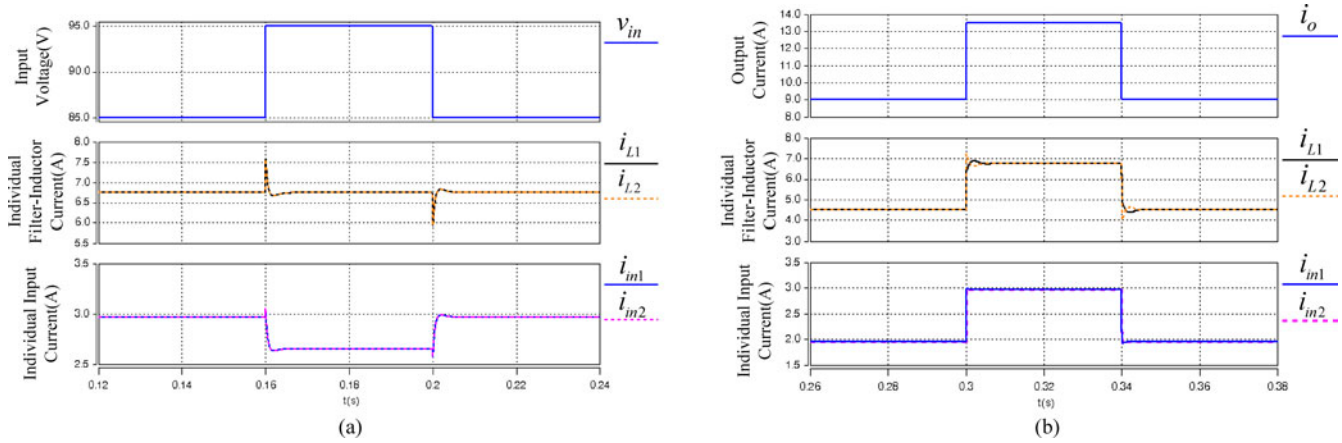

Fig. 14. With $L_1 = 180\,\mu$H and $L_2 = 115\,\mu$H, simulation responses of filter-inductor currents and input currents, to step change of (a) 10 V in input voltage and (b) 4.5 A in total load current.

and dynamic state, which corresponds with the theoretical analysis as shown in (20) and (34)–(40).

Fig. 13 shows the simulation results in the presence of difference in transformer turn ratios ($n_1 = 1.50$, $n_2 = 1.27$), which is similar to the mismatched circumstance in duty ratios.

Fig. 14 shows the simulation results for different filter-inductor inductances ($L_1 = 180\,\mu$H, $L_2 = 115\,\mu$H). From Fig. 14, mismatched filter-inductor inductances slightly affect dynamic load-current sharing, with a difference of 0.2 A between inductor currents at the 10 V input-voltage step change and a difference of 0.3 A between inductor currents at the 4.5 A total load-current step change. Furthermore, the inductance mismatches have no effect on the steady-state load-current sharing, and also do not affect input-current sharing both in steady state and dynamic state, which corresponds with the theoretical analysis as shown in (19), (34), and (40).

Fig. 15 shows the simulation results in the presence of differences in equivalent resistances ($R_1 = 0.2\,\Omega$, $R_2 = 0.4\,\Omega$), which are similar to the circumstance for mismatched filter-inductor inductances.

Fig. 16 shows the simulation results for multiple parameter mismatches ($d_1 = 0.31$, $d_2 = 0.27$, $n_1 = 1.5$, $n_2 = 1.27$, $L_1 = 180\,\mu$H, $L_2 = 115\,\mu$H, $R_1 = 0.2\Omega$, $R_2 = 0.4\,\Omega$), illustrating that the dynamic-state sharing of inductor currents is slightly affected by multiple parameter mismatches. The multiple parameter mismatches have no effect on inductor current steady-state sharing, as shown in (19). Input-current dynamic-state sharing is slightly affected by the mismatches, and input-current steady-state sharing is only affected by turn ratio and duty ratio mismatches, which is the case with the theoretical analysis based on (20) in Section III.

From Fig. 10, in order to study the duty ratio disturbance to inductor current variation in the closed-loop system, a step-change of 10 V is added to reference output voltage, and the simulation results are presented in Fig. 17. From Fig. 17(a), input- and load-current sharing are well achieved with designed matched parameters. Fig. 17(b) shows that the worst case mismatched parameters slightly affect the dynamic load-current sharing, but have no effect on the steady-state load-current sharing. Steady-state and dynamic input-current sharing are mainly affected by turn ratio and duty ratio mismatches, but can still be achieved by reducing the mismatches in turn ratio and duty ratio.

Therefore, the presented simulation results indicate that steady-state sharing of the IPOP system load currents is achieved

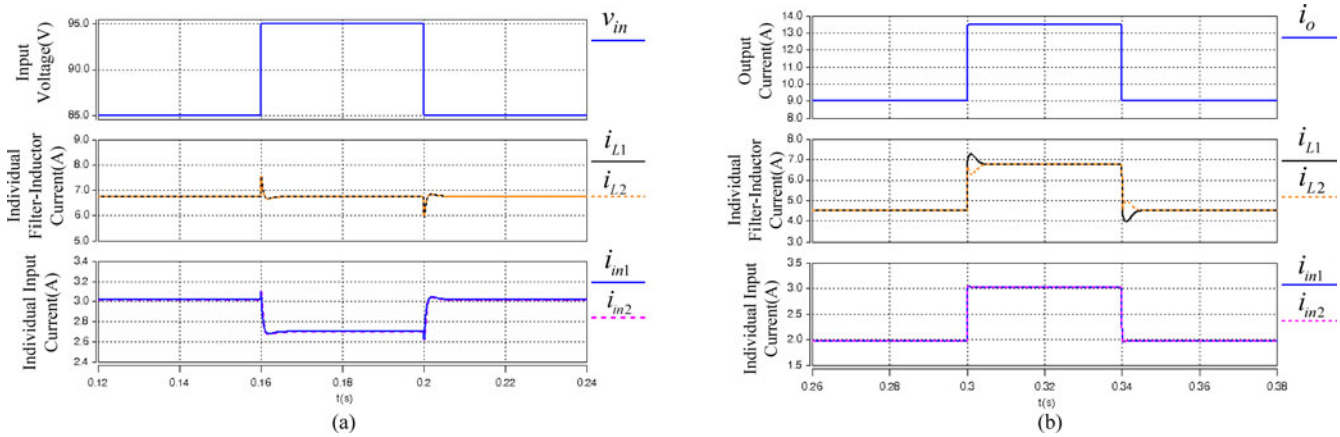

Fig. 15. With $R_1 = 0.2\,\Omega$ and $R_2 = 0.4\,\Omega$, simulation responses of filter-inductor currents and input currents, to step change of (a) 10 V in input voltage and (b) 4.5 A in total load current.

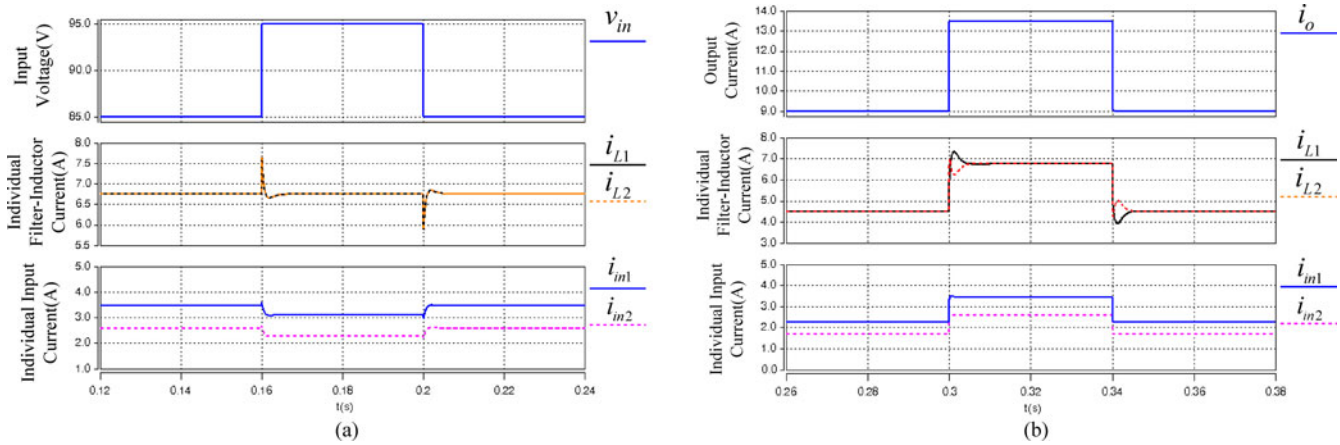

Fig. 16. Under a worst case mismatch of converter parameters ($d_1 = 0.37$, $d_2 = 0.33$, $n_1 = 1.50$, $n_2 = 1.27$, $L_1 = 180\,\mu$H, $L_2 = 115\,\mu$H, $R_1 = 0.2\,\Omega$, and $R_2 = 0.4\,\Omega$), simulation response of inductor currents to step change of (a) 10 V in input voltage and (b) 4.5 A in total load current.

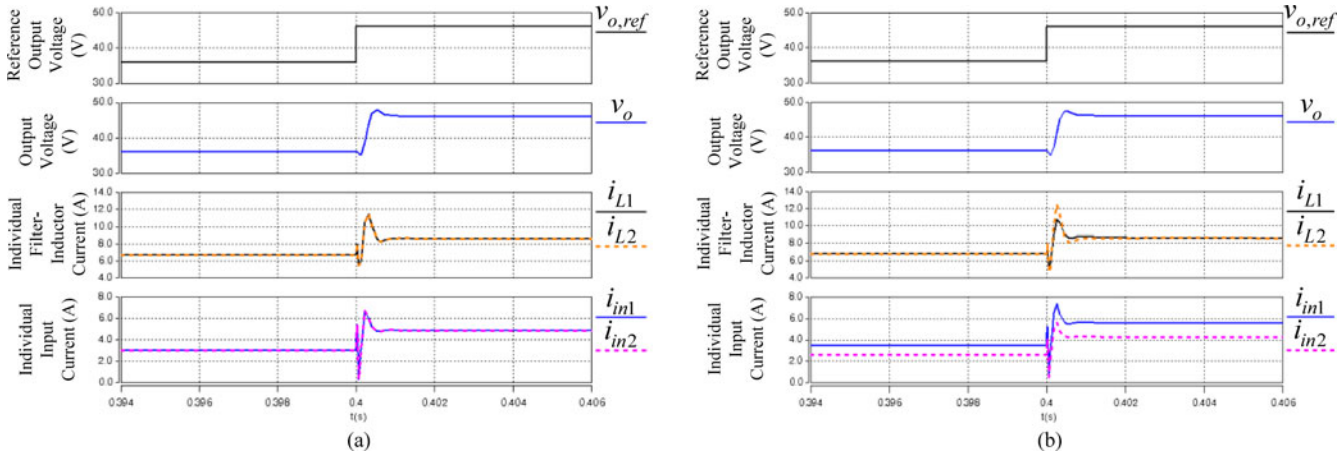

Fig. 17. Responses of output voltage, filter-inductor currents, and input currents to reference output voltage which steps from 36 to 46 V, with (a) aforementioned matched parameters ($d_1 = d_2 = 0.33$, $n_1 = n_2 = 1.50$, $L_1 = L_2 = 180\,\mu$H and $R_1 = R_2 = 0.2\,\Omega$), and (b) a worst case mismatched parameters ($d_1 = 0.37$, $d_2 = 0.33$, $n_1 = 1.50$, $n_2 = 1.27$, $L_1 = 180\,\mu$H, $L_2 = 115\,\mu$H, $R_1 = 0.2\,\Omega$, and $R_2 = 0.4\,\Omega$).

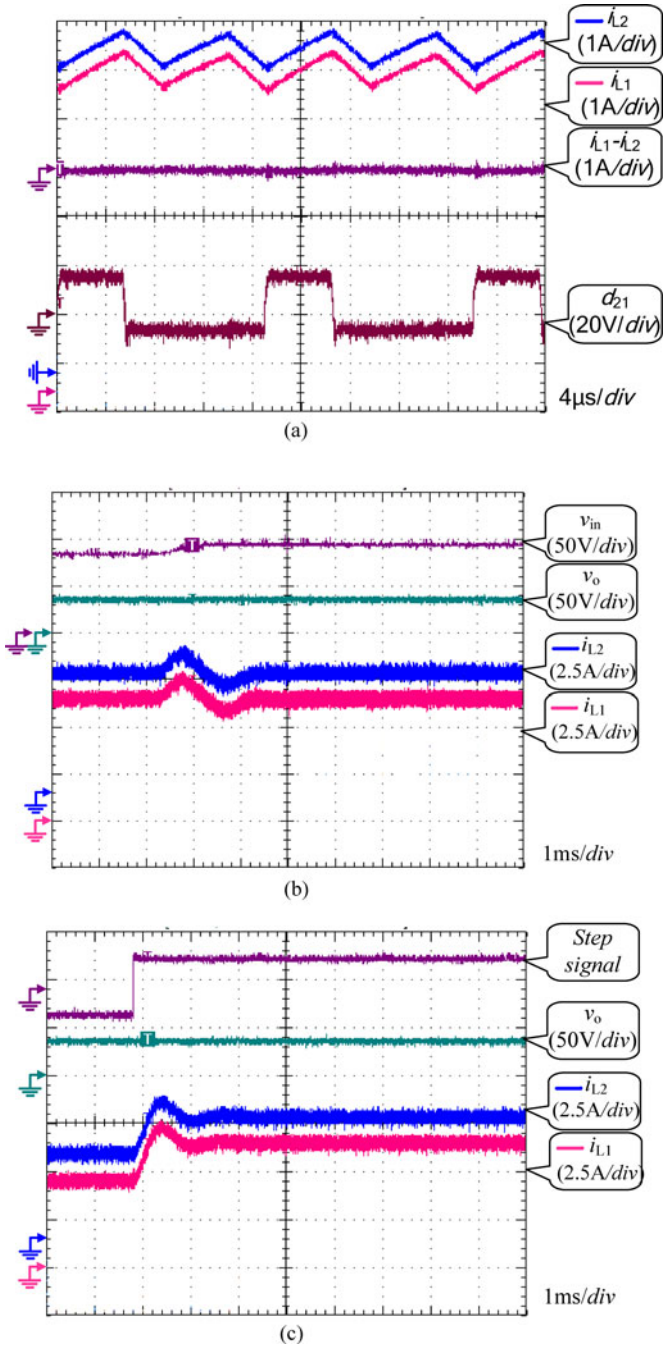

Fig. 18. Experimental waveforms for the IPOP converter with matched designed parameters. (a) Steady-state inductor-current and driving-signal waveforms at full load of 13.5 A. (b) Dynamic-state voltage and current waveforms with step change of input voltage from 85 to 95 V. (c) Dynamic-state voltage and current waveforms with step load current change from 9 to 13.5 A.

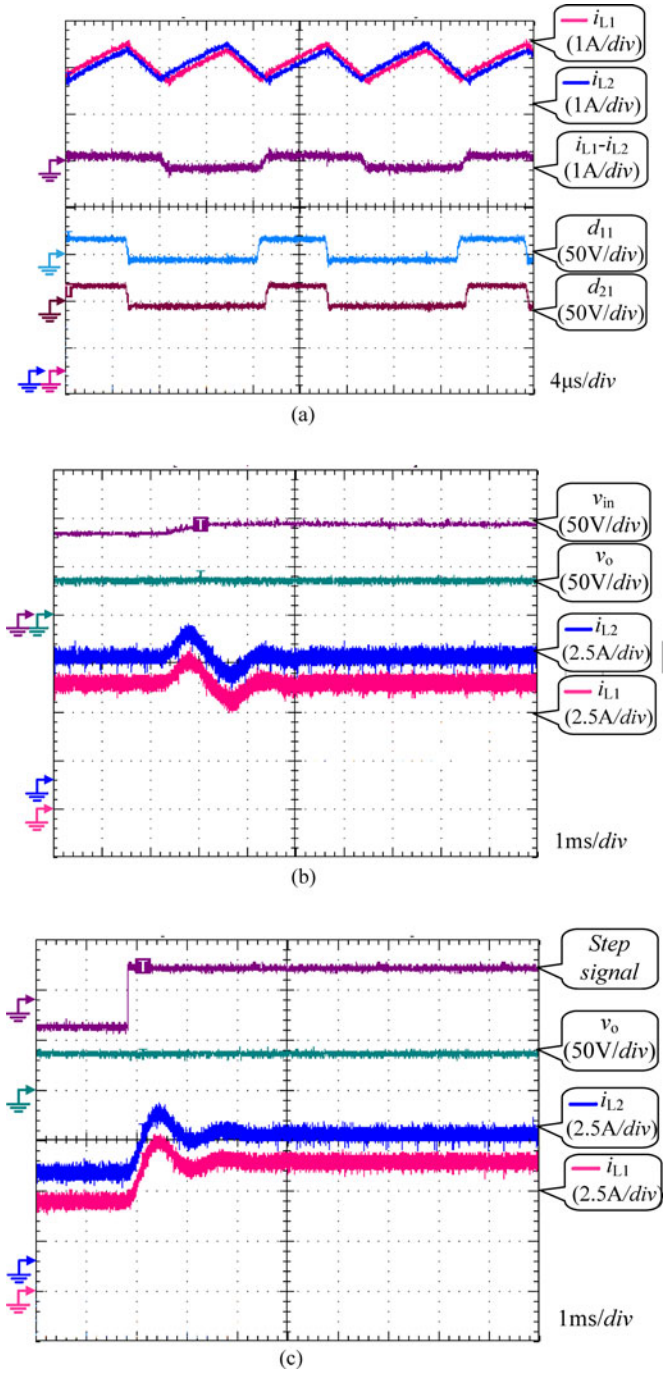

Fig. 19. Experimental waveforms for IPOP converter with $d_1 = 0.31$ and $d_2 = 0.27$. (a) Steady-state waveforms at full load of 13.5 A. (b) Dynamic-state waveforms with step change of input voltage from 85 to 95 V. (c) Dynamic-state waveforms with step change of load current from 9 to 13.5 A.

in the presence of converter parameter mismatches, and input-current sharing and dynamic load current sharing are slightly affected in the presence of the converter parameter mismatches. Moreover, the simulation results validate the theoretical analysis presented in Sections III and IV. Thus, equal sharing of input and load currents among modules can be realized by employing a common-duty-ratio control scheme and reducing various module parameter mismatches, which is practically viable.

VI. Experimental Verification

A prototype IPOP system consisting of two HB converter modules, as shown in Fig. 1, is used to verify the inherent current-sharing performance. The parameters of voltage loop are the same as those shown in Fig. 10. The overall system specification is as in Section V and as follows: 1) input dc voltage, 85–95 V; 2) output voltage, 36 V, directly regulated by

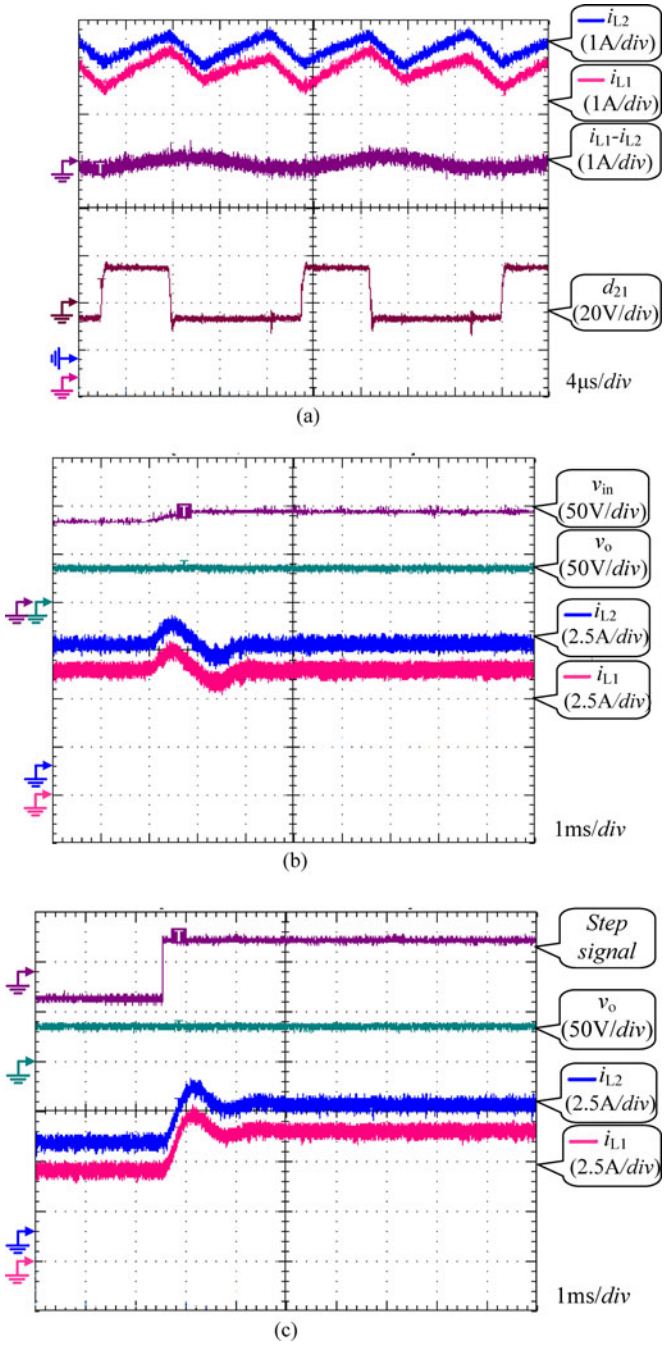

Fig. 20. Experimental waveforms for the IPOP converter with $n_1 = 1.5$ and $n_2 = 1.27$. (a) Steady-state waveforms at full load of 13.5 A. (b) Dynamic-state waveforms with step change of input voltage from 85 to 95 V. (c) Dynamic-state waveforms with step change of load current from 9 to 13.5 A.

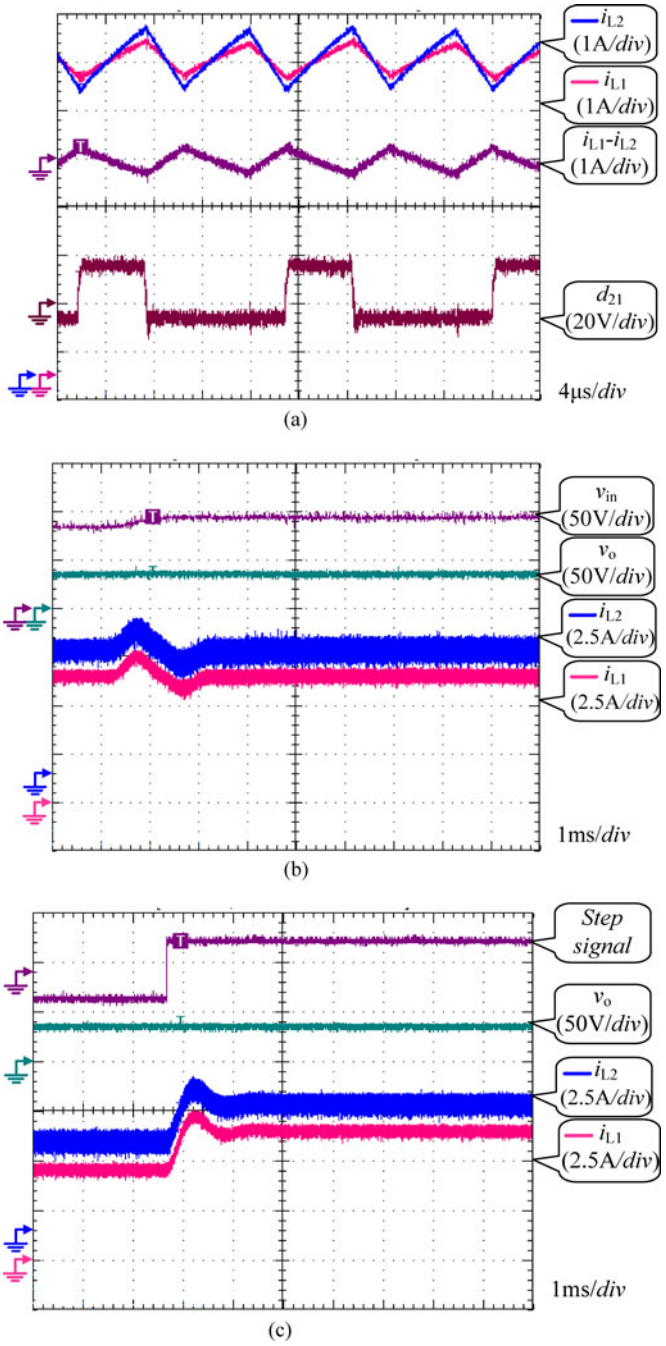

Fig. 21. Experimental waveforms for the IPOP converter with $L_1 = 180\,\mu$H and $L_2 = 115\,\mu$H. (a) Steady-state waveforms at full load of 13.5 A. (b) Dynamic-state waveforms with step change of input voltage from 85 to 95 V. (c) Dynamic-state waveforms with step change of load current from 9 to 13.5 A.

a closed-loop controller; and 3) maximum load current, 13.5 A. The power stage component values are as follows: primary HB capacitances of C_{11}, C_{12}, C_{21}, and C_{22}, 2000 μF; output-filter inductances of L_1 and L_2, 180 μH; turn ratios n_1 and n_2, 6:9; duty ratio D_1 and D_2, 0.30. The switching frequency for each converter is 60 kHz. Power MOSFETs are IRFP250, and the diodes are DESI60-02A.

Since experimental waveforms for the average input current of each module are inaccessible and the relationship between instantaneous input current and inductor current in one module is readily seen, only experimental waveforms of inductor currents for each module are shown in this Section.

Fig. 18 shows experimental waveforms for the IPOP system in the presence of the designed matches in various module parameters. Fig. 18(a) shows steady-state operation at 13.5 A, full load; Fig. 18(b) shows IPOP system dynamic operation with a 10 V input-voltage step change and Fig. 18(c) shows dynamic

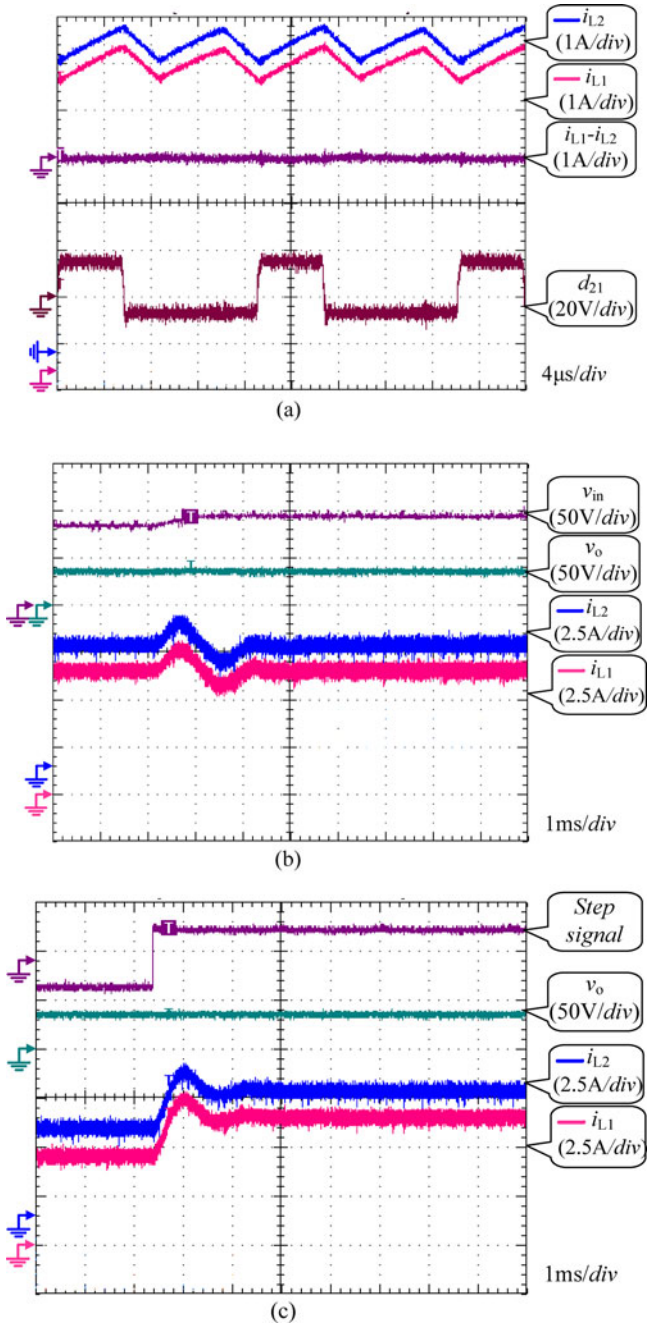

Fig. 22. Experimental waveforms for the IPOP converter with $R_1 = 0.2\,\Omega$ and $R_2 = 0.4\,\Omega$. (a) Steady-state waveforms at full load of 13.5 A. (b) Dynamic-state waveforms with step change of input voltage from 85 to 95 V. (c) Dynamic-state waveforms with step change of load current from 9 to 13.5 A.

operation with 4.5 A load current step change. From Fig. 18, it is confirmed that the total load current has been shared evenly between the two modules, both in steady-state and dynamic-state operation.

In order to further verify that the proposed IPOP converter system can achieve equal load current sharing in the presence of mismatched module parameters, some parameters are purposely adjusted. Fig. 19 shows experimental waveforms with different duty ratios, namely, $d_1 = 0.31$ and $d_2 = 0.27$. From Fig. 19(a),

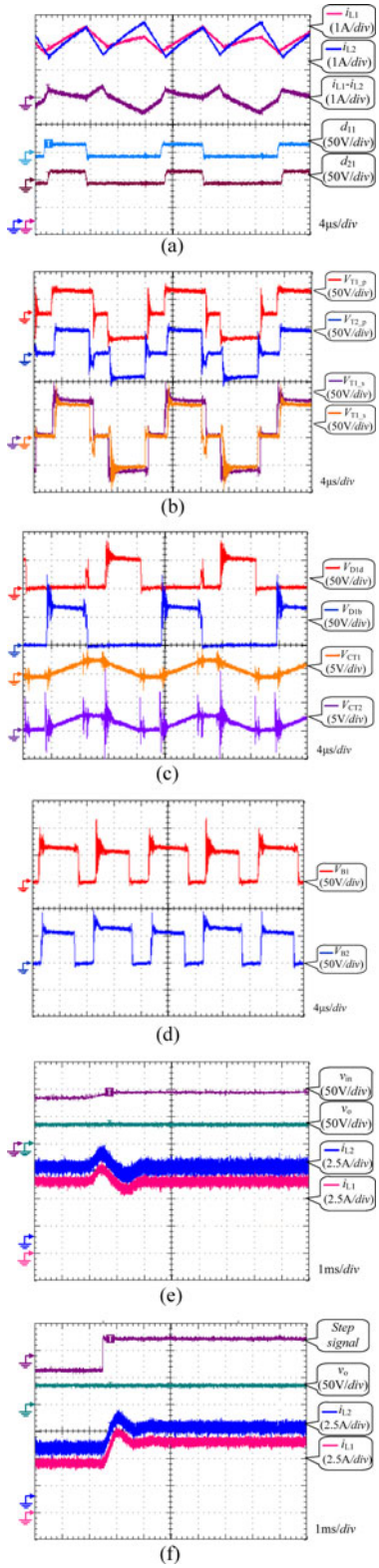

Fig. 23. Experimental waveforms of the IPOP converter with the mismatched module parameters ($d_1 = 0.35$, $d_2 = 0.31$, $n_1 = 1.5$, $n_2 = 1.27$, $L_1 = 180\,\mu$H, $L_2 = 115\,\mu$H, $R_1 = 0.2\,\Omega$, and $R_2 = 0.4\,\Omega$). (a) Steady-state current waveforms at full load of 13.5 A. (b) Primary and secondary voltage waveforms of transformer T_1 and T_2. (c) Voltage waveforms of D_{1d}, D_{1b}, C_{T1}, and C_{T2}. (d) Voltage waveforms after chain-connected rectifier. (e) Dynamic-state waveforms with step change of input voltage from 85 to 95 V. (f) Dynamic-state currents waveforms with step change of load current from 9 to 13.5 A.

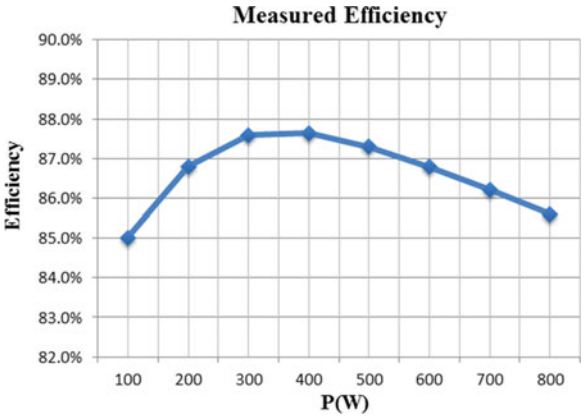

Fig. 24. Efficiency of the proposed IPOP converter system.

equal steady-state sharing of load current has been achieved with root mean square of inductor currents $I_{L_1} = I_{L_2} = 6.75\,\text{A}$, which is the same as the theoretical analysis described by (19) in Section III. From Fig. 19(b), even with a step change of input voltage from 85 to 95 V, general equal dynamic-state sharing of load current is achieved. From Fig. 19(c), with a step load current change from 9 to 13.5 A, general equal dynamic-state sharing of load current is achieved. In addition, Fig. 19(b) and (c) shows that the IPOP system has a good closed-loop performance for controlling the output voltage. Therefore, it is experimentally verified that the IPOP system realizes both the steady-state and dynamic-state sharing of load current in the presence of mismatched duty ratios.

Fig. 20 shows experimental waveforms for the IPOP system, with the difference in transformer turn ratios, namely, $n_1 = 1.5$ and $n_2 = 1.27$. From Fig. 20, both steady-state and dynamic-state sharing of load current are achieved even with mismatched turn ratios, as with mismatched duty ratios.

Fig. 21 shows experimental waveforms at a full load of 13.5 A, with mismatched output-filter inductances, namely, $L_1 = 180\,\mu\text{H}$ and $L_2 = 115\,\mu\text{H}$. From Fig. 21, mismatched output-filter inductances slightly affect the dynamic-state load current sharing, but have no effect on the steady-state sharing of load current.

Fig. 22 shows experimental waveforms for the IPOP system, with different resistances, namely, $R_1 = 0.2\,\Omega$ and $R_2 = 0.4\,\Omega$. From Fig. 22, mismatched effective resistances slightly affects the dynamic-state sharing of load current, but have no effect on the steady-state sharing of load current, as with output-filter inductance mismatch.

Fig. 23 shows experimental waveforms with mismatched parameters $d_1 = 0.35$, $d_2 = 0.31$, $n_1 = 1.5$, $n_2 = 1.27$, $L_1 = 180\,\mu\text{H}$, $L_2 = 115\,\mu\text{H}$, $R_1 = 0.2\,\Omega$, and $R_2 = 0.4\,\Omega$. In Fig. 23(b), V_{T1_p} and V_{T1_s} are the primary and secondary voltages of T_1. V_{T2_p} and V_{T2_s} are the primary and secondary voltages of T_2. From Fig. 23, the mismatched module parameters slightly affect the dynamic-state sharing of load current, but have no effect on the steady-state load current. Also, from Fig. 23, the steady-state experimental waveforms well demonstrate the operating stages shown in Figs. 2 and 3 in Section II.

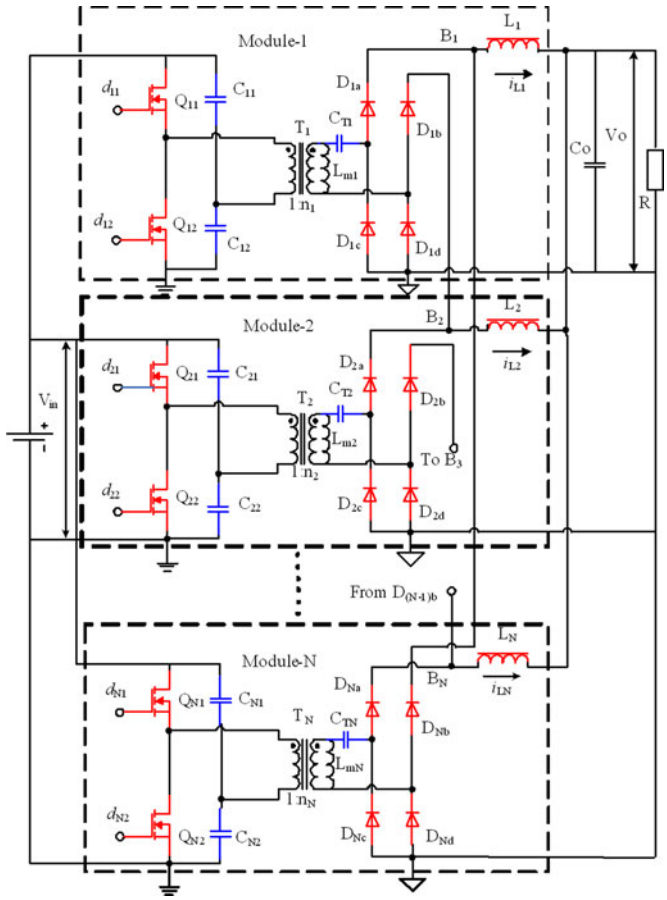

Fig. 25. Topology of IPOP converter system consisting of N ($N \geqslant 3$) HB dc–dc converter modules.

Fig. 24 shows the efficiency of the proposed IPOP converter system, with input voltage of 85 V and output voltage of 36 V. It should be noted that the rectifier diodes are DESI60-02A. If the diodes are replaced by Schottky diodes or synchronous rectification is applied, the efficiency will be substantially optimized.

As shown in Figs. 18–23, the experimental results indicate that the automatic current sharing performance has been achieved well in the proposed IPOP converter system, even with module parameters mismatched by more than 10%. Furthermore, the experimental results are identical to simulations and theoretical analysis presented in previous sections.

VII. Conclusion

In this paper, an IPOP converter system with chain-connected rectifiers has been proposed. Based on steady-state dc and small-signal models, it has been verified that, without the need for a dedicated current-sharing controller and current sensors, good steady-state and transient current-sharing performance can be achieved by using a common-duty-ratio control scheme and by reducing various module parameter mismatching, which is practically viable. The simulation and experimental results verify the feasibility of practically implementing the proposed IPOP system.

However, unlike interleaved converters, which use displaced carriers, no reduction of input or output ripple current is achieved with the half-wave, daisy chain connection of the output rectifier.

In addition, the proposed IPOP converter system can be extended to three or more converter modules, as shown in Fig. 25, and the constituent module can be the FB converter.

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