A Two-Phase Fully-Integrated DC–DC Converter With Self-Adaptive DCM Control and GIPD Passive Components

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***Abstract*—This paper presents a two-phase fully-integrated dc–dc converter for system-in-package systems with passive components fabricated using a glass-substrate-integrated passive device (GIPD) process. The proposed self-adaptive discontinuous conduction mode (DCM) controller and low-swing/full-swing buffer were incorporated to reduce the switching loss and maintain high efficiency at high switching frequency. A secondary phase and phase controller were added to increase the output power and reduce the output ripple. The proposed GIPD solution packages a standard complementary metal–oxide–semiconductor process and GIPD process in 3-D format to reduce the footprint of the system. The proposed self-adaptive DCM controller and low-swing/full-swing buffer improve efficiency of 15% in measurement compared to our previous work on the GIPD process in simulation. The peak efficiency of the proposed converter was 79.09% at a 400-mA load current, 5% higher than the peak efficiency presented in previous study. The maximal output power could reach 720 mW and the maximal switching frequency (f_{CCM}) was designed to be 70 MHz (measured at 50 MHz) with only two 6-nH inductors and one 15-nF capacitor.**

***Index Terms*—Fully-integrated dc–dc converter, glass-substrate-integrated passive device (GIPD) process, self-adaptive discontinuous conduction mode (DCM) controller.**

I. Introduction

THE modern electronic systems require powerful functionality, a small size, and the ability to operate for a long period. To reduce the sizes of systems, utilizing few discrete integrated circuits (ICs) and passive components on a small printed circuit board is necessary. Using SoC techniques can decrease the number of discrete ICs, but discrete passive components are still required to ensure an effective performance, particularly in power management circuits. The switched-inductor dc–dc converter is one of the major power management circuits, which can yield high efficiency levels, but requires large external passive components such as inductors and capacitors [1]–[3]. Therefore, a fully-integrated switched-inductor dc–dc converter can be used for maintaining high efficiency levels and integration [4], [5]. The size of electronic systems can be substantially reduced as shown in Fig. 1.

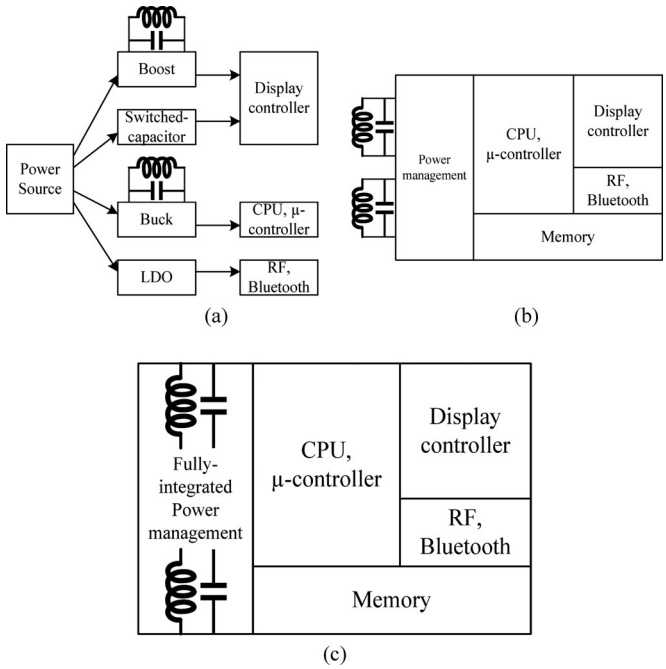

Fig. 1. Different solutions of electronic systems. (a) Discrete. (b) SoC with external passives. (c) SoC with fully-integrated passives.

SoC is a crucial technique in contemporary design; however, integrating various circuits in a single chip yields difficulties, such as increased design complexity and noise. Thus, alternative techniques have been proposed such as the 3-D IC techniques in [6], [7] Fig. 2(a) and the system-in-package (SiP) techniques [8]–[10] in Fig. 2(b). These techniques may not be as efficient as the SoC technique is, but they can decrease the design complexity and system noise. In this paper, the proposed switched-inductor dc–dc converter using a standard 0.18 μm CMOS process and passive components using a glass-substrate-integrated passive device (GIPD) process are packaged in a 3-D format as shown in Fig. 2(c). Using the GIPD process also enhances the quality of the passive components and extends the performance throughout the system.

To realize systems on a single chip or in a single package, a fully-integrated dc–dc converter can be used. Recent studies

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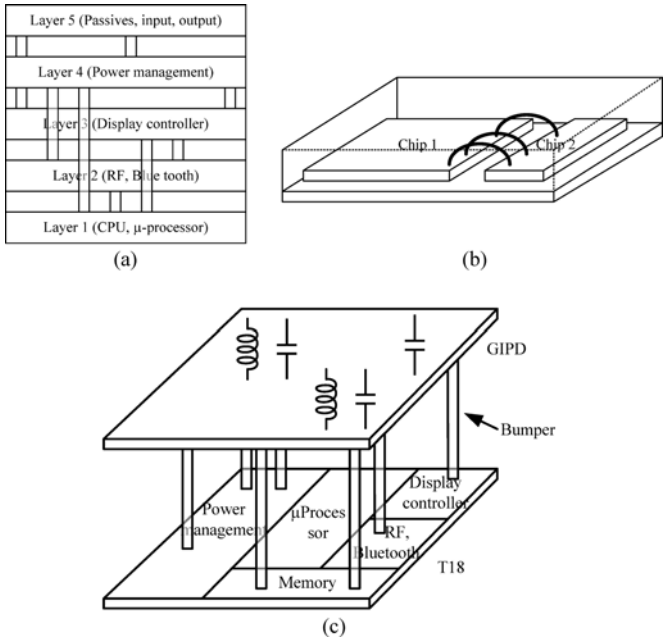

Fig. 2. Alternative solutions of electronic systems. (a) Three-dimensional IC solution. (b) SiP solution. (c) GIPD solution.

on fully-integrated switched-inductor dc–dc converters have focused on integration and efficiency. A 300-MHz dual-mode pulse-width modulation (PWM) and pulse-frequency modulation (PFM) fully-integrated dc–dc converter was presented in [11], which includes a PMOS switch-scaling and a stacked inductor. Dual-mode and PMOS switch-scaling are used to improve their efficiency, and the stacked inductor reduces the layout area and inductor resistance. The peak operating efficiency was 77%. However, their maximum output power was only 266 mW. A four-phase semiconstant on/off-time buck converter was proposed in [12], which operated only in discontinuous conduction mode (DCM), using four 3.9-nH inductors and a 12.17-nF capacitor. However, their peak efficiency was only 58%. In [13], a resonant gate driver was used in a 200-MHz integrated buck converter to improve the efficiency under light-to-medium load conditions. This converter was realized using a BiCMOS process and yielded a peak efficiency of 77%. However, this converter required a large inductor of 51 nH. A three-level dc–dc converter was proposed in [14], which was a hybrid of a buck and switched-capacitor converter. The inductor per phase was 1 nH and the total capacitance was 29 nF. The switching frequency of the converter varied from 50 to 250 MHz and the peak efficiency was 77%. However, their light-load efficiency at 10 mA is unreported. Fully-integrated converters realized on only CMOS or BiCMOS process were presented in [11]–[14] and large silicon area was necessary to realize those inductors.

A 3-D capacitor and a spiral-type inductor using thick conductors as the *LC* output filter for designing a fully-integrated dc–dc converter were presented in [15]. The *LC* filter area was 3 mm^2, yielding an inductance of 110 nH and a capacitance of 560 nF. However, a special process was needed to minimize the resistive losses of the passive components. In [16], a tapered inductor was implemented in the fully-integrated converter to reduce the loss of the inductor. The switching frequency was 76.8 MHz and the peak efficiency was 64.5% when a 49.57-nH inductor and 0.89-nF capacitor were used. However, this converter uses the BiCMOS process and the passives are off-chip. The concept of a package inductor was introduced in [17]–[19], which facilitates the development of high-quality inductors. They also used distinct circuit improvements to enhance the performance of fully-integrated converters to reach peak efficiencies of 76.8%, 84.7%, and 82.4%, respectively. These converters are also suitable for SoC systems but need additional pads and pins to realize the inductor. Note that chip-to-chip variation of the package inductors is critical. Our previous work on the fully-integrated converter with the GIPD process was presented in [20]. With only PWM control, the peak efficiency is 78.5% in simulation and the efficiency at 10 mA is only 40%.

In this paper, several techniques were designed in the proposed converter to obtain high peak efficiency and light-load efficiency, and large output power with small passive components. The low-swing buffer and buffer control provide the power transistors with the proper driving voltage to minimize the switching loss, conduction loss, and power consumption. The proposed self-adaptive DCM control provides adaptive switching frequency and cancels the reverse inductor current without increasing the complexity of the control. A secondary phase and phase control were added to increase the converter output power and reduce the output ripple. The GIPD process was employed to ensure a high-quality inductor and effective integration of the proposed converter. Because of the characteristics of the GIPD process, the proposed converter suits for systems requiring fully integration, especially for RF and wireless communication systems. The proposed converter was designed at 70-MHz switching frequency with two inductors of 6 nH and a capacitor of 15 nF. The maximum output power of 720 mW is designed suitable for RF or wireless communication systems. In Section II, the circuit implementation of the proposed two-phase fully-integrated dc–dc converter is presented. The simulation, measurement, and comparison results are given in Section III. Section IV presents the conclusion.

II. Circuit Implementation of the Proposed Two-Phase Fully-Integrated DC–DC Converter

The primary losses in dc–dc converters are switching, conduction, and reverse inductor current losses. If the switching frequency of the converter increases, the switching loss proportionally increases. Besides, integrated passive components typically exhibit a larger parasitic resistance compared with that of discrete passives so that this large parasitic resistance increases the conduction loss. Thus, loss reductions are more crucial in fully-integrated converters than they are in traditional converters. In addition, higher switching frequency in fully-integrated converters causes the difficulty of designing the control circuit and increases the power consumption of the control circuit. Thus, the power budget of the control circuit becomes critical in the fully-integrated converter design. The control circuit needs to be simplified to reduce the delay and the power consumption.

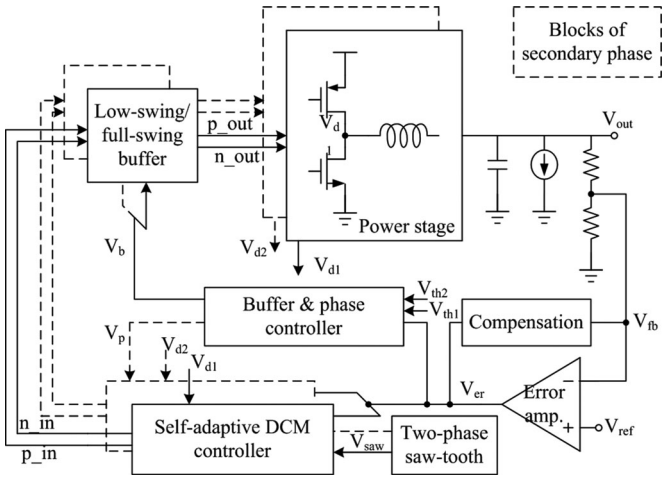

Fig. 3. Schematic of the proposed dc–dc converter.

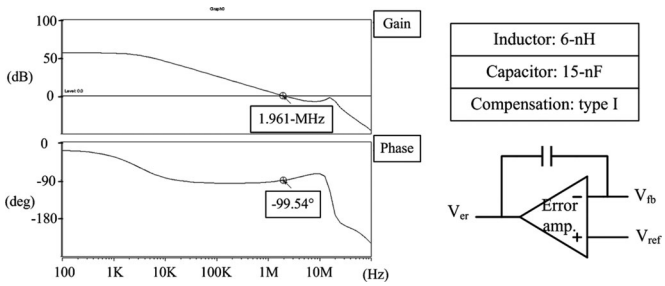

Fig. 4. Small-signal simulation of the proposed converter.

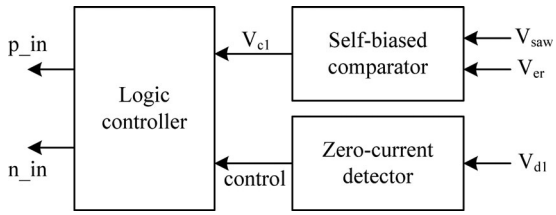

Fig. 5. Block diagram of the proposed self-adaptive DCM controller.

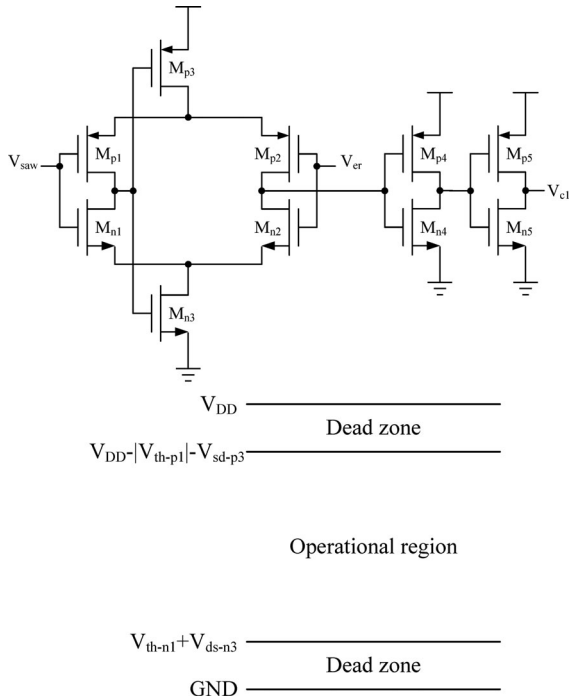

Fig. 6. Schematic of the self-biased comparator and operational region.

Fig. 3 shows the schematic of the proposed fully-integrated dc–dc converter with switching frequency of 70 MHz. The two-phase voltage-mode structure was designed to increase the output power and decrease the circuit complexity. The small-signal simulation of the proposed converter at load current of 600 mA is shown in Fig. 4. The crossover frequency is 1.961 MHz and the phase margin is 99.54°, which can reject the switching noise coming from switching frequency of 70 MHz, provides fast transient response and indicates that the converter is stable. The inductor and output capacitor were fabricated using a GIPD process. The feedback resistors sense the output voltage, and send it to the error amplifier, which assesses the value. The error signal and fixed-frequency saw-tooth signal are sent to the self-adaptive DCM controller to provide the proper control signals, whether is DCM or PWM signal. The output of the self-adaptive DCM controller is sent to the buffer, which outputs a low-swing or full-swing signal to drive the power transistors, depending on the value of the load current. The control principle of the second phase is nearly identical to that of the first phase except that the saw-tooth signal is delayed half-cycle and the second phase is shut down when the load current is light. To improve the performance, circuit-level improvements were added. The following sections detail these improvements.

A. Self-Adaptive DCM Controller

In order to achieve high efficiency and low power consumption, the self-adaptive DCM controller is proposed for the fully-integrated converter. The self-adaptive DCM controller is formed with a self-biased comparator [21], zero-current detector, and logic controller, as shown in Fig. 5. The output signals *p*_in and *n*_in are the modified control signals and sent to buffer to drive the power switches properly. The schematic of the self-biased comparator is shown in Fig. 6, which consumes small power and has fast response. The input range of the comparator is limited between $V_{\rm dd} - |V_{{\rm th}-p1}| - V_{sd-p3}$ and $V_{{\rm th}-n1} + V_{ds-n3}$ to avoid shutting down M_{P1}, M_{P2}, M_{N1} or M_{N2} and keep the comparator functional. This limitation is used in self-adaptive DCM control to produce adaptive switching frequency without a complex controller.

The zero-current detector in Fig. 7 detects the condition of the load current and whether the reverse inductor current happens. If the load current of the proposed converter is heavy, the logic controller is bypassed and the converter operates in the continuous conduction mode (CCM) by PWM signal. When the load current lessens and the zero-current detector detects that the inductor

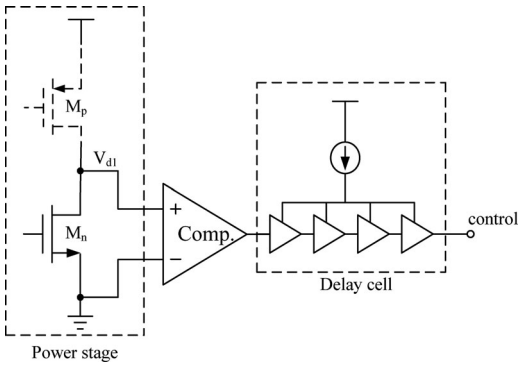

Fig. 7. Zero-current detector.

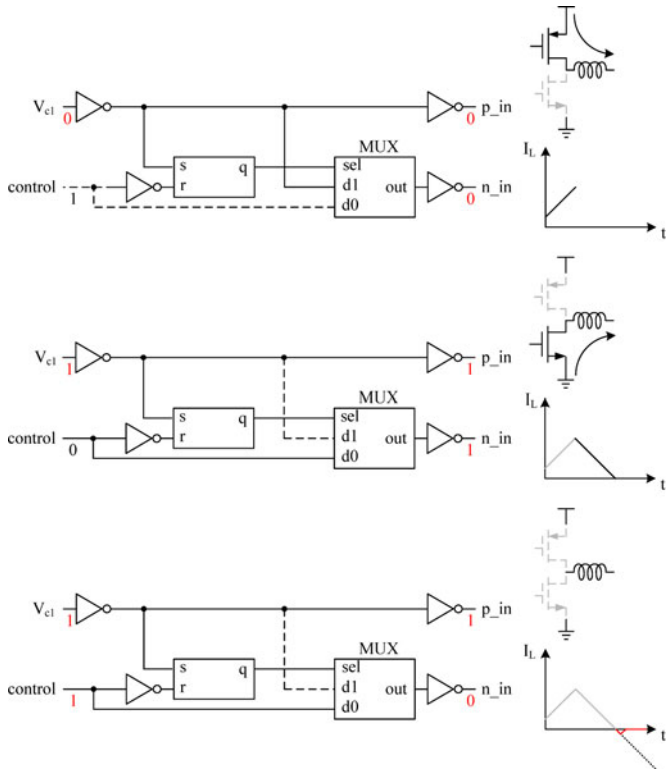

Fig. 8. Mechanism of the logic controller in the self-adaptive DCM controller.

current drops below zero, the self-adaptive DCM controller activates and turns off both the n-type and p-type power transistors, and then forces the converter into idle, as shown in Fig. 8. When both power transistors are OFF, the converter idles and the output voltage begins to drop. The idle situation is maintained until the next signal is sent by the self-biased comparator.

If the load current is heavy, the converter operates in PWM mode as shown in Fig. 9(a) with the switching frequency (f_{CCM}) of 70 MHz. If the load current is medium, the self-adaptive DCM controller activates, the self-biased comparator sends the signal every cycle, the converter operates in DCM mode, and the switching frequency is the same as f_{CCM}, shown in Fig. 9 (b). If the load current lightens further, the output level of the error amplifier (V_{er}) decreases. When V_{er} falls outside the

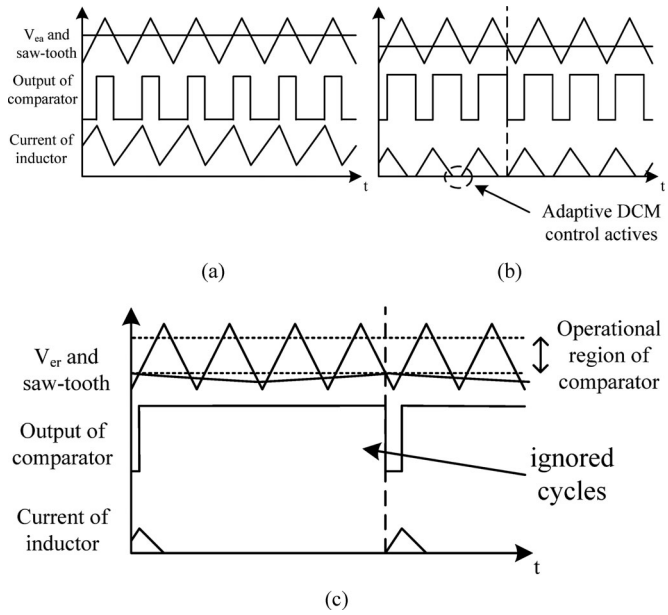

Fig. 9. Control mechanism of the reaction of the self-adaptive DCM controller. (a) Heavy load. (b) Medium load. (c) Light load.

operational region of the self-biased comparator, the comparator fails and begins to ignore switching cycles until the output of the converter drops and V_{er} climbs back into the operational region again, as shown in Fig. 9(c). The number of the ignored cycles depends on the value of the load current. If the load current is lighter, the comparator ignores additional cycles and the switching frequency of the converter is slower.

Compared to the similar control circuit presented in [22], the proposed controller uses the unique characteristic of the self-biased comparator to exhibit an adaptive switching frequency without using additional current and voltage sources and complex control circuits. Thus, the switching loss and the power cost are reduced.

B. Low-Swing/Full-Swing Buffer

The calculation and modeling results presented in [23] indicate that, depending on the load current, the driving voltage should be linearly changed to yield the lowest driving loss. However, this solution expends excessive power, particularly at the high switching frequencies used in fully-integrated dc–dc converters. A constant low-swing voltage to drive n-type power transistors at all load current ranges is used in [17]. This solution reduces the driving loss at a light-load current, but increases the conduction loss at a heavy-load current, because of the high turn-on resistance of the power transistor. Therefore, this study presents a two-level solution to maintain efficiency at all loading ranges.

The power consumption by a charging gate capacitor of power transistors is given in (1) and (2) for full-swing and low-swing condition, respectively [17]. Fig. 10 shows the simulation results of efficiency under low-swing and full-swing conditions, where the low-swing solution improves 9% efficiency compared to the

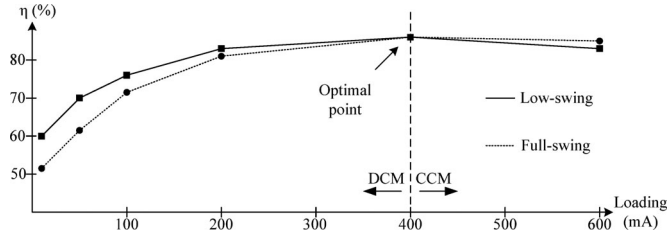

Fig. 10. Simulation results of low-swing driving voltage and full-swing driving voltage.

full-swing solution at 10-mA load current

$$P_{\text{gate}} = C_{\text{gate}} \times V_{\text{in}}^2 \times f_{\text{sw}} \quad (1)$$

$$P_{\text{gate}} = C_{\text{gate}} \times V_{\text{in}} \times V_{\text{LS}} \times f_{\text{sw}} \quad (2)$$

where V_{LS} is low-swing voltage (1.2 V in this paper) and V_{in} is the supply voltage (1.8 V in this paper).

By the results in Fig. 10, the proposed converter is designed to operate with low-swing driving voltage when the load current is under 400 mA and to operate with full-swing driving voltage when the load current is over 400 mA for reducing the power loss. Fig. 11 shows the schematic of the low-swing/full-swing buffer. The voltage across the diode-connected transistor (M_{b2}) produces a low-swing output signal ($n\_\text{out} = V_{\text{in}} - V_{\text{th}}$, where V_{th} is the threshold voltage of M_{b2}) of approximately 1.2 V. Switches S_1 and S_2 decide whether *n*_out is full-swing or low-swing signal. *n*_in is the output from the self-adaptive DCM controller and *n*_out is the signal that drives the n-type power transistor. Two switches decide whether the buffer output voltage is 1.2 or 1.8 V and the error amplifier output controls the switches.

C. Phase Controller

The advantages of a two-phase structure are increased output power and decreased output ripples [24], because the two phases share the output current and compensate for each other by using opposite phases. When the converter operates in the DCM, the advantages of the two-phase structure cease to exist, especially at light load. The switching frequency in the DCM at light-load current is typically much lower compared with half the f_{CCM}, and the idle situations between switching cycles are longer than the switching cycle itself. Under this condition, the two phases of the converter no longer compensate for each other and the output ripple is not improved, compared to the converter at heavy-load current. From the results in Fig. 12(a), the output ripples of single-phase and two-phase structure are almost the same at light-load current (under 100 mA). The simulated efficiencies of the proposed converter with single-phase and two-phase structures are shown is Fig. 12(b). Additional power consumed by the controller of the second phase lowers efficiency of the two-phase structure at light-load current. Consequently, the second phase of the proposed converter is designed to be shut down at light-load current and the converter is turned into a single-phase structure to save power consumption. When the load current is heavy, the second phase is activated, providing additional output power and a decreased output ripple.

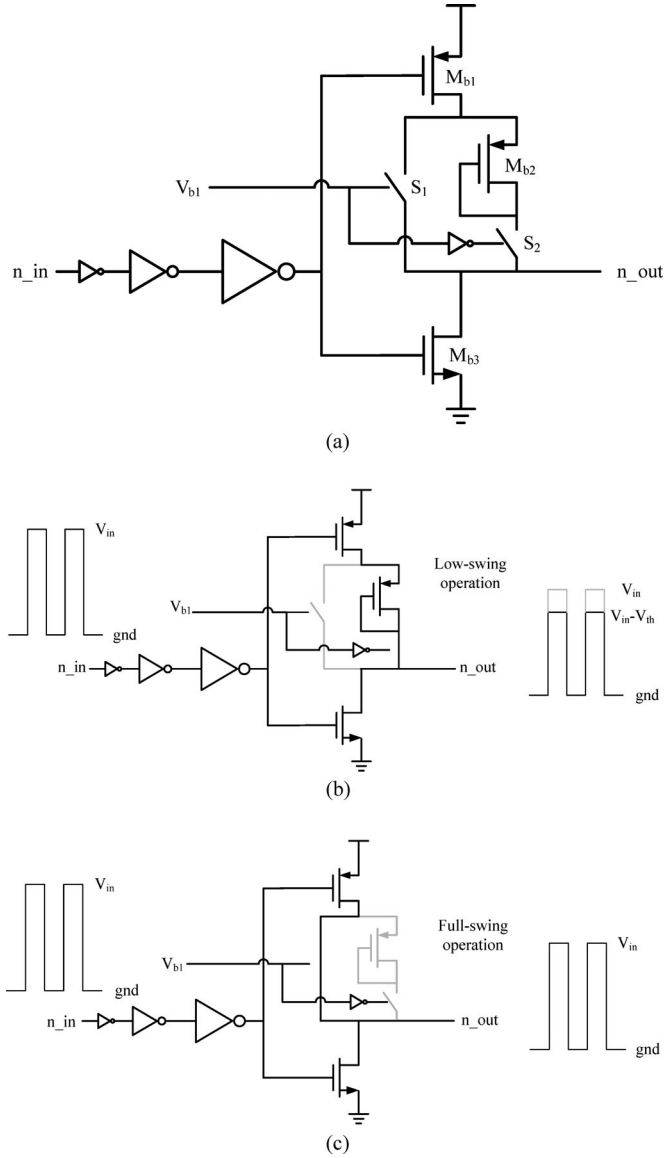

Fig. 11. Low-swing/full-swing buffer and operation principle. (a) Schematic. (b) Low-swing operation. (c) Full-swing operation.

Equation (3) illustrates the characteristic of voltage-mode dc–dc converters operating in the DCM [25]. If V_i and V_o are constant, the output of the error amplifier, which determines the duty-cycle *D*, decreases when the load current decreases, as shown in Fig. 13. Thus, the load current condition can be simply estimated by monitoring the output of the error amplifier in the DCM. The buffer and phase controller are shown in Fig. 14

$$\frac{V_o}{V_i} = \frac{D^2}{D^2 + \frac{1}{4}\left(I_o \Big/ \left(\frac{T_s V_i}{8L}\right)\right)} \quad (3)$$

where I_{o} is the load current, T_{s} is the cycle time of the converter, *D* is the duty-cycle, and *L* is the value of the inductor.

Summarizing all the improvements presented earlier, the load current range of the proposed can be defined as three

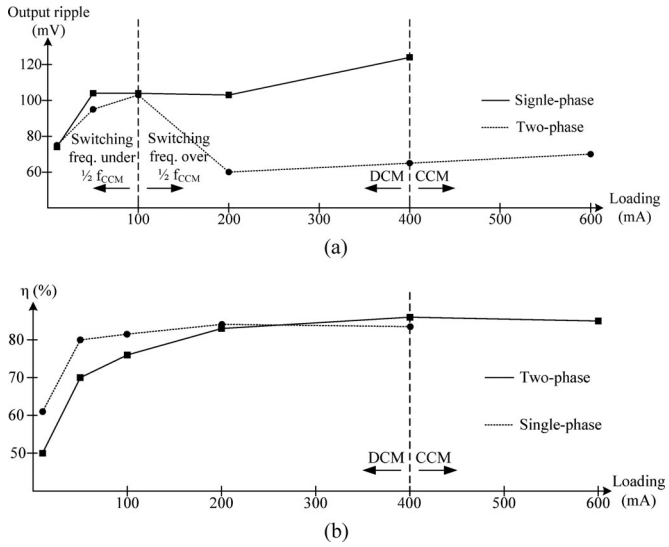

Fig. 12. Simulated output ripples and efficiencies of the converter with single-phase and two-phase structures. (a) Output ripples. (b) Efficiencies.

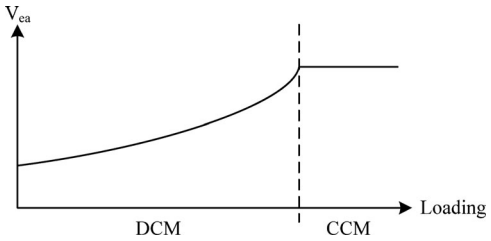

Fig. 13. Relationship between V_{ea} and load current.

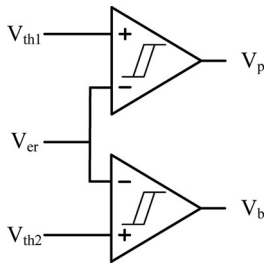

Fig. 14. Buffer and phase controller.

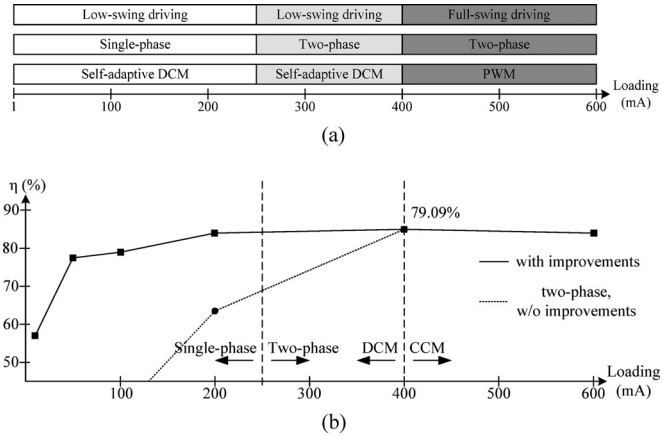

Fig. 15. (a) Different operations at different load currents. (b) Efficiency difference between two-phase converter with and without improvements.

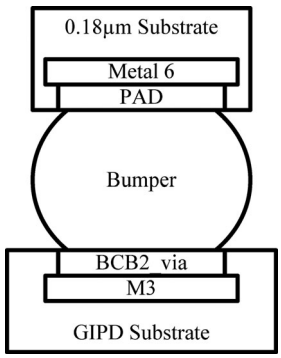

Fig. 16. Diagram of combining GIPD and CMOS dies.

different stages: single-phase DCM for light-load current, two-phase DCM for medium load current, and two-phase CCM for heavy-load current, as shown in Fig. 15(a). The efficiency improved from a two-phase converter without improvements presented earlier is shown in Fig. 15(b). The two-phase converter without improvements yields efficiency of 64% at load current of 200 mA and 13% at load current of 10 mA.

D. Passives in GIPD Processes

Although several circuits are added to the converter to improve its efficiency, this improvement is also limited by the quality of the passive components, particularly that of the inductor. Recent studies have indicated that the low-resistance inductors for use in fully-integrated converters come from the package, including bondwire and package frames [17]–[19]. These studies have demonstrated that the series resistance of on-chip inductors is approximately 150–250 mΩ/nH, whereas the series resistance of package inductors, which is typically smaller, is approximately 50 mΩ/nH. Package inductors substantially improve efficiency levels when the series resistance is low, but the process variation of these inductors is more severe compared with that of on-chip inductors. Package inductors can vary from 1.5 to 9 nH, depending on the techniques used. The variation of the package inductor can exceed 50%, which causes the prediction of operational boundaries to be difficult. Other techniques of realizing inductor for integration target only on power converters, such as magnetic film inductors [26]–[33]. These techniques provide high-quality inductors increasing the performance of converters but not for the integration of the system. The GIPD process was originally used to fabricate the passive components of RF or wireless communication circuits, to provide inductors that exhibit a low series resistance (approximately 80 mΩ/nH), and decrease the substrate loss of the passive components at high frequencies by using glass substrates. Therefore, using a GIPD process can yield high-quality inductors for converters, and facilitate integration for a whole system, as shown in Fig. 2(c). Using the CMOS and GIPD process

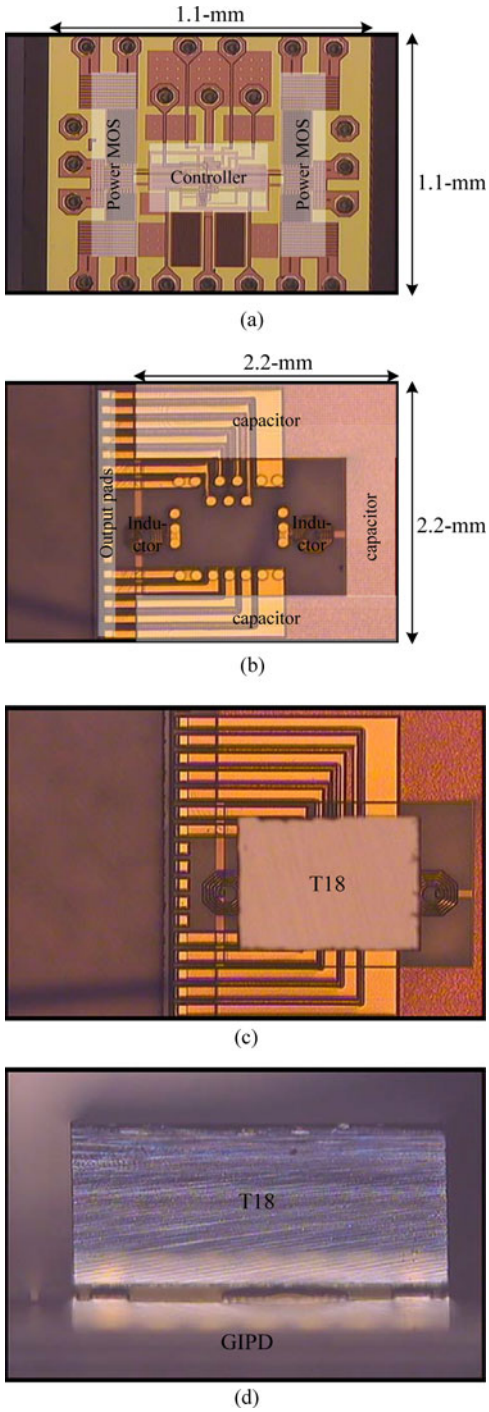

Fig. 17. Micrographs of the proposed converter. (a) Die photograph of T18 chip and the bumpers around the chip. (b) Die photograph GIPD chip with inductors, capacitors, and output pads. (c) Top view of the two chips stacked together. (d) Side view of the two chips.

to fabricate fully-integrated converters with passives involves stacking the controller die (using a typical 0.18-μm process) on the GIPD die and connecting the dies by using a solder ball as the bumper, as shown in Fig. 16. The input and output pads are built on the GIPD die, packing the stack structure into one package. The stack structure and bumper provide space to dissipate the heat generated by the converter thereby reducing the possibility of damaging the chip.

TABLE I
PERFORMANCE SUMMARY

Parameter	Value
Technology	TSMC 180 nm + GIPD
Peak efficiency	85.98%—simulation/79.09%—measurement
Max output power	720 mW
Input voltage	1.8–2 V
Output voltage	1.2 V
Max. output ripple	110 mV—simulation/125 mV—measurement
Max. switching freq.	70 MHz—simulation/50 MHz—measurement
Load regulation	35.22 mV/A
L/*C*	6 nH*2/15 nF
Series resistance of *L*	0.5 Ω each

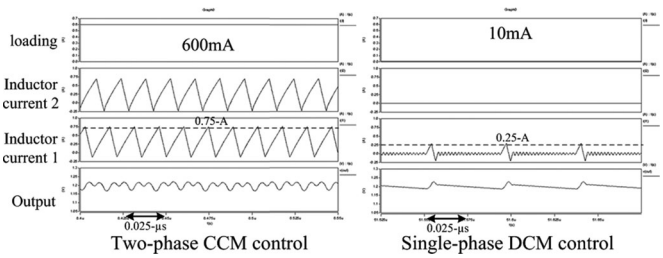

Fig. 18. Simulation results of the proposed converter at different load currents.

III. RESULTS AND COMPARISON

The proposed converter was designed using the TSMC 0.18-μm CMOS 1P6M process and the tMt GIPD process. Fig. 17 shows the micrographs of the proposed converter. The area of T18 chip was 1.21 mm^2 and that of GIPD chip was 4.84 mm^2. Each inductor on GIPD chip occupies 0.1 mm^2. The other GIPD area was filled with a dummy capacitor to satisfy the area requirement of the tape-out chip. The input voltage was 1.8 V and the converter output voltage was 1.2 V. The switching frequency was fixed at 70 MHz to facilitate CCM operation. The passive components used in the converter were two inductors of 6 nH and one output capacitor of 15 nF. Table I summarizes the performance of the proposed converter.

Fig. 18 shows the simulated results in a steady state at heavy-load current and light-load current, which clearly demonstrates the phase and switching frequency differences between various load conditions. If the load current is extremely heavy, the converter operates in the CCM at a switching frequency of 70 MHz. When the load current begins decreasing, the converter begins to operate in the DCM and the switching also decreases.

Fig. 19 shows the chip measurement at a load current of 1 mA and Fig. 20 shows the transient response results. Because of the loading of the test instruments, the frequency of the clock and saw-tooth signal were slightly slower compared with the expected values and the output ripple in the CCM was larger compared with that was in the simulated results. The ripple in the DCM is not closely related to the frequencies of the clock and saw-tooth. Thus, the output ripple in the DCM is not severely affected, causing the output ripple at a heavy-load current to be larger compared with that at a light-load current, as shown

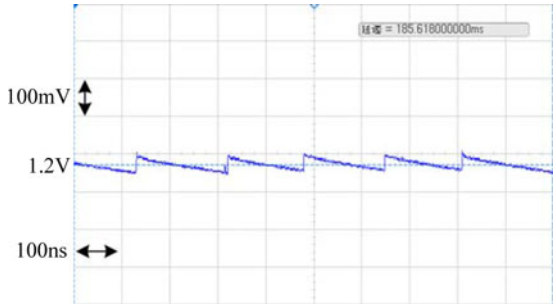

Fig. 19. Measurement results of output voltage at load current of 1 mA.

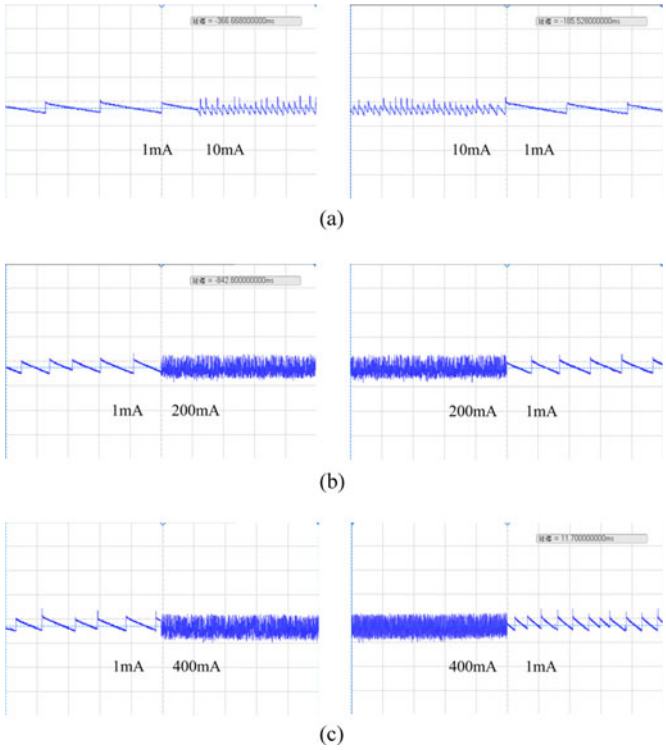

Fig. 20. Measurement results of transient response.

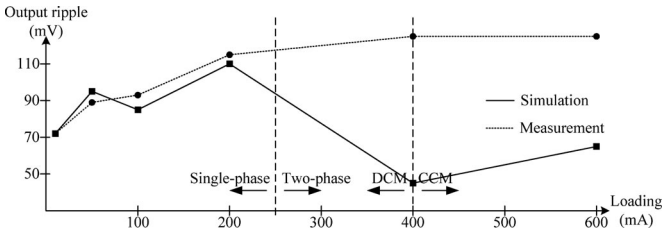

Fig. 21. Output ripple at different load currents.

in the measurement results of Figs. 21 and 22. To satisfy the requirements to tape-out chips of T18 and GIPD, all the pads of the proposed converter are designed at the left of the chips, which causes additional loading coming from the long power path and bonding, and the measured switching frequency is decreased to 50 MHz and the peak efficiency is 4% lower than

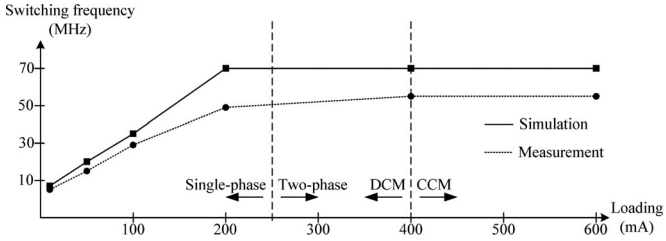

Fig. 22. Switching frequency at different load currents.

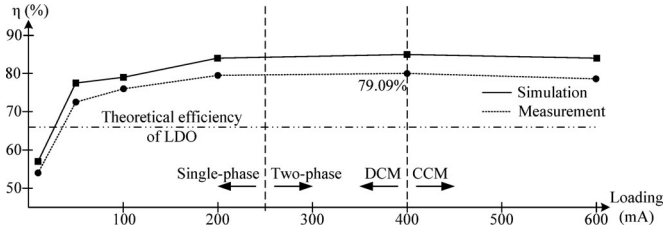

Fig. 23. Efficiency at different load currents.

the expectation. Fig. 23 displays the efficiency of the simulations and measurements.

Table II shows a comparison of the performance of the proposed fully-integrated converter and the converters developed in other studies. Compared with [11]–[14], which utilized the CMOS process to realize both converters and passives, the proposed controller yields a good performance that approximates 80% efficiency with small passives of two 6-nH inductors and one 15-nF capacitor. Compared with [17]–[19], which used package inductors, the proposed converter uses accurate inductors on the GIPD process to decrease the variation of operation condition of the converter and to reduce the needs of additional external pins of the package. Compared to our previous work in simulation using the same GIPD process [20], the proposed converter has higher peak efficiency and efficiency at 10 mA in measurement. With the circuit-level improvements and low-loss passives on GIPD, the proposed work shows a high performance power solution for functional SiP systems.

IV. Conclusion

The proposed two-phase fully-integrated dc–dc converter was designed with passives using the GIPD process and involved circuit-level improvements. The proposed self-adaptive DCM controller and low-swing/full-swing buffer reduce the switching loss at light-load currents. The phase control increases the output power and decreases the output ripple at heavy-load currents. The GIPD process provides low-loss passives that improve efficiency levels. Because of these improvements, passive components can be integrated in the dc–dc converter, simultaneously yielding high performance levels. The peak efficiency was 79.09% at a load current of 400 mA when converting 1.8 to 1.2 V. The inductors were approximately 6 nH and the capacitor was 15 nF. The proposed converter yielded a higher efficiency compared with that of an LDO regulator at load currents exceeding 50 mA. The SiP concept presented in this paper

TABLE II
COMPARISON TABLE

Ref.	[11]	[12]	[13]	[14]	[17]	[18]	[19]	[20]	**This work**
Source	2011 JSSCC	2011 ITPE	2012 ITPE	2012 JSSCC	2012 ITPE	2013 JSSCC	2013 JSSCC	2012 ISCAS	
Process	130 nm CMOS	130 nm CMOS	250 nm BiCMOS	130 nm CMOS	130 nm CMOS	130 nm CMOS	130 nm CMOS	180 nm CMOS + GIPD	180 nm CMOS + GIPD
$V_{\rm in}$	1.2 V	2.6 V	3.6 V	2.4 V	2.5∼3.3 V	1.2 V	1.2 V	1.8 V	1.8 V
$V_{\rm out}$	0.88 V	1.2 V	2.2 V	0.4∼1.4 V	1.8∼2 V	0.9 V	0.6∼1.05 V	0.6∼1.3 V	1.2 V
Number of phase	1-phase	4-phase	1-phase	2, 2-phase	1-phase	1-phase	1, 2, 4-phase	1 phase	1, 2-phase
Topology	PWM+PFM	DCM	PWM	3-level converter	PWM	PWM+DCM	PWM+DCM	PWM	PWM+DCM
Switching frequency	200 MHz	N/A	200 MHz	50–200 MHz	50 MHz	100 MHz	100 MHz	200 MHz	1–50 MHz
Max. output power	266 mW	800 mW	723 mW	1 W	600 mW	333 mW	1.26 W	195 mW	720 mW
Peak efficiency	77%	58%	77%	77%	76.8%	84.7%	82.4%	78.5% (simulation)	79.09%
Efficiency at 10 mA	55%	57%	N/A	N/A	35%	75%	N/A	40%	55%
Inductor	2 nH	4*3.9 nH	51 nH	4*1 nH	19.9 nH (package)	>3 nH (package)	2*1.5 nH / 2*4 nH (package)	9 nH (GIPD)	2*6 nH (GIPD)
Capacitor	5 nF	12.17 nF	4.7 nF	18 nF/10 nF	3.4 nF/ 3nF	9.8 nF	3.37 nF	3 nF (GIPD)	15 nF (GIPD)
Chip size	1.59 mm^2	3.76 mm^2	N/A	∼4.8 mm^2	10.08 mm^2 (package inductor)	2.25 mm^2 (package inductor)	2 mm^2 (package inductor)	22.9 mm^2 (GIPD)	4.84 mm^2 (GIPD)

involves dividing the entire system into two parts: circuits and passives. The circuits can be readily designed using standard CMOS processes (e.g., 0.18 μm) and the major passives can be fabricated using the GIPD process, thereby reducing the losses of the passives. Thus, the proposed GIPD process provides both high-quality passive components and a solution for designing SoC or SiP systems.

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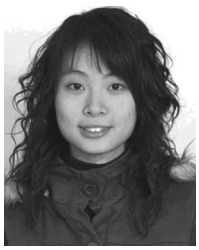

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