A Digitally Controlled Critical Mode Boost Power Factor Corrector With Optimized Additional On Time and Reduced Circulating Losses

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***Abstract*—In many low-to-mid power applications, critical mode boost power factor corrector converters are widely used because of its low switching loss and simple control. However, near the zero crossing of the input line voltage, an input current distortion and a low power factor are caused by delayed switching period and negative input currents. Generally, an additional on-time method according to the input voltage is used to compensate the input current distortion. However, a detailed quantitative analysis for the exact additional on time has not been studied till now. In this paper, the explicit form of the optimized additional on time has been obtained using a quantitative analysis and the advantage of the digital control. From a state trajectory and "net input charge" analysis, it is shown that the optimized on time should be related to not only the input voltage, but also the output power. Also, in order to improve the efficiency in a high input and light load condition, circulating currents are reduced in the inevitable dead angle with a gate turning-off technique. By using digital control, the optimized additional on time and the gate turn-off technique have been implemented with the 90–230 $V_{\rm rms}$ input and 380 V/200 W output prototype.**

***Index Terms*—Additional on time, critical mode (CRM) boost power factor corrector (PFC), digital control.**

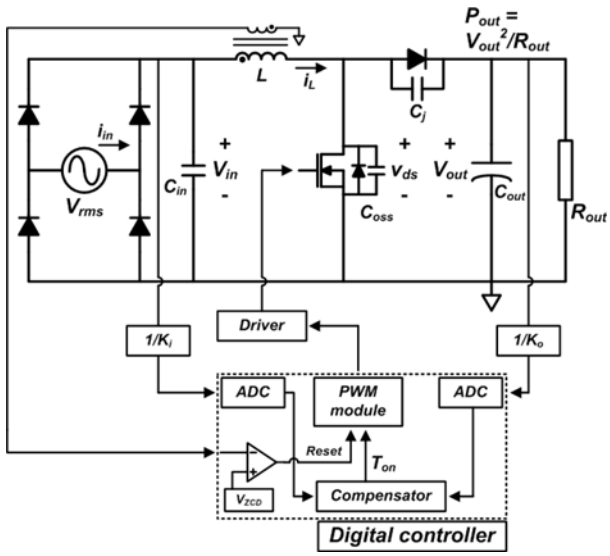

Fig. 1. Schematic diagram of a digitally controlled CRM boost PFC.

I. Introduction

THE input current shape of an offline power supply should be in-phase with the input voltage for a high power factor (PF) and a low total harmonic distortion (THD). This is because an effective power delivery and minimizing unfavorable effects on the other electronic devices using the same ac line are required. For these reasons, boost power factor corrector (PFC) converters are widely used, due to its input-current-control capability. The control methods for boost PFC converters can be divided according to its output power. In high power applications, continuous conduction mode (CCM) PFC is used to reduce the ripple currents and the conduction losses. However, in low-to-mid power applications, critical conduction mode (CRM) boost PFC is widely used although it has a large ripple current, because of its low switching losses and simple constant on-time control [1]–[13].

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Nowadays, the digital control of power converters comes into the spotlight, because of its flexible control, reduced components, and no aging problems. For these reasons, a digital control of the CRM boost PFC has also been studied by many researchers [1]–[3], [16]. Fig. 1 shows a schematic diagram of a digitally controlled CRM boost PFC. As shown in Fig. 1, the input and output voltages are sensed by two analog-to-digital converter (ADC) modules and the zero current detection (ZCD) can be implemented by using an analog comparator in the digital controller. The on-time of the main switch ($T_{\rm on}$) is determined by a digital compensator using the output voltage ($V_{\rm out}$). The ZCD enables the switch to be turned on when the voltage across the switch ($v_{\rm ds}$) is the minimum value, to minimize the switching losses. However, this valley switching results in negative currents of the boost inductor and a delay time in a switching period, causing a distortion of the input current especially near the zero crossing of the ac input voltage ($V_{\rm ac_{rms}}$).

In order to reduce the input current distortion, the additional on-time methods have been developed by researchers [4], [5]. The additional on-time methods can cancel out the effect of the delayed switching period and negative inductor current, because it allows the inductor current to build up more. Because the distortion factors become larger when the input voltage of the boost PFC ($V_{\rm in}$) is smaller, the methods use a larger additional on time as $V_{\rm in}$ decreases. Also, the additional on-time methods prevent

the switching frequency from increasing near the zero crossing of the ac input voltage. Because of its simplicity and significant improvement, the commercial IC and many researchers also adopted it [4]–[6], [15]. However, many previous research studies use only the input voltage to obtain the additional on time. Since the distortion factors are dependent on not only the input voltage but also the output power, only considering the input voltage cannot provide an optimized additional on time. Despite the fact that the optimized on time considering both the input voltage and output power is not studied yet, it is impossible to obtain high PF in the entire input voltage and load conditions. Also, the trial-and-error method is unavoidable to obtain the optimized additional on time, causing difficulties for the design procedure.

In this paper, the optimal additional on time is obtained according to both the input voltage and output power. By using a state trajectory analysis and "net input charge" concept, it is shown that the optimal additional on time depends on both the input voltage and the output power. Also, a simplified form of the additional on time is obtained, so that it can be implemented with a cost-effective controller. Because the proposed research provides the optimal additional on time according to both the input voltage and the output power, the CRM boost PFC converter with the proposed control can have a high PF in the entire input and load conditions. Although the proposed method provides the ideal envelope of the additional on time, mismatches of the component value and parasitic components makes it hard to obtain a unity PF, causing an inevitable dead angle and circulating losses especially in high input voltage and light load conditions. Because circulating current during the dead angle results in decreased light load efficiency, the gate turning-off technique to reduce the circulating losses is also presented in this paper.

II. State Trajectory and Actual Average Input Current Analysis

In this section, a state trajectory analysis and the actual average input current of CRM boost PFC during a switching period are studied. In order to avoid complexity, some assumptions are made as follows:

1) $V_{\rm in}$ is constant during several switching periods, because the switching frequency is much larger than that of the input ac voltage;
2) the main switch is turned ON when $v_{\rm ds}$ reaches the minimum value.

A. State Trajectory and the Input Charge Analysis

Case I ($V_{\rm in} > V_{\rm out}/2$): Fig. 2 shows the key waveforms and the state trajectory of the CRM boost PFC, when $V_{\rm in}$ is larger than $V_{\rm out}/2$. In this case, the switch is turned ON with the valley switching when $v_{\rm ds}$ is equal to $2V_{\rm in} - V_{\rm out}$. Because the switch is turned ON when $v_{\rm ds}$ is minimum, i_L is zero at t_0. The inductor current builds up with the slope of $V_{\rm in}/L$ during the on time ($T_{\rm on}$). The input charge during $T_{\rm on}$ ($Q_{\rm on}$) can be obtained as $V_{\rm in}T_{\rm on}^2/2L$ by integrating i_L. After the switch is turned OFF,

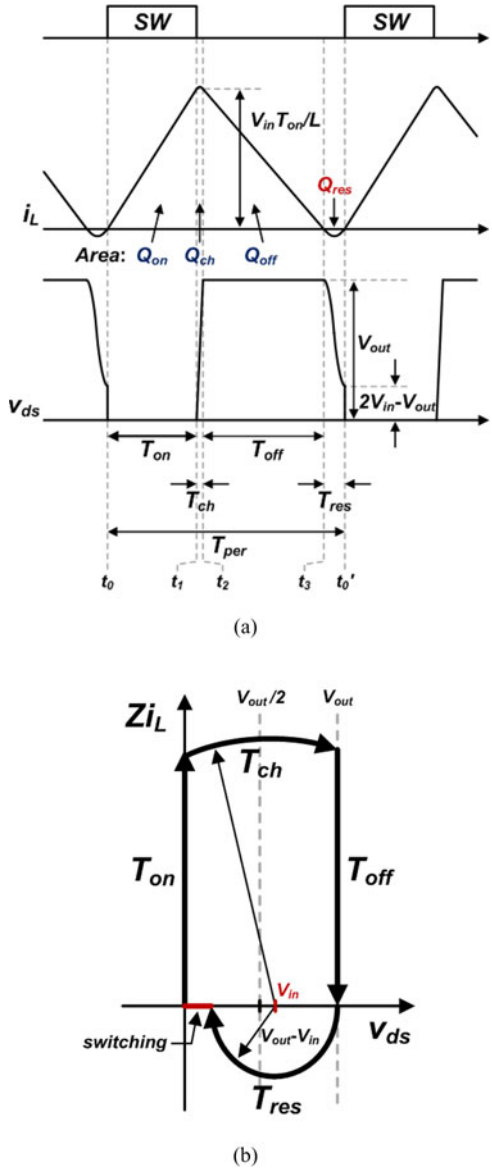

Fig. 2. CRM boost PFC in case I ($V_{\rm in} > V_{\rm out}/2$). (a) Its key waveforms and (b) state trajectory.

$v_{\rm ds}$ and i_L can be expressed as follows:

$$Zi_L(t) = V_{\rm in}\sin(\omega(t-t_1)) + Zi_L(t_1)\cos(\omega(t-t_1)) \quad (1)$$

$$v_{\rm ds}(t) - V_{\rm in} = Zi_L(t_1)\sin(\omega(t-t_1)) - V_{\rm in}\cos(\omega(t-t_1)) \quad (2)$$

$$(v_{\rm ds} - V_{\rm in})^2 + (Zi_L)^2 = V_{\rm in}^2 + (Zi(t_1))^2 \quad (3)$$

where $C = C_{\rm oss} + C_j$, $Z = \sqrt{L/C}$, and $\omega = 1/\sqrt{LC}$. As shown in (3) and Fig. 2, the trajectory of $v_{\rm ds}(t)$ and $Zi_L(t)$ during the time $C_{\rm oss}$ and $C_j(T_{\rm ch})$ are charged and discharged follows a circle, which has the center at $(V_{\rm in}, 0)$ and the radius of $\sqrt{V_{\rm in}^2 + (Zi(t_1))^2}$. Because $i_L(t_1)$ is very large during $T_{\rm ch}$, the change of i_L is small enough to be neglected. The input charge during $T_{\rm ch}$ ($Q_{\rm ch}$) is $CV_{\rm out} = (C_{\rm oss} + C_j)V_{\rm out}$ by the charge conservation rule, because the capacitors are charged and discharged from zero voltage to $V_{\rm out}$. After $v_{\rm ds}$ reaches $V_{\rm out}$, i_L

decreases linearly. During the time i_L decreases to zero ($T_{\rm off}$), the input charge ($Q_{\rm off}$) is almost equal to $V_{\rm in}^2 T_{\rm on}^2/2L(V_{\rm out}-V_{\rm in})$. The exact expression of $Q_{\rm off}$ will be considered in case III. After i_L reaches zero, $v_{\rm ds}$ begins to decrease due to the *LC* resonance. $v_{\rm ds}(t)$ and $i_L(t)$ can be expressed as follows:

$$Zi_L(t) = (V_{\rm out}-V_{\rm in})\sin(\omega(t-t_3)) \tag{4}$$

$$v_{ds}(t)-V_{\rm in} = (V_{\rm in}-V_{\rm out})\cos(\omega(t-t_3)) \tag{5}$$

$$(v_{ds}-V_{\rm in})^2+(Zi_L)^2 = (V_{\rm out}-V_{\rm in})^2 \tag{6}$$

where $C=C_{\rm oss}+C_j$, $Z=\sqrt{L/C}$, and $\omega=1/\sqrt{LC}$. As shown in (6) and Fig. 2, during the valley switching resonance ($T_{\rm res}$), the trajectory of $v_{\rm ds}(t)$ and $Zi_L(t)$ follows a circle, which has the center at $(V_{\rm in},0)$ and the radius of $V_{\rm out}-V_{\rm in}$. During $T_{\rm res}$, the amount of the negative charges ($Q_{\rm res}$) is $2C(V_{\rm out}-V_{\rm in})$ by the charge conservation, because the voltage across switch is decreased by $2V_{\rm in}$. The switch is turned on when $V_{\rm ds}=2V_{\rm in}-V_{\rm out}$, and the boost converter starts the next switching period.

Case II ($V_{\rm in}<V_{\rm out}/2$): Fig. 3 shows the key waveforms and the state trajectory of the CRM boost PFC, when $V_{\rm in}$ is smaller than $V_{\rm out}/2$. In this case, the switch is turned on with the zero voltage switching (ZVS) when $v_{\rm ds}$ is equal to 0. Because the switch is turned on before i_L becomes zero, i_L is still negative during T_n. By rearranging (4) and (5), $i_L(t_0)$, T_n, and the amount of negative charge during $T_n(Q_n)$ can be obtained as follows:

$$i_L(t_0) = \frac{1}{\omega}\sin\left(\arccos\left(\frac{V_{\rm in}}{V_{\rm in}-V_{\rm out}}\right)\right) = \frac{V_{\rm in}-V_{\rm out}}{Z}\sqrt{1-\left(\frac{V_{\rm in}}{V_{\rm in}-V_{\rm out}}\right)^2} \tag{7}$$

$$T_n = -\frac{L}{V_{\rm in}}i_L(t_0) = \frac{L}{Z}\sqrt{\left(\frac{V_{\rm out}-V_{\rm in}}{V_{\rm in}}\right)^2-1} \tag{8}$$

$$Q_n = -\frac{L}{2V_{\rm in}}i_L^2(t_0) = \frac{CV_{\rm out}}{2V_{\rm in}}\left(V_{\rm out}-2\frac{V_{\rm in}}{V_{\rm out}}\right). \tag{9}$$

In this case, $i_L(t_1)$ is equal to $V_{\rm in}(T_{\rm on}-T_n)/L$ and the sum of $Q_{\rm on}$ and $Q_{\rm off}$ can be obtained as $V_{\rm in}(T_{\rm on}-T_n)^2/2L$ by integrating i_L during $T_{\rm on}$. $Q_{\rm off}$ is the same with case I, because $i_L(t_1)$ is still large. $Q_{\rm ch}$ is equal to $CV_{\rm out}$, and $Q_{\rm res}$ is also equal to $CV_{\rm out}$ by the charge conservation because full ZVS operation is possible in case II.

Case III ($V_{\rm in}<<V_{\rm out}/2$): Fig. 4 shows the key waveforms and the state trajectory of the CRM boost PFC, when $V_{\rm in}$ is *much* smaller than $V_{\rm out}/2$. In this case, the switch is also turned on with the ZVS when $v_{\rm ds}$ is equal to 0, and i_L increases by the slope of $V_{\rm in}/L$.Q_n, $Q_{\rm on}$, $Q_{\rm ch}$, and $Q_{\rm res}$ can be obtained by the same equation with case II. However, $Q_{\rm off}$ becomes much smaller, because i_L manages to charge *C* up to $V_{\rm out}$ due to small $i_L(t_1)$ and decreases significantly during $T_{\rm ch}$. By substituting $v_{\rm ds}$ with $V_{\rm out}$ in (3), $i_L(t_2)$, $T_{\rm off}$, and the exact $Q_{\rm off}$ in all cases

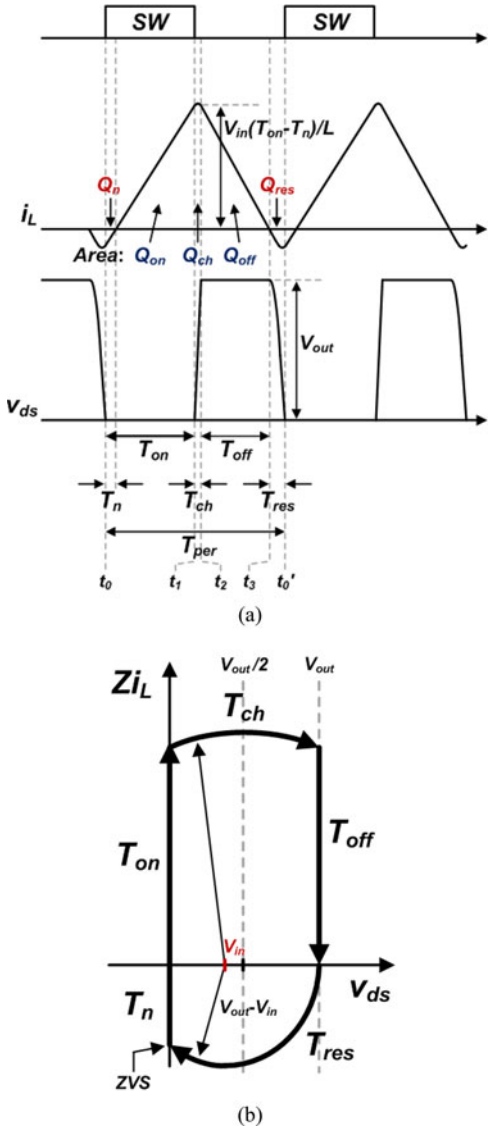

Fig. 3. CRM boost PFC in case II ($V_{\rm in}<V_{\rm out}/2$). (a) Its key waveforms and (b) state trajectory.

can be obtained as follows:

$$i_L(t_2) = \frac{V_{\rm in}}{L}\sqrt{(T_{\rm on}-T_n)^2-LC\left[\left(\frac{V_{\rm out}}{V_{\rm in}}\right)^2-2\frac{V_{\rm out}}{V_{\rm in}}\right]} \tag{10}$$

$$T_{\rm off} = \frac{Li_L(t_2)}{V_{\rm out}-V_{\rm in}} \tag{11}$$

$$Q_{\rm off} = \frac{i_L(t_3)T_{\rm off}}{2} = \frac{V_{\rm in}}{2L(V_{\rm out}-V_{\rm in})} \times\left[(T_{\rm on}-T_n)^2-LC\left\{\left(\frac{V_{\rm out}}{V_{\rm in}}\right)^2-2\frac{V_{\rm out}}{V_{\rm in}}\right\}\right]. \tag{12}$$

Case IV (dead angle): Fig. 5 shows the key waveforms and the state trajectory of the CRM boost PFC, when $V_{\rm in}$ is *close to zero* so that i_L cannot charge *C* up to $V_{\rm out}$. In this case, $T_{\rm off}$ becomes

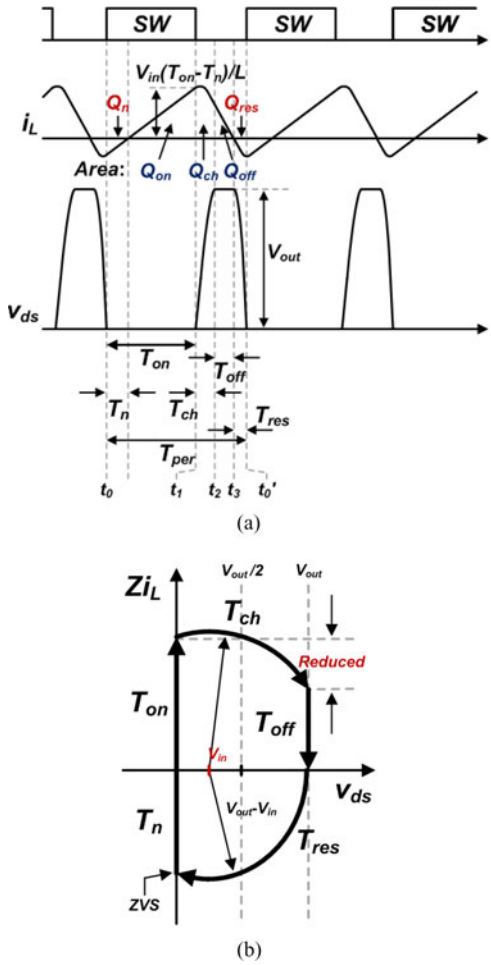

Fig. 4. CRM boost PFC in case III ($V_{\rm in} << V_{\rm out}/2$). (a) Its key waveforms and (b) state trajectory.

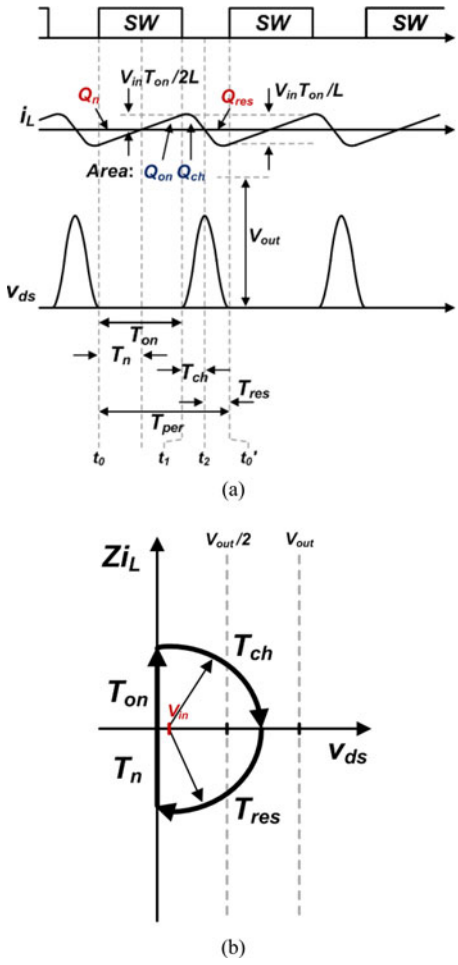

Fig. 5. CRM boost PFC in dead angle. (a) Its key waveforms and (b) state trajectory.

zero and the total input charge during a switching period also becomes zero because all input charges returns to the input side by *LC* resonance. As shown in the state trajectory, T_n becomes $T_{\rm on}/2$. This region is generally called the dead angle.

B. Actual Average Input Current During a Switching Period

From the previous analysis, the actual average input current during a switching period can be obtained. Table I shows the list of charges during a switching period in all cases. In order to obtain the average current, it is required to calculate the "net input charges" ($Q_{\rm net}$) during a switching period. The net input charges can be obtained by the following equation:

$$Q_{\rm net} = Q_{\rm pos} - Q_{\rm neg} = Q_{\rm on} + Q_{\rm ch} + Q_{\rm off} - Q_n - Q_{\rm res} \tag{13}$$

where $Q_{\rm pos}$ are the positive charges during $i_L > 0$ and $Q_{\rm neg}$ are the negative charges during $i_L < 0$.

Now, the actual average input current during a switching period ($< i_{\rm in} >_{T\rm per}$) can be obtained by dividing $Q_{\rm net}$ by a switching period ($T_{\rm per}$) as follows:

$$< i_{\rm in} >_{T\rm per} = Q_{\rm net}/(T_{\rm on} + T_{\rm ch} + T_{\rm off} + T_{\rm res}) = Q_{\rm net}/T_{\rm per}. \tag{14}$$

In this paper, an explicit form of $T_{\rm per}$ according to $V_{\rm in}$ and $V_{\rm out}$ is omitted because of the complexity and the limitation of the paper.

III. Optimal Additional On Time

In this section, the optimal additional on time which is required to obtain the unity PF is theoretically obtained. From the analysis, it is shown that the actual average input current during a switching period can be *explicitly* expressed according to $V_{\rm in}$, $V_{\rm out}$, $T_{\rm on}$, $T_{\rm per}$, L, and C. The concept of the additional on time, the additional on time required to eliminate the dead angle, and the explicit form of the optimal additional on time are discussed.

A. Concept of the Additional On-Time Technique

From Table I, it can be noted that the unwanted negative charges $Q_{\rm neg}$ depends on $V_{\rm in}$ and $V_{\rm out}$. In other words, $Q_{\rm neg}$ is independent on $T_{\rm on}$. On the other hand, the positive charges $Q_{\rm pos}$ are the function of $T_{\rm on}$. Therefore, as $T_{\rm on}$ increases, $Q_{\rm pos}$

TABLE I
LIST OF CHARGES DURING A PERIOD IN ALL CASES

Charge	Case I ($V_{\rm in} > V_{\rm out}/2$)	Case II ($V_{\rm in} < V_{\rm out}/2$)	Case III ($V_{\rm in} << V_{\rm out}/2$)	Case IV (dead angle)
$\mathbf{Q}_n$	0	$CV_{\rm out}(V_{\rm out} - 2V_{\rm in}/V_{\rm out})/2V_{\rm in}$		-
$\mathbf{Q}_{\rm on}$	$V_{\rm in}(T_{\rm on} - T_n)^2/2L$			-
$\mathbf{Q}_{\rm ch}$	$CV_{\rm out}$			-
$\mathbf{Q}_{\rm off}$	$V_{\rm in}^2[(T_{\rm on} - T_n)^2 - LC\{(V_{\rm out}/V_{\rm in})^2 - 2V_{\rm out}/V_{\rm in}\}]/2L(V_{\rm out} - V_{\rm in})$			-
$\mathbf{Q}_{\rm res}$	$2C(V_{\rm out} - V_{\rm in})$	$CV_{\rm out}$		-
$\mathbf{Q}_{\rm net}$	$Q_{\rm pos} - Q_{\rm neg} = Q_{\rm on} + Q_{\rm ch} + Q_{\rm off} - Q_n - Q_{\rm res}$			0
$< i_{\rm in} >_{Ts}$	$Q_{\rm net}/T_{\rm per} = Q_{\rm tot}/(T_{\rm on} + T_{\rm ch} + T_{\rm off} + T_{\rm res})$			0

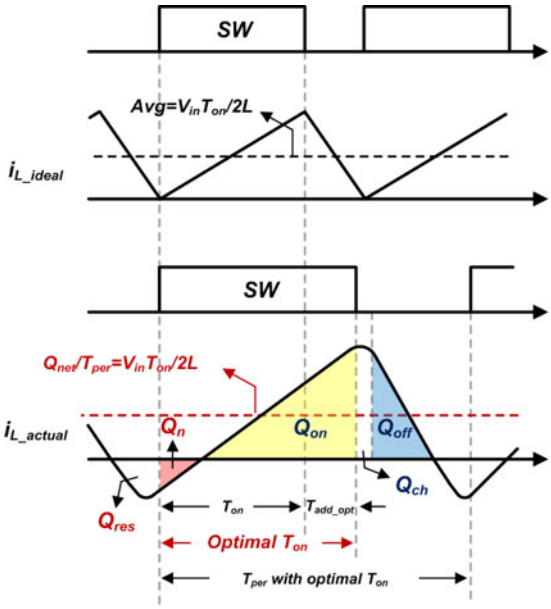

Fig. 6. Concept of the proposed optimal on-time control.

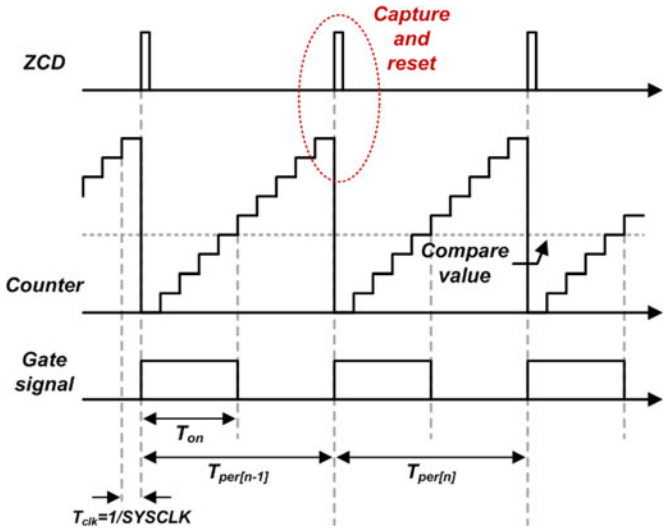

Fig. 7. Capturing a switching period in the digital controllers.

increases but $Q_{\rm neg}$ remain constant during a switching period. From the point, it can be noted that the additional on time can cancel out the distortional effect on the average input current by increasing $Q_{\rm pos}$.

B. Explicit Form of the Optimal Additional On Time ($T_{\rm add\_opt}$)

In an ideal case, as shown in the upper one of Fig. 6, the *intended* average current during a switching period ($< i_{\rm in\_int} >_T$ per) can be obtained as follows:

$$< i_{\rm in\_int} >_{T\rm per} = V_{\rm in}T_{\rm on}/2L \tag{15}$$

where the on time determined by the compensator is $T_{\rm on} = 2LP_{\rm out}/V_{\rm rms}^2$.

In the actual case, as shown in the lower one of Fig. 6, the value of the optimal additional on time ($T_{\rm add_opt}$) should make the *actual* average input current ($< i_{\rm in\_act} >_{T\rm per}$) equal to the *intended* average current during a switching period ($T_{\rm per}$) as follows:

$$< i_{\rm in\_act} >_{T\rm per} = \left.\frac{Q_{\rm net}}{T_{\rm per}}\right|_{T_{\rm on}=T_{\rm on}+T_{\rm add\_opt}} = \frac{V_{\rm in}T_{\rm on}}{2L}. \tag{16}$$

In the digital controllers, as shown in Fig. 7, it is possible to obtain the switching period by capturing the maximum value of the counter register before the reset. As mentioned in the assumptions in Section II, assuming a switching period is the same with the prior switching period ($T_{\rm per} = T_{{\rm per}[n]} \approx T_{{\rm per}[n-1]}$), the switching period of the prior cycle can be used to determine the optimal additional on time. Then, the optimal on time to obtain the unity PF and zero THD can be obtained by rearranging (16) as shown in (17) and (18)

$$T_{\rm on\_opt} = T_{\rm on} + T_{\rm add\_opt} = \sqrt{k} + T_n \tag{17}$$

where (18), as shown at the bottom of the next page.

As shown in (17) and (18), the optimal additional on time should be determined considering not only the input voltage but also the output power of the boost converter, because the optimal additional on time is also related to the output-power-related $T_{\rm on}$. Also, because $T_{\rm per}(T_n + T_{\rm on} + T_{\rm ch} + T_{\rm off} + T_{\rm res})$ is in a very complicate form to be calculated, capturing $T_{\rm per}$ in a digital controller makes it much simpler to obtain the optimal additional on time.

C. Simplified Form of the Additional On Time for Eliminating Dead Angle ($T_{\rm add\_nodead}$)

The optimal additional on time can allow the boost PFC to have an ideal input current shape. However, as shown in (17) and

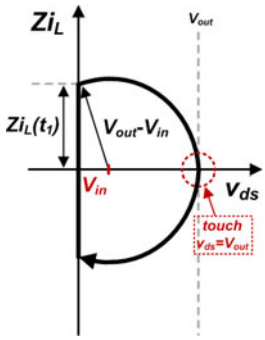

Fig. 8. State trajectory at the boundary of cases III and IV.

TABLE II
DESIGN PARAMETERS

Input voltage	90–230 $V_{\rm rms}$
Output voltage	380 V
Main switch	IPP60R125C6 ($C_{\rm oss} = 125$ pF)
Boost diode	BYV29X-600 ($C_j = 10$ pF)
C	565 pF($C_{\rm oss} + C_j + 2 \times 220$ pF)
L	230 μH
$\mathbf{C_{in}}$	470 nF
$\mathbf{C_{out}}$	164 μF
Controller	TMS320F28069PZT
Capturing period	Using eCAP module

(18), their form is very complicated so that it is inevitable to use a lower sampling frequency or a high-cost digital controller. For these reasons, a simple additional on-time form is also presented in this paper. The simplified additional on time aims to remove the dead angle.

In order to obtain the minimum additional on time for eliminating dead angle, the condition for the dead angle can be obtained from Fig. 8. From the state trajectory, it can be noted that the dead angle occurs when a state trajectory is located at the boundary of cases III and IV. In this case, the trajectory touches the line $v_{\rm ds} = V_{\rm out}$, and T_n is equal to $T_{\rm on}/2$ because of the symmetry. The boundary of the dead angle can be obtained geometrically as follows:

$$(Zi_L(t_1))^2 + V_{\rm in}^2 = (ZV_{\rm in}T_{\rm on}/2L)^2 + V_{\rm in}^2 = (V_{\rm out} - V_{\rm in})^2. \tag{19}$$

With given Z, L, $V_{\rm out}$, and $V_{\rm in}$, the minimum $T_{\rm on}$ to avoid the dead angle can be obtained by rearranging (19) as follows:

$$T_{\rm on} > \frac{2LV_{\rm out}}{ZV_{\rm in}}\sqrt{1 - 2\frac{V_{\rm in}}{V_{\rm out}}}. \tag{20}$$

Also, with given Z, L, $V_{\rm out}$, and $T_{\rm on}$, the minimum $V_{\rm in}$ to avoid dead angle can also be obtained by rearranging (20) as follows:

$$V_{\rm in} > \frac{4L^2V_{\rm out}}{Z^2T_{\rm on}^2}\left(-1 + \sqrt{1 + \frac{Z^2T_{\rm on}^2}{4L^2V_{\rm out}^2}}\right). \tag{21}$$

From (21), the minimum additional on time for eliminating dead angle ($T_{\rm add\_nodead}$) can be obtained as follows:

$$T_{\rm add\_nodead} = \frac{2LV_{\rm out}}{ZV_{\rm in}}\sqrt{1 - 2\frac{V_{\rm in}}{V_{\rm out}}} - T_n \tag{22}$$

when $T_{\rm add_nodead} > 0$.

By adding $T_{\rm add\_nodead}$ to $T_{\rm on}$ determined by the compensator, a CRM boost PFC can eliminate the dead angle in the entire ac input voltage angles. Compared with (17), the simplified additional on time has a much simpler form, allowing a reduced calculation time of the digital controller.

The optimal on-time calculation requires several square roots and divisions. The complexity results in a long calculation time so that the sampling frequency of the system could be small. High-cost and fast digital controller is required to obtain a high sampling frequency. However, because the cutoff frequency of the control loop of the boost PFC is very low (e.g., 10 Hz), high sampling frequency is not required. Also, the simplified form of the additional on time is presented to reduce the calculation time, so that it can be implemented with a cost-effective digital controller. Furthermore, the calculation time can be reduced using lookup tables for square rooting and dividing calculations.

IV. IMPLEMENTATION AND EXPERIMENTAL RESULTS

In order to prove the effectiveness of the proposed method, it is designed with a prototype of 90–230 $V_{\rm rms}$ input and 380 V/200 W output CRM boost PFC. Table II shows the design result of the boost converter. In the prototype, the parameters and switching frequency are selected considering the tradeoff to maximize the efficiency of the prototype. IPP60R125C6($C_{\rm oss} = 125$ pF) and BYV29X-600($C_j = 10$ pF) are selected as the main switch and boost diode, respectively. In order to remove a voltage spike right after the switch is turned off, 220 pF capacitors are connected in parallel with the main switch and diode. Therefore, the total capacitance during the resonance for valley switching of the CRM boost PFC (C) becomes 565 pF($C_{\rm oss} + C_j + 2 \times 220$ pF). L is selected as 230 μH. The input capacitor $C_{\rm in}$ is selected as 470 nF. The output capacitor $C_{\rm out}$ is selected as 164 μF. TMS320F28069PZT is used as the digital controller. The switching frequency varies about from 50 to 300 kHz. Capturing period can be implemented using eCAP module in the controller [14]. The proposed method provides the optimized additional on time with the given converter parameters.

$$k = \begin{cases} \left(1 - \dfrac{V_{\rm in}}{V_{\rm out}}\right)T_{\rm on}T_{\rm per} + LC\left(\left(\dfrac{V_{\rm out}}{V_{\rm in}}\right)^2 - 4\right), & \text{when } V_{\rm in} < \dfrac{V_{\rm out}}{2}. \\ \left(1 - \dfrac{V_{\rm in}}{V_{\rm out}}\right)T_{\rm on}T_{\rm per} + LC\left(3\dfrac{V_{\rm out}}{V_{\rm in}} + 4\dfrac{V_{\rm in}}{V_{\rm out}} - 8\right), & \text{when } V_{\rm in} > \dfrac{V_{\rm out}}{2} \end{cases} \tag{18}$$

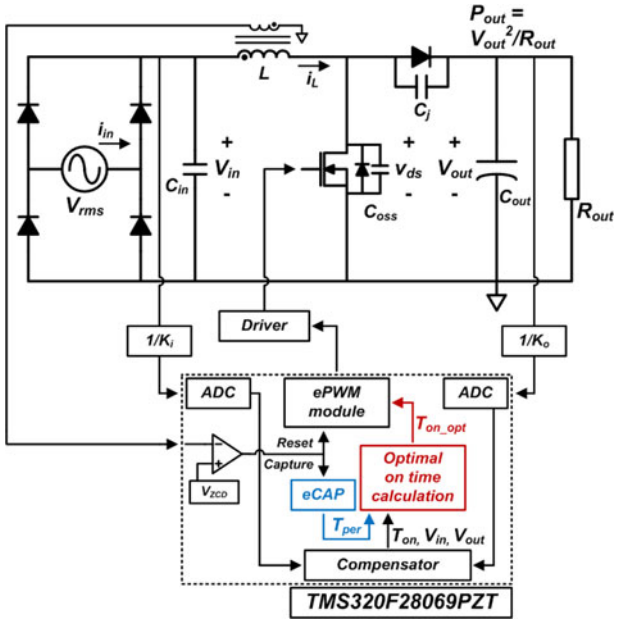

Fig. 9. Implementation of the proposed control.

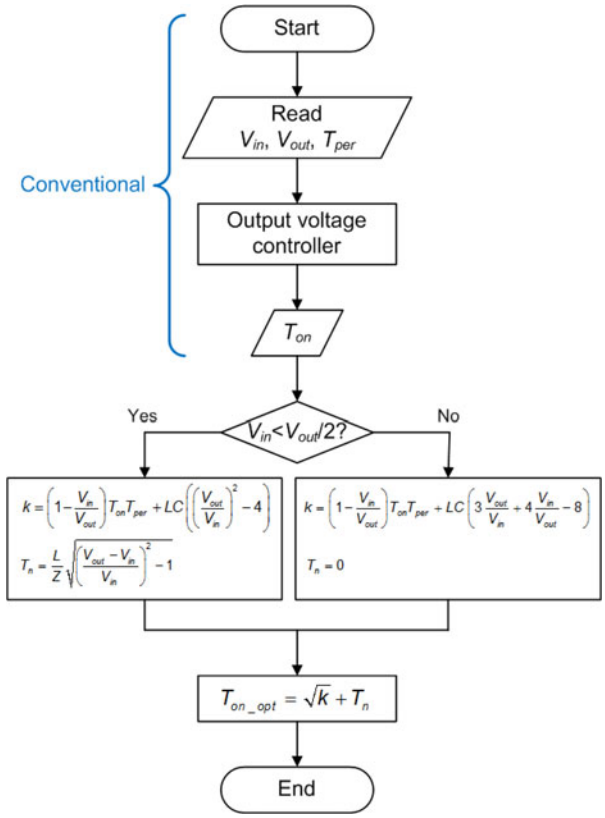

Fig. 10. Flowchart of the proposed method during every sampling period.

A. Implementation of the Proposed Method

Fig. 9 shows the implementation of the proposed method. With the conventional constant on-time control, on time of the main switch is determined by $T_{\rm on}$. However, in the proposed method, the optimal on-time calculation part is added to the control block. The eCAP module captures $T_{\rm per}$ at the every rising edge of the analog comparator. The optimal on time $T_{\rm on\_opt}$ can be calculated with (18) according to $V_{\rm in}$, $V_{\rm out}$, $T_{\rm on}$, and $T_{\rm per}$.

Fig. 10 shows the flowchart of the proposed method during every sampling period. Turn-on-time control of the proposed method is conducted every sampling period. At the beginning, two ADCs and eCAP module provide $V_{\rm in}$, $V_{\rm out}$, and $T_{\rm per}$ to the digital controller. Output voltage controller provides constant $T_{\rm on}$ according to $V_{\rm out}$. In conventional constant on-time control, this $T_{\rm on}$ is used as the gate signal for the main switch. However, in the proposed method, T_n and k are determined according to (8) and (18). Then, the optimized on time $T_{\rm on\_opt}$ can be determined and updated as $\sqrt{k}+T_n$ according to (17).

The output voltage controller design is the same with the conventional constant on-time control. Generally, in the boost PFC converter, the cutoff frequency of the voltage control loop is designed to be about 10 Hz. This is because the control loop should not affect the input current shape of the boost PFC converter. The prototype converter is also designed to have the cutoff frequency of the loop gain at 10 Hz with 45-kHz sampling frequency, considering the small signal model of CRM boost converter in [18]. The design procedure is omitted because it is the same with the conventional digital controller design. The only difference is that some calculations are added in the proposed method to obtain the optimized additional on time.

B. Experimental Results

The experimental waveforms with the optimal additional on time ($T_{\rm add\_opt}$) are shown in Fig. 11. The ac component of $T_{\rm on\_opt}$ can be regarded as the $T_{\rm add\_opt}$. The additional on time in Fig. 11(b) is compared with Fig. 11(a), because the larger output power results in the larger $T_{\rm on}$ from the compensator resulting in the reduced dead angle region as mentioned before. Therefore, it can be noted that the optimal on time depends on not only the input voltage, but also the output power.

The performance of the prototype is shown in Fig. 12. As shown in Fig. 12(a) and (b), the proposed additional on-time method shows a high PF and low THD in the entire input and output conditions. The optimal additional on time shows higher PF and lower THD at 230 $V_{\rm rms}$ input condition to a large extent, which is the worst case for the PF and THD. Fig. 12(c) shows the efficiency of the prototype with the optimal additional on-time method. As shown here, a high efficiency of the prototype can be achieved with the proposed control method. The efficiency with the simplified on-time control is omitted because it shows very similar value with the optimal additional on-time method. Fig. 12(d) shows the performance of the CRM boost PFC without the proposed method. As shown here, the proposed method

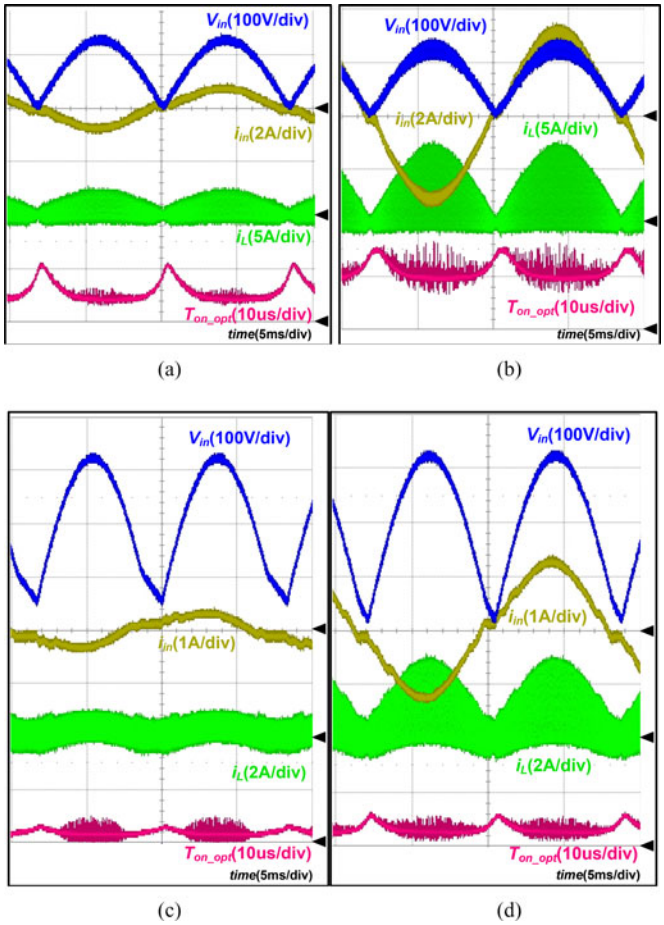

Fig. 11. Experimental waveforms with the optimal additional on time ($T_{\mathrm{add\_opt}}$) at: (a) 90 V_{rms} 20% load, (b) 90 V_{rms} 100% load, (c) 230 V_{rms} 20% load, and (d) 230 V_{rms} 100% load conditions.

significantly improves the PF and THD in the entire input and output conditions.

Table III shows the comparison of performances between the proposed method and the previous works. The proposed work made use of the advantage of digital control and removed trial-and-error design in CRM boost PFC, resulting in a much simpler design procedure with good performances.

C. Gate Turning-Off Technique

The proposed method provides an *ideal envelope* of the additional on time. However, because of the mismatches on the component values and parasitic components, there exists an inevitable dead angle. This dead angle becomes larger as the input voltage increases and the output power decreases. In the dead angle, circulating losses are produced because the net input charge becomes zero, as analyzed before. The circulating losses can be estimated using the input voltage of the boost PFC, as shown in Fig. 13(a). In the dead angle, the bridge diodes are turned OFF and the stored energy in the input capacitor freewheels causing the conduction loss. The circulating loss becomes larger in a lighter load condition, because the dead angle increases in the lighter load condition. According to the energy conservation,

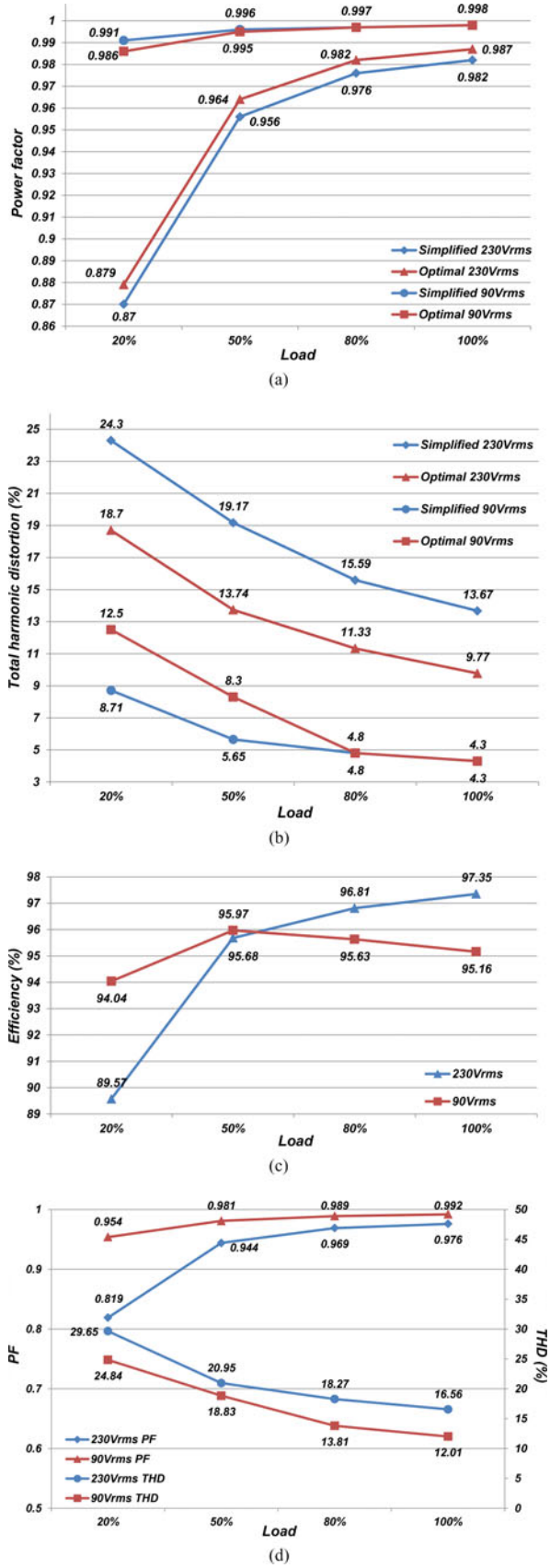

Fig. 12. Performance of the prototype: (a) power factor, (b) total harmonics distortion, (c) efficiency with the proposed method, and (d) without the proposed method.

TABLE III
COMPARISON OF THE PERFORMANCES

	Proposed work	[4]	[5]	[15]	[17]
Input line voltage	90–230 $V_{\rm rms}$	265 $V_{\rm rms}$	90–264 $V_{\rm rms}$	90–264 $V_{\rm rms}$	85–265 $V_{\rm rms}$
Output voltage	380 V	400 V	400 V	400 V	392.5 V
Output power	200 W	100 W	90 W	90 W	300 W
Control method	*CRM*, digital	*CRM*, analog	*CRM*, analog	*CRM*, analog	CCM/DCM, digital
Efficiency (maximum)	97.35%	95.4%	95%	94.8	99.17%
THD (minimum)	4.3%	6%	8%	1.7%	3.59%
Trial-and-error design	No	Yes	Yes	Yes	No

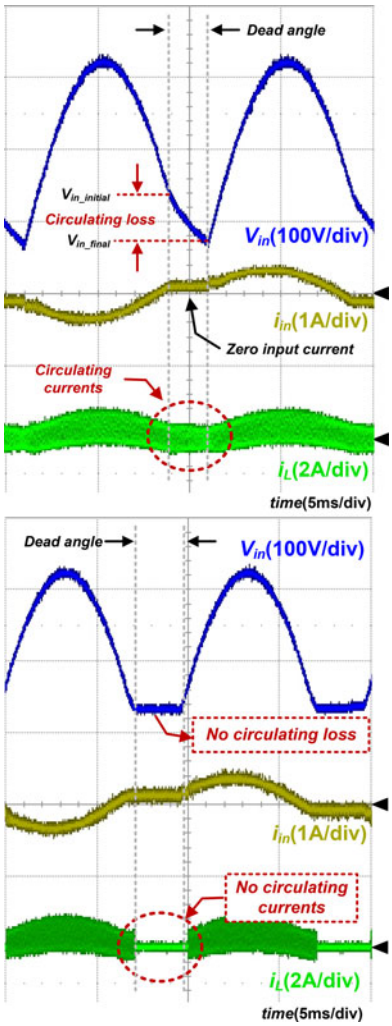

Fig. 13. Key waveforms in the 230 $V_{\rm rms}$ input and a light load condition: (a) without and (b) with the gate turning-off technique.

circulating loss can be calculated by the following equation:

$$P_{\rm loss\_circulating} = 0.5\, C_{\rm in}(V^2_{\rm in\_initial} - V^2_{\rm in\_final}) \times 2 \times \text{line frequency}. \quad (23)$$

In the dead angle, a gate turning-off technique can remove the circulating loss because the stored charges in the input capacitor are conserved during the dead angle, as shown in Fig. 13(b). Using (21), the controller turns off the gate signals when the input voltage is smaller than the dead angle voltage. The efficiency can be improved in a high input voltage–low output power condition, as shown in Fig. 14.

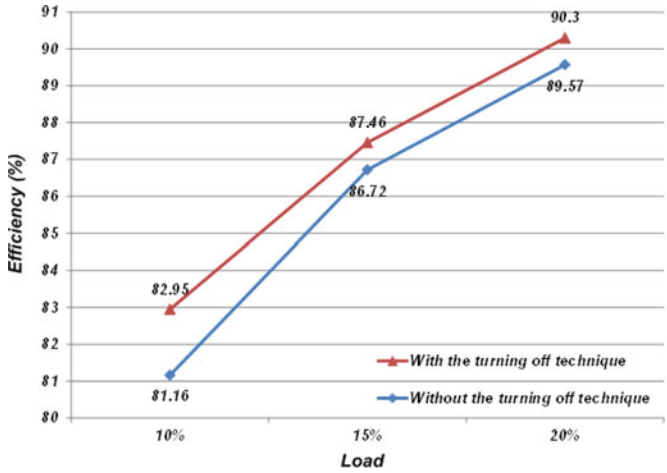

Fig. 14. Efficiency improvement with the gate turning-off technique at 230 $V_{\rm rms}$ input.

V. CONCLUSION

In this paper, an explicit form of the optimal additional on time for a CRM boost PFC is analyzed and verified. Using the "net input charge" analysis and capturing the switching period allow obtaining the explicit form of the optimal additional on time according to the fixed variables. Because of the complexity of the optimal additional on time, a simplified additional on time is also presented in an explicit form, which allows using a cost-effective digital controller. Both methods show a high PF and low THD in the entire input and output conditions. The proposed additional on-time method is powerful because of the following reasons:

1) The proposed method does NOT use additional sensing network. The required sensing variables are only the input and output voltage of the CRM PFC.
2) NO optimization procedure is required and implementation is also easy. It only requires the fixed variables of the PFC.

Also, the gate turning-off technique is presented so that the efficiency in a high input voltage-low output power condition can be improved without degrading the input current shape by reducing circulating losses in an inevitable dead angle. This result is very meaningful in that power consumption in a light load condition is gaining importance in many industrial applications.

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